



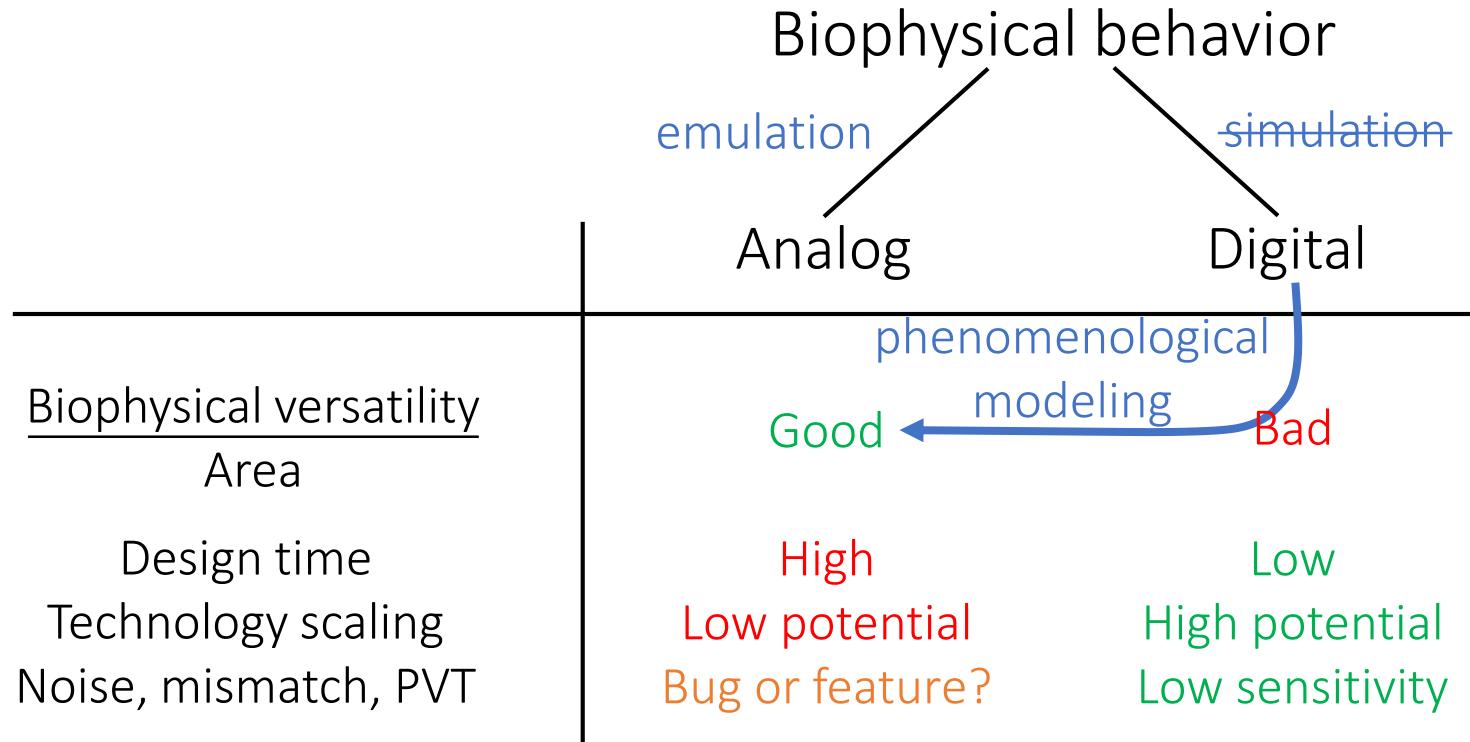
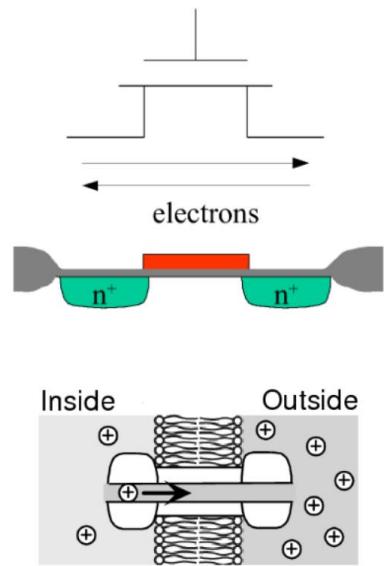
Open (Digital) Neuromorphic (Hardware)

Charlotte Frenkel

Delft University of Technology, Microelectronics Department
c.frenkel@tudelft.nl

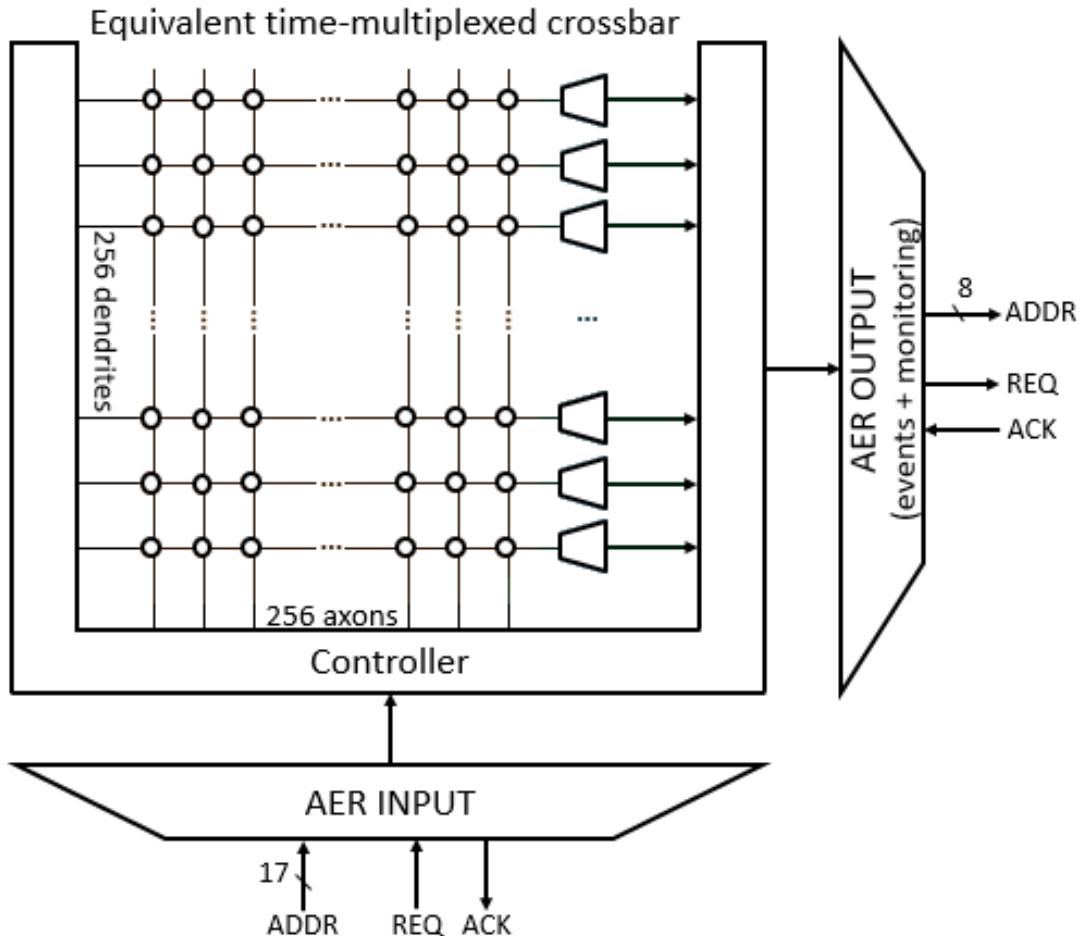
Open Neuromorphic, Politecnico di Torino (online)
13th of December 2022

Why the (digital) in the title?



The first neuromorphic hardware?

Overview of ODIN: An experimentation platform for the edge



The basis: a nice (not-so-interesting) crossbar core

- 256 neurons
- 64k synapses

The rationale: simplicity and efficiency

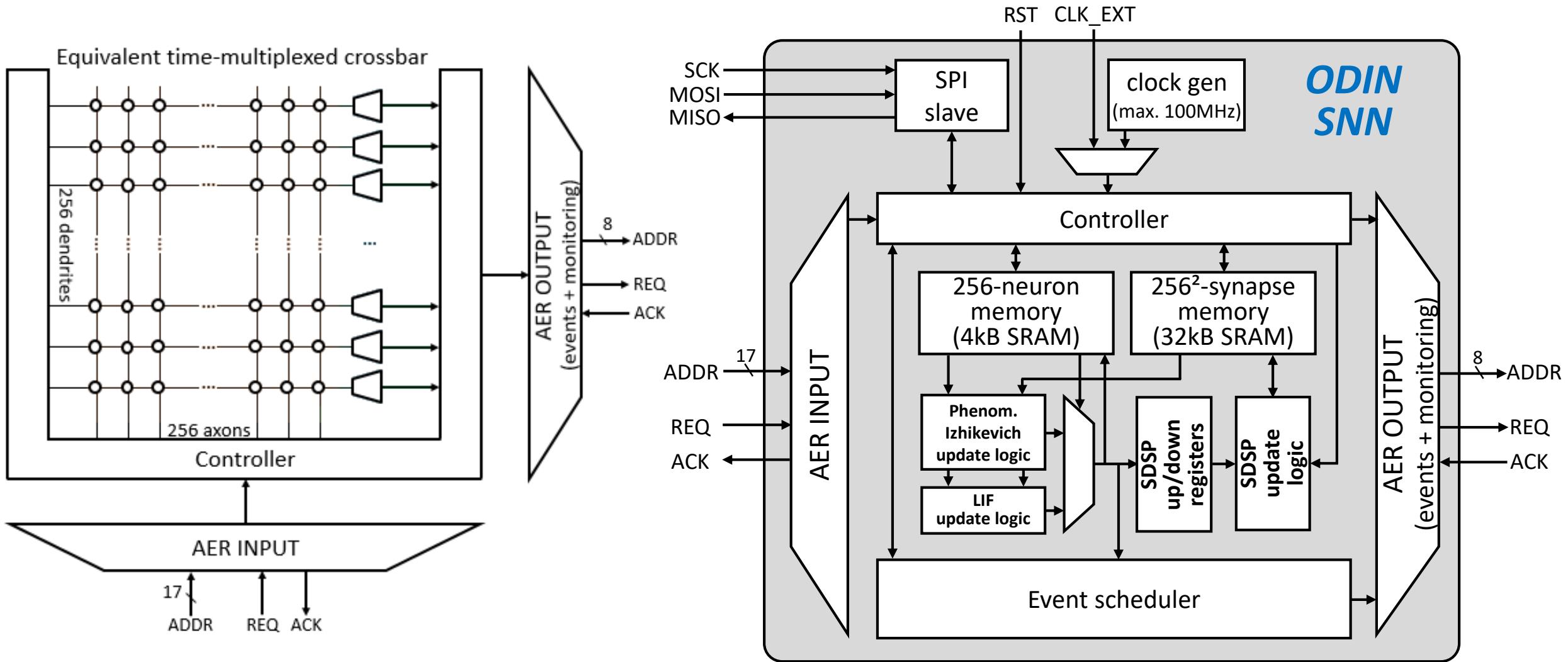
- Time multiplexing
- No PDE solvers (phenomenological modelling)
- Full space and time locality

The salt and pepper: an experimentation platform

- Synaptic plasticity (SDSP)
- Large neuronal repertoire (LIF + Izhikevich)

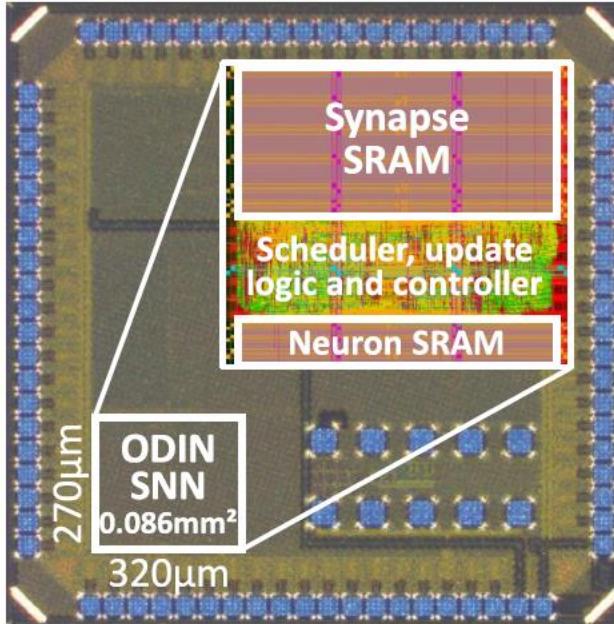
The first neuromorphic hardware?

Overview of ODIN: An experimentation platform for the edge



The first neuromorphic hardware?

ODIN: The silicon demonstration



<https://github.com/ChFrenkel/ODIN/>

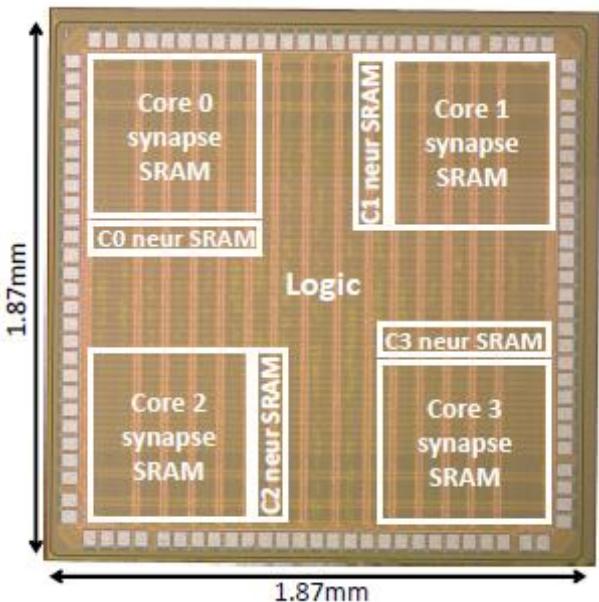


| | | |
|--|---------------------------|--|
| Technology | 28nm FDSOI | |
| Implementation | Digital | |
| Area | 0.086mm ² | Record density |
| # neurons | 256 | |
| # synapses | 64k | |
| # Izhikevich behav. | 20 | |
| Online learning | SDSP, (3+1)-bit weight | |
| Time constant | Biological to accelerated | Large feature set |
| Supply voltage | 0.55V – 1.0V | |
| Leakage power (P_{leak}) | 27.3µW @0.55V | |
| Idle power (P_{idle}) | 1.78µW/MHz @0.55V | Lowest energy/SOP among digital designs at the time of publication, competitive with mixed-signal |
| Incr. energy/SOP (E_{SOP}) | 8.43pJ @0.55V | |
| Global energy/SOP ($E_{\text{tot.SOP}}$) | >12.7pJ @0.55V | |
| Routing flexibility/efficiency | ⌚ (AER) | |
| Fan-in | 256 | |
| Fan-out | 256 | |

Today: 2-5pJ/SOP

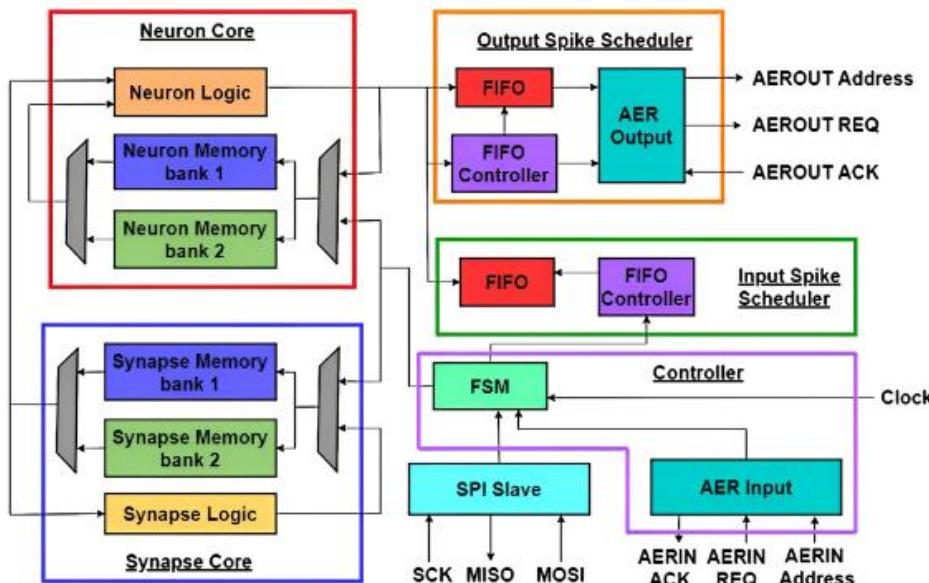
The first neuromorphic hardware? *ODIN: the offspring*

MorphIC



[Frenkel, *Trans. BioCAS*, 2019b]

THOR



[Senapati, arXiv:2212.01696, 2022]

tinyODIN

The basis: a nice (not-so-interesting) crossbar core

- 256 neurons
- 64k synapses

The rationale: simplicity and efficiency

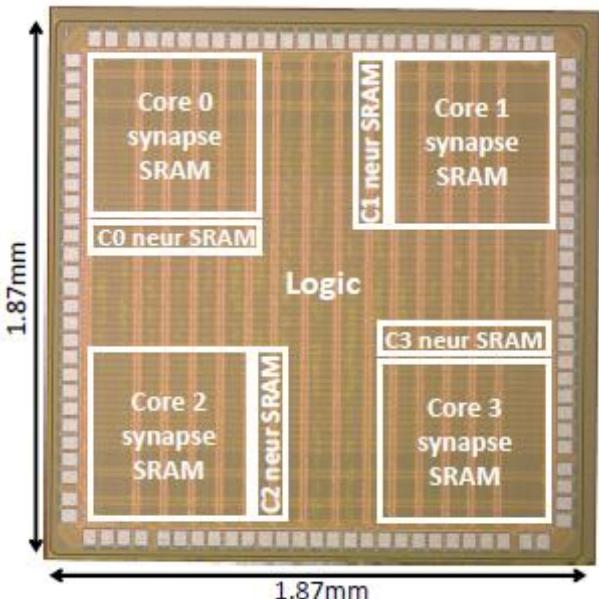
- Time multiplexing
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The salt and pepper: an experimentation platform

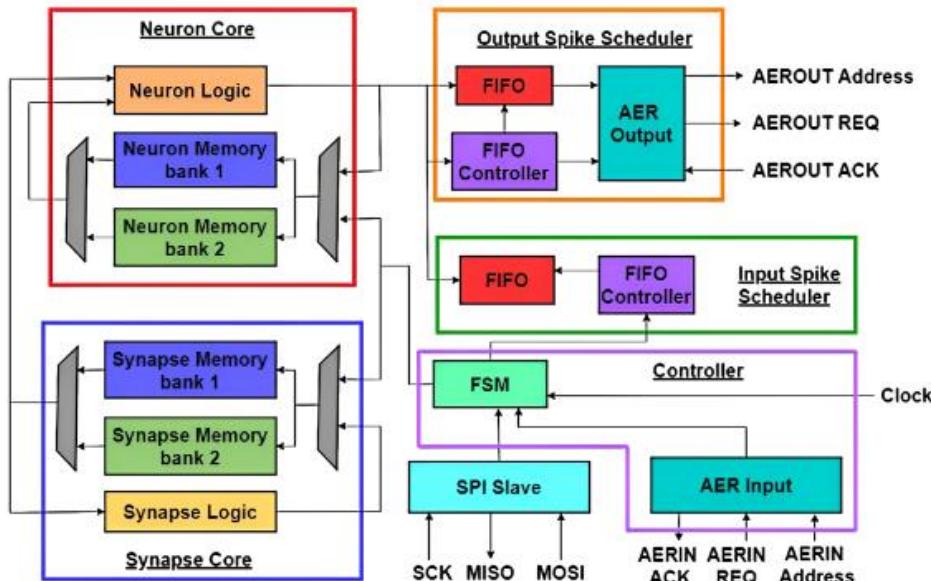
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The first neuromorphic hardware? *ODIN: the offspring*

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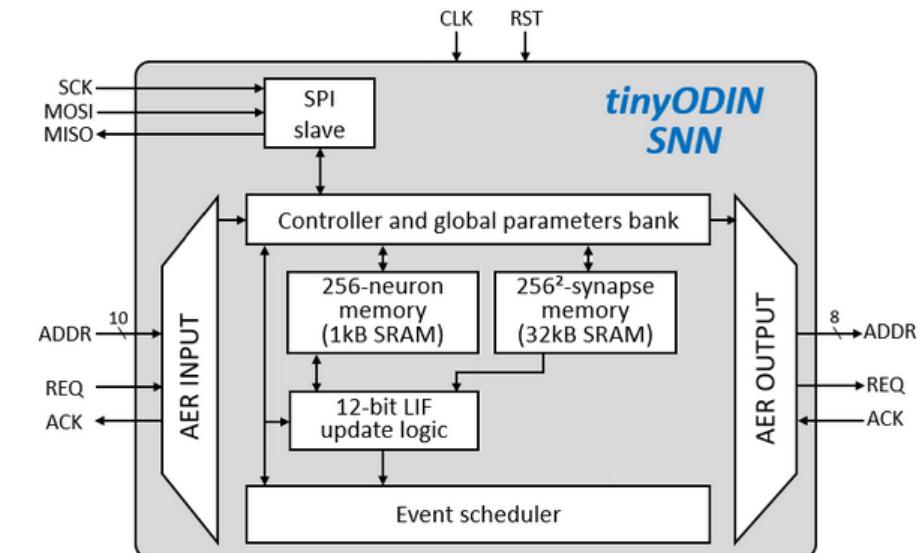


THOR



[Frenkel, *Trans. BioCAS*, 2019b]

tinyODIN



To be released soon!

Why should we open neuromorphic hardware? *(Just in case you still have doubts!)*

Neuromorphic hardware is not (yet) as available as the Raspberry Pi

There's a strong need for flexible testbeds for new experiments!



Opening neuromorphic hardware is good for the community

Remember this time you had to redesign published work from scratch?

Open results = reproducible results.

You can accelerate new progress in the field!

Opening neuromorphic hardware is good for you!

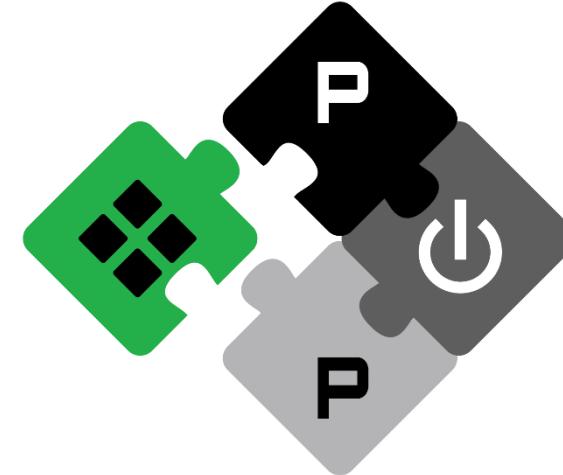
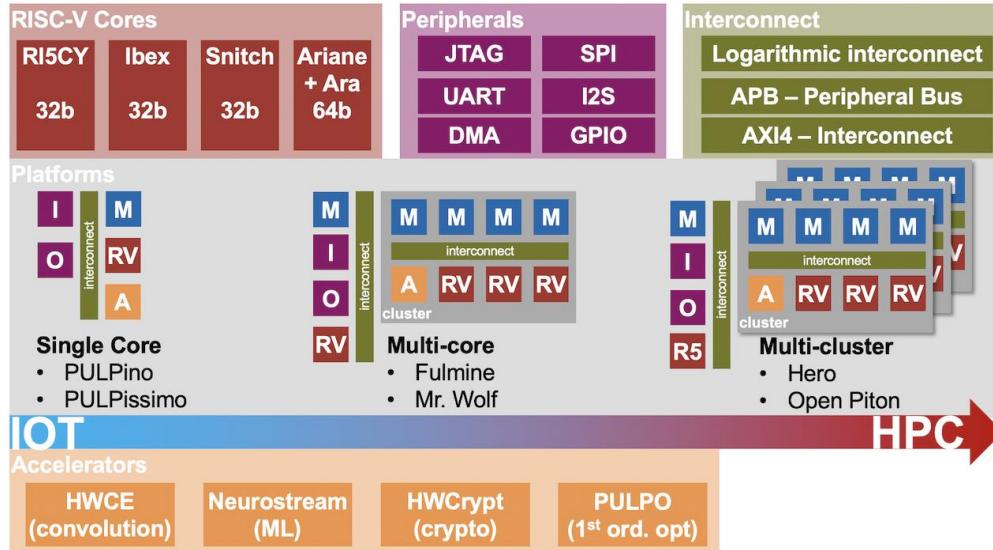
Opening your developments is good for your citations. ☺



How should we open the hardware as well?

From full open-source ecosystems to licenses

Take a (humbling) inspiration from the champions: the PULP platform



<https://pulp-platform.org/>

Which license?

For a permissive license, the *Solderpad Hardware License* is the way to go!
(Although in theory, the *Apache 2.0* license should be applicable to hardware too)

<https://solderpad.org/>

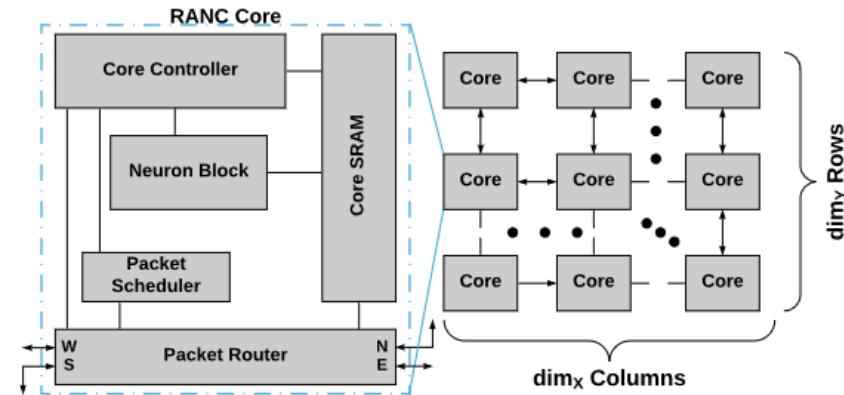
For a copyleft use, see also the *CERN Open Hardware License (OHL)*.

<https://ohwr.org/cernohl/>

Well, this is not all about ODIN either!

Large-scale, flexible and scalable, or tiny and adaptive?

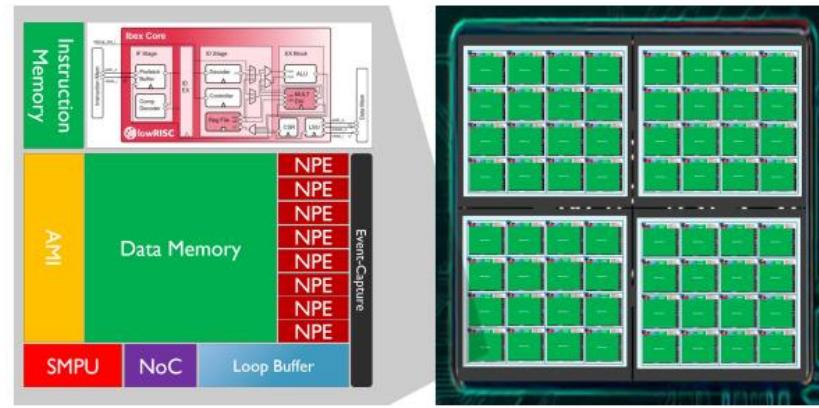
RANC



[Mack, *Trans. CAD*, 2020]

<https://github.com/UA-RCL/RANC>

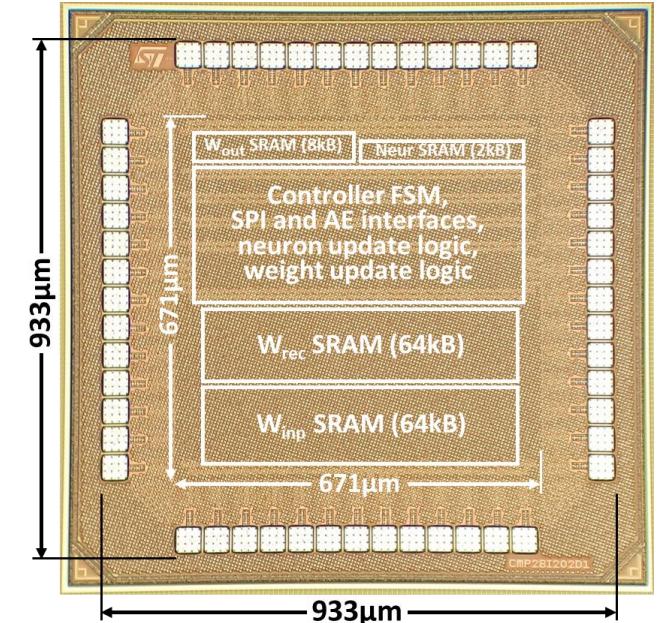
SENeCA



[Yousefzadeh, *A/CAS*, 2022]

...Soon-to-be open-source. ☺

ReckOn

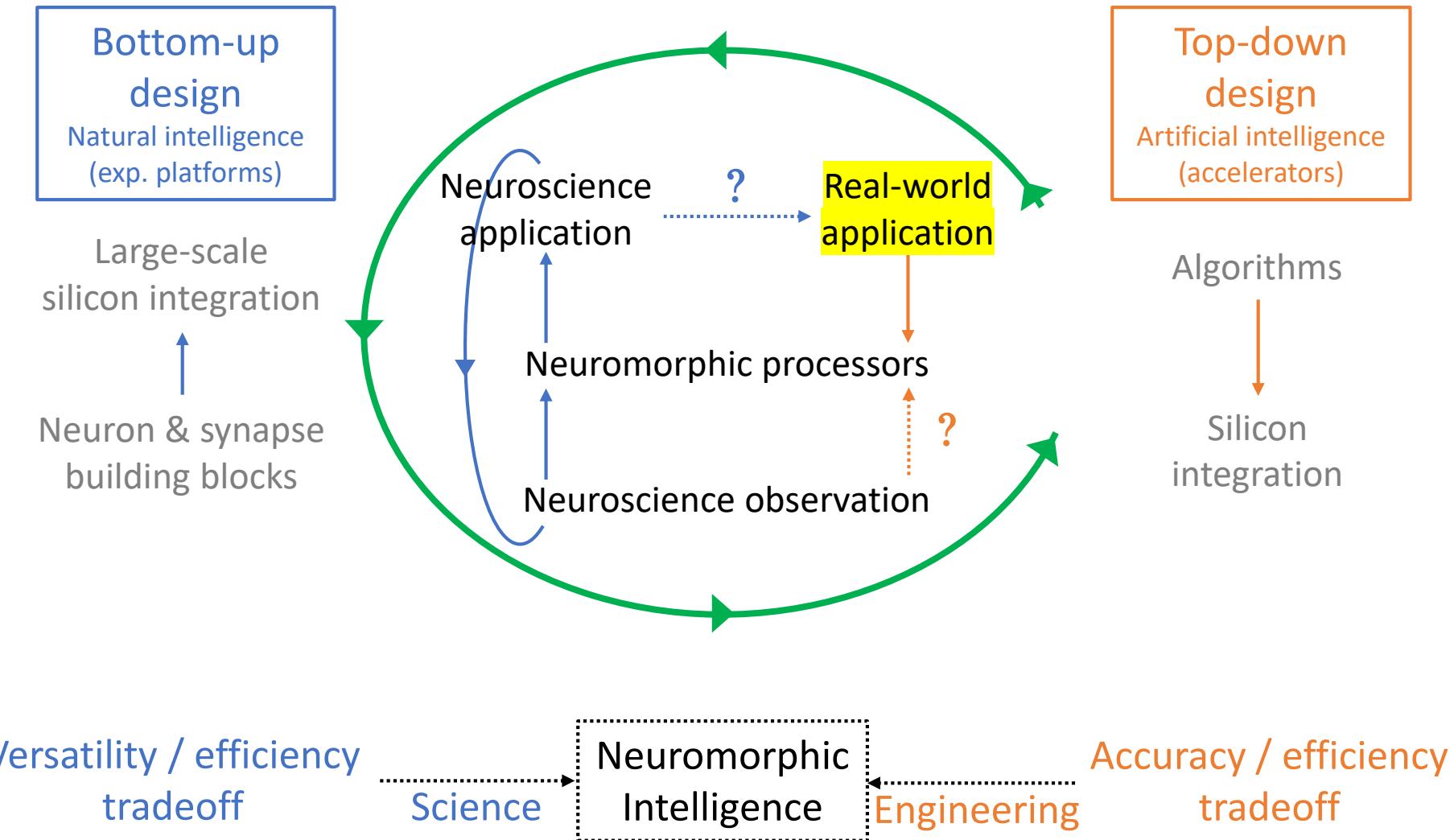


[Frenkel, *ISSCC*, 2022]

<https://github.com/ChFrenkel/ReckON>

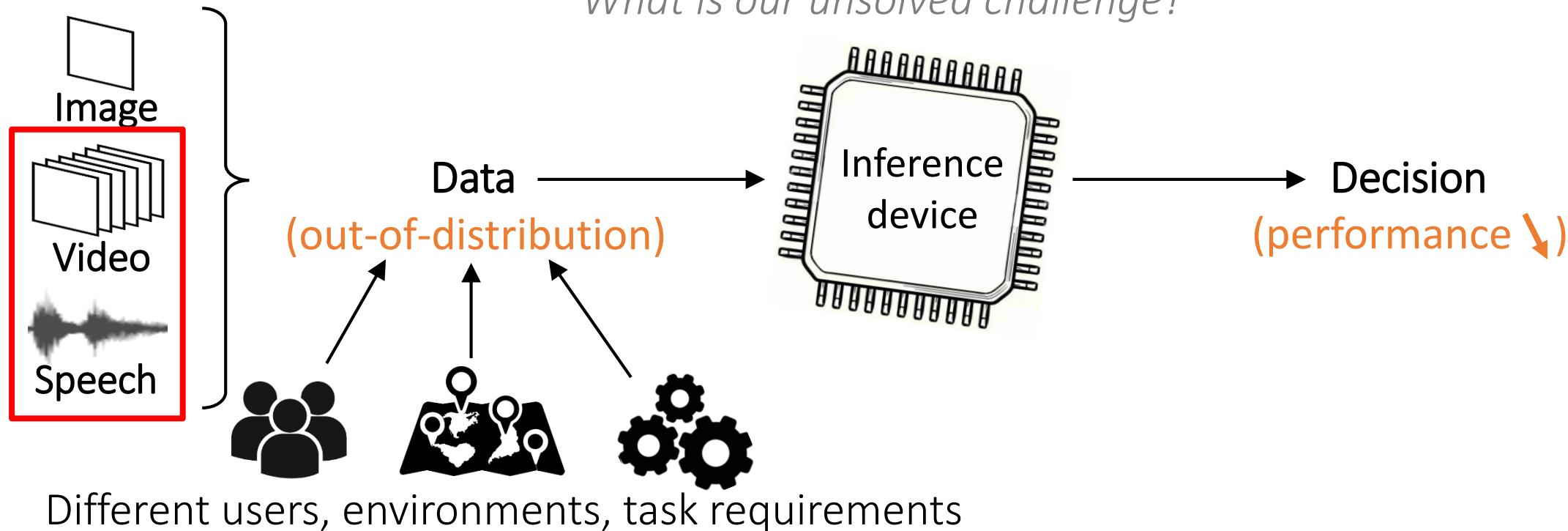
Neuromorphic Engineering – How?

Which design strategy toward neuromorphic intelligence?



The real world application

What is our unsolved challenge?



More training data before deployment?

Issues: cost, robustness, flexibility

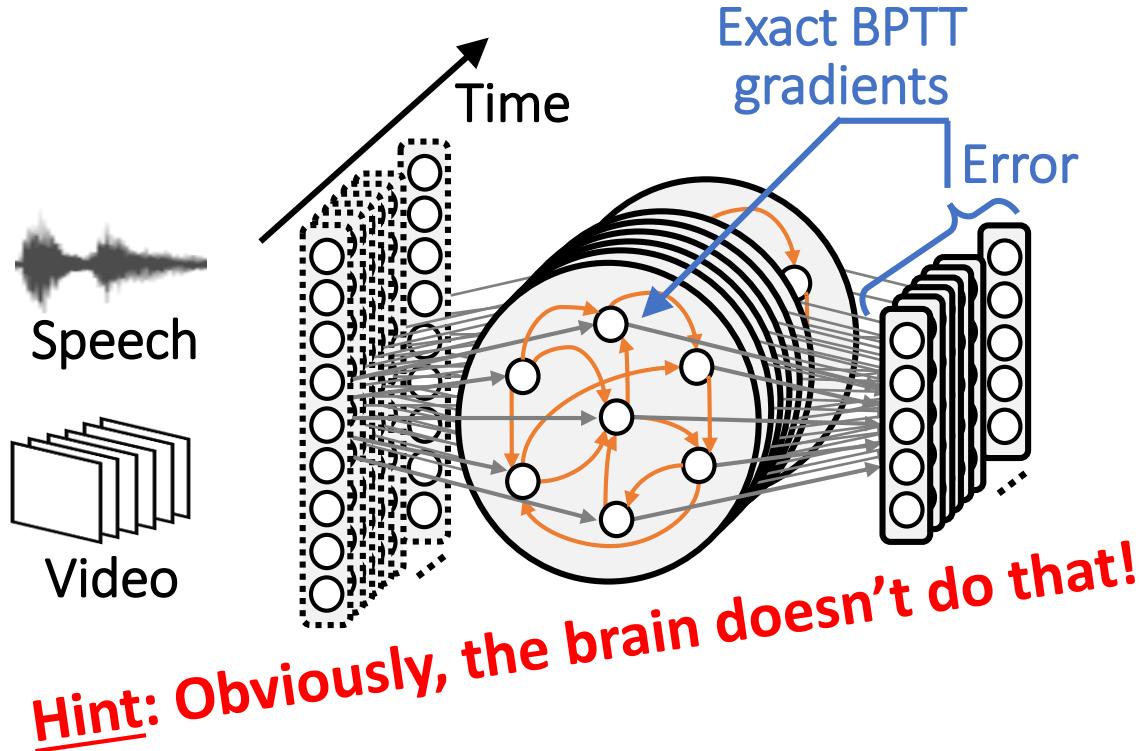
Data exchange with the cloud?

Issues: power budget, privacy

**On-chip training
(end-to-end)**

The real world application

What is our unsolved challenge?

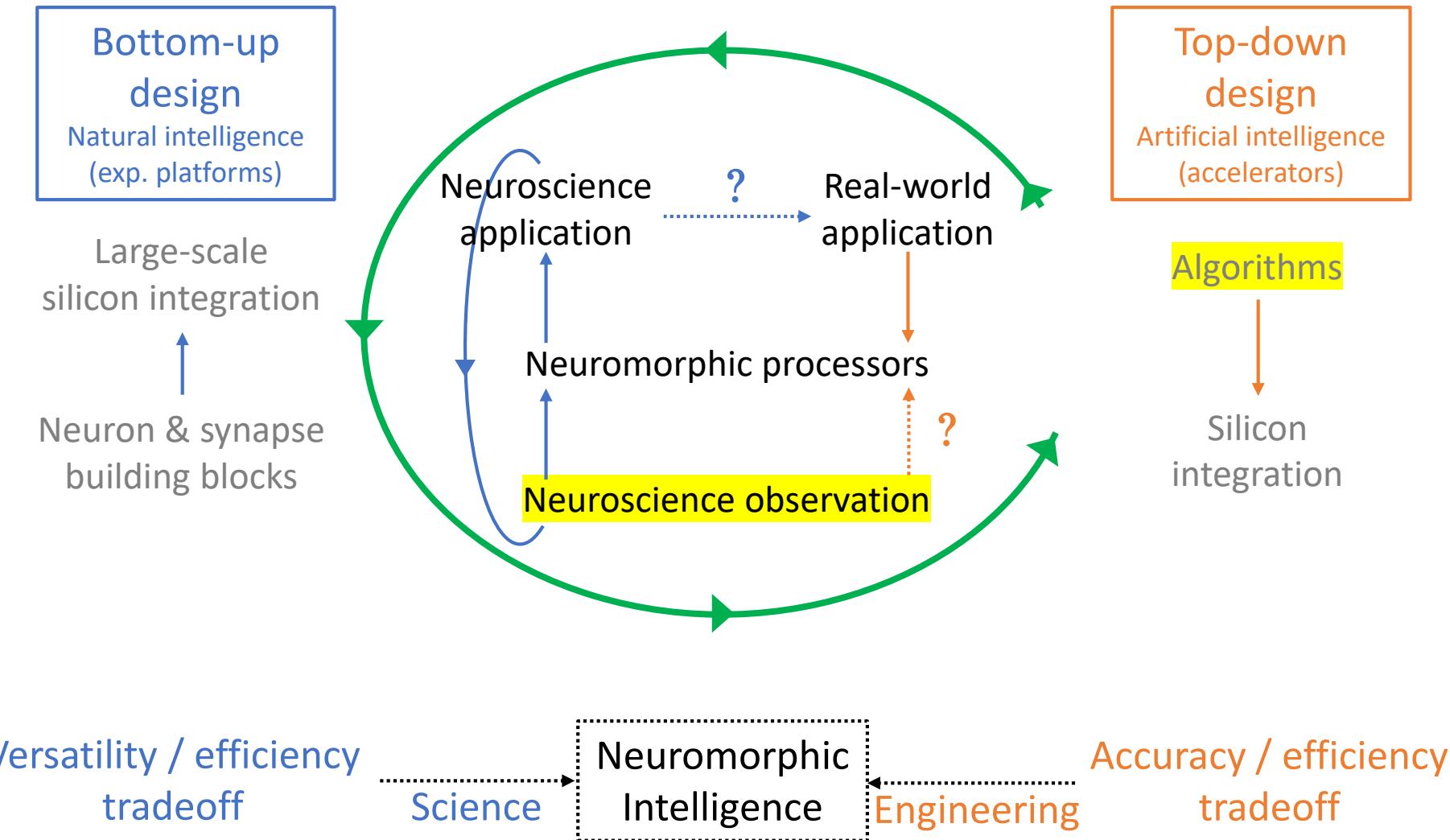


- Unrolling in time: very deep network (current learning ICs for static stimuli: ≤ 3 layers)
- Intractable memory/latency requirements
- No end-to-end on-chip solution to date

Key challenge: On-chip learning over long timescales while keeping a fine-grained temporal resolution

Neuromorphic Engineering – How?

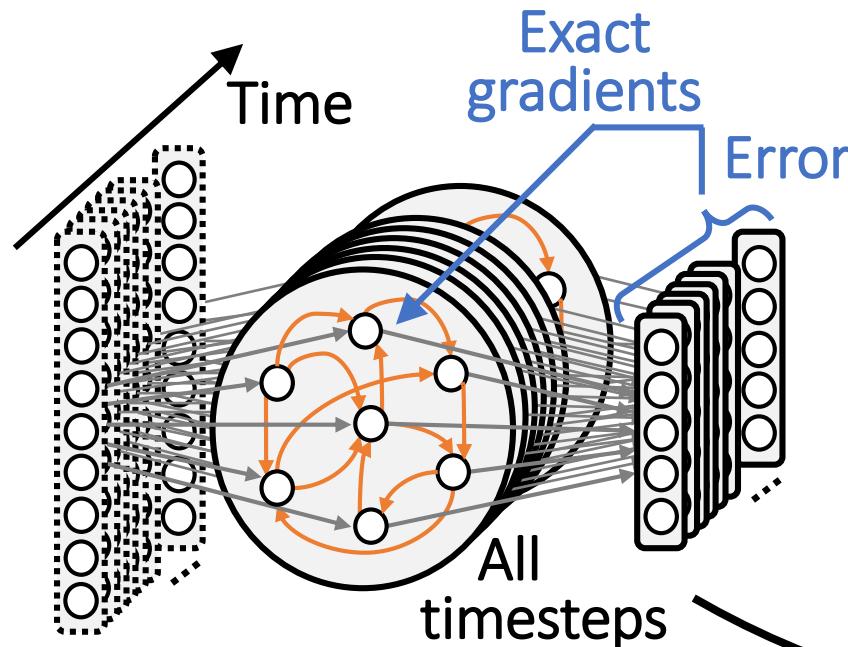
Which design strategy toward neuromorphic intelligence?



What does neuroscience tell us?

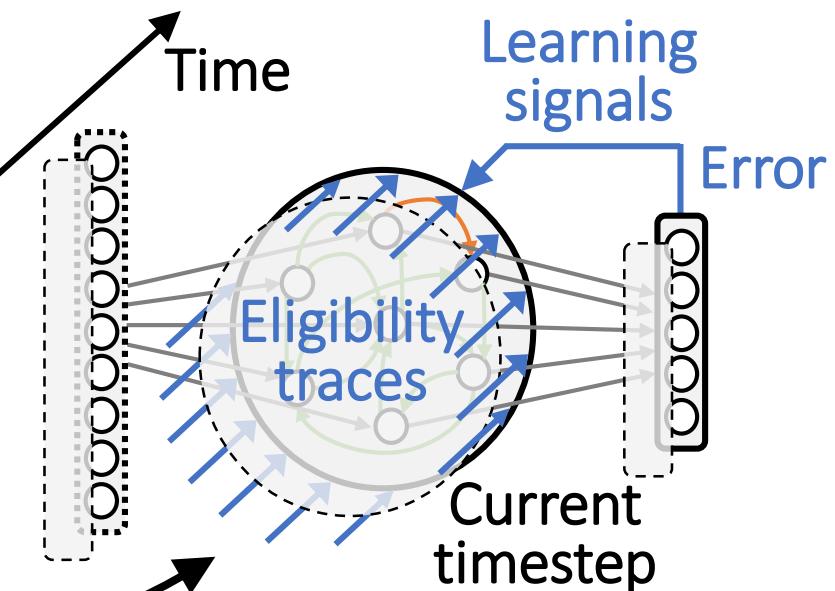
Synaptic eligibility traces are worth looking into!

Backprop through time (BPTT, backward)



Eligibility propagation (e-prop, forward)

[Bellec, Nat. Comms'20]



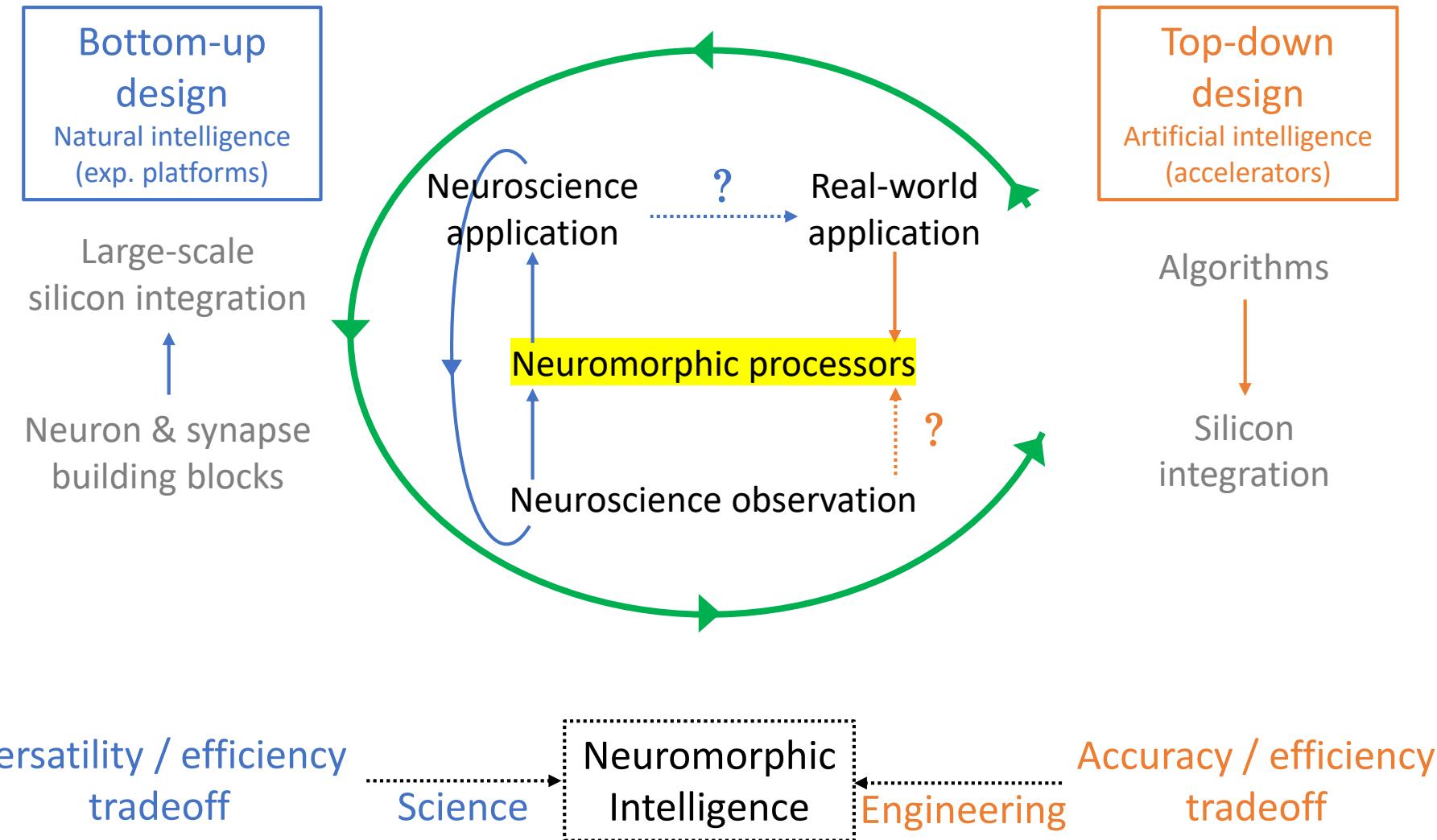
$$\frac{dE}{dW_{ij}} \approx \sum_t L_j^t e_{ji}^t$$

**HW/algo co-design:
Local decoupling of
space and time**

Biological plausibility ↑
Space and time locality ↑
On-chip memory requirements ↓

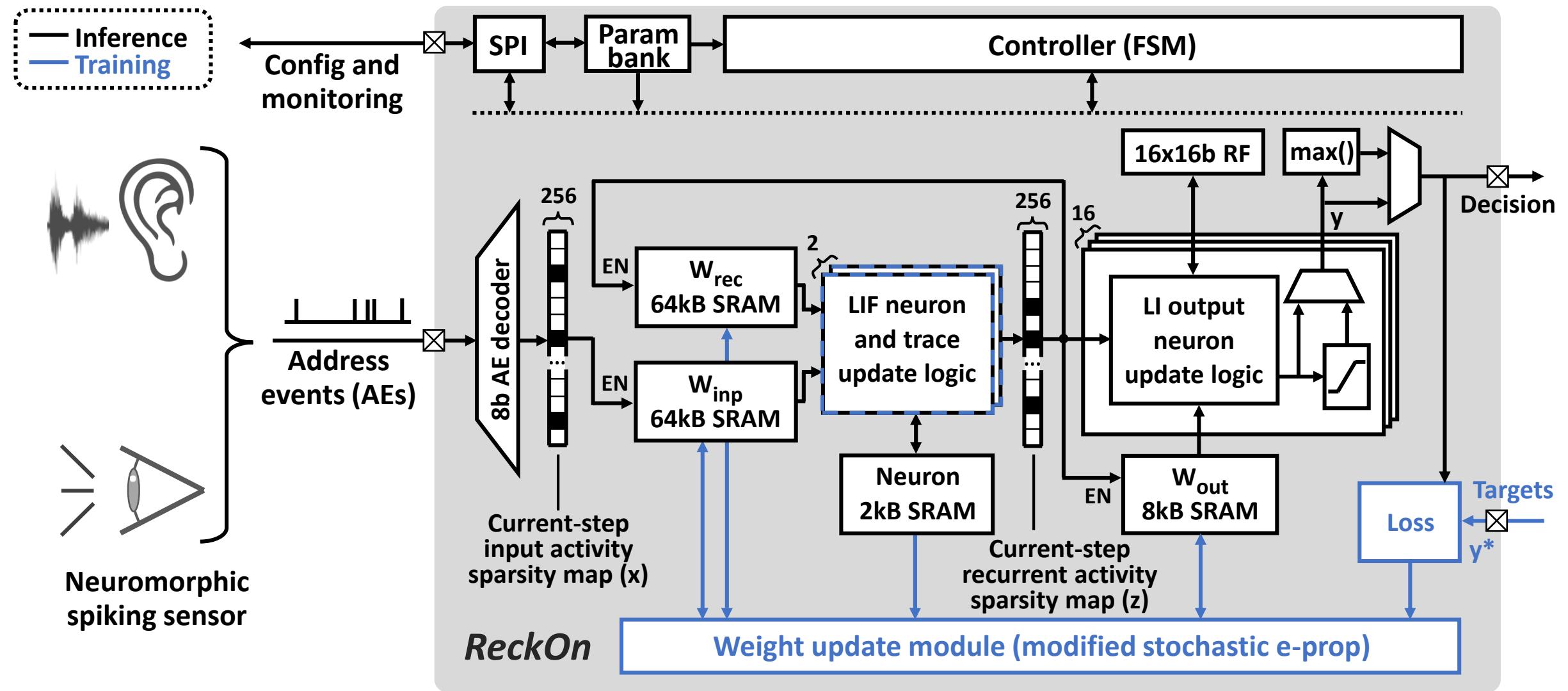
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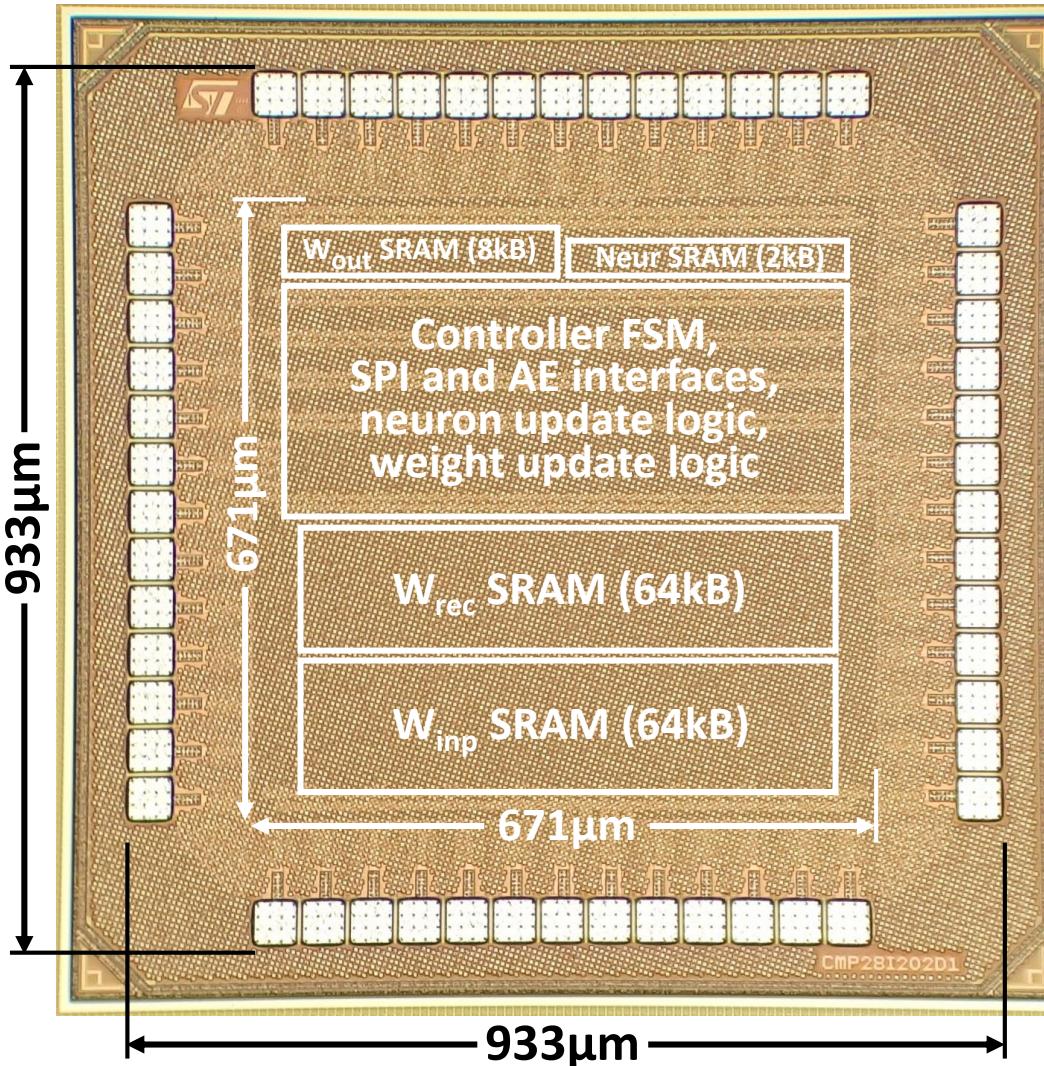
The ReckOn open-source neuromorphic processor

System diagram



The ReckOn open-source neuromorphic processor

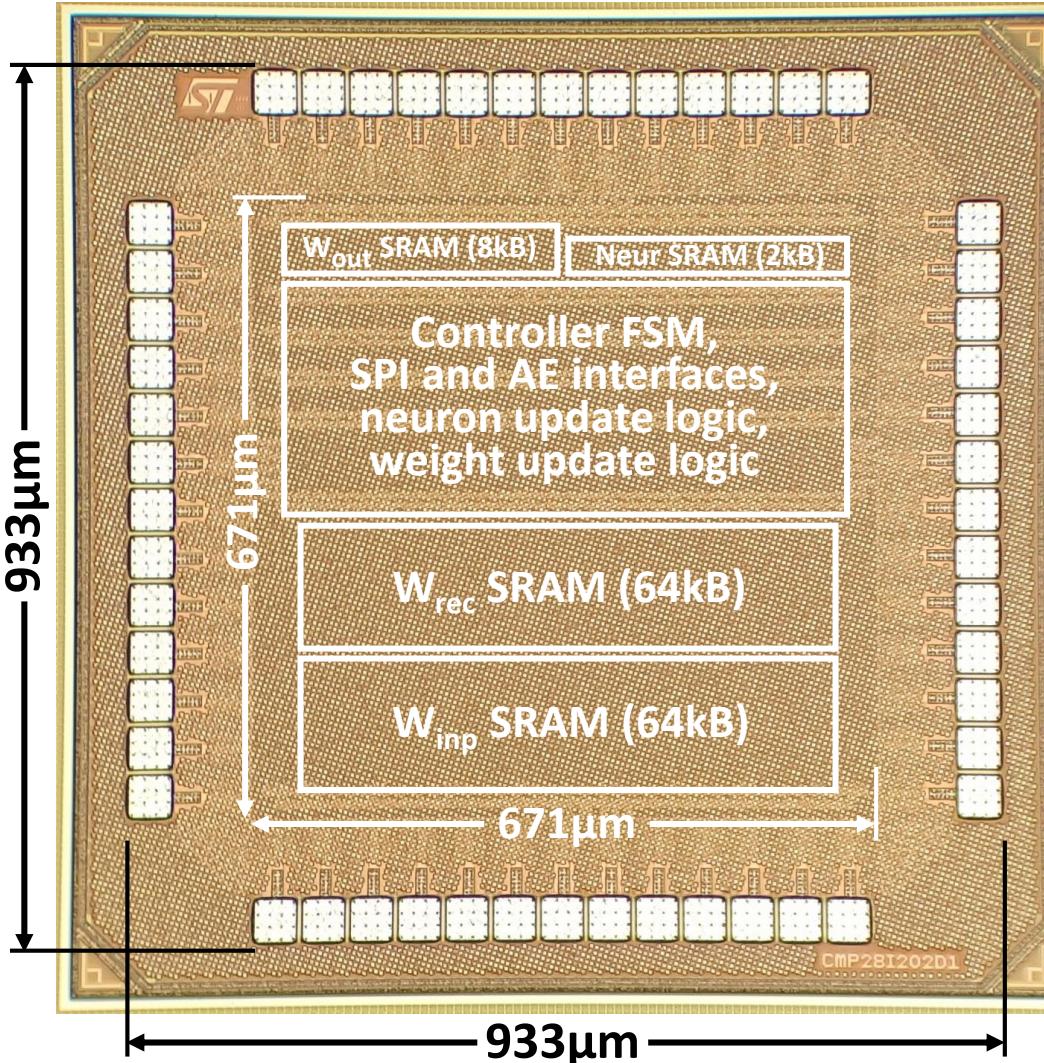
Chip microphotograph and summary



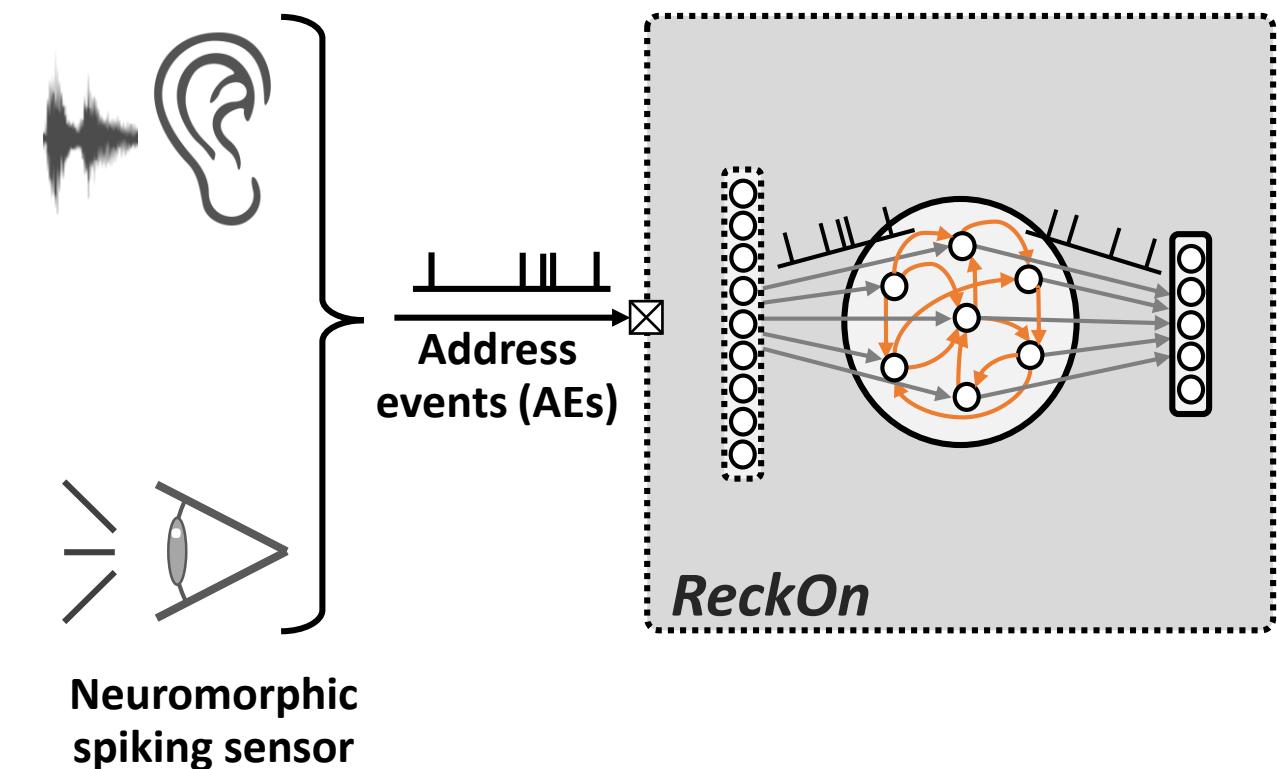
| | |
|-------------------|---|
| Technology | 28nm FDSOI CMOS |
| Core size | 0.67 x 0.67 mm² 0.45mm² |
| Die size | 0.93 x 0.93 mm ² |
| SRAM | 138kB + 0kB ext. DRAM! |
| Network | Spiking RNN |
| Training timespan | Max. 32k steps |

The ReckOn open-source neuromorphic processor

Chip microphotograph and summary



- Event-driven / sparsity-aware computation
- Sensor-agnostic raw-data processing
- Task-agnostic processing and learning

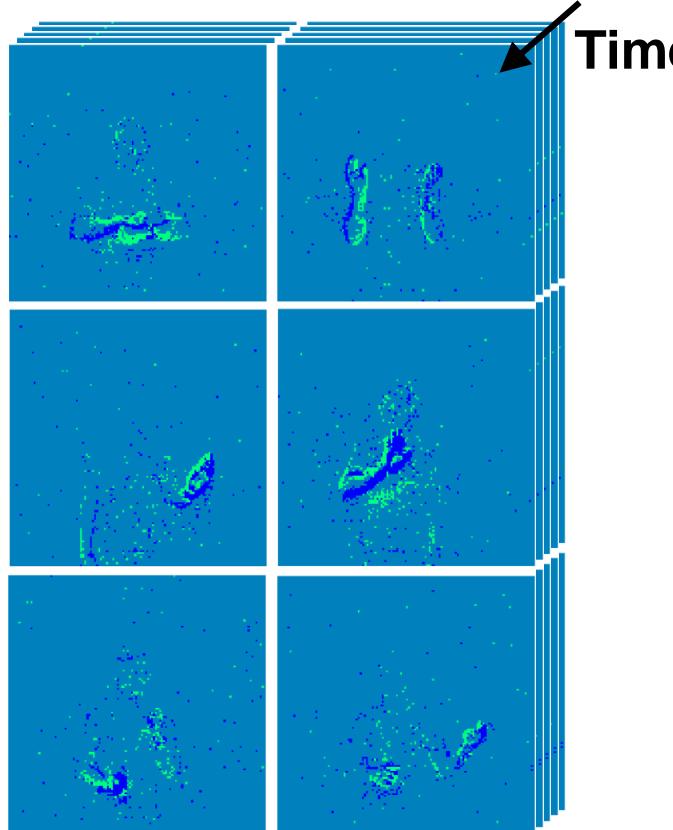


The ReckOn open-source neuromorphic processor

Benchmarking for task-agnostic processing

Vision

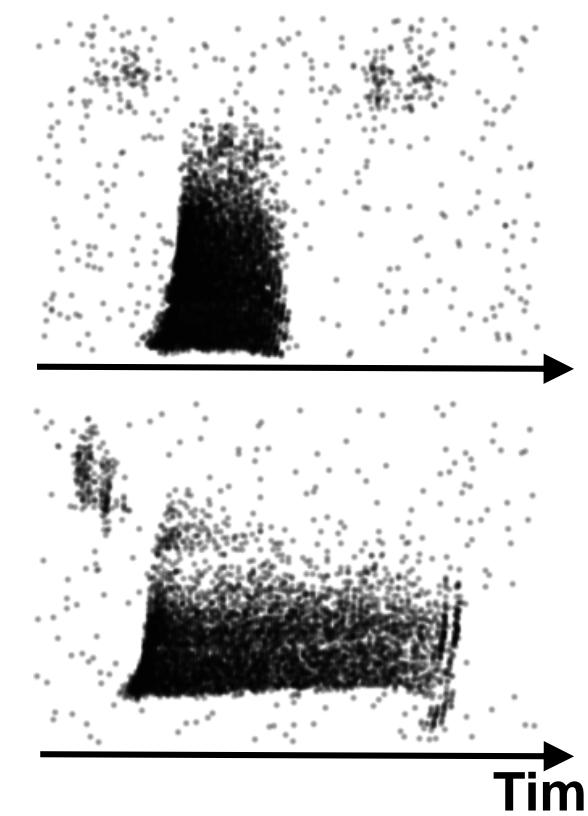
IBM DVS Gestures dataset
(10 classes, shrunked to 16x16)



Accuracy: 87.3% (28 μ W @0.5V)

Audition

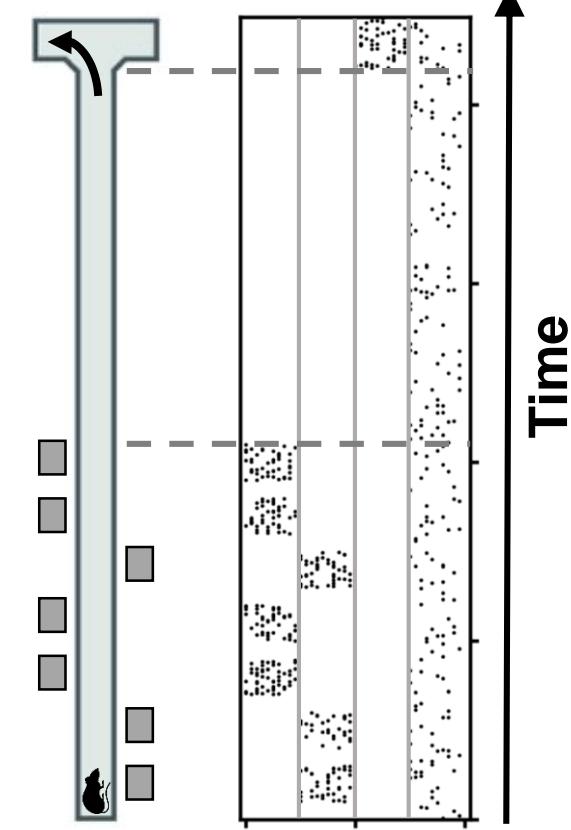
Spiking Heidelberg Digits (EN) dataset
(1-word KWS, 1:1 target vs. filler, 1:3 sub)



Accuracy: 90.7% (46 μ W @0.5V)
[Frenkel, ISSCC, 2022]

Navigation

Delayed-supervision cue accumulation



Accuracy: 96.4% (14 μ W @0.5V)

Conclusions and Perspectives

- The neuromorphic community is enthusiastic and young: open-source developments are especially welcome!
- Open neuromorphic HW today is still mostly digital. Open PDKs now outline open-sourced mixed-signal neuromorphic HW as well.
- We have most pieces of the puzzle. How/when will we have a full neuromorphic ecosystem (like the PULP platform)?

Questions?



@C_Frenkel



cfrenkel



ChFrenkel



Charlotte-Frenkel



c.frenkel@tudelft.nl



chfrenkel.github.io

- **(tiny)ODIN:** C. Frenkel et al., "A 0.086-mm² 12.7-pJ/SOP 64k-synapse 256-neuron online-learning digital spiking neuromorphic processor in 28nm CMOS," *IEEE Trans. BioCAS*, 2019.
- **MorphIC:** C. Frenkel et al., "MorphIC: A 65-nm 738k-synapse/mm² quad-core binary-weight digital neuromorphic processor with stochastic spike-driven online learning," *IEEE Trans. BioCAS*, 2019.
- **THOR:** M. Senapati et al., "Thor – A neuromorphic processor with 7.29 G TSOP²/mm²Js energy-throughput efficiency," *arXiv preprint arXiv:2212.01696*, 2022.
- **RANC:** J. Mack et al., "Ranc: Reconfigurable architecture for neuromorphic computing," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2020.
- **SENeCA:** A. Yousefzadeh et al., "SENeCA: Scalable energy-efficient neuromorphic computer architecture," *IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)*, 2022.
- **ReckOn:** C. Frenkel and G. Indiveri, "ReckOn: A 28-nm sub-mm² task-agnostic spiking recurrent neural network processor enabling on-chip learning over second-long timescales", *IEEE International Solid-State Circuits Conference (ISSCC)*, 2022.
- **Review:** C. Frenkel, D. Bol and G. Indiveri, "Bottom-up and top-down neural processing systems design: Neuromorphic intelligence as the convergence of natural and artificial intelligence", *arXiv preprint arXiv:2106.01288*, 2021.

Open-sourced!

github.com/ChFrenkel/ODIN,
with *tinyODIN* to be released soon.

Soon-to-be open-sourced

Open-sourced!
github.com/UA-RCL/RANC

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