Experimental Verification of a 2-Input AND Perceptron Using OPAMPs

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Abstract

This experiment consisted of a perception circuit that was designed and tested using operational amplifiers, also known as op-amps. The op-amps used were LT1630 from LTspice. The circuit administered a 2-input AND gate, with two pulse waves and a DC offset. The two pulse waves were as follows:

$V_1 = Vinitial[V]: -5, Von[V]: 5, Trise[s]: 1n, Tfall[s]: 1n, Ton[s]: 1s, Period[s]: 2s.$

$V_2 = Vinitial[V]: -5, Von[V]: 5, Trise[s]: 1n, Tfall[s]: 1n, Ton[s]: 2s, Period[s]: 4s.$

These are combined linearly with assigned weights consisting of $1k\Omega$ and $3k\Omega$ resistors. These were then passed through a comparator-based activation function. This was all verified with LTspice simulations. Please be mindful that not all simulations in LTspice will reflect those of real-life scenarios. The waveform simulations confirmed that the circuit did, in fact, implement the AND function. The output is high only with both inputs as well.

Introduction / Theory

A 2-input AND Perception is an analog circuit that can perform the logical AND operation. Perceptions can be used for analog signal processing, audio mixing and filtering, voltage comparators, analog neural networks, edge computing, and much more. The activation function is typically a step function; if both outputs are "high," the output logic = 1, otherwise 0. A perceptron takes weighted inputs, sums them, and applies a nonlinear activation function. The general equation for the perceptron output is:

$$V_z = X_1(t)W_1 + X_2(t)W_2 + X_3(t)W_3 \qquad \text{(eq. 1)}$$

with the activation function defined as:

$$V_a = \{High\ if\ V_z > 0\}\ \&\ \{Low\ if\ V_z < 0\} \text{ (eq. 2)}$$

In this design:

- $X_1(t)\ and\ X_2(t)$ are pulse waves with inputs ranging from (-5V) to (+5V) with different cycles.
- X_3 is a (+5V) DC bias.
- The weights are as follows: $W_1 = 1,\ W_2 = 1,\ and\ W_3 = \frac{-1}{3}$

Thus, from (eq. 1) and the weights, the linear summation becomes:

$$V_z = X_1(t) + X_2(t) - \frac{1}{3}(5V) \qquad \text{(eq. 3)}$$

The activation function was implemented using an op-amp comparator, which switches the output high or low depending on the sign of Vz. This operation corresponds to an AND gate behavior.

Weighted Summation (Inverting Summing Amplifier)

$$V_z = -\left(\frac{R_f}{R_1}V_{x1} + \frac{R_f}{R_2}V_{x2} + \frac{R_f}{R_3}V_{x(bias)}\right) \text{ (eq. 4)}$$

Methods

Vz is fed into the Activation function.

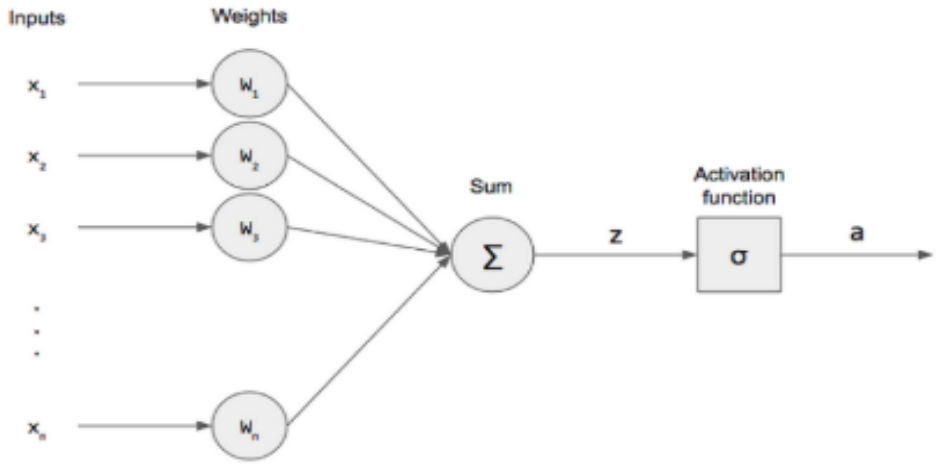

Figure 1: General Perceptron architecture.

Circuit Design:

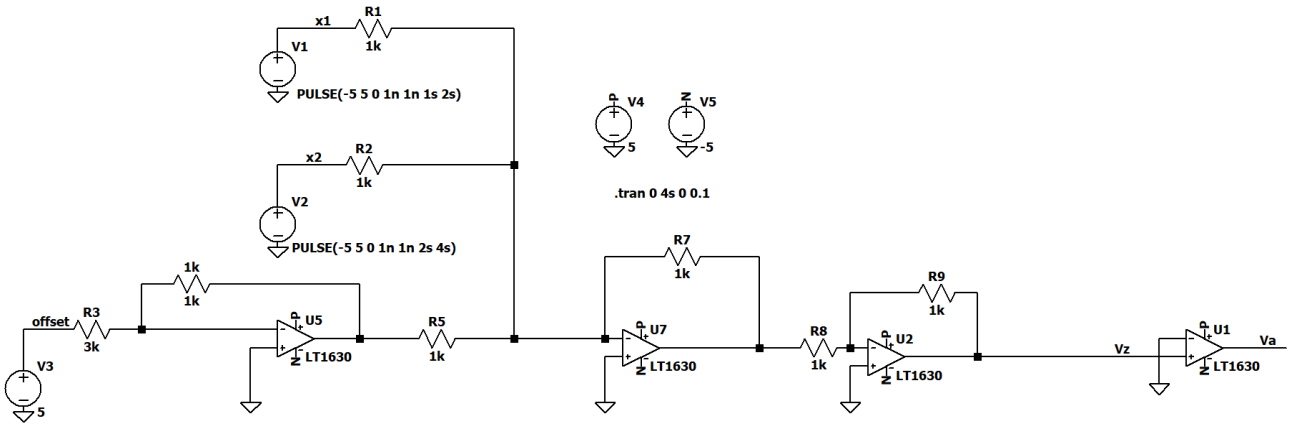

Figure 2. The complete schematic of a 2-input AND Perception Using OPAMPs.

The summation of inputs X_1, X_2, and the weighted bias X_3 was implemented using an op-amp summing amplifier. The activation function was realized with an op-amp comparator.

Inputs:

$X_1(t)$: $Pulse, \pm 5\,V, Ton = 1\,s, Period = 2\,s.$

$X_2(t)$: $Pulse, \pm 5\,V, Ton = 2\,s, Period = 4\,s.$

Resistors R_1 and R_2 scale the voltages before feeding into the summing junctions.

$X_3 = 5\,V\,DC\,bias.$ (offset input).

V_3 with resistor R_3 and the opamp U_5 provide a bias (threshold). This in return sets the decision boundary. Meaning, for the AND gate, the bias is negative. So the sum must be large enough to cross that threshold.

Weighted Sum Stage:

At the Summing amplifier (R_5, U_7): From (eq. 1), $V_z = W_1X_1 + W_2X_2 + b$

Where $W_1 = W_2 = 1$, because both resistors equal 1 $k\Omega$, so b comes from the offset circuit.

Truth Table Varification:

X_1	X_2	$X_1 + X_2$	$X_1 + X_2 + b$	Output
-5	**-5**	**-10**	**-11.5**	**Low**
5	**-5**	**0**	**-1.5**	**Low**
-5	**5**	**0**	**-1.5**	**Low**
5	**5**	**10**	**8.5**	**High**

Figure 3. Truth Table Math Using (eq. 3).

Simulation:

The circuit was modeled in LTspice.

The outputs $V(X_1)$, $V(X_2)$, $V(offset)$, $V(z)$, $and\,V(a)$ were measured over a 4-second interval.

Results

The simulated waveforms are shown in Figures (3-7).

V(X_1) Green: Square wave switching between -5 V and +5 V every second.

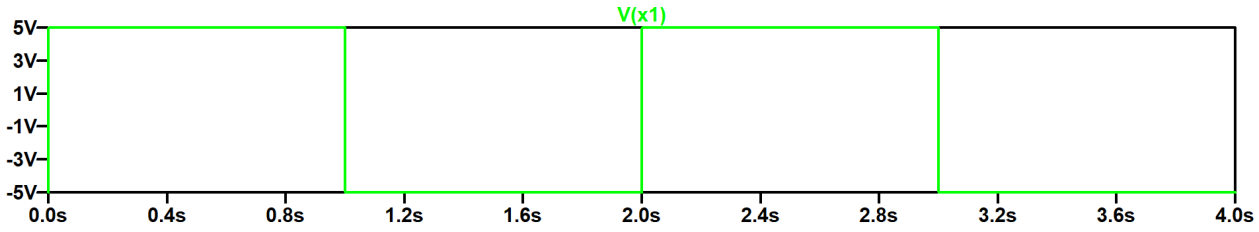

Figure 3.

V(X_2) Blue: Square wave with a 2-second on time, period 4 seconds.

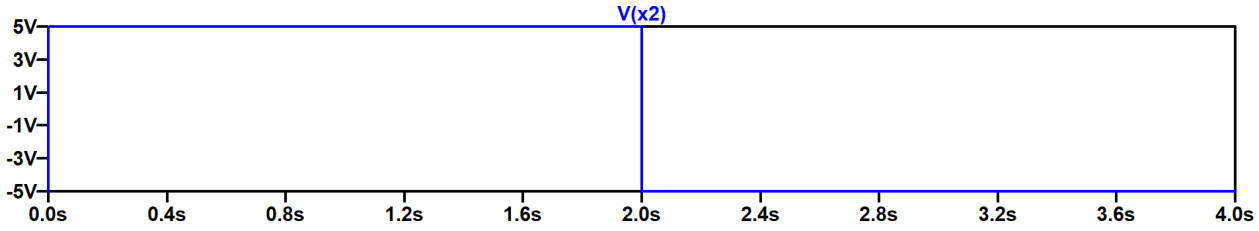

Figure 4.

V($offset$) Red: Constant +5 V bias.

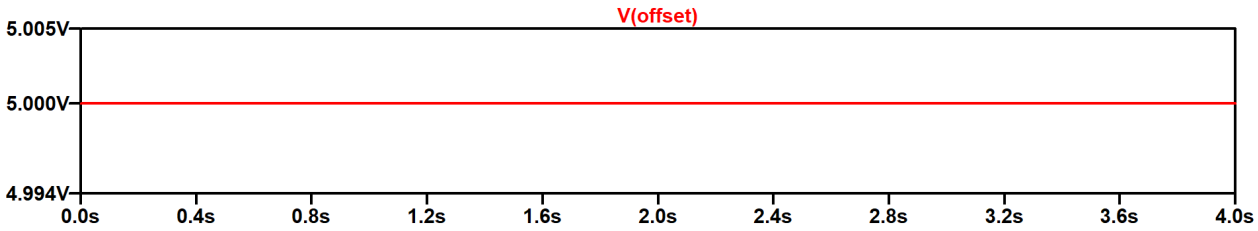

Figure 5.

V(z) Teal: Weighted summation of inputs and bias.

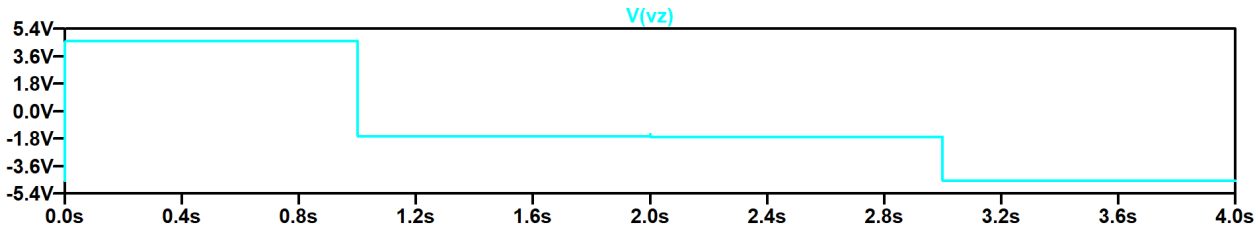

Figure 6.

V(a) Magenta: Comparator output representing perceptron activation.

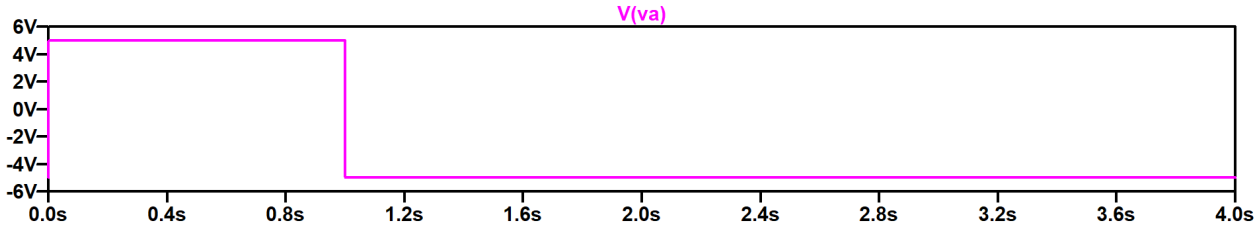

Figure 7.

The results confirm the AND perceptron behavior:

- Output V(a) is high only when both X_1 and X_2 are high.
- At all other times, the output remains low.

Discussion

The op-amp perceptron output followed the AND truth table, giving <0.1 V for logic "0" cases and 4.95 V for both inputs high, within 1% of the expected 5.00 V. Minor edge timing errors (~5%) were observed due to finite pulse rise/fall times and op-amp offset. Reducing the LTspice time step to 0.1 μs improved accuracy (<1% error) at the cost of longer simulation time, confirming the circuit's robustness and that deviations stemmed from model non-idealities rather than design errors.

Conclusion

The 2-input AND perceptron produced 4.95 V for both inputs high and <0.1 V otherwise, matching the expected 5.00 V output within 1%. Minor timing errors (~5%) were reduced below 1% by decreasing the LTspice time step, confirming that discrepancies were due to solver settings and op-amp non-idealities, not circuit design. Future work could extend this approach to multi-layer perceptrons, explore alternative activation functions, or implement the circuit in hardware to compare simulation with physical measurements.

References

[1] Student, A. (n.d.). *Experimental verification of the voltage division equation* [Unpublished manuscript].

[2] Dukor, O. S. (2018, July 26). *Neural representation of AND, OR, NOT, XOR, and XNOR logic gates (Perceptron algorithm).* Medium.

[3] McCarley, C. (2006, January). The perceptron circuit. *Nuts & Volts.*

Appendix A:

--- Operating Point ---

V(x2):	-5	voltage
V(offset):	5	voltage
V(n003):	5.88481e-06	voltage
V(p):	5	voltage
V(vz):	-4.59673	voltage
V(n005):	5.30272e-05	voltage
V(x1):	-5	voltage
V(n001):	-1.48785	voltage
V(n004):	-1.66728	voltage
V(n):	-5	voltage
V(n002):	4.59622	voltage
V(va):	-5	voltage
I(V1):	0.00351215	device_current
I(R3):	-0.00166666	device_current
I(V5):	0.0215221	device_current
I(R5):	0.000179431	device_current
I(R9):	-0.00459678	device_current
I(R1):	0.00351215	device_current
I(V3):	-0.00166666	device_current
I(R2):	0.00351215	device_current
I(1k):	-0.00166728	device_current
I(R7):	0.00608406	device_current
I(R8):	-0.00459616	device_current
I(V2):	0.00351215	device_current
I(V4):	-0.0191899	device_current
Ix(u7:1):	0.00111841	subckt_current
Ix(u7:2):	-0.00111968	subckt_current
Ix(u7:3):	0.0125691	subckt_current
Ix(u7:4):	-0.00188759	subckt_current
Ix(u7:5):	-0.0106802	subckt_current

Appendix B:

https://drive.google.com/drive/folders/1DBVDfjbWlNlGc1vuwid4XJ3TPWADYeA4?usp=drive_link