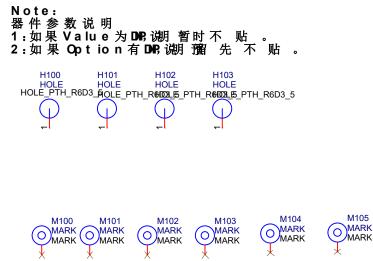
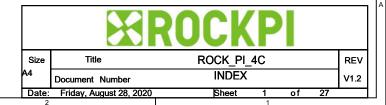
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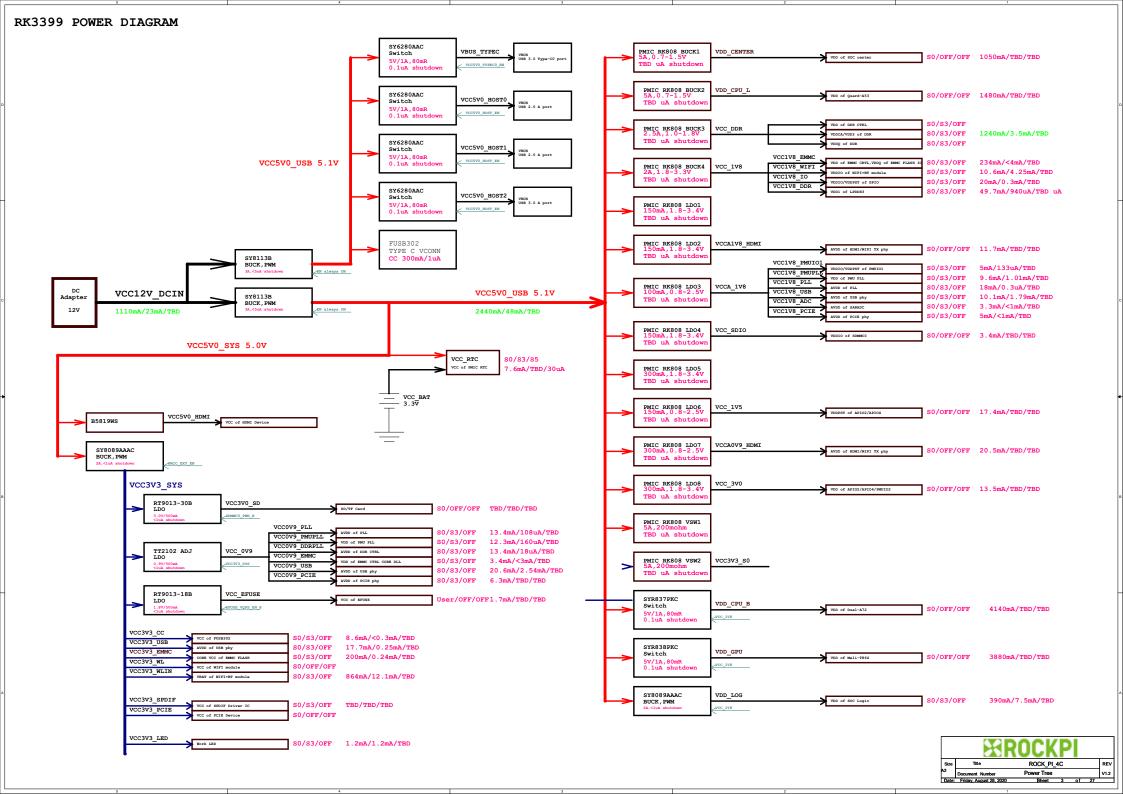




Change List

Version	Date	Author	Change Note	Approved
V1.0	201708	Charlie	First edition	





I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	vcc_1v8	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
I2C0					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
12C1	I2C1 GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL			VCC_1V8			Low Speed CONNECTOR	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2		vcc_1v8			High Speed CONNECTOR	
I2C3	3 GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX		I2C_SDA_HDMI I2C_SCL_HDMI	vcc_3v0				
I2C4	C4		I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
12C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2		VCC_1V8			Low Speed CONNECT	DR
12C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2		vcc_1v8			High Speed CONNEC	TOR

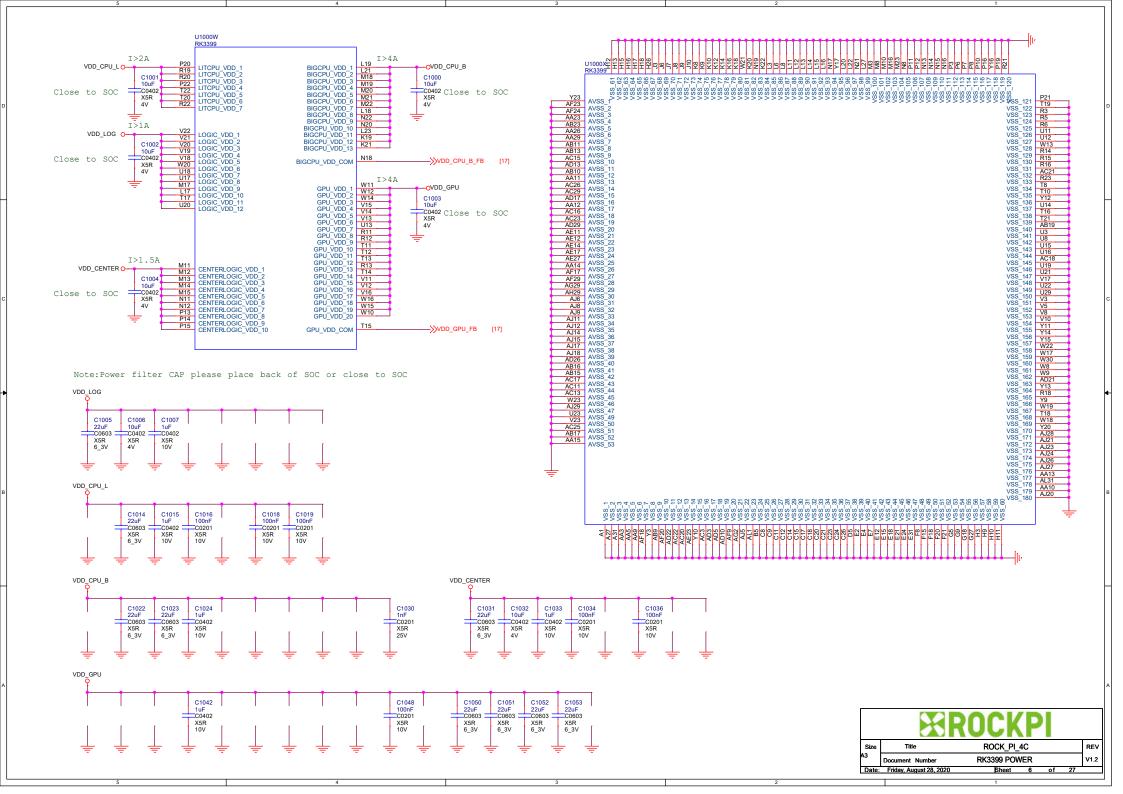
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A4	Document Number	I2C MAP				V1.2		
Date: Friday, August 28, 2020 Sheet 4 of 27								

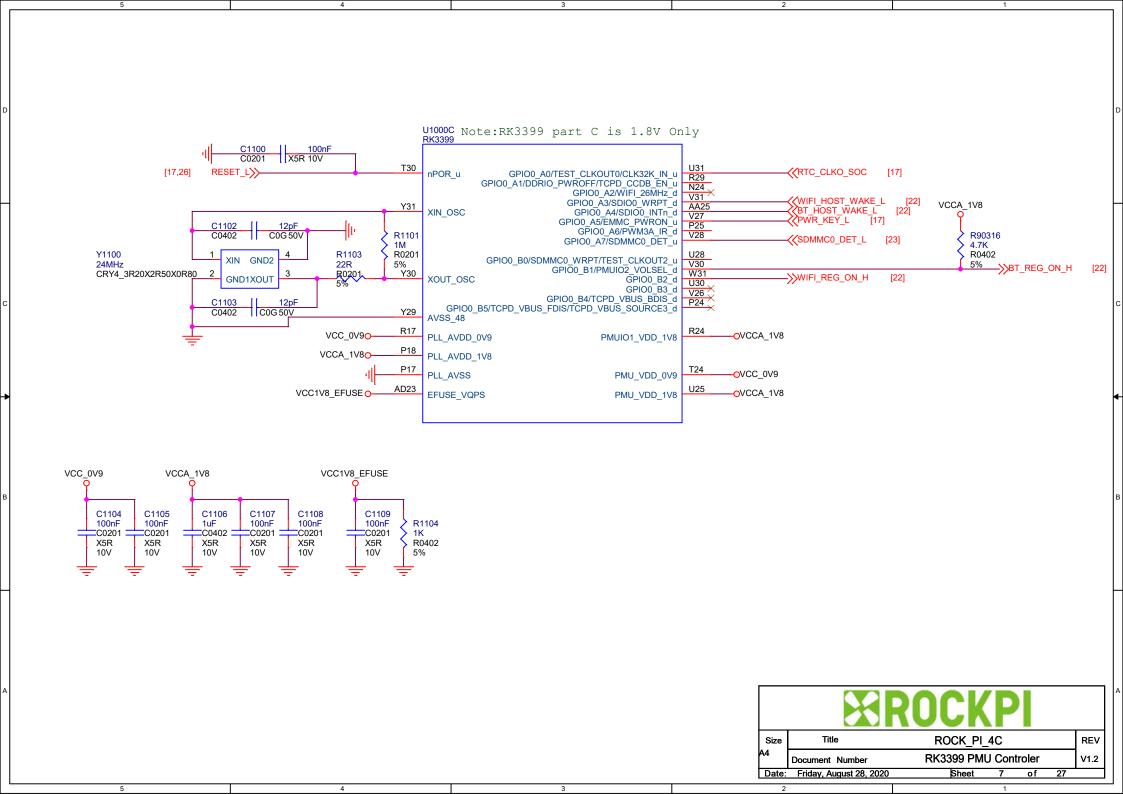
Power Domain Map

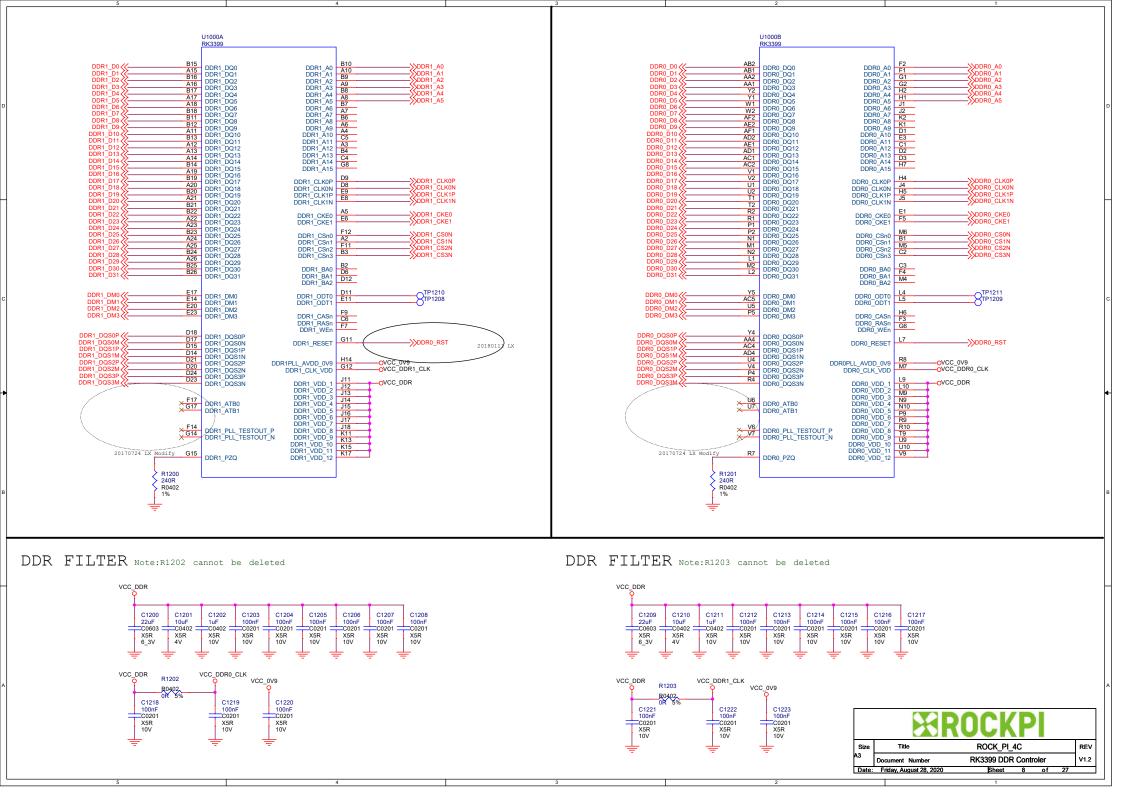
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	pmuio1_gpio0ab	1.8V only	VCCA_1V8	RK808-D VLDO3
Part E	PMUIO2	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part I	APIO1 gmac_gpio3abc 3		3.3V only	VCC_1V8 VCC3V3_SYS	RK808-D Buck4
Part L	APIO2	bt656_gpio2ab	1.8V(Default) 3.0V	VCC_1V8	RK808-D VLDO3
Part G	APIO3	wifi/bt_gpio2cd	1.8V only	VCC_1V8	RK808-D Buck4
Part K	APIO4	gpio1830_gpio4cd	1.8V 3.0V(Default)	vcc_1v5 vcc_3v0	RK808-D VLD06
Part J	APIO5	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCC_1V8	RK808-D Buck4
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808-D VLD04

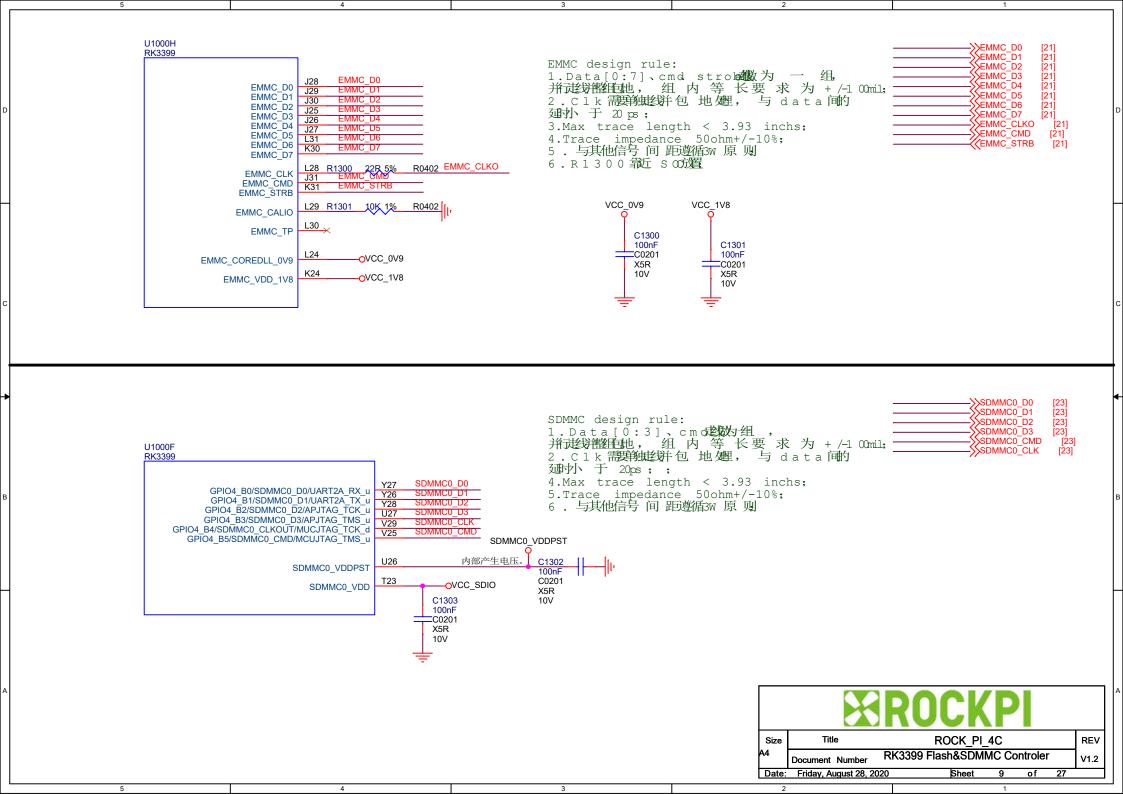
X ROCKPI								
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A4	Document Number	Power Domain Map						
Date: Friday, August 28, 2020 Sheet 5 of 27								

5 4 3 2 1



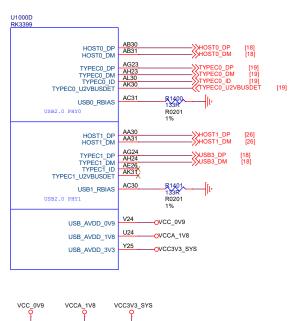


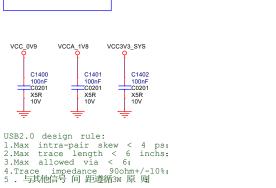




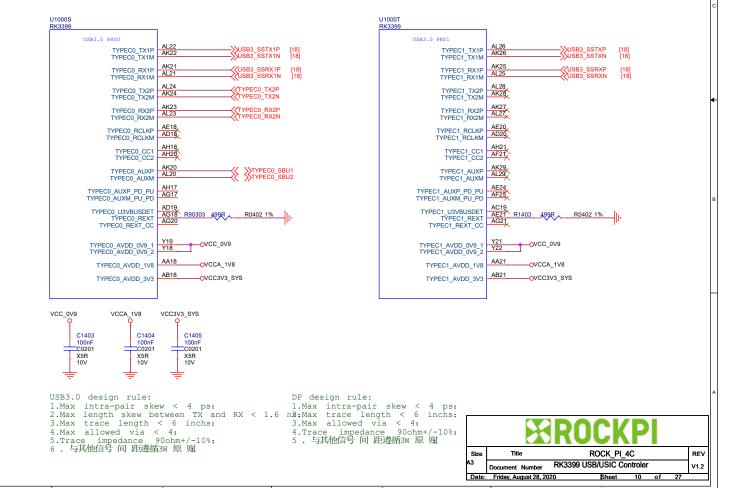


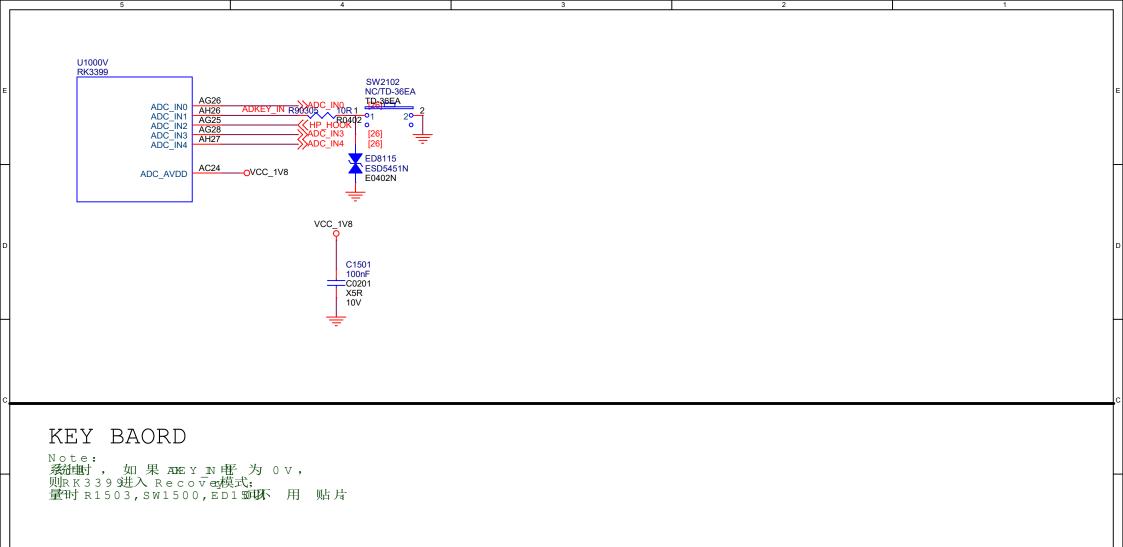
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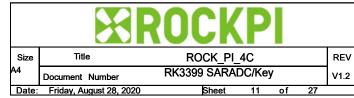


USB3.0

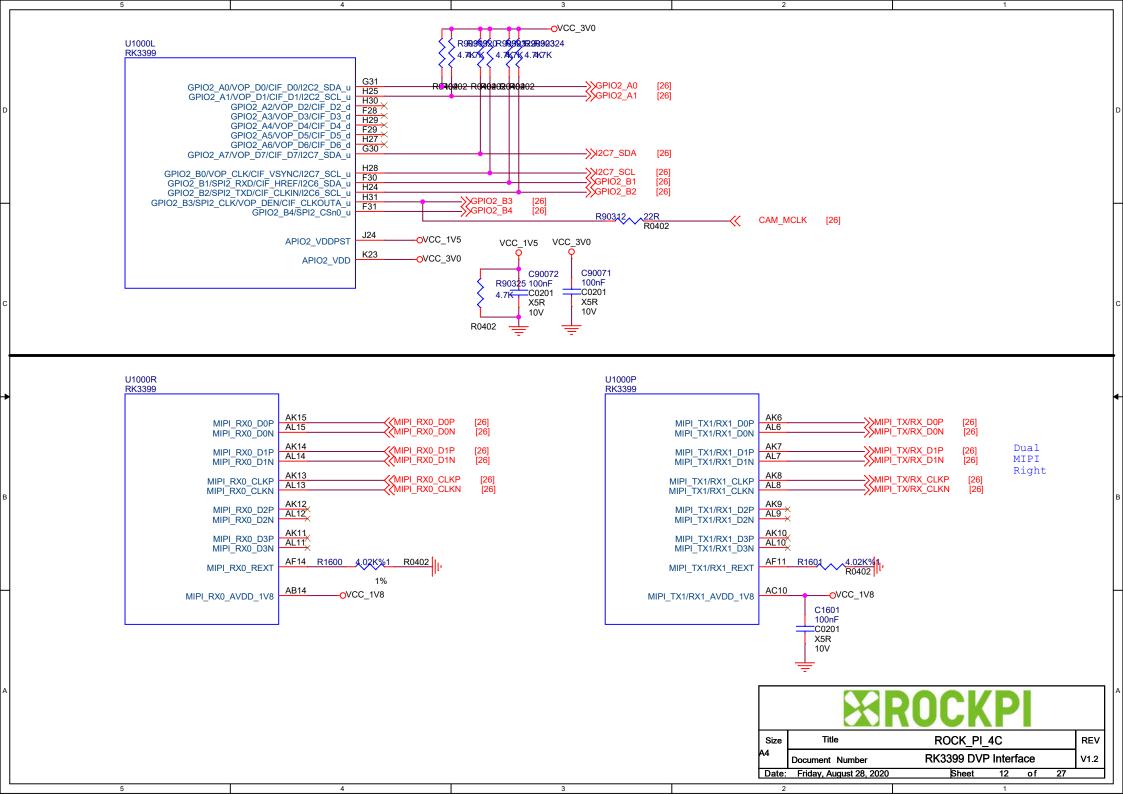


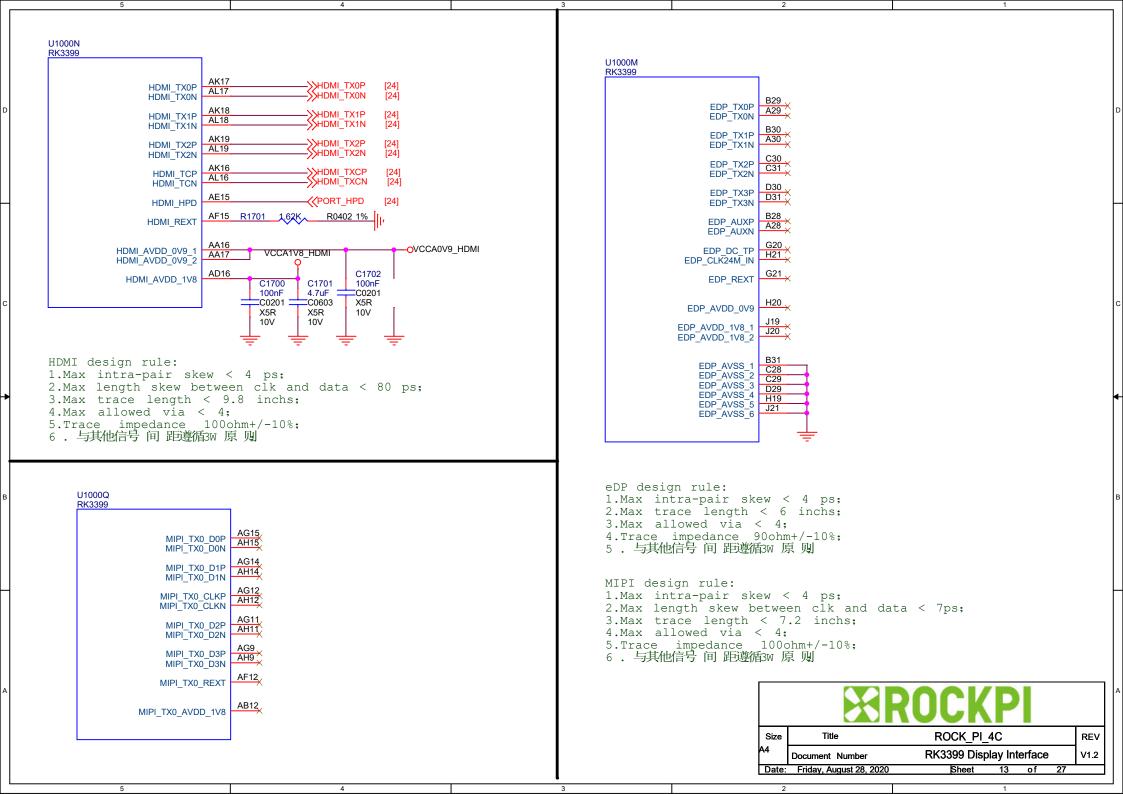


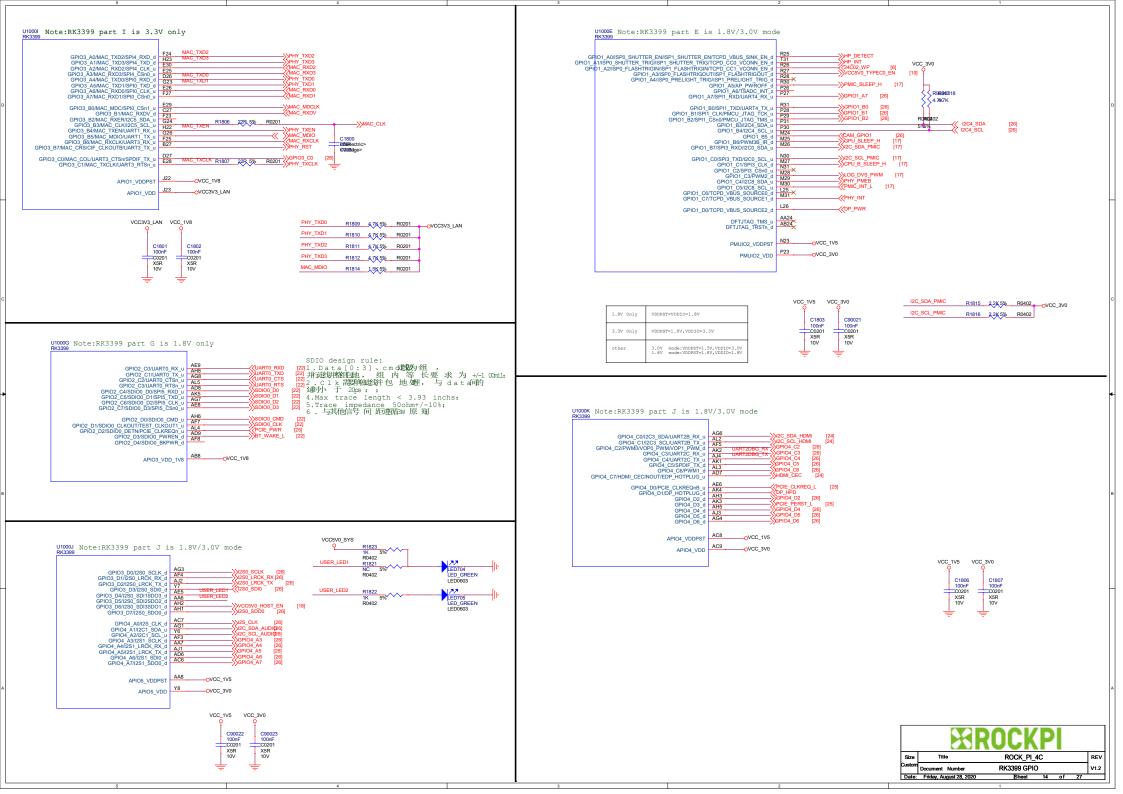
ADKEY_IN R1502 10K 1% OVCC_1V8

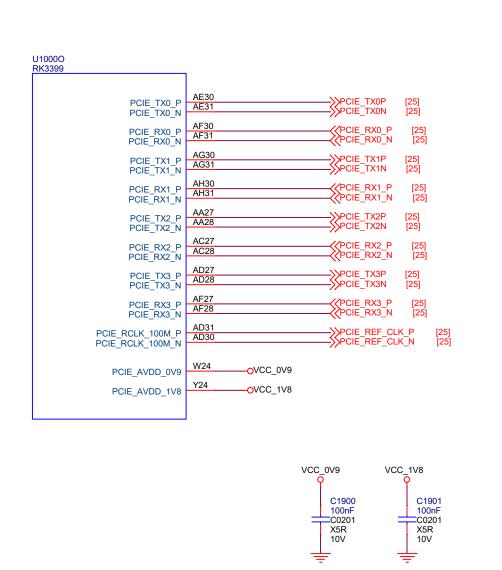


3 2









PCIE design rule: 1.Max intra-pair skew < 4ps; 2.Max inter-pair skew < 1.6 ns;
3.Max trace length < 14 inchs;</pre> 4.Max allowed via < 4; 5.Trace impedance 100ohm+/-10%; 6.与其他信号 间 距遵循3W 原 则

