Register Name	Address	Value (Hex)	Value (Decimal)	
ANALOG_GAIN_GLOBAL	0x0157	0x00	0	
COARSE_INTEGRATION_TIME_A	0x015A	0x0185	389	
FRM_LENGTH_A	0x0160	0x0189	393	this mode is line doubled
LINE_LENGTH_A	0x0162	0x0DE8	3560	
X_ADD_STA_A	0x0164	0x0168	360	
X_ADD_END_A	0x0166	0x0B67	2919	
Y_ADD_STA_A	0x0168	0x0200	512	
Y_ADD_END_A	0x016A	0x079F	1951	
x_output_size	0x016C	0x0500	1280	
y_output_size	0x016E	0x02D0	720	
X_ODD_INC_A	0x0170	0x01	1	
Y_ODD_INC_A	0x0171	0x01	1	
BINNING_MODE_H_A	0x0174	0x03	3	
BINNING_MODE_V_A	0x0175	0x03	3	
CSI_DATA_FORMAT_A	0x018C	0x0A0A	2570	
VTPXCK_DIV	0x0301	0x05	5	
VTSYCK_DIV	0x0303	0x01	1	
PREPLLCK_VT_DIV	0x0304	0x03	3	
PREPLLCK_OP_DIV	0x0305	0x03	3	
PLL_VT_MPY	0x0306	0x0035	53	
OPPXCK_DIV	0x0309	0x0A	10	
OPSYCK_DIV	0x030B	0x01	1	
PLL_OP_MPY	0x030C	0x0066	102	

Register Name	Address	Value (Hex)	Value (Decimal)
ANALOG_GAIN_GLOBAL	0x0157	0x00	0
COARSE_INTEGRATION_TIME_A	0x015A	0x036C	876
FRM_LENGTH_A	0x0160	0x0370	880
LINE_LENGTH_A	0x0162	0x0D78	3448
X_ADD_STA_A	0x0164	0x0168	360
X_ADD_END_A	0x0166	0x0B67	2919
Y_ADD_STA_A	0x0168	0x0200	512
Y_ADD_END_A	0x016A	0x079F	1951
x_output_size	0x016C	0x0500	1280
y_output_size	0x016E	0x02D0	720
X_ODD_INC_A	0x0170	0x01	1
Y_ODD_INC_A	0x0171	0x01	1
BINNING_MODE_H_A	0x0174	0x01	1
BINNING_MODE_V_A	0x0175	0x01	1
CSI_DATA_FORMAT_A	0x018C	0x0A0A	2570
VTPXCK_DIV	0x0301	0x05	5
VTSYCK_DIV	0x0303	0x01	1
PREPLLCK_VT_DIV	0x0304	0x03	3
PREPLLCK_OP_DIV	0x0305	0x03	3
PLL_VT_MPY	0x0306	0x0039	57
OPPXCK_DIV	0x0309	0x0A	10
OPSYCK_DIV	0x030B	0x01	1
PLL_OP_MPY	0x030C	0x0072	114

Register Name	Address	Value (Hex)	Value (Decimal)
ANALOG_GAIN_GLOBAL	0x0157	0x00	0
COARSE_INTEGRATION_TIME_A	0x015A	0x06DE	1758
FRM_LENGTH_A	0x0160	0x06E2	1762
LINE_LENGTH_A	0x0162	0x0D78	3448
X_ADD_STA_A	0x0164	0x02A8	680
X_ADD_END_A	0x0166	0x0A27	2599
Y_ADD_STA_A	0x0168	0x02B4	692
Y_ADD_END_A	0x016A	0x06EB	1771
x_output_size	0x016C	0x0780	1920
y_output_size	0x016E	0x0438	1080
X_ODD_INC_A	0x0170	0x01	1
Y_ODD_INC_A	0x0171	0x01	1
BINNING_MODE_H_A	0x0174	0x00	0
BINNING_MODE_V_A	0x0175	0x00	0
CSI_DATA_FORMAT_A	0x018C	0x0A0A	2570
VTPXCK_DIV	0x0301	0x05	5
VTSYCK_DIV	0x0303	0x01	1
PREPLLCK_VT_DIV	0x0304	0x03	3
PREPLLCK_OP_DIV	0x0305	0x03	3
PLL_VT_MPY	0x0306	0x0039	57
OPPXCK_DIV	0x0309	0x0A	10
OPSYCK_DIV	0x030B	0x01	1
PLL_OP_MPY	0x030C	0x0072	114

Register Name	Address	Value (Hex)	Value (Decimal)	
ANALOG_GAIN_GLOBAL	0x0157	0x00	0	
COARSE_INTEGRATION_TIME_A	0x015A	0x09BD	2493	
FRM_LENGTH_A	0x0160	0x09C1	2497	
LINE_LENGTH_A	0x0162	0x0D78	3448	this seems to be the preferred value in the datasheet (?)
X_ADD_STA_A	0x0164	0x0008	8	also sets B frame buffer to these dimensions too
X_ADD_END_A	0x0166	0x0CC7	3271	
Y_ADD_STA_A	0x0168	0x0000	0	
Y_ADD_END_A	0x016A	0x099F	2463	
x_output_size	0x016C	0x0CC0	3264	
y_output_size	0x016E	0x09A0	2464	
X_ODD_INC_A	0x0170	0x01	1	
Y_ODD_INC_A	0x0171	0x01	1	
BINNING_MODE_H_A	0x0174	0x00	0	
BINNING_MODE_V_A	0x0175	0x00	0	
CSI_DATA_FORMAT_A	0x018C	0x0A0A	2570	
VTPXCK_DIV	0x0301	0x05	5	
VTSYCK_DIV	0x0303	0x01	1	
PREPLLCK_VT_DIV	0x0304	0x03	3	
PREPLLCK_OP_DIV	0x0305	0x03	3	
PLL_VT_MPY	0x0306	0x0039	57	
OPPXCK_DIV	0x0309	0x0A	10	
OPSYCK_DIV	0x030B	0x01	1	
PLL_OP_MPY	0x030C	0x0072	114	

Register Name	Address	Value (Hex)	Value (Decimal)	Comment
ANALOG_GAIN_GLOBAL	0x0157	0x00	0	Default gain? whatever
COARSE_INTEGRATION_TIME_A	0x015A	0x01F5	501	Made this 4 less than FRM_LENGTH_A (what the datasheet says and the other modes do too)
FRM_LENGTH_A	0x0160	0x01F9	505	Page 56 of the datasheet has a formula. Went backwards with the pixel clock value (348800000Hz), the magic 3448 number below, and 200FPS (which should be the max given the pixel clock below). Removed the factor of 2 in the time per line the datasheet says since there's two bytes per pixel. 1/(200 * 3448 / 348800000)
LINE_LENGTH_A	0x0162	0x0D78	3448	Other modes have this; datasheet references this specific value a few times (this is apparently the minimum value)
X_ADD_STA_A	0x0164	0x0168	360	(Active pixels X (3280) – horizontal resolution x 4 (2560))/2
X_ADD_END_A	0x0166	0x0B67	2919	X_ADD_STA_A + horizontal resolution x 4 (2560) – 1
Y_ADD_STA_A	0x0168	0x0110	272	(Active pixels Y (2464) – vertical resolution x 4 (1920))/2
Y_ADD_END_A	0x016A	0x088F	2191	Y_ADD_STA_A + vertical resolution x 4 (1920) – 1
x_output_size	0x016C	0x0280	640	
y_output_size	0x016E	0x01E0	480	
X_ODD_INC_A	0x0170	0x01	1	Everything has this at 1, idk what other values would do
Y_ODD_INC_A	0x0171	0x01	1	
BINNING_MODE_H_A	0x0174	0x02	2	2 = bin 4x (combine groups of 16 pixels for one output pixel)
BINNING_MODE_V_A	0x0175	0x02	2	
CSI_DATA_FORMAT_A	0x018C	0x0A0A	2570	Might try to set to 0x0808 to see if we can get 8-bit output since we don't need 10-bit
VTPXCK_DIV	0x0301	0x05	5	
VTSYCK_DIV	0x0303	0x01	1	
PREPLLCK_VT_DIV	0x0304	0x03	3	
PREPLLCK_OP_DIV	0x0305	0x03	3	
PLL_VT_MPY	0x0306	0x006D	109	I think the max clock speed here is 350MHz (datasheet says 700 but that's really high so probably a factor of two in there somewhere), so 109 should give 348.8MHz based on the multiplier values in the other modes and the resulting clock speeds given in the device tree file. 182.4MHz / 57 * 109 = 348.8MHz
OPPXCK_DIV	0x0309	0x0A	10	
OPSYCK_DIV	0x030B	0x01	1	
PLL_OP_MPY	0x030C	0x00DA	218	2x PLL_VT_MPY seems to work
		1F5	501	