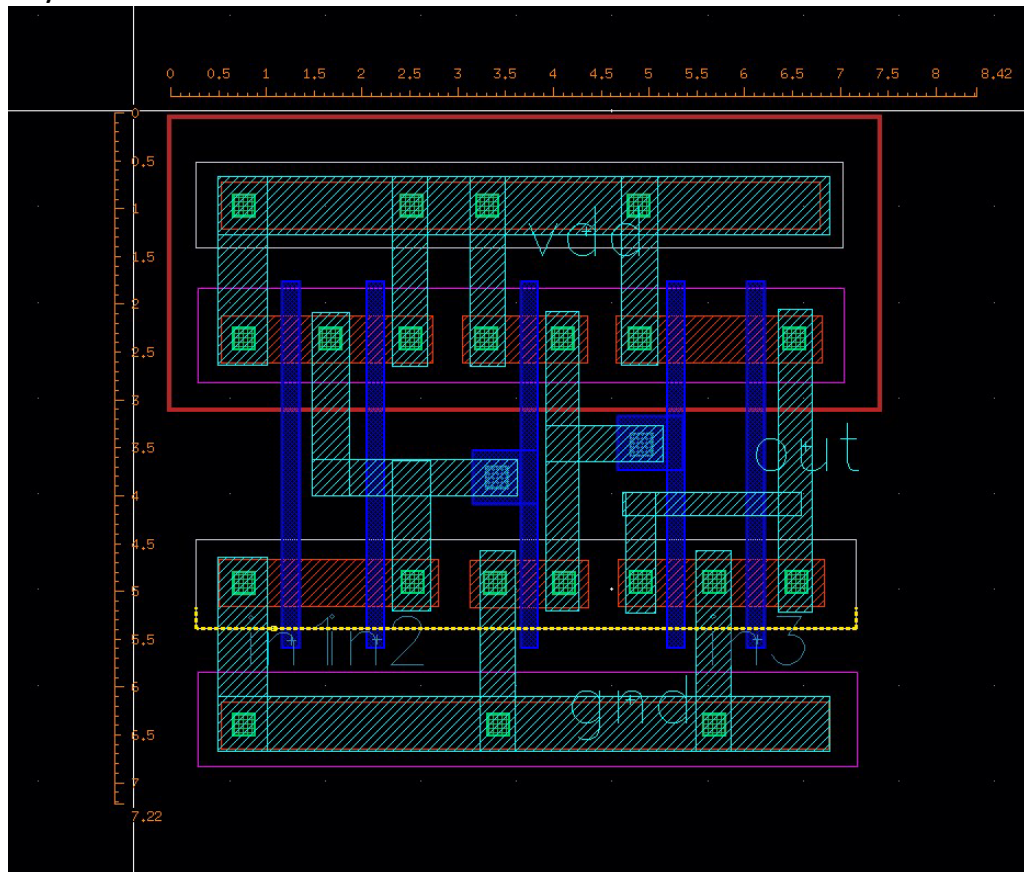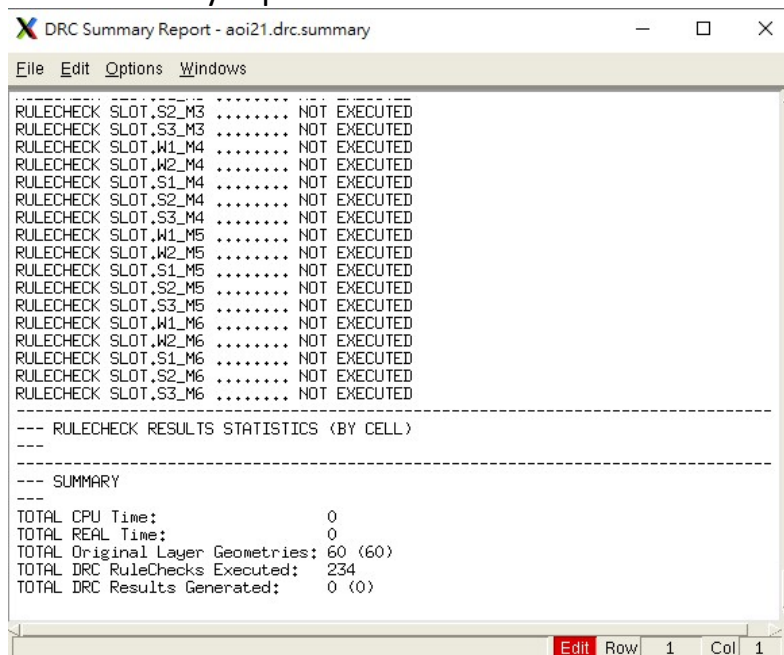# 積體電路設計 HW1 Report

108062135 呂佳恩
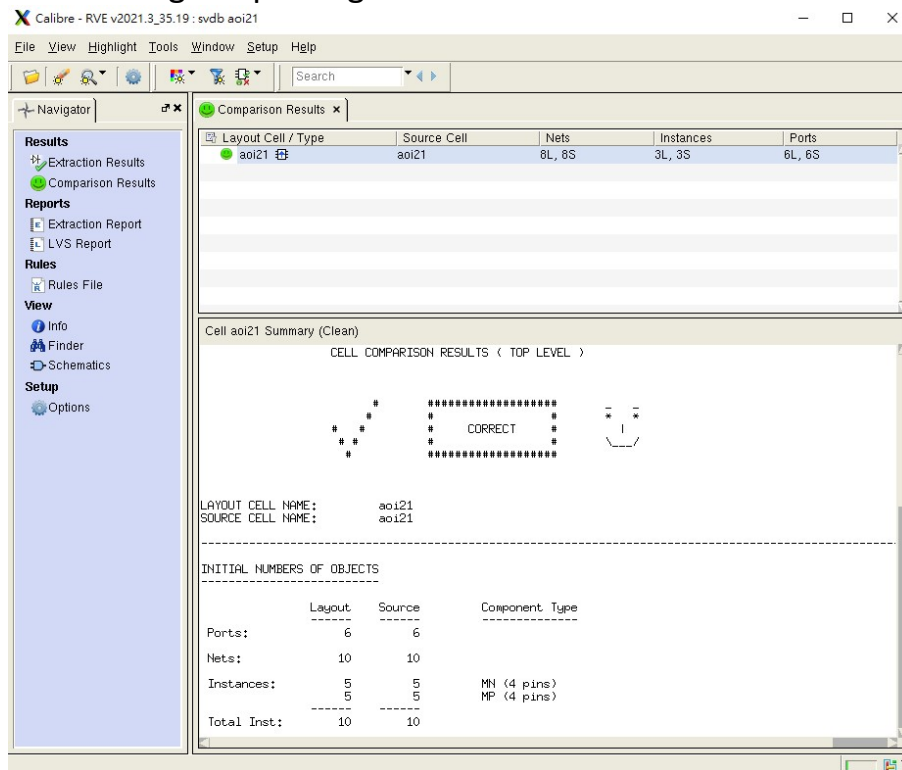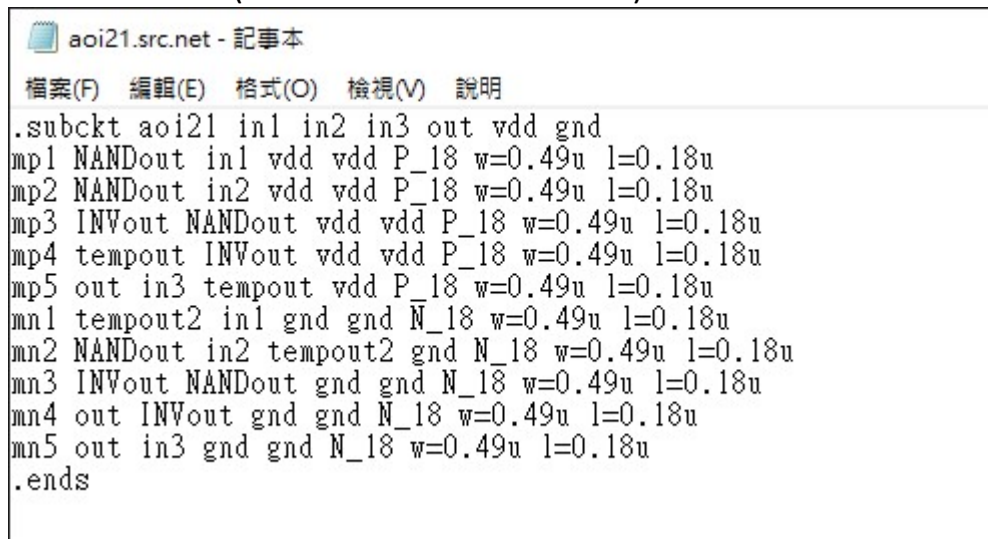
1. Screenshots
   (1) Layout with Rulers

   (2) DRC summary report

(3) The message of passing LVS

(4) LVS schematic (screenshot of the text file)

2. What else did you do to enhance your layout quality

First, I drew the three gates individually, then connected the vdd, gnd together. I tried to find routes so that the wires could be ran parallel to each other. This way, the width of the layout would significantly decrease.

I also calculated the minimum requirements of the width, height for each part in the layout, although the final result might not be precisely the minimum possible since dragging the layout would be much more difficult since it has to be super precise.

3. What have you learned from this homework

This homework gave me a grasp on how hard designing a layout manually is. You have to consider so many factors, also, one suboptimal placement of a component of the layout might result in the whole layout to be significantly worse, since the effect of the placement might compound if the design is complex.

This homework also taught me how to use Virtuoso and the tools it provided, it provides a intuitive process for designing layouts. Also, throughout the homework, it made us be able to solve the problems we encountered, which is always a valuable experience.

4. What problems have you encountered in this homework

The first problem I encountered is that when I want to improve my design of the layout, it would affect other parts of the design since it might affect the distance between components and violate the Design Rule Check.

The second problem I encountered is that the LVS schematic. It was super confusing how it should be written, but after some trial and error, the problems were all solved.2135