Report 2

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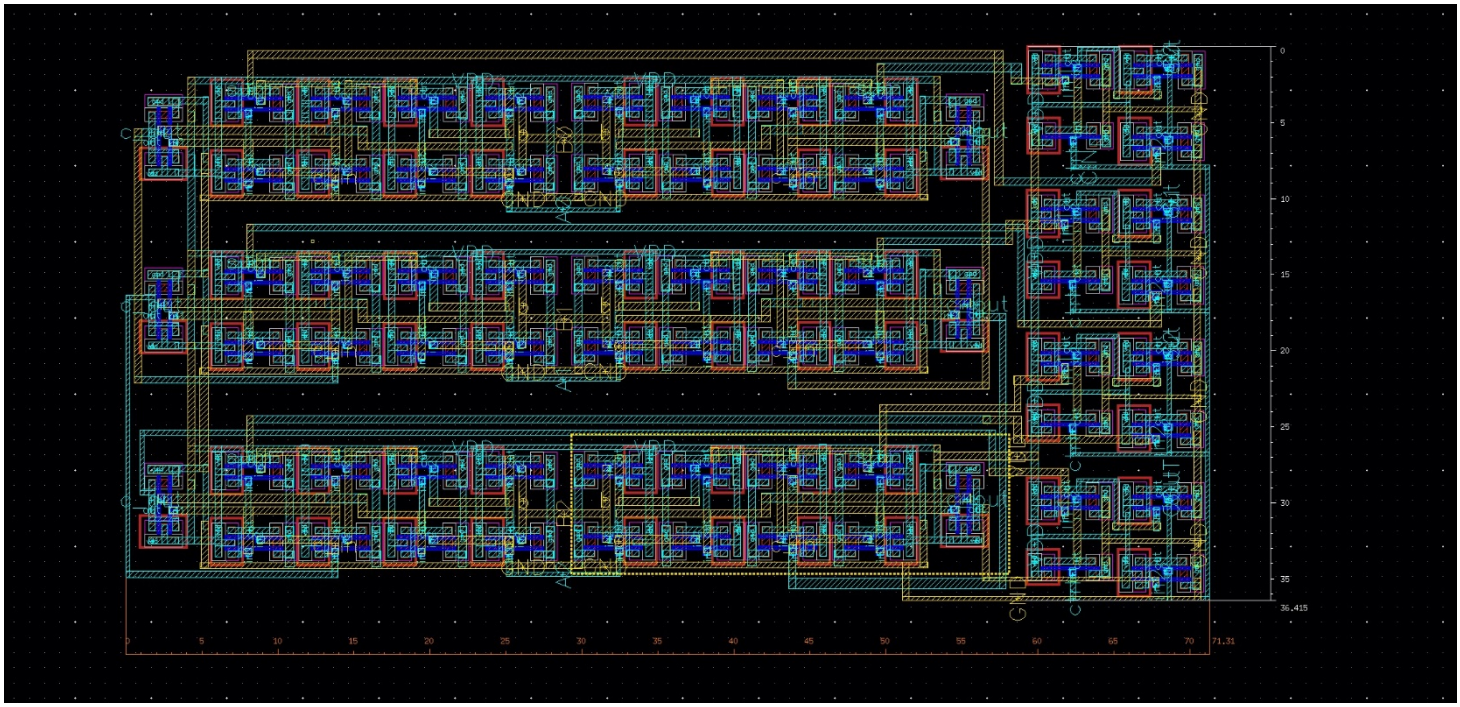
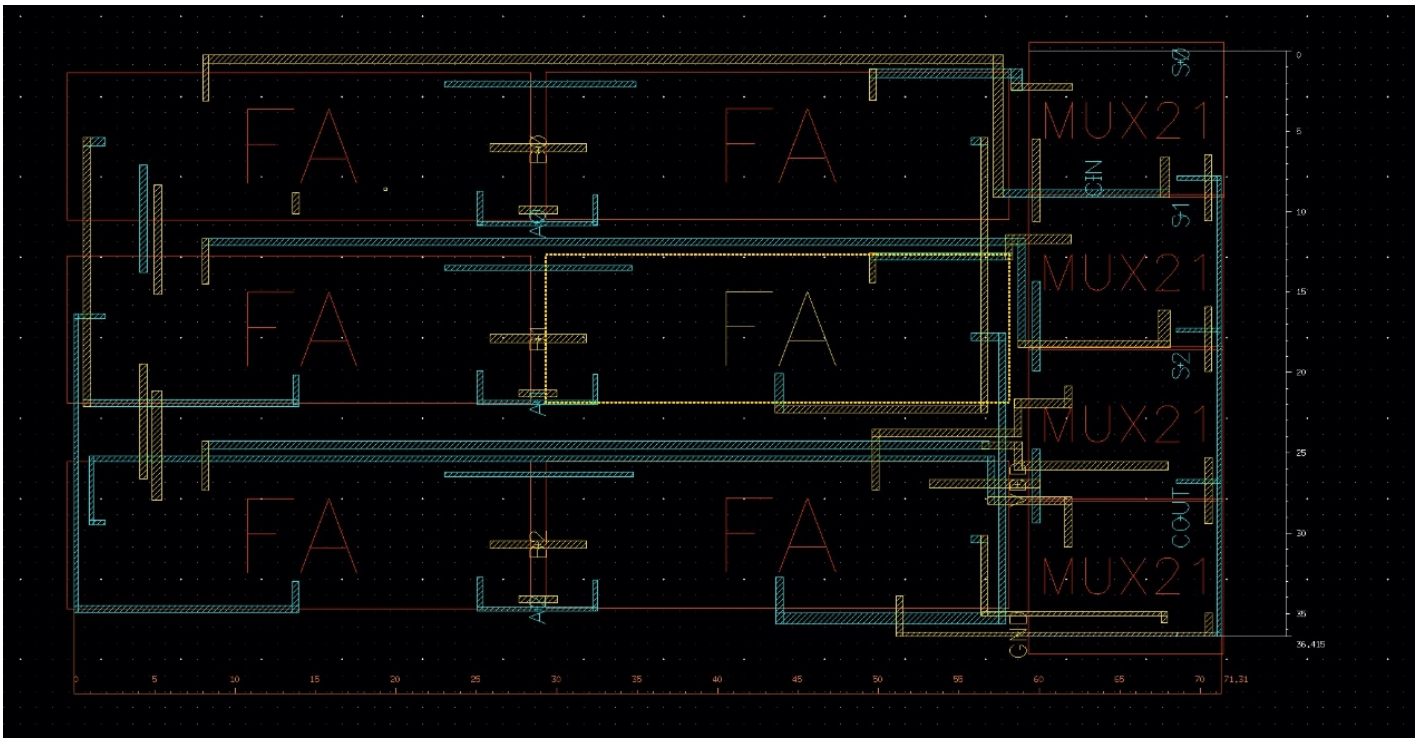
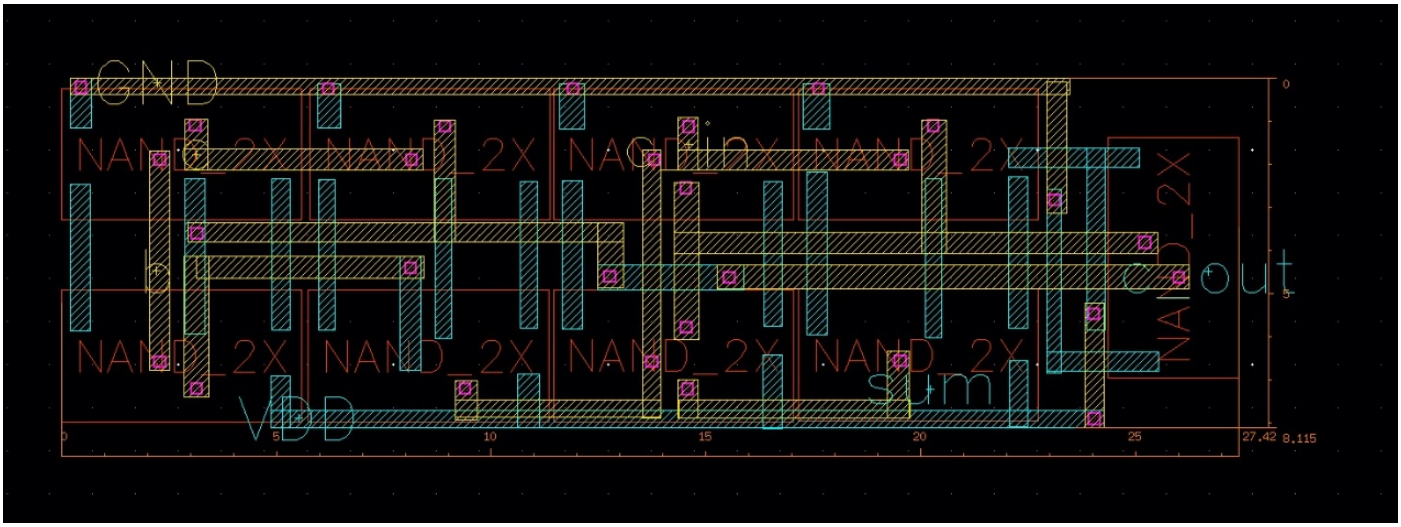
1. Screenshots

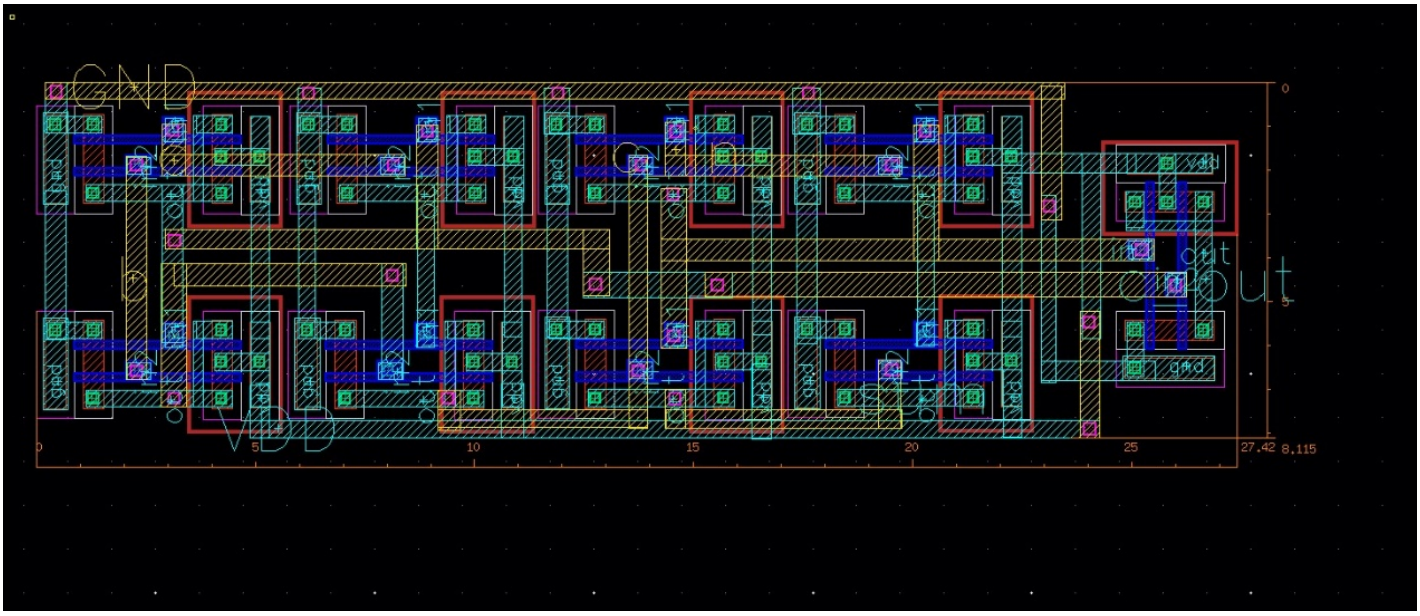
   Screenshot of ADDER3



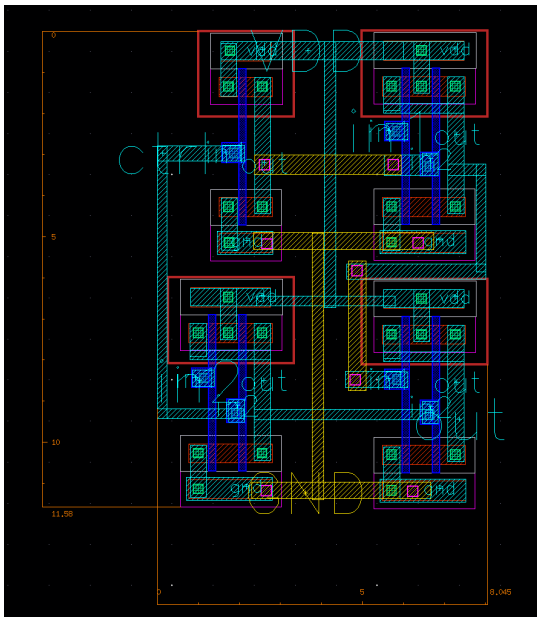


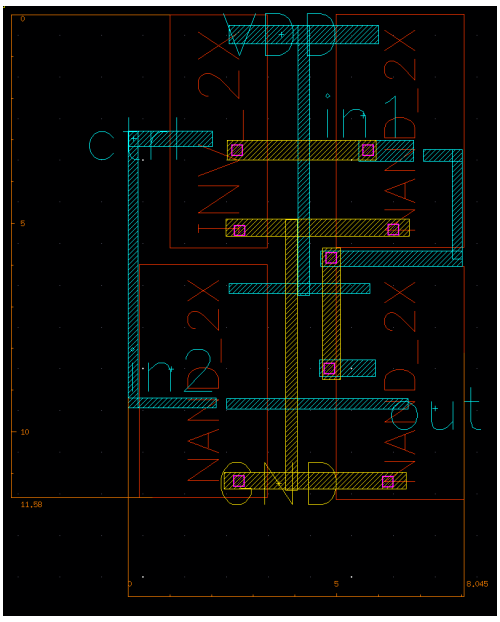
Screenshot of FA



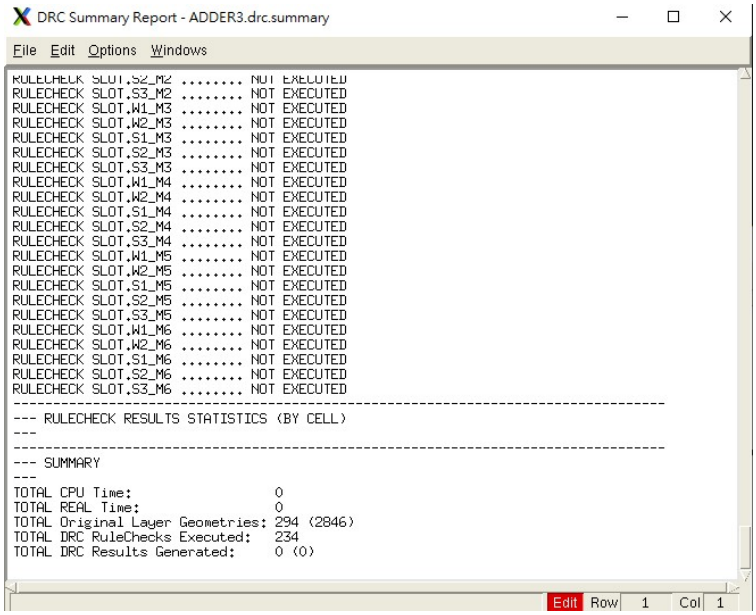


Screenshot of MUX

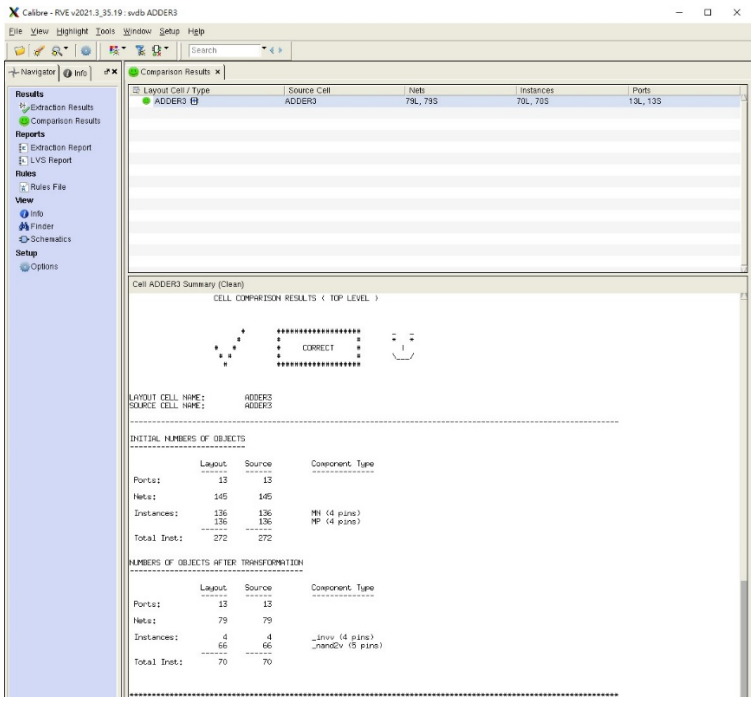




Screenshot of DRC summary report



Screenshot of LVS report



Screenshot of LVS schematic of Adder3.src.net

ADDER3.src.net - 記事本

檔案(F) 編輯(E) 格式(O) 檢視(V) 說明

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.subckt ADDER3 A0 A1 A2 B0 B1 B2 CIN S0 S1 S2 COUT VDD GND
x_FA1          A0      B0      GND     SUM0    COUT0   VDD     GND     FA
x_FA2          A1      B1      COUT0   SUM1    COUT1   VDD     GND     FA
x_FA3          A2      B2      COUT1   SUM2    COUT2   VDD     GND     FA
x_FA4          A0      B0      VDD     SUM00   COUT00  VDD     GND     FA
x_FA5          A1      B1      COUT00  SUM11   COUT11  VDD     GND     FA
x_FA6          A2      B2      COUT11  SUM22   COUT22  VDD     GND     FA
x_MUX1         COUT2   COUT22  CIN     COUT    VDD     GND     MUX21
x_MUX2         SUM00   SUM0    CIN     S0      VDD     GND     MUX21
x_MUX3         SUM11   SUM1    CIN     S1      VDD     GND     MUX21
x_MUX4         SUM22   SUM2    CIN     S2      VDD     GND     MUX21
.ends

.subckt FA a b c_in sum c_out VDD GND
x_NAND1        a       b       tmp1    VDD     GND     NAND_2X
x_NAND2        a       tmp1    tmp2    VDD     GND     NAND_2X
x_NAND3        b       tmp1    tmp3    VDD     GND     NAND_2X
x_NAND4        tmp2    tmp3    tmp4    VDD     GND     NAND_2X
x_NAND5        tmp4    c_in    tmp5    VDD     GND     NAND_2X
x_NAND6        tmp4    tmp5    tmp6    VDD     GND     NAND_2X
x_NAND7        tmp5    c_in    tmp7    VDD     GND     NAND_2X
x_NAND8        tmp6    tmp7    sum     VDD     GND     NAND_2X
x_NAND9        tmp5    tmp1    c_out   VDD     GND     NAND_2X
.ends

.subckt MUX21 in1 in2 ctrl out VDD GND
x_in1_ctrlinv_nand      in1       ctrl_inv_out   sel1_out       VDD     GND     NAND_2X
x_invl                  ctrl      ctrl_inv_out                  VDD     GND     INV_2X
x_in2_ctrl_nand         in2       ctrl           sel2_out       VDD     GND     NAND_2X
x_sel12_nand            sel1_out  sel2_out       out            VDD     GND     NAND_2X
.ends

.subckt NAND_2X in1 in2 out vdd gnd
mp1 out in1 vdd vdd P_18 w=0.47u l=0.18u
mp2 out in2 vdd vdd P_18 w=0.47u l=0.18u
mn1 net in1 gnd gnd N_18 w=0.47u l=0.18u
mn2 out in2 net gnd N_18 w=0.47u l=0.18u
.ends

.subckt INV_2X in out vdd gnd
mp1 out in vdd vdd P_18 w=0.47u l=0.18u
mn1 out in gnd gnd N_18 w=0.47u l=0.18u
.ends
```

2. What else did I do to enhance my layout quality?

   I started with the idea of making the design of FA and MUX easy to use in FA, so the output placement was crucial when I began the design. Also, the VDD and GND placement was place into consideration when the initial design was started. Also, I sometimes flipped the design as it would benefit the routing of the total design.

3. What have you learned from this homework?

   I have a deep understanding of how Virtuoso works, and during the process of doing the homework, I have a better understanding of all things that need to be considered when doing designs, it made me appreciate the work of others more.

4. What problems have you encountered in this homework?

   The main problem I encountered is that I don't know whether a placement would cause problems in the future or not. Also, small problems cascade into bigger ones as the layout scales. This made me have to go back to re-arrange the layouts that I first placed again and again, which was very time consuming.