Chapter 1

Logic Design with MOSFET

何宗易

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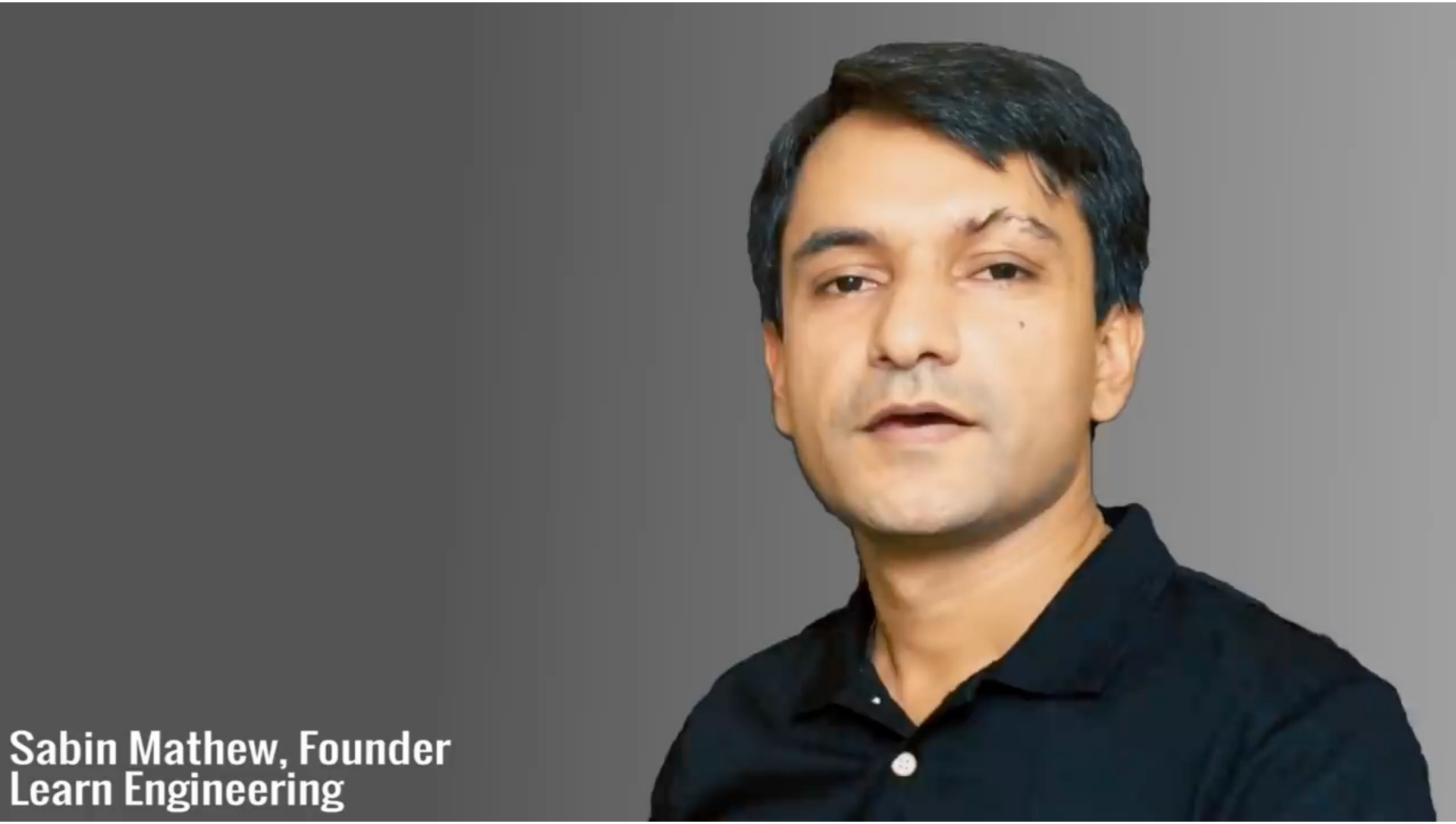
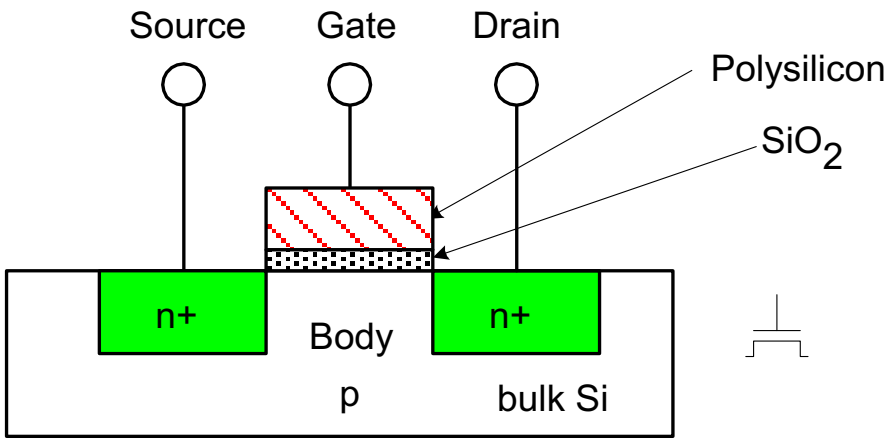

Sabin Mathew, Founder
Learn Engineering

nMOS Transistor

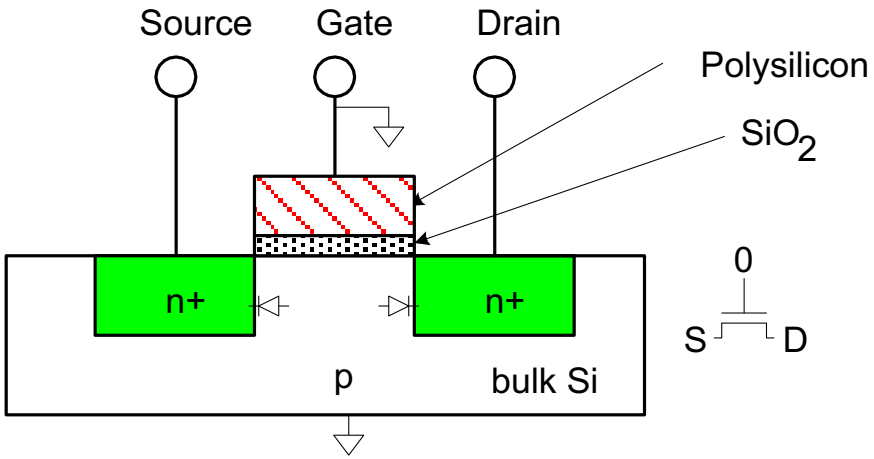
- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal*



* Metal gates are returning today!

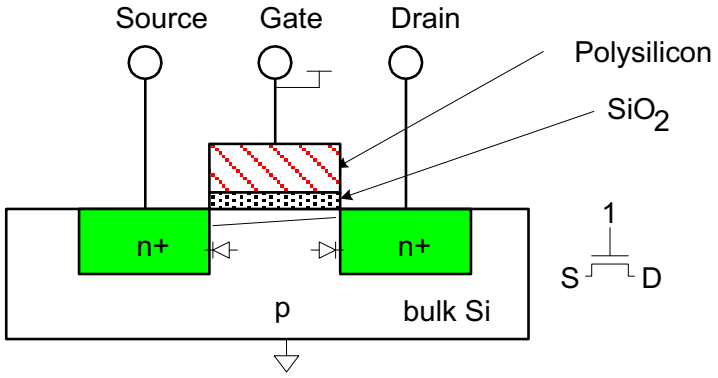
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



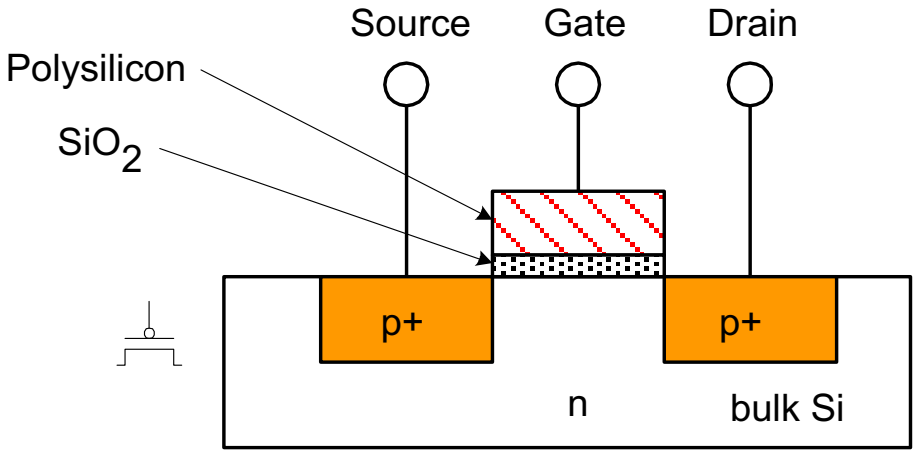
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



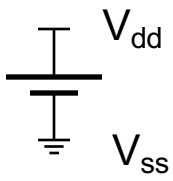
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

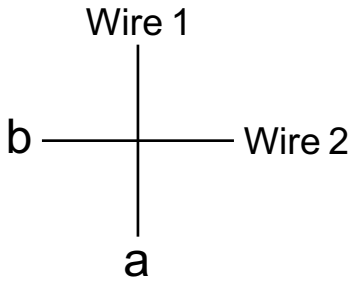


Signals and Wires

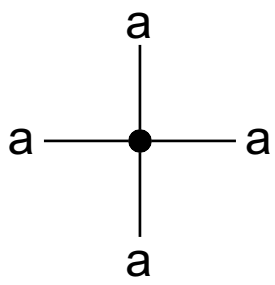
- Signals
  - 0 = V_{ss}= Ground = GND = Low = 0V
  - 1 = V_{dd} = Power = PWR = High = 5V, 3.3V, 1.5V, 1.2V, 1.0V, etc.



- Wires



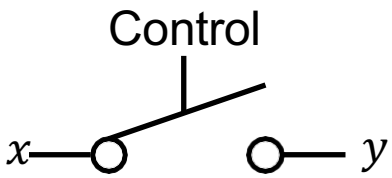
No connection



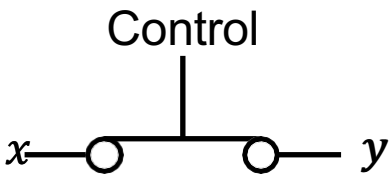
Connection

Ideal Switches

- Switch

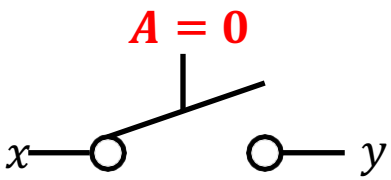


Electrically **open**

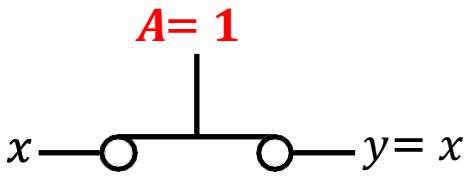


Electrically **short**

- Assert-high switch (nMOS)

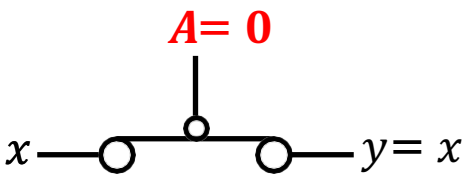


Open (y is **undefined**)

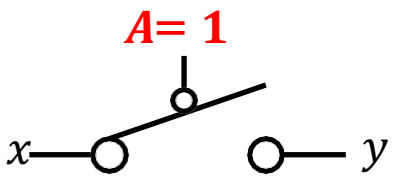


Closed ($y = x$)

- Assert-low switch (cMOS)



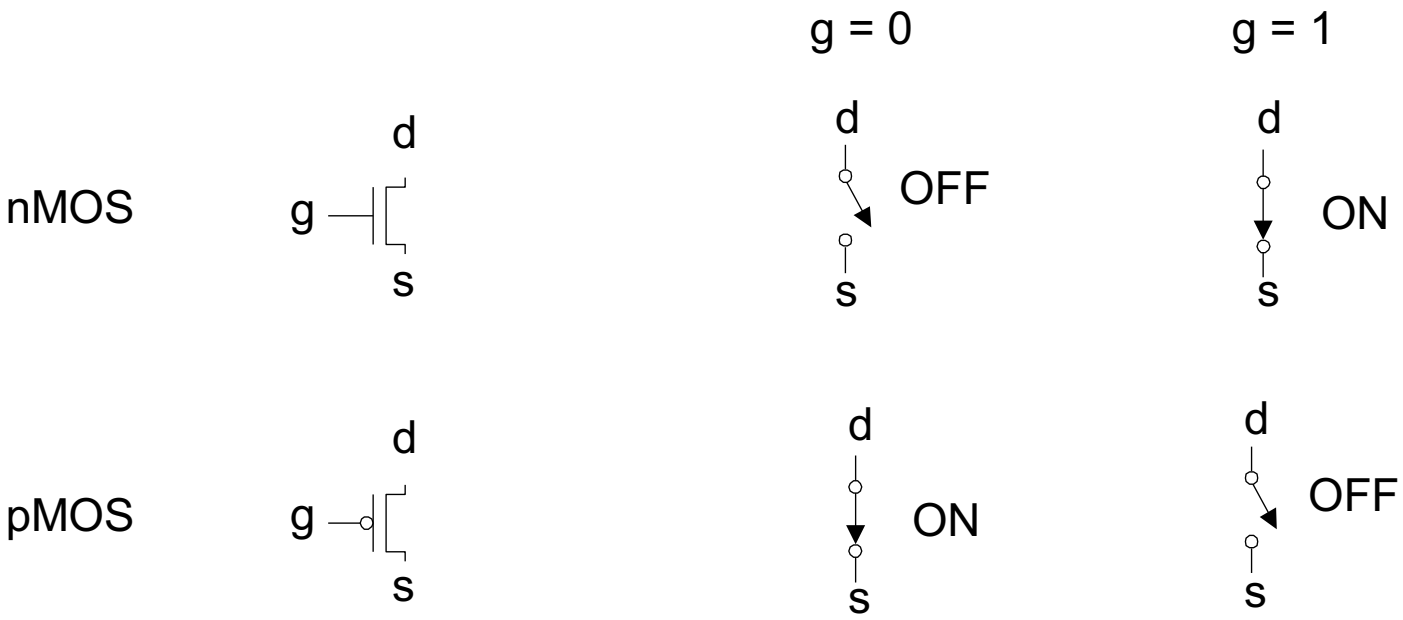
Closed ($y= x$)



Open (y is **undefined**)

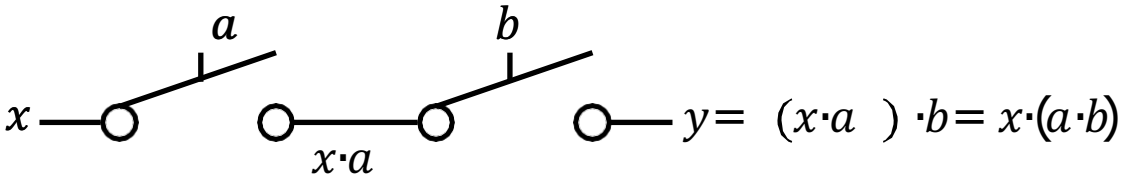
Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



Series/Parallel Connections of Switches

- Series



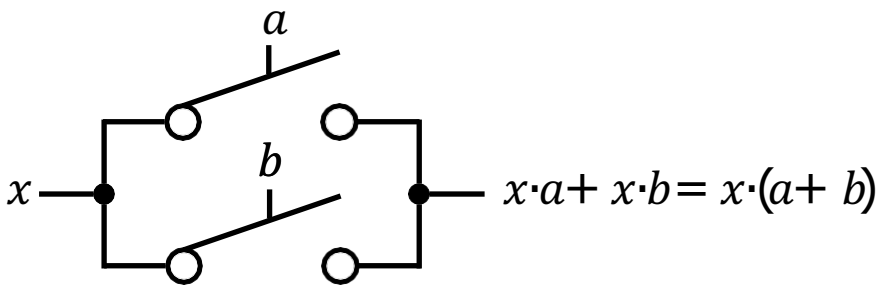
AND operation

(y is defined only when $a = 1$ and $b = 1$)

(y is undefined if $a = 0$ or $b = 0$)

a	b	y
0	0	undefined
0	1	
1	0	
1	1	x

- Parallel



OR operation

(y is defined only when $a = 1$ or $b = 1$)

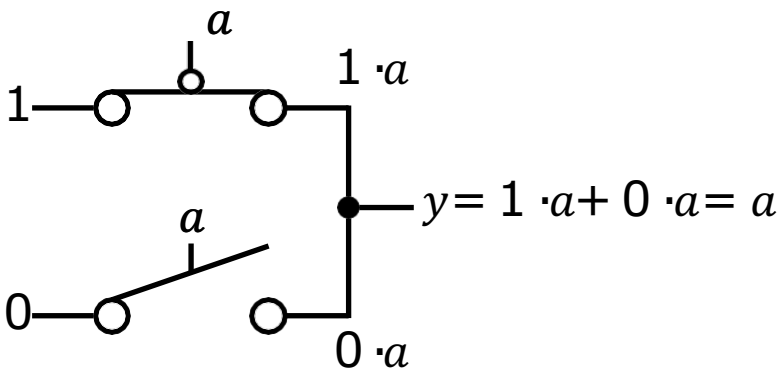
(y is undefined if $a = 0$ and $b = 0$)

a	b	y
0	0	undefined
0	1	x
1	0	
1	1	

Inverter Design with Switches

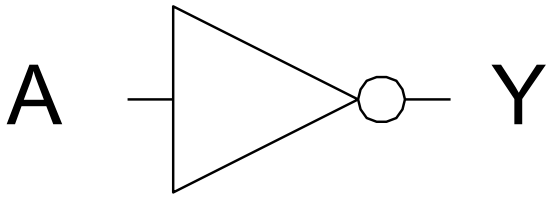
- Inverter
  - The output is defined both when $a = 0$ and when $a = 1$.

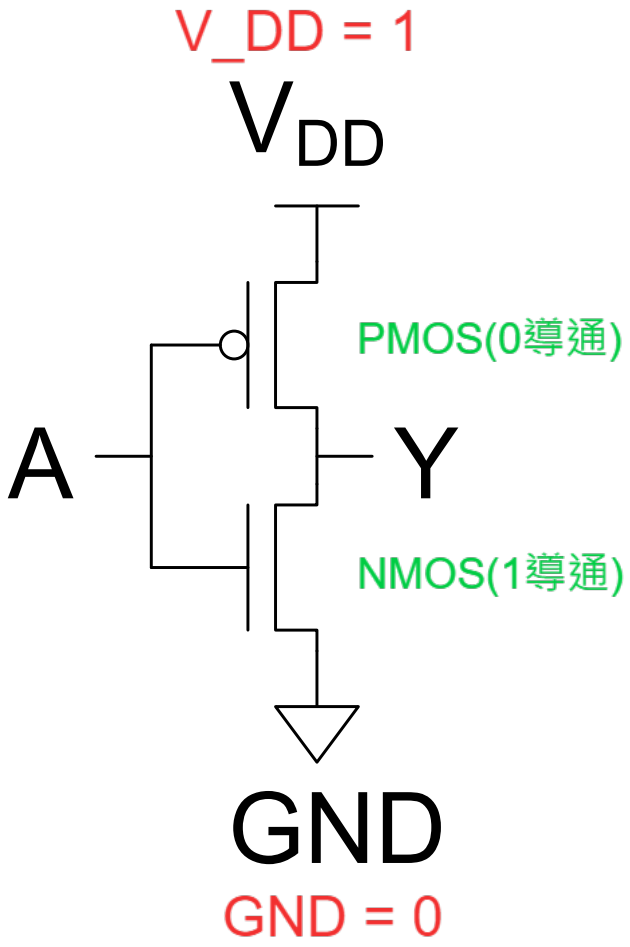
a	y
0	1
1	0



CMOS Inverter

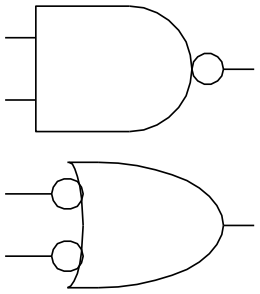
A	Y
0	1
1	0

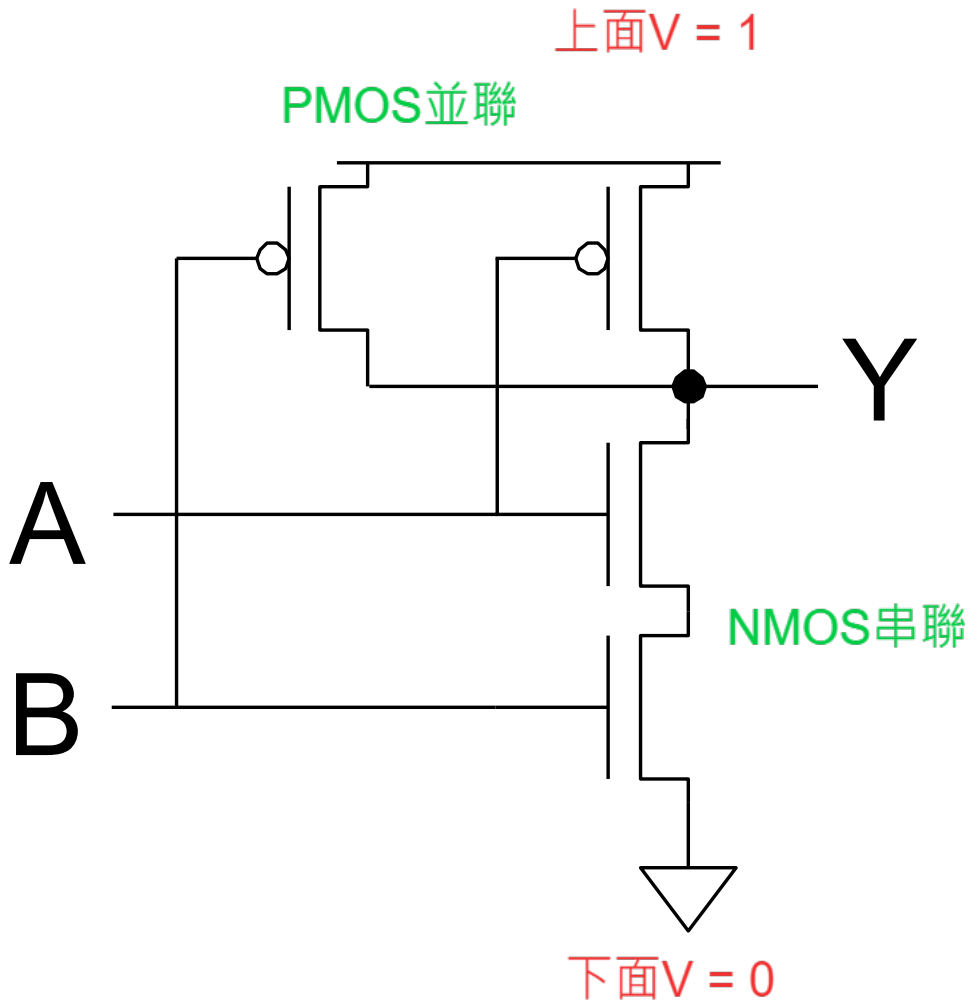




CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

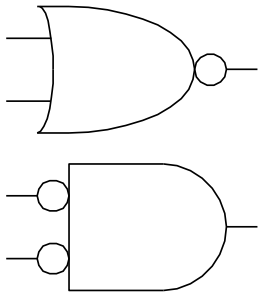


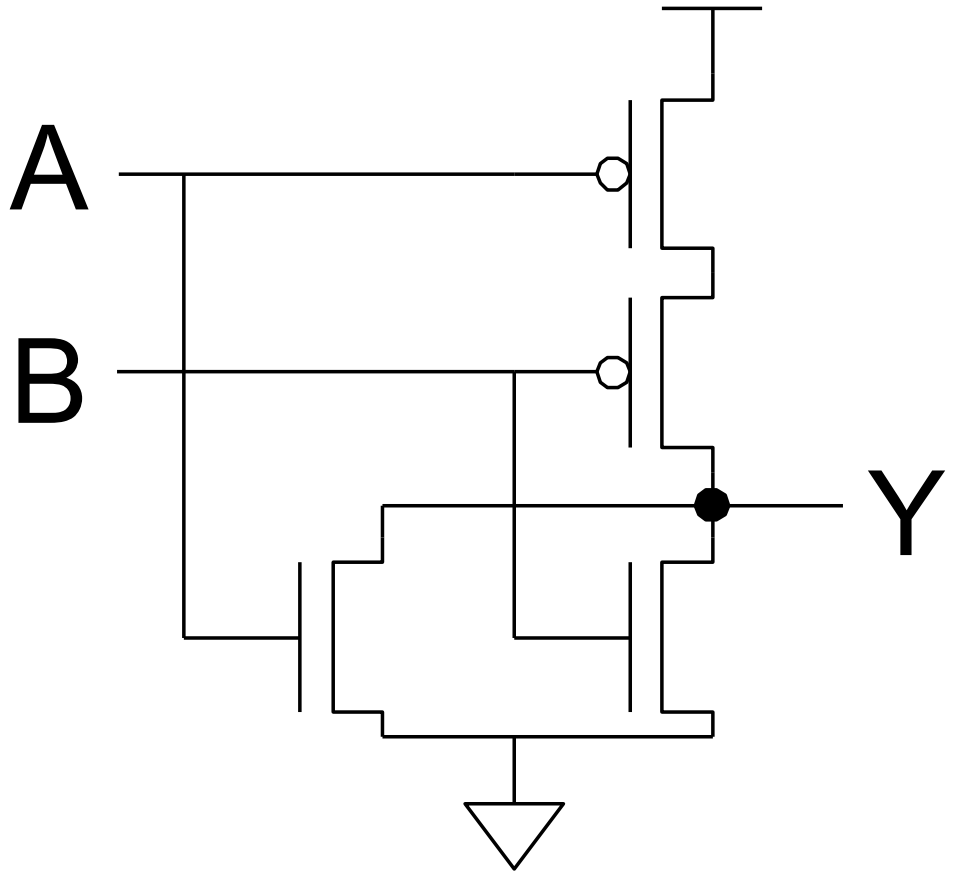


CMOS NOR Gate

(上面接V_DD一定是PMOS, 下面GND一定是NMOS)

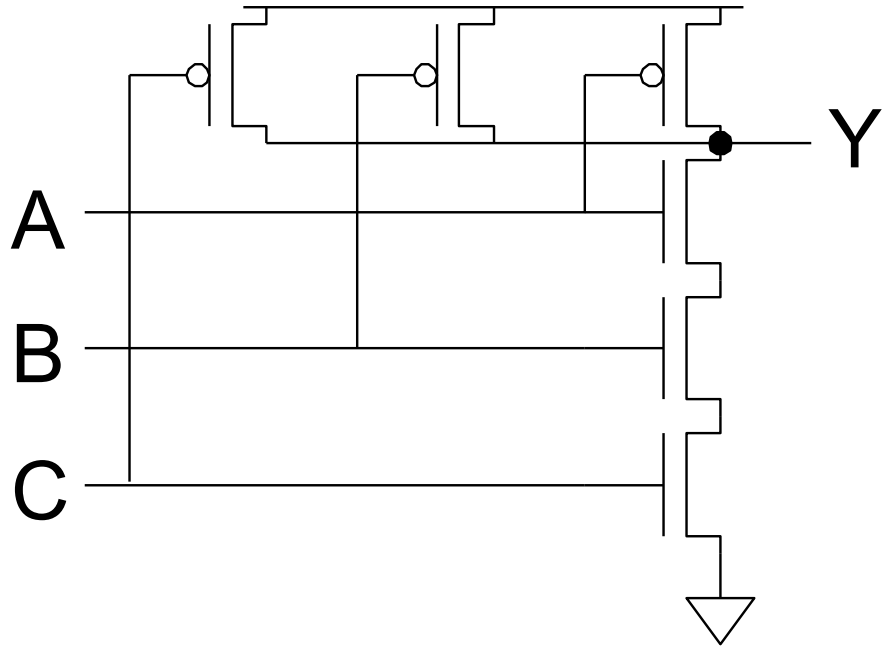
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





3-input NAND Gate

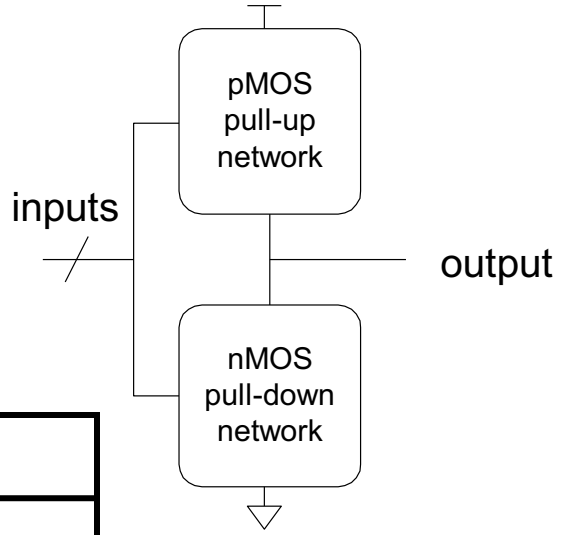
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



Complementary CMOS

- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS

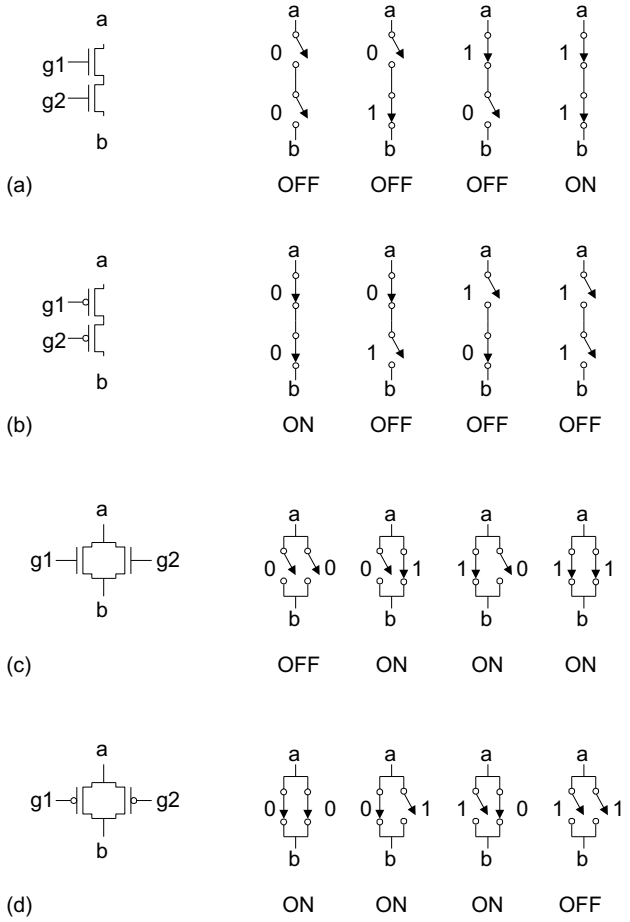
pull-down: GND
pull-up: V_DD



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

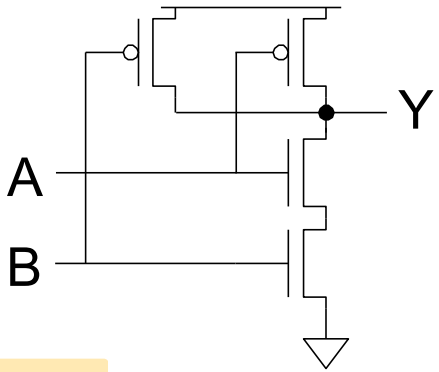
Series and Parallel

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON



Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS

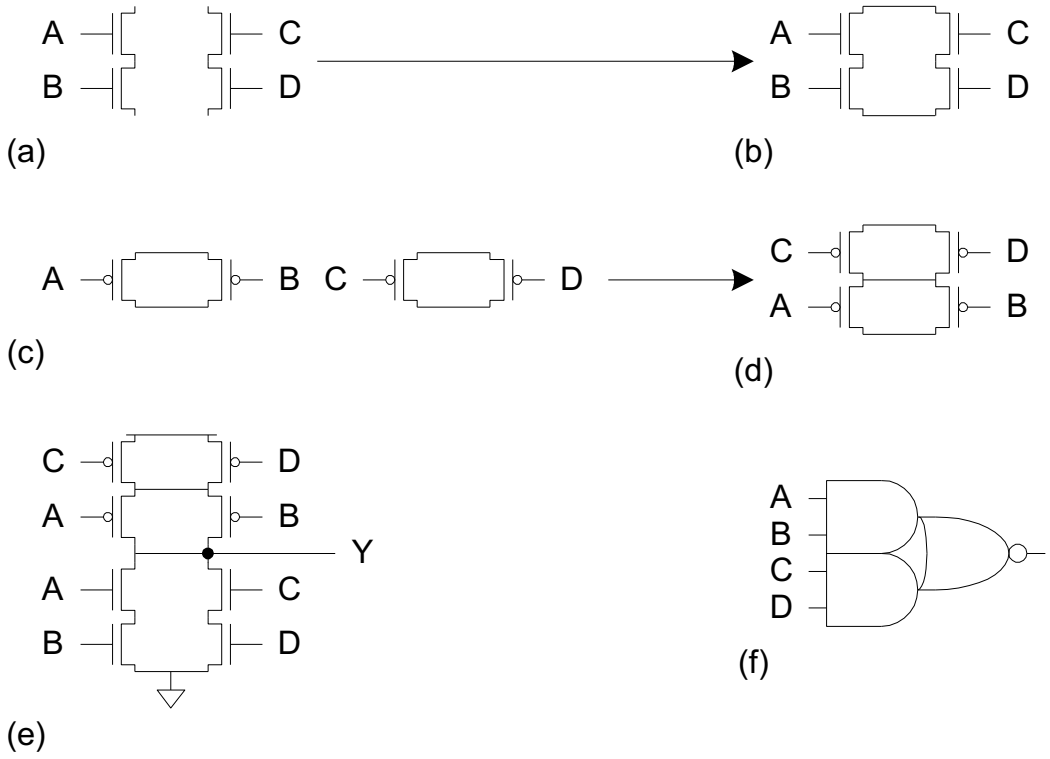


- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

Compound Gates

- *Compound gates* can do any inverting function
- Ex:

$$Y = \overline{A \bullet B + C \bullet D}$$ (AND-AND-OR-INVERT, AOI22)

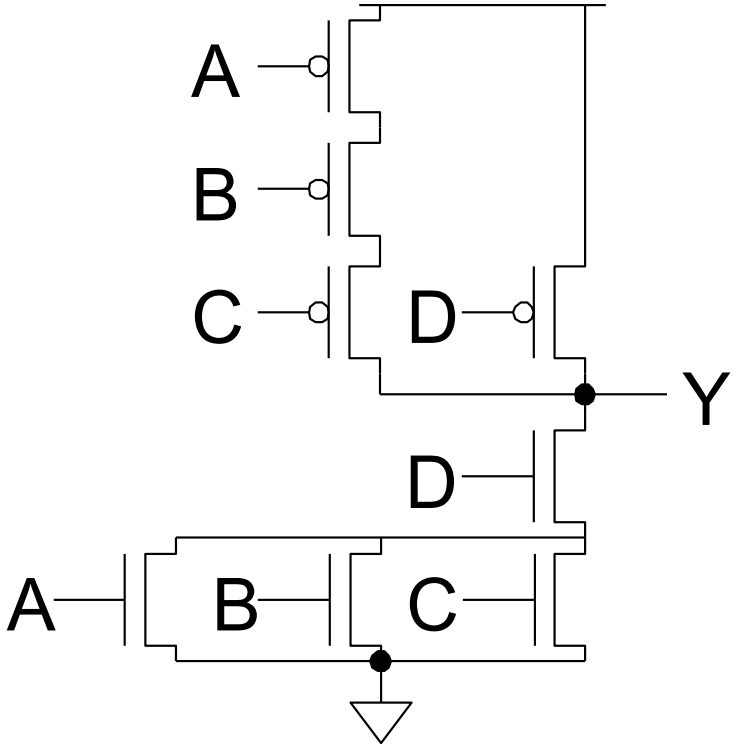


(1) ignore complement, 然後做complement底下的expression=>NMOS
(2) PMOS則做相反
=> and改or, or改and

Example: O3AI

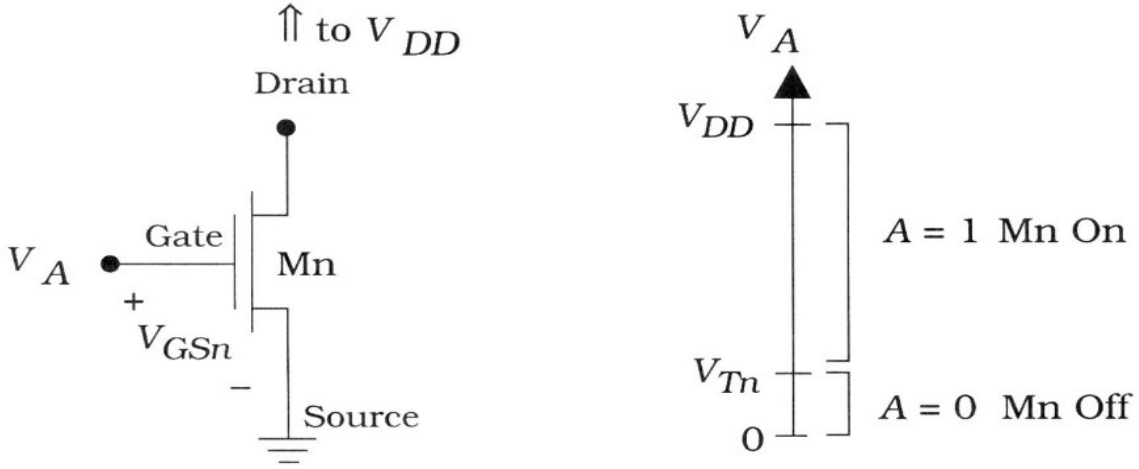
- $$Y = \overline{(A + B + C) \bullet D}$$

(1) ignore complement，做 (A+B+C)・D => NMOS
(2) 接著做PMOS => or改and, and改or => (A・B・C) + D



nFET Threshold voltages

- MOSFET has a characterizing parameter called the **threshold voltage** V_T.
- V_T is established during manufacturing process and is assumed to be a given value to the designer.
- nFET has a threshold voltage V_{Tn} a positive number (0.5V~0.7V).



(a) Gate-source voltage (b) Logic translation

Figure 2.14 Threshold voltage of an nFET

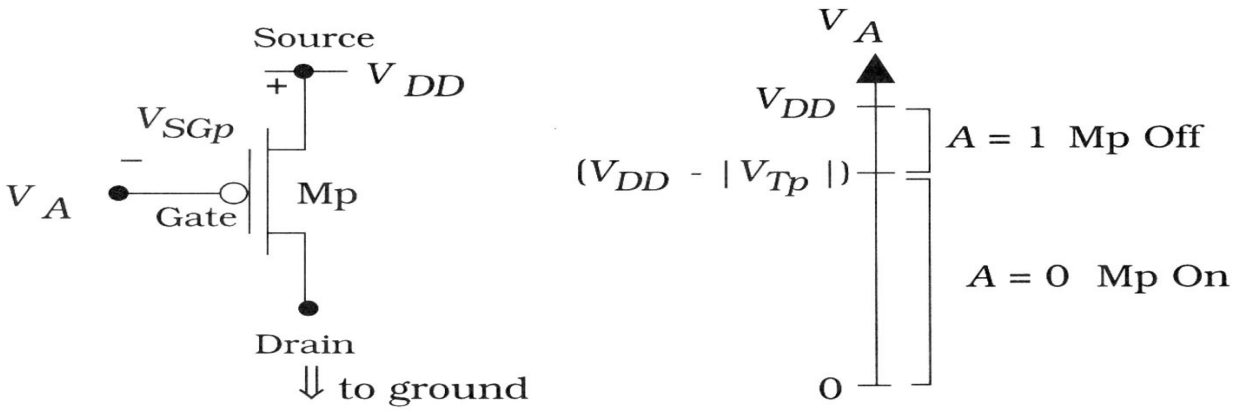
nFET Threshold voltages

- If $V_{GSn} \leq V_{Tn}$ the transistor acts like an open circuit. A transistor is OFF.
  - The drain terminal is the one close to Vdd and the source terminal is the one connected to Gnd.

- If $V_{GSn} \geq V_{Tn}$ the nFET drain and source are connected. A transistor is ON.

pFET Threshold voltages

- A pFET behaves in a complementary manner. V_{Tp} is a negative number (-0.5V~-0.8V). We use $V_{SGp}= -V_{GSp}$
- If $V_{SGp} \leq |V_{Tp}|$, the transistor acts like an open circuit. A transistor is OFF.
- If $V_{SGp} \geq |V_{Tp}|$, the pFET drain and source are connected. A transistor is ON.

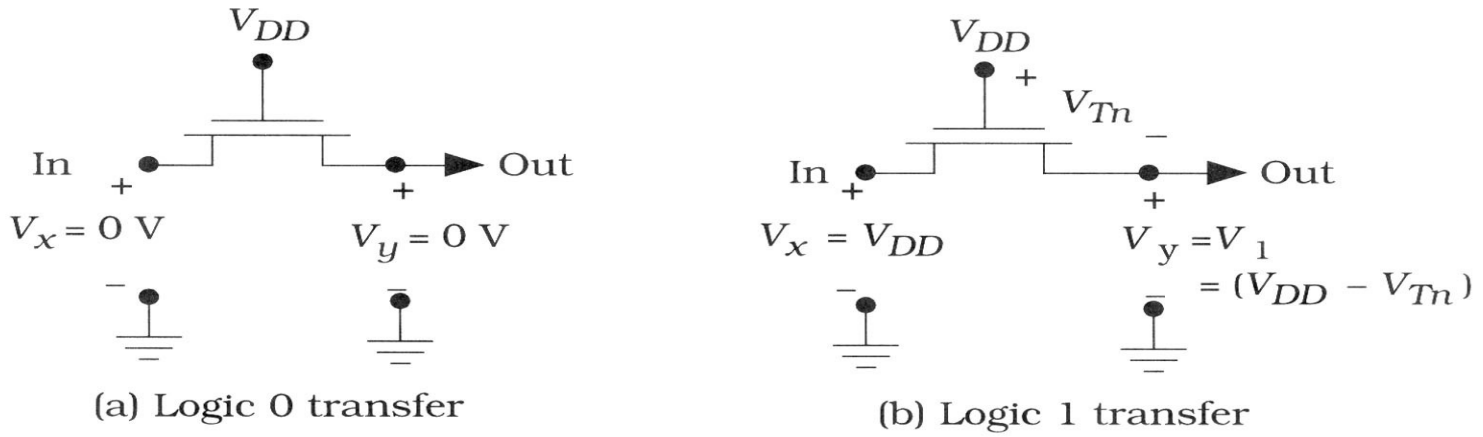


(a) Source-gate voltage (b) Logic translation

Figure 2.15 pFET threshold voltage

Pass Characteristics (nFET)

- Ideal electrical switch can pass any voltage.
- The pass characteristics of nFET.
  - Fig 2.16a, a logic 0 is connected from left to the right.
  - Fig 2.16b, a VDD is applied in the left. The output voltage is reduced to a value V_{DD}-V_{Tn}. (Threshold voltage loss)
  - nFET can only pass a weak logic 1 but strong logic 0.



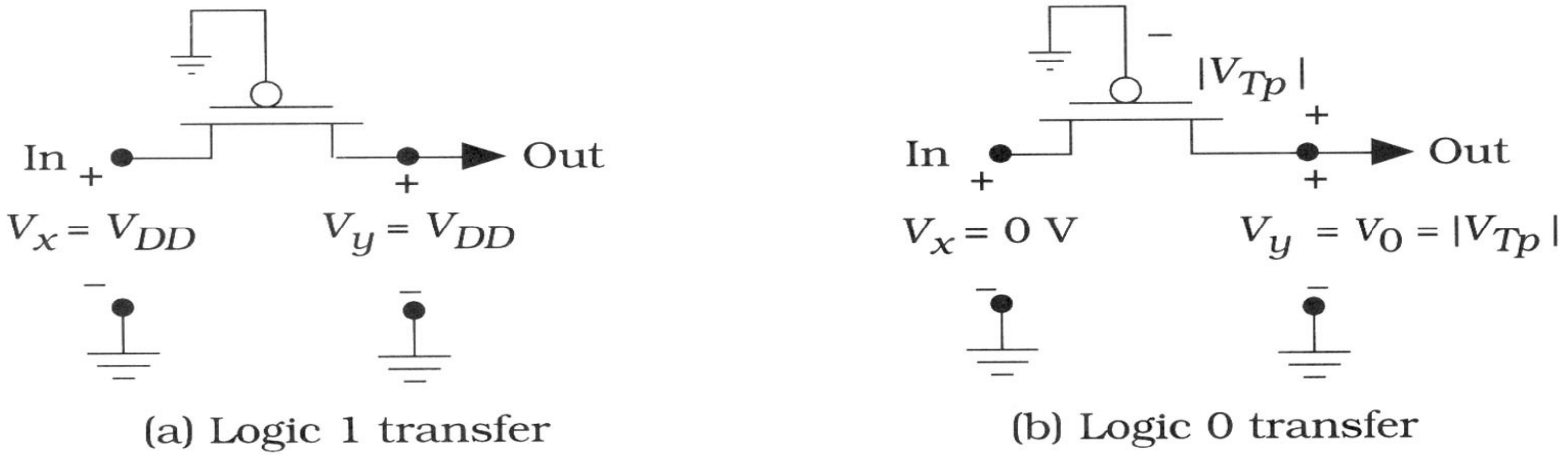
(a) Logic 0 transfer

(b) Logic 1 transfer

Figure 2.16 nFET pass characteristics

Pass Characteristics (pFET)

- The pass characteristics of pFET.
  - Fig 2.17a, a logic 1 is connected from left to the right.
  - Fig 2.17b, a VSS is applied in the right. The output voltage drops to a value $|V_{Tp}|$ (Threshold voltage loss)
  - pFET can only pass a weak logic 0 but strong logic 1.



(a) Logic 1 transfer

(b) Logic 0 transfer

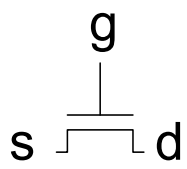
Figure 2.17 pFET pass characteristics

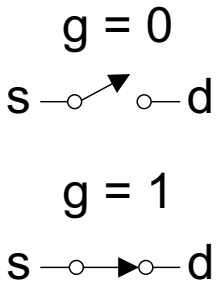
Signal Strength

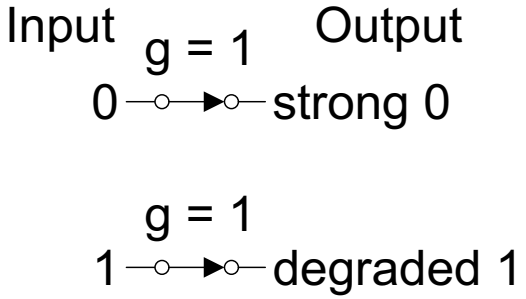
- *Strength* of signal
  - How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus nMOS are best for pull-down network

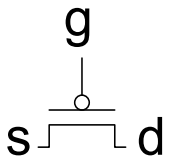
Pass Transistors

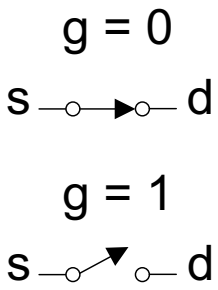
- Transistors can be used as switches

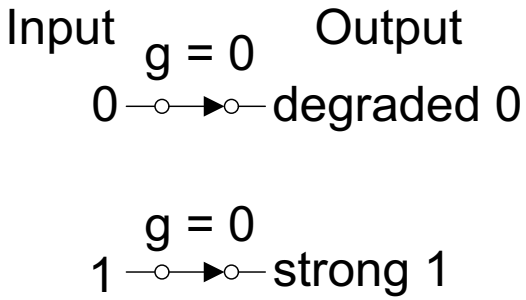








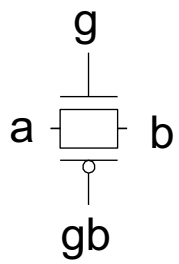




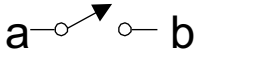
Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both 0 and 1 well

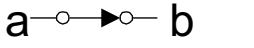
NMOS, PMOS串在一起, g跟gb為dual訊號



g = 0, gb = 1

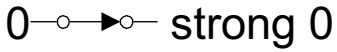


g = 1, gb = 0

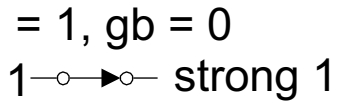


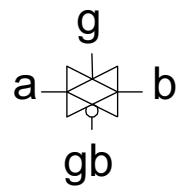
Input Output

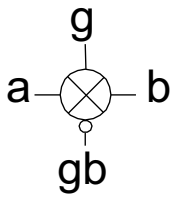
g = 1, gb = 0

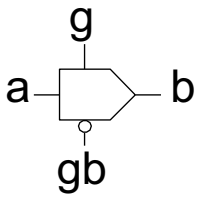


g = 1, gb = 0







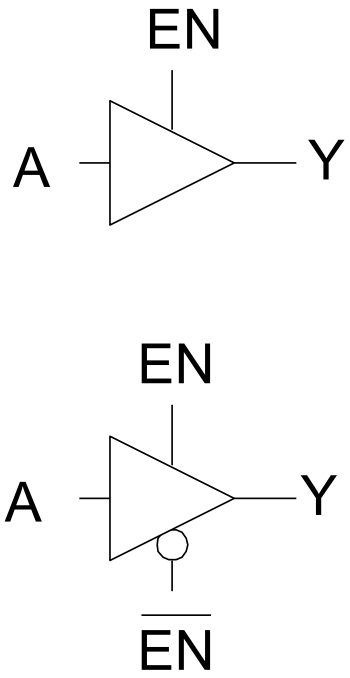


Tristates

- *Tristate buffer* produces Z when not enabled

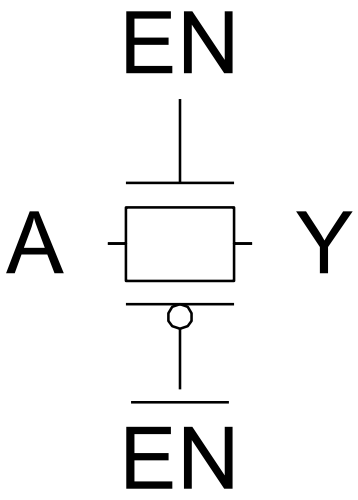
=>with enable

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



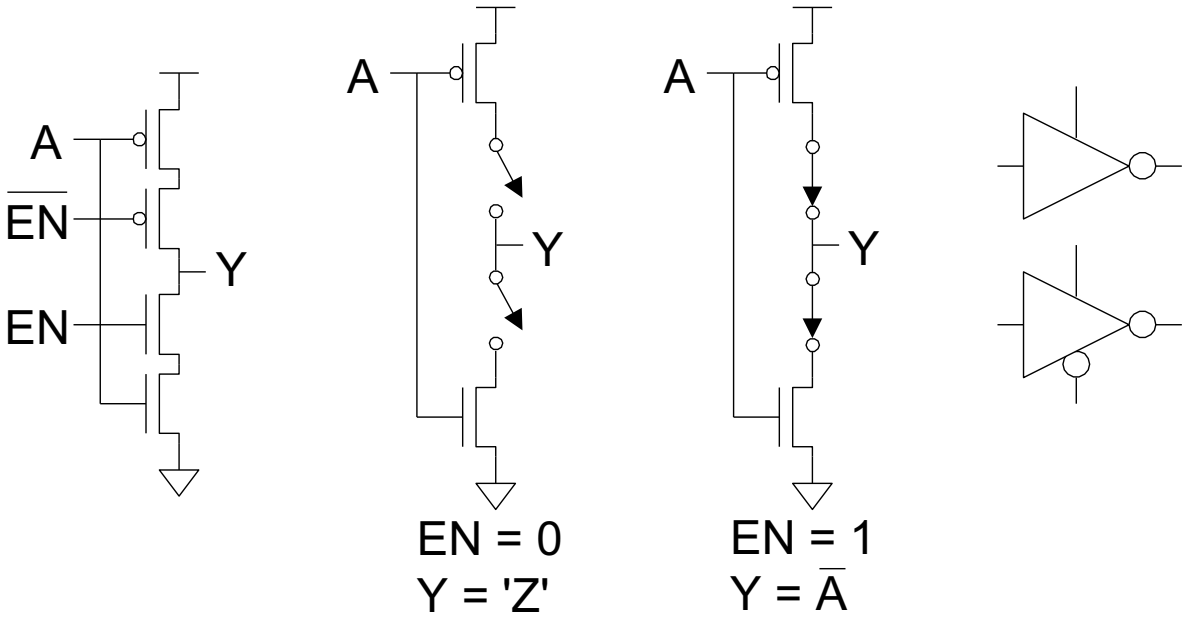
Nonrestoring Tristate

- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y



Tristate Inverter

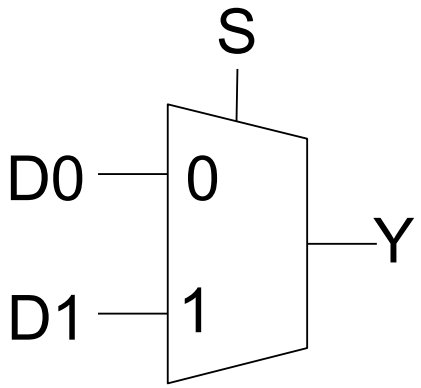
- Tristate inverter produces restored output
  - Violates conduction complement rule
  - Because we want a Z output



Multiplexers

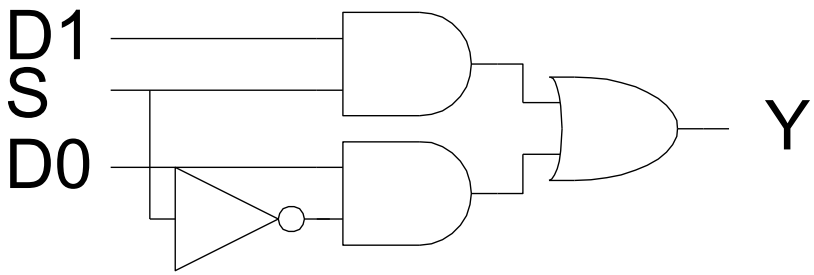
- 2:1 multiplexer chooses between two inputs

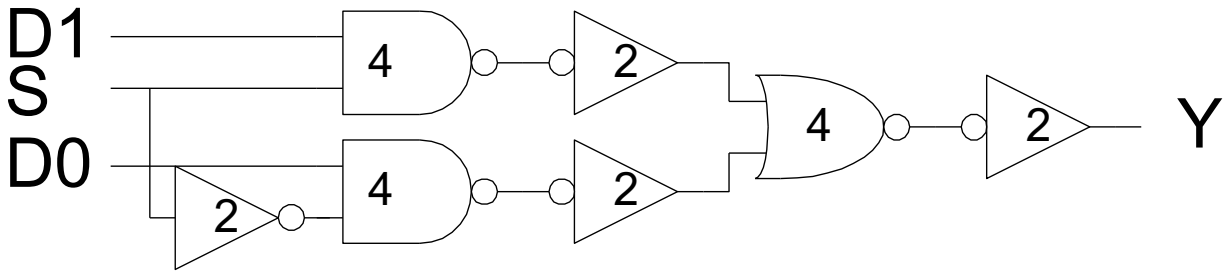
S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1



Gate-Level Mux Design

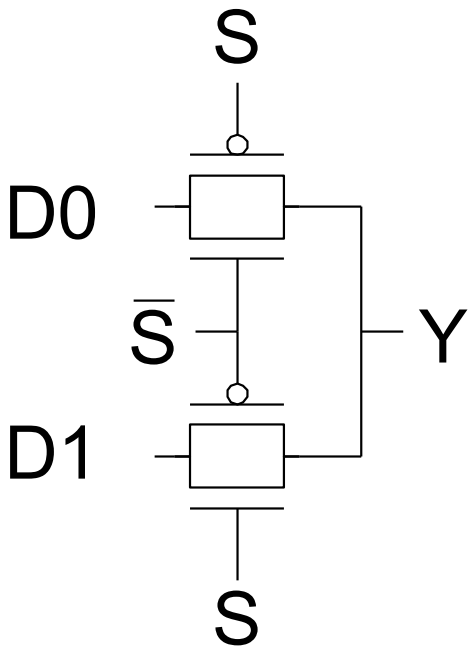
- $Y = SD_1 + \overline{S}D_0$ (too many transistors)
- How many transistors are needed?





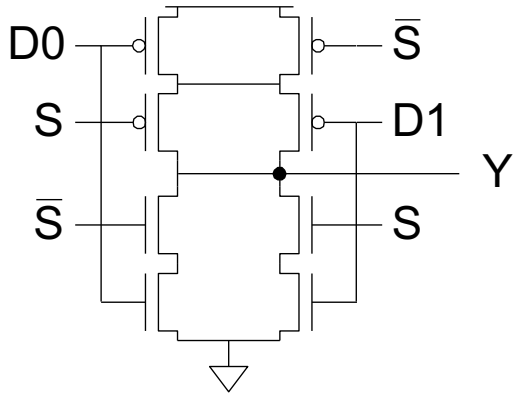
Transmission Gate Mux

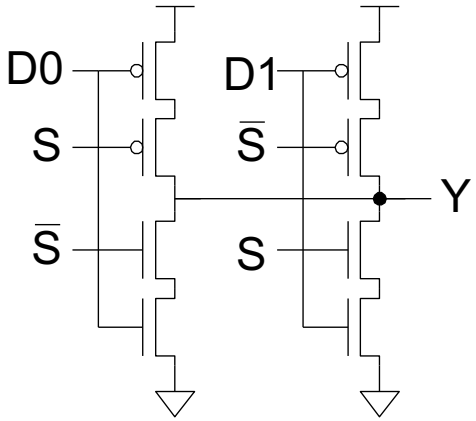
- Nonrestoring mux uses two transmission gates
  - Only 4 transistors

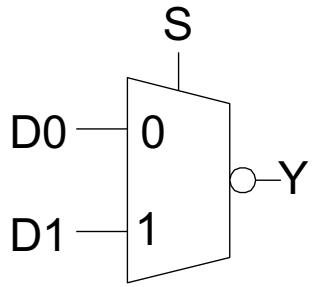


Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter

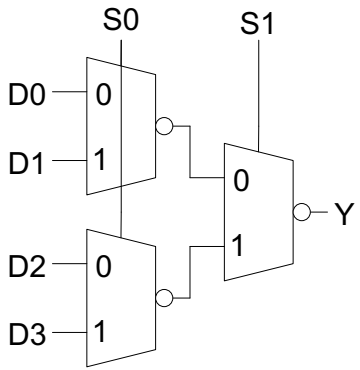


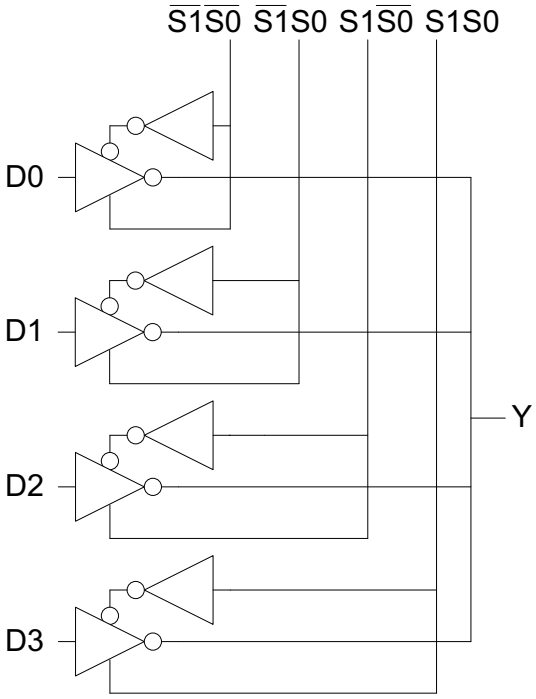




4:1 Multiplexer

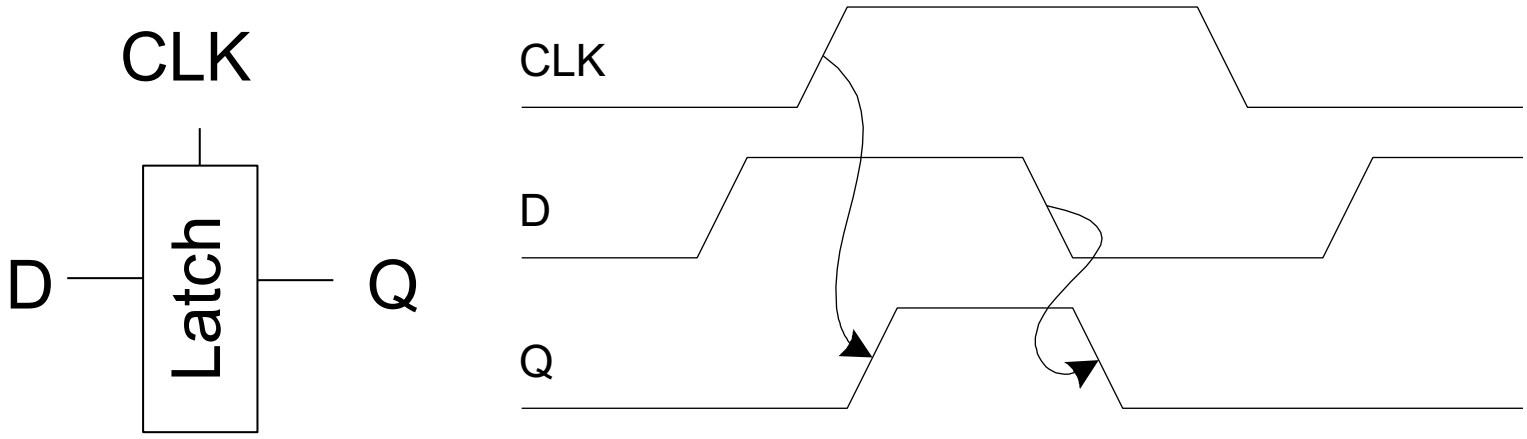
- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates





D Latch

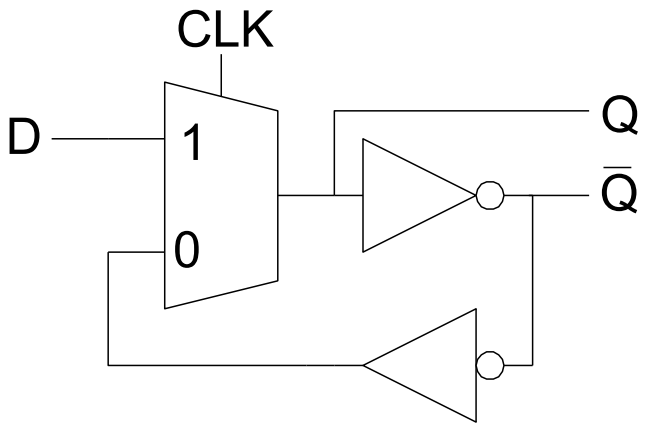
- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*

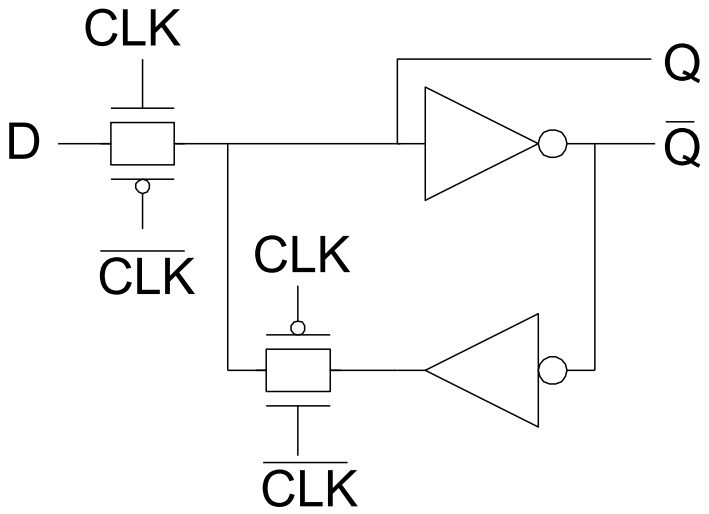


D Latch Design

- Multiplexer chooses D or old Q

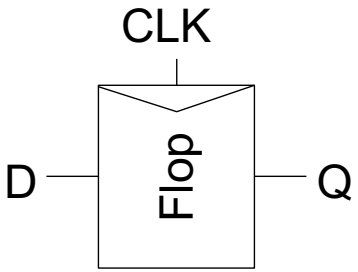
=> Set CLK as enable

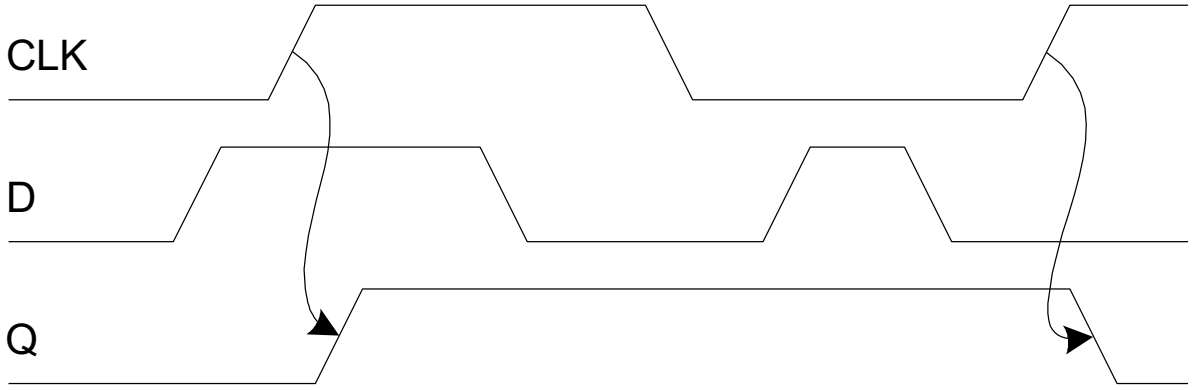




D Flip-flop

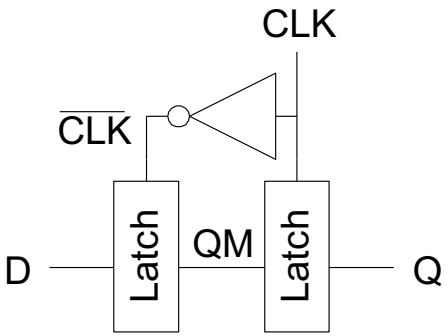
- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop*, *master-slave flip-flop*

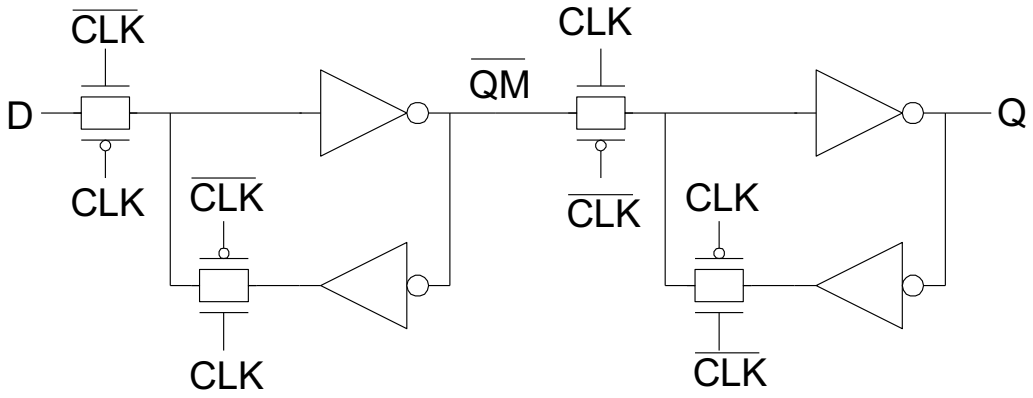




D Flip-flop Design

- Built from master and slave D latches



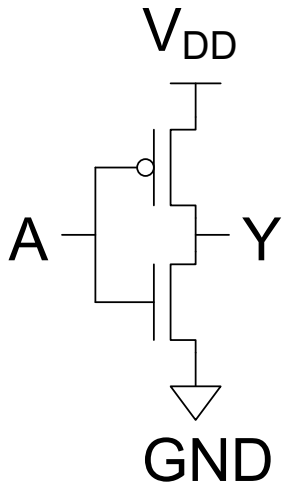


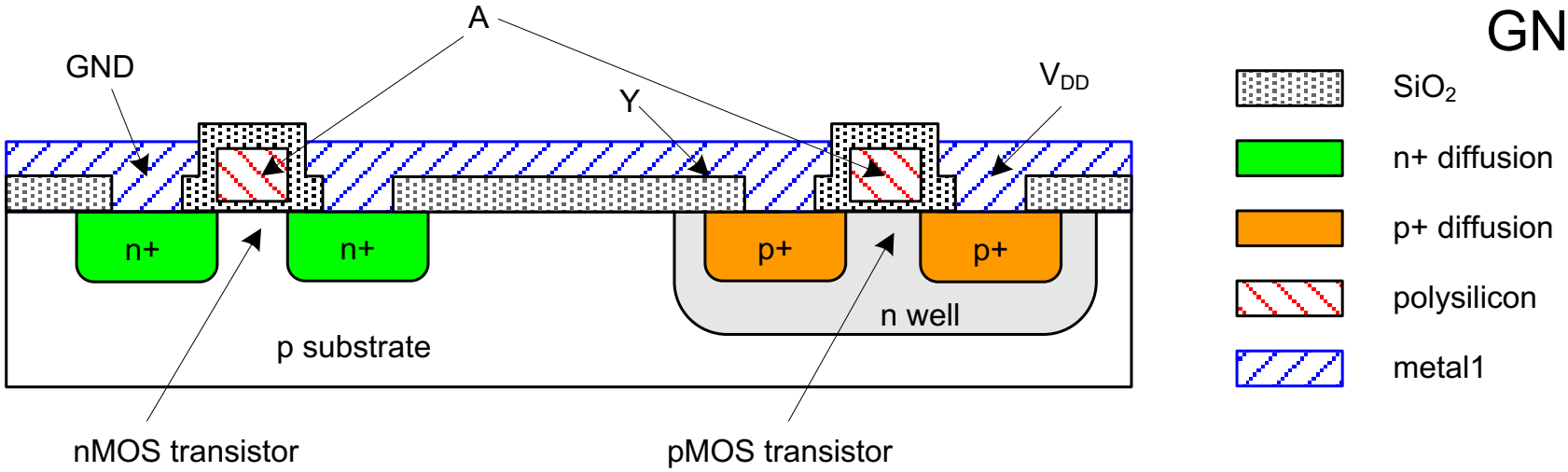
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Inverter Cross-section

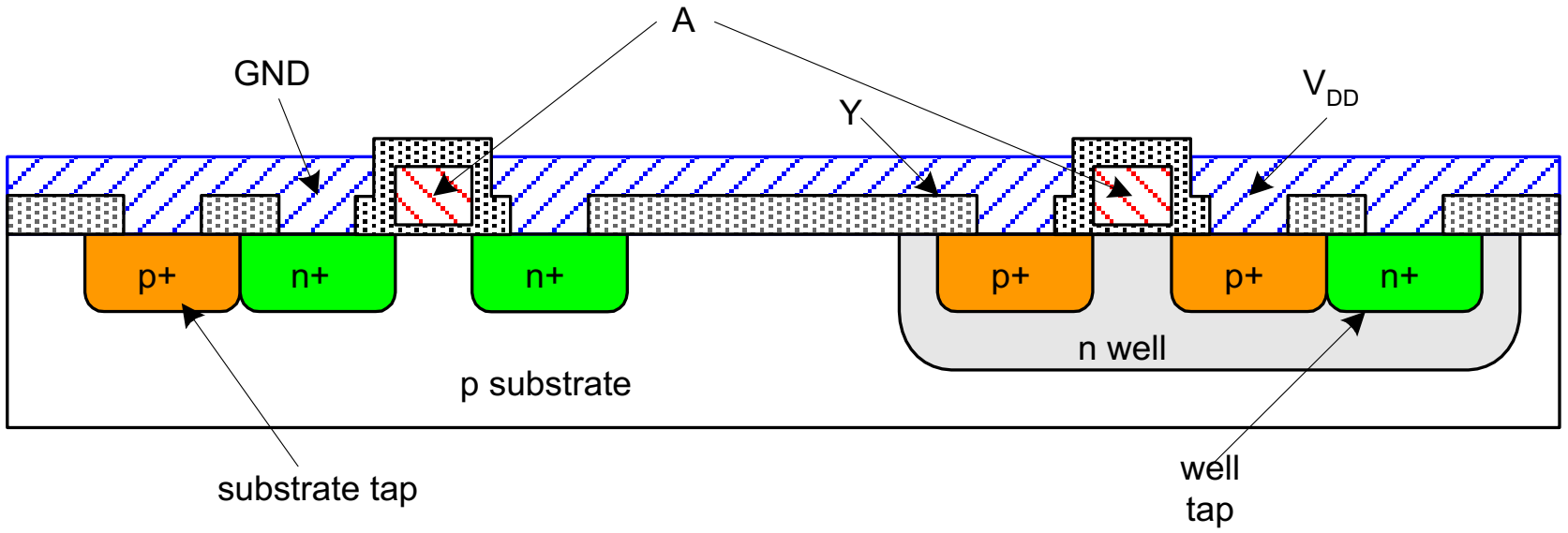
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors





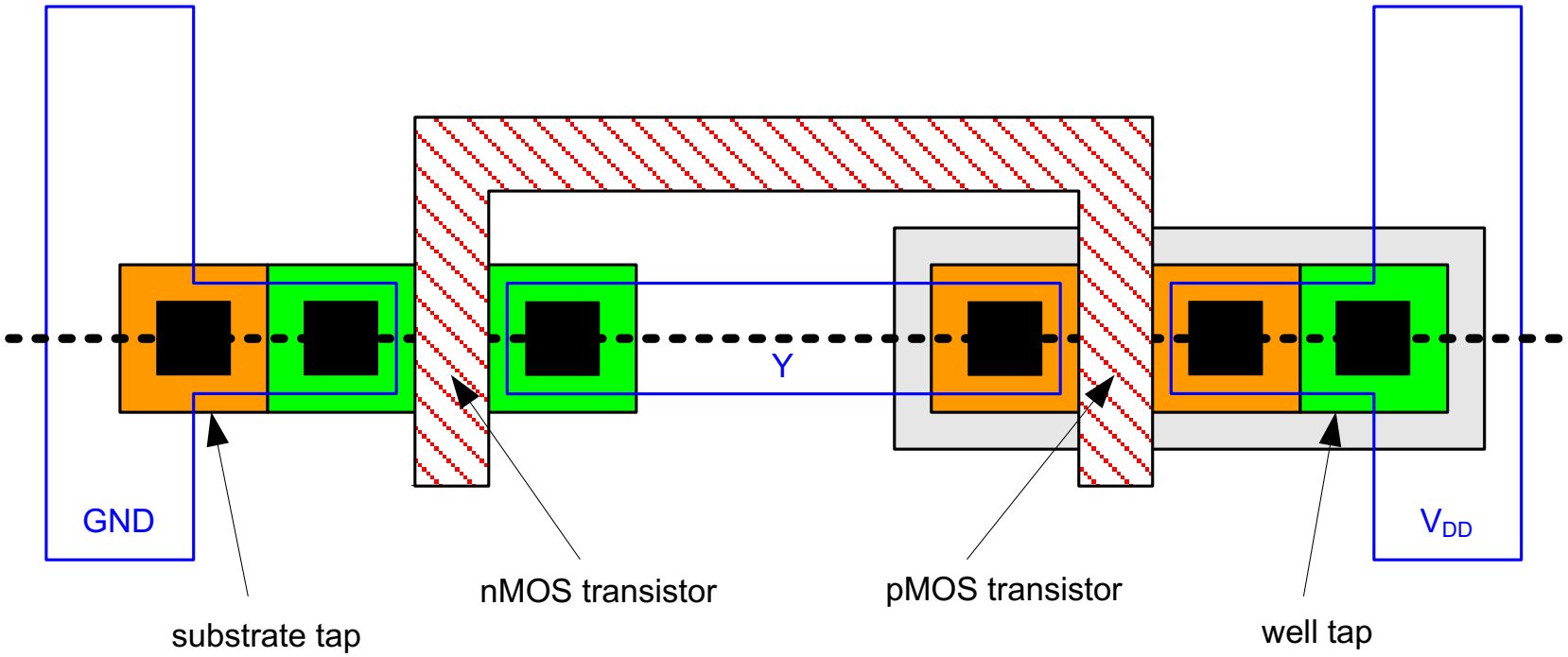
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



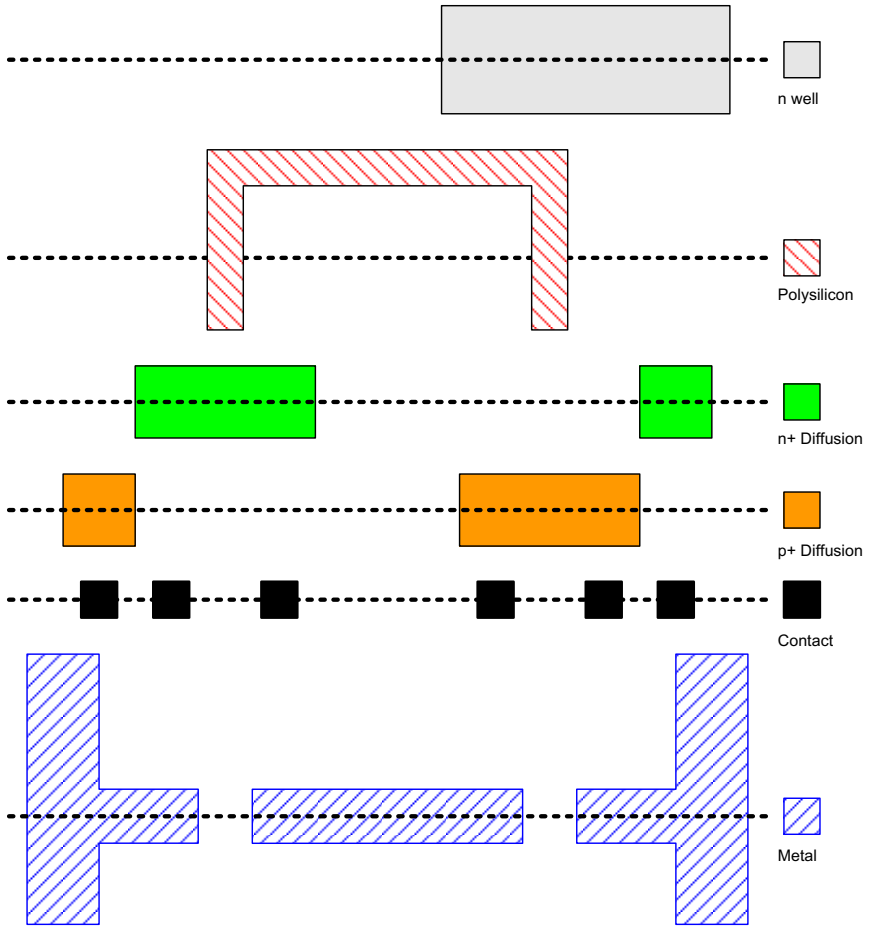
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
    (for 連線)



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields

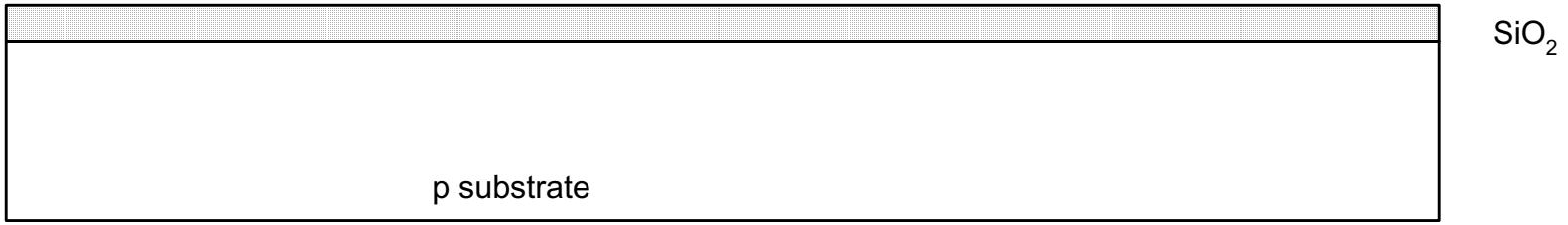
Courtesy of International
Business Machines Corporation.
Unauthorized use not permitted.

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

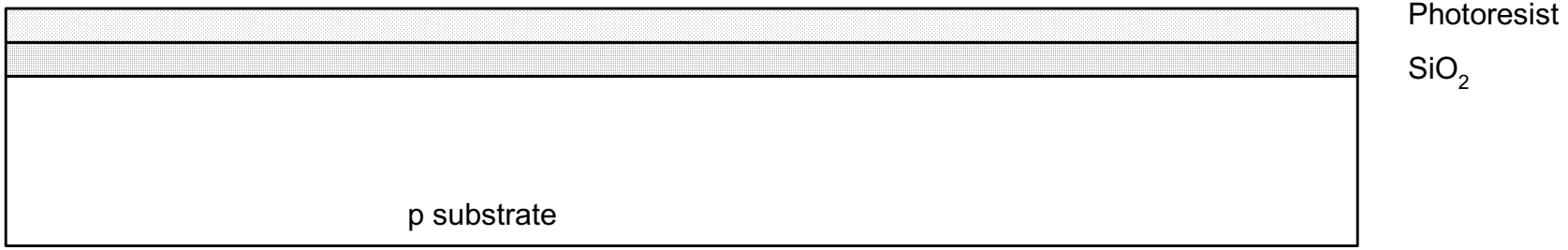
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



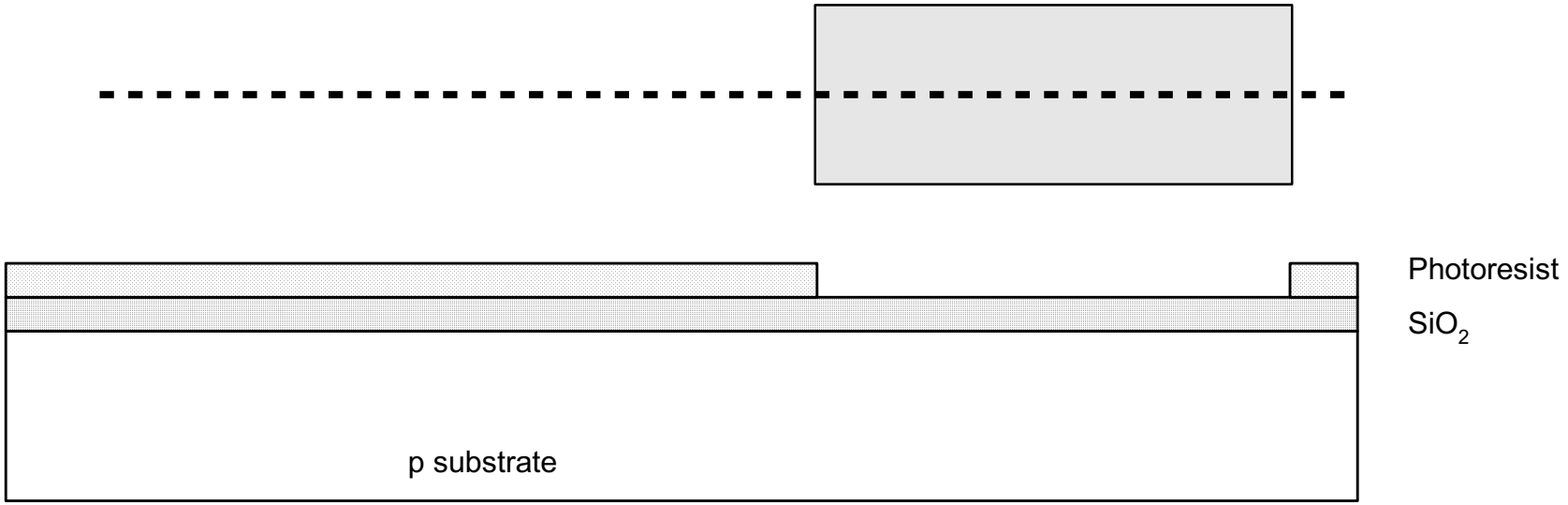
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



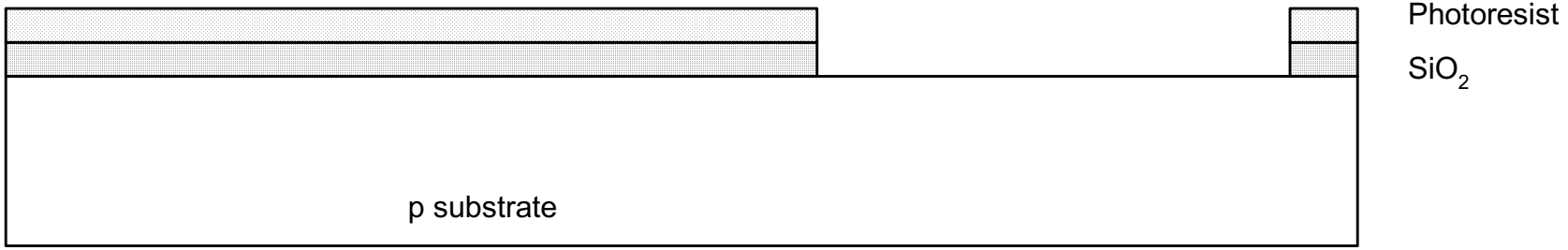
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



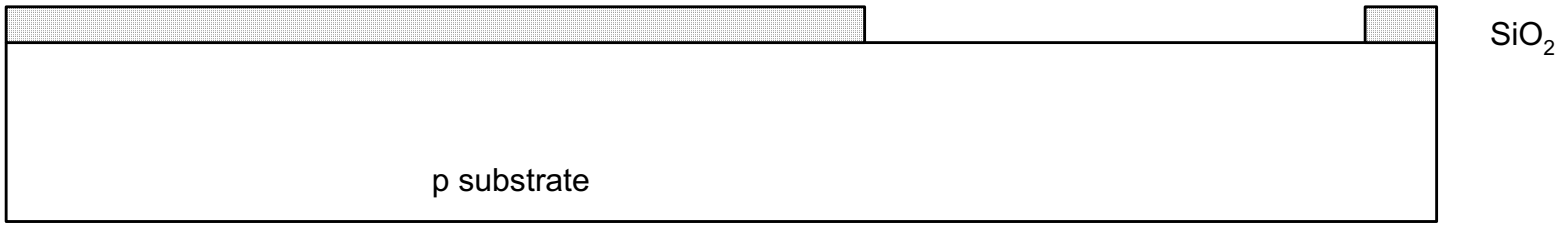
Etch (蝕刻)

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



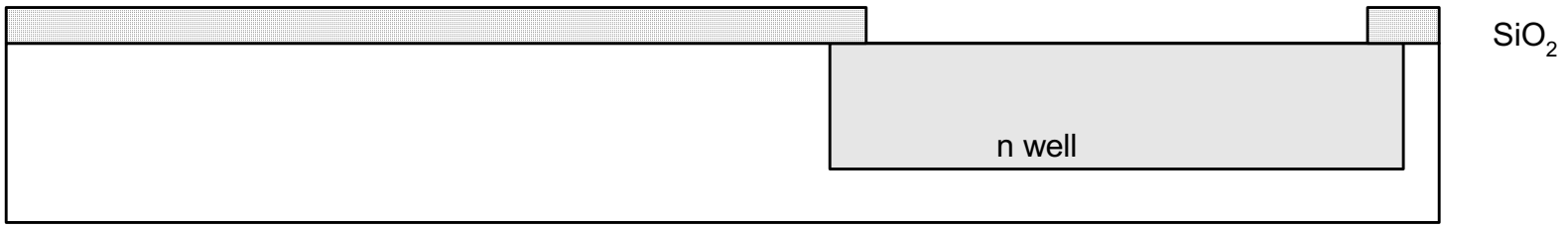
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

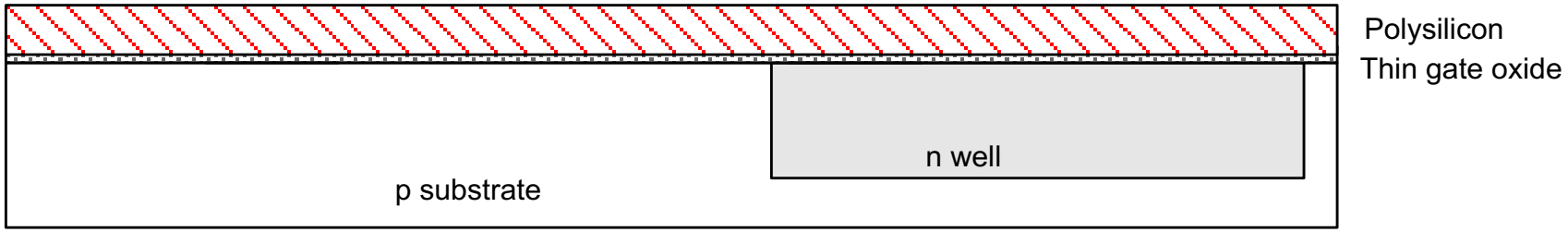


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

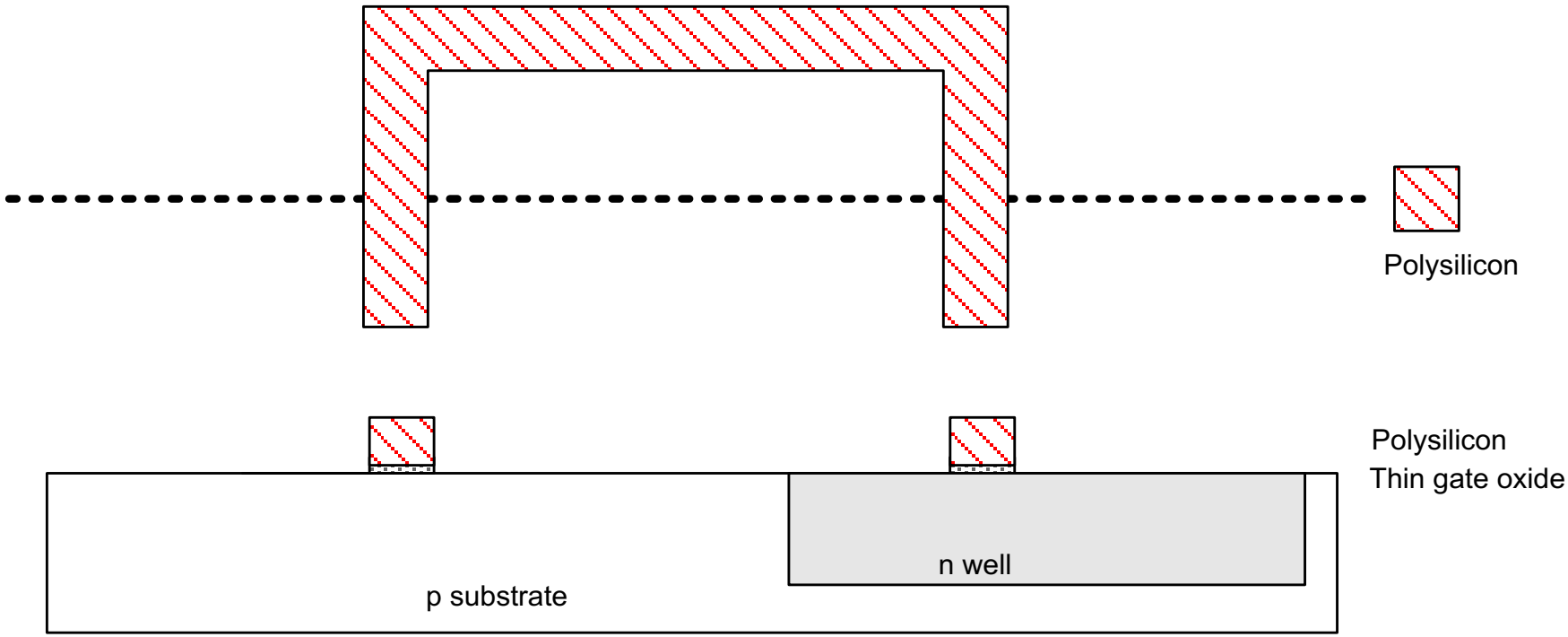
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



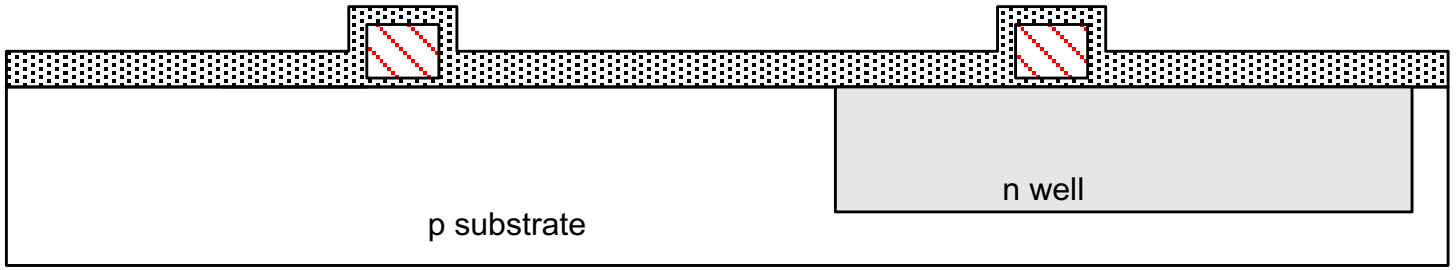
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



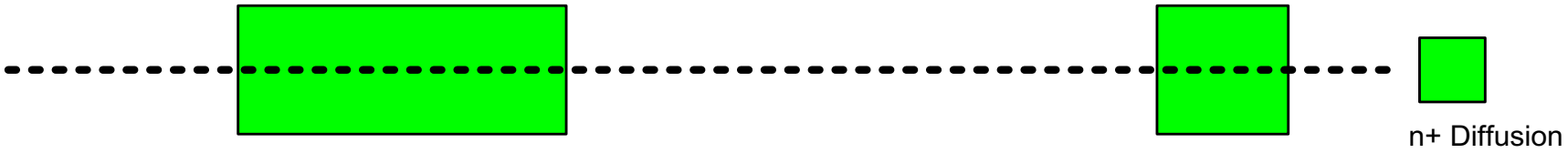
Self-Aligned Process

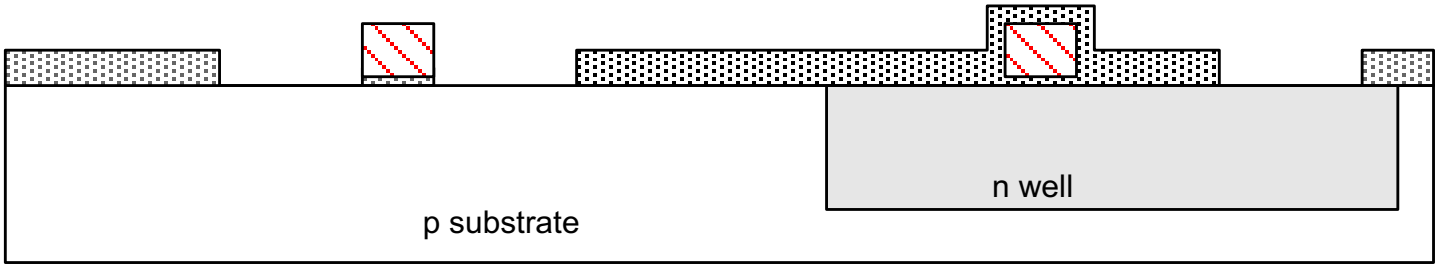
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



N-diffusion

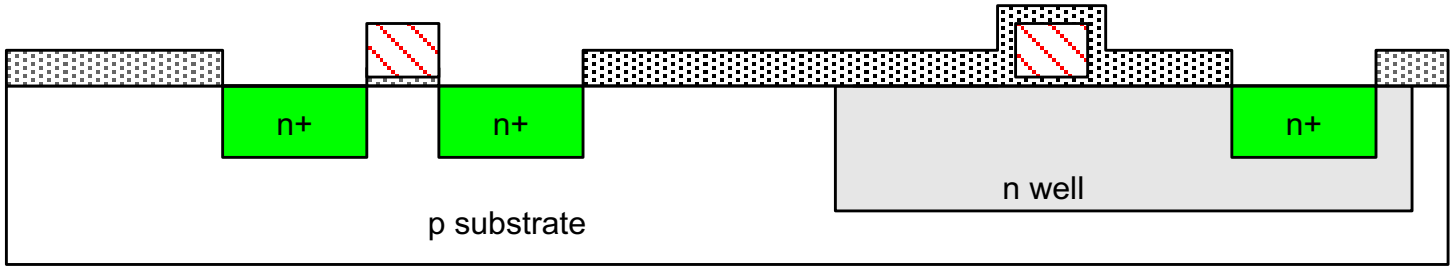
- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing





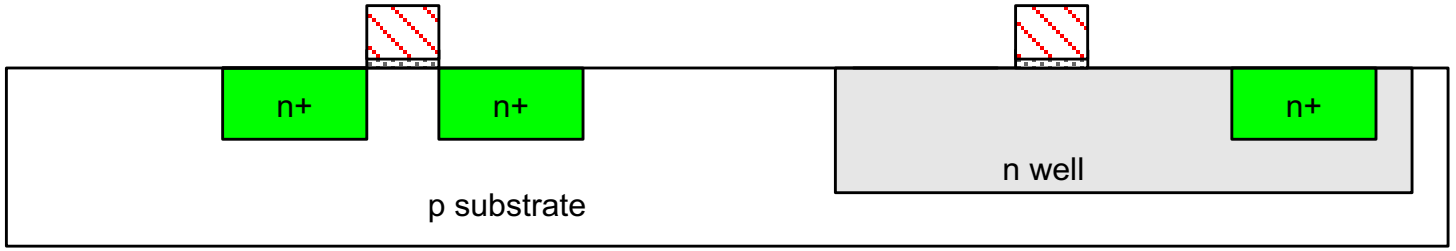
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



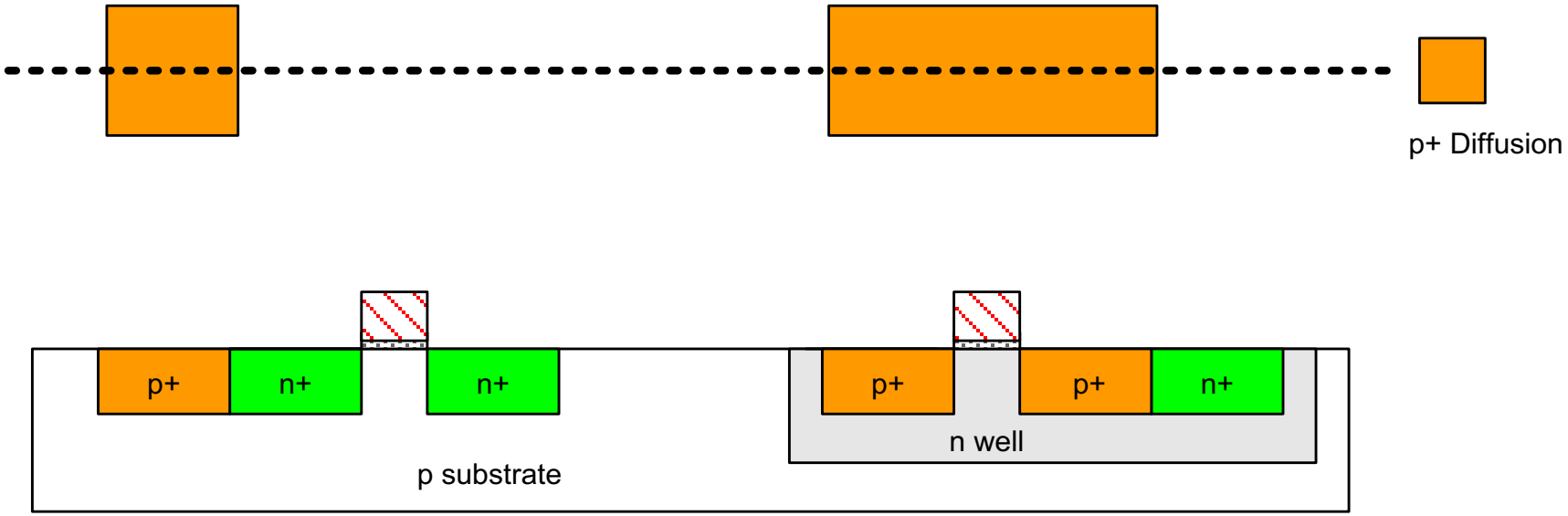
N-diffusion cont.

- Strip off oxide to complete patterning step



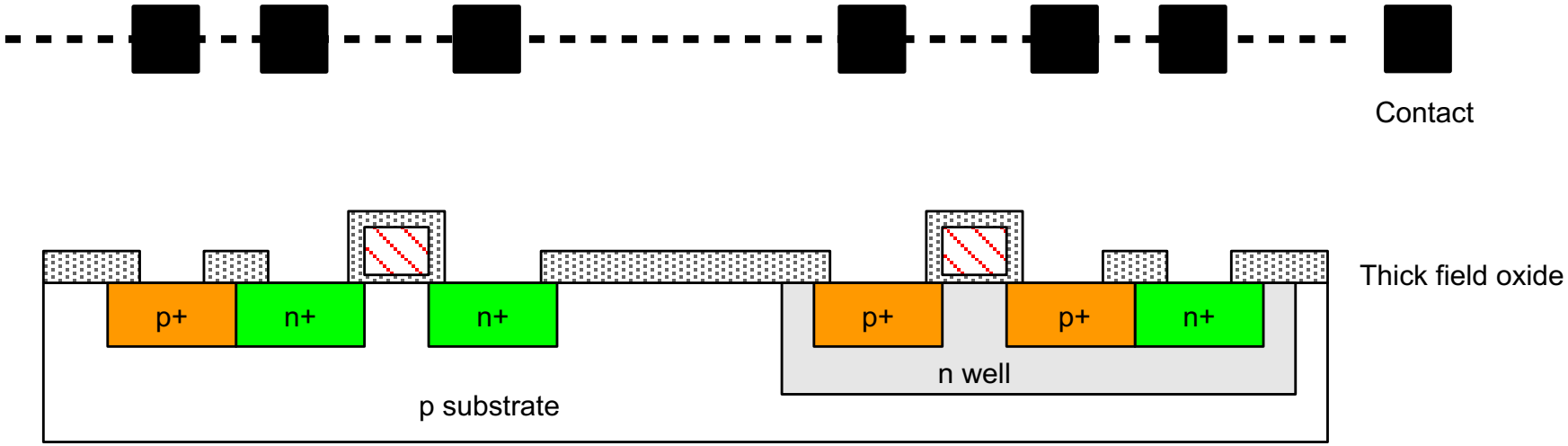
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



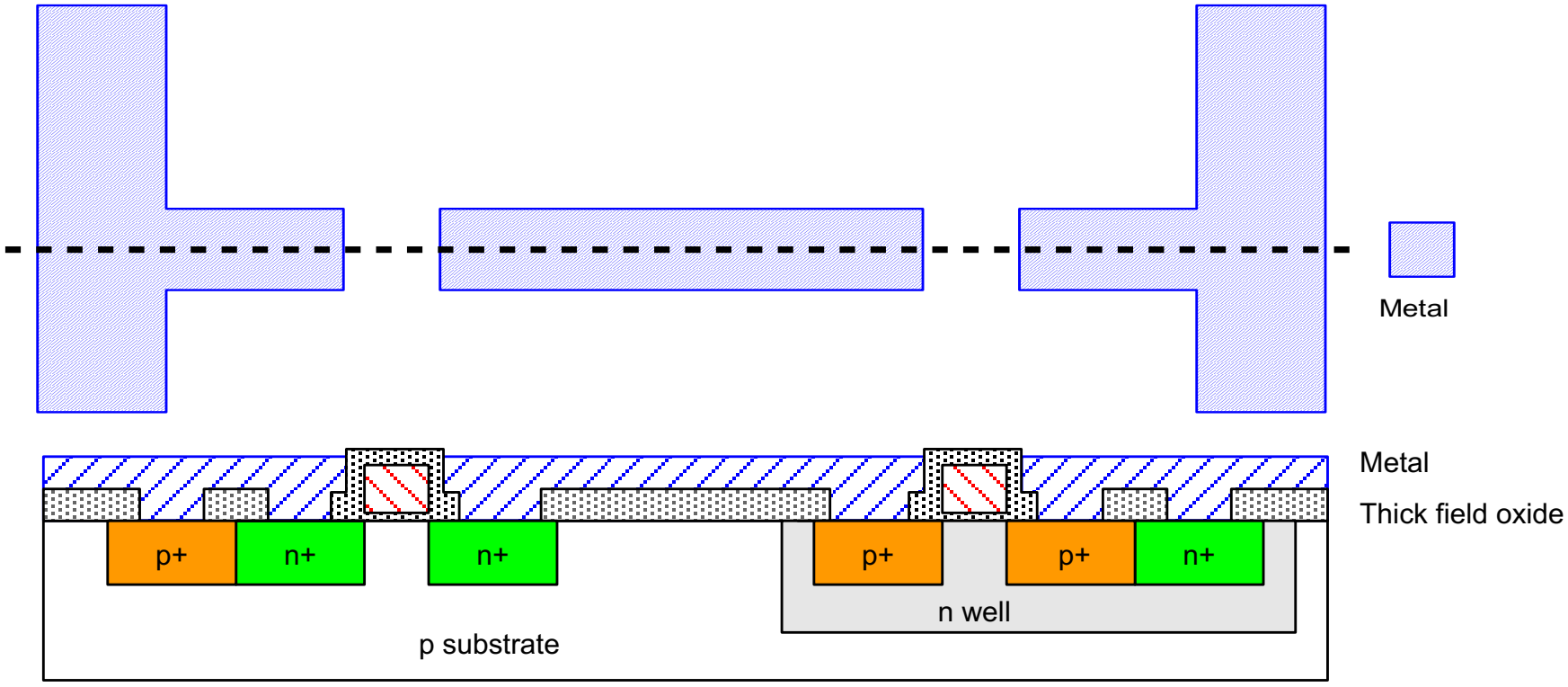
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. λ = 0.3 μm in 0.6 μm process

Gate Layout

- Layout can be very time consuming
  - Design gates to fit together nicely
  - Build a library of standard cells
- Standard cell design methodology
  - V_{DD} and GND should abut (standard height) =>在相同高度
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts

(所有單一或複合式的gate都會存成library)

Basic Gate Design

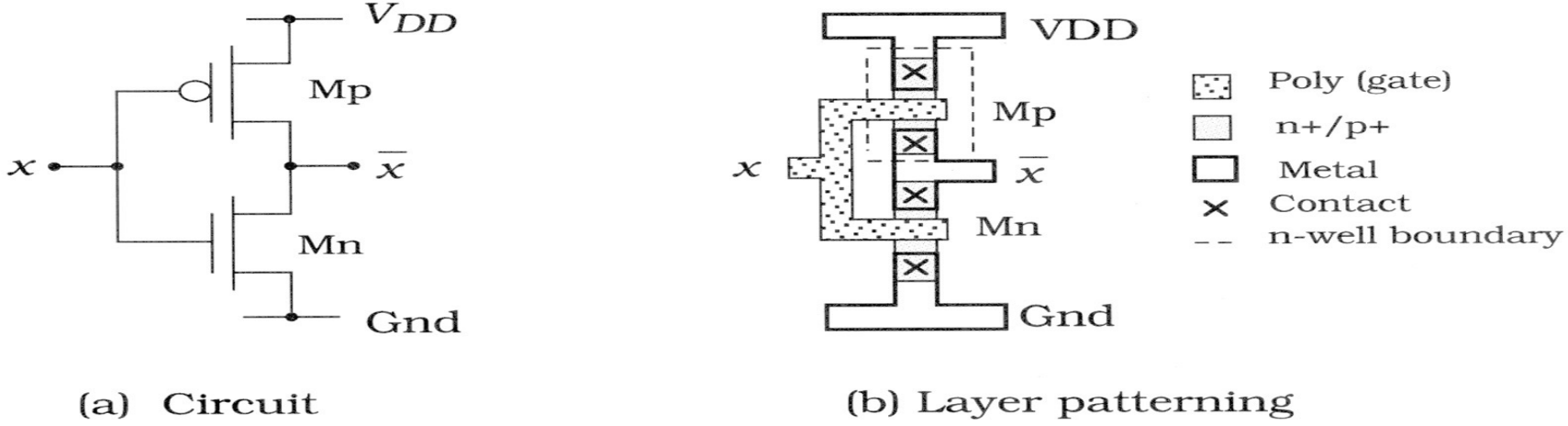


Figure 3.31 Translating a NOT gate circuit to silicon

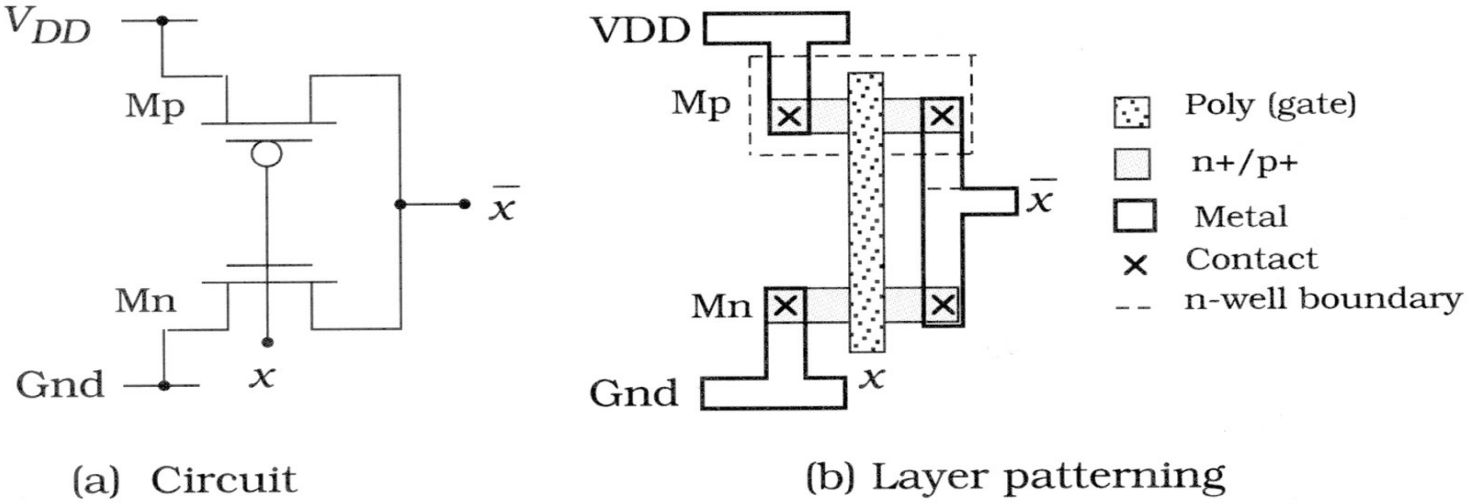
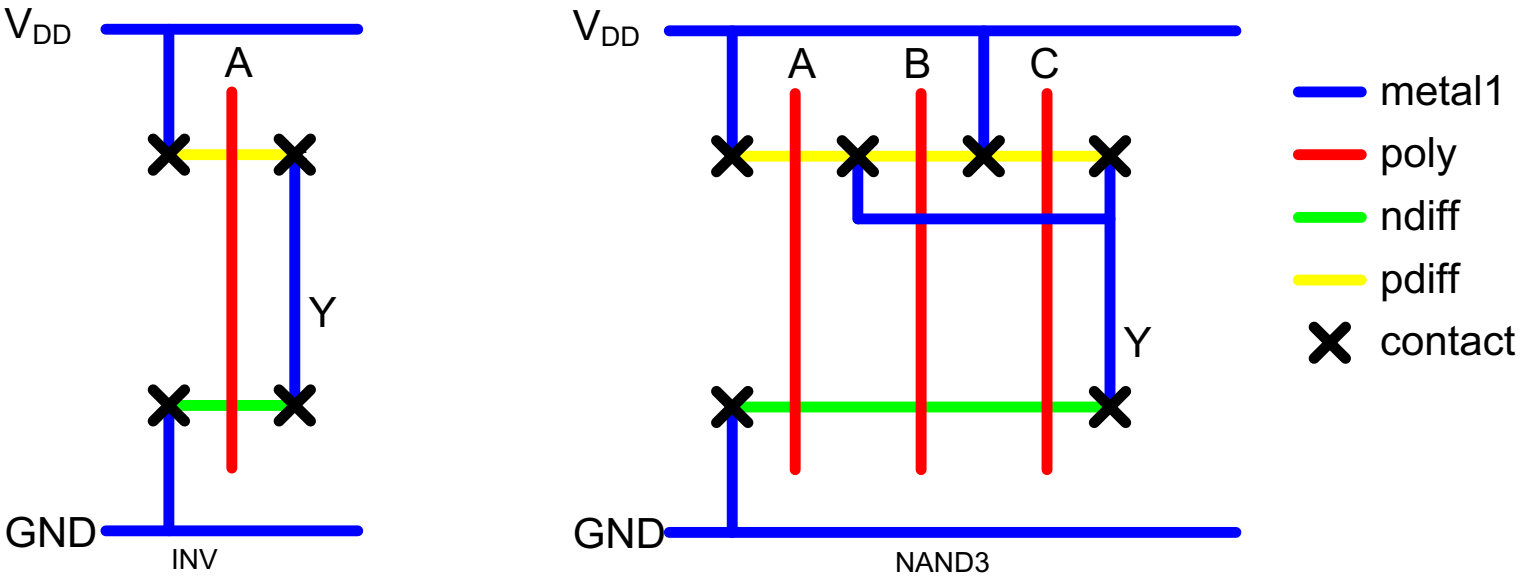


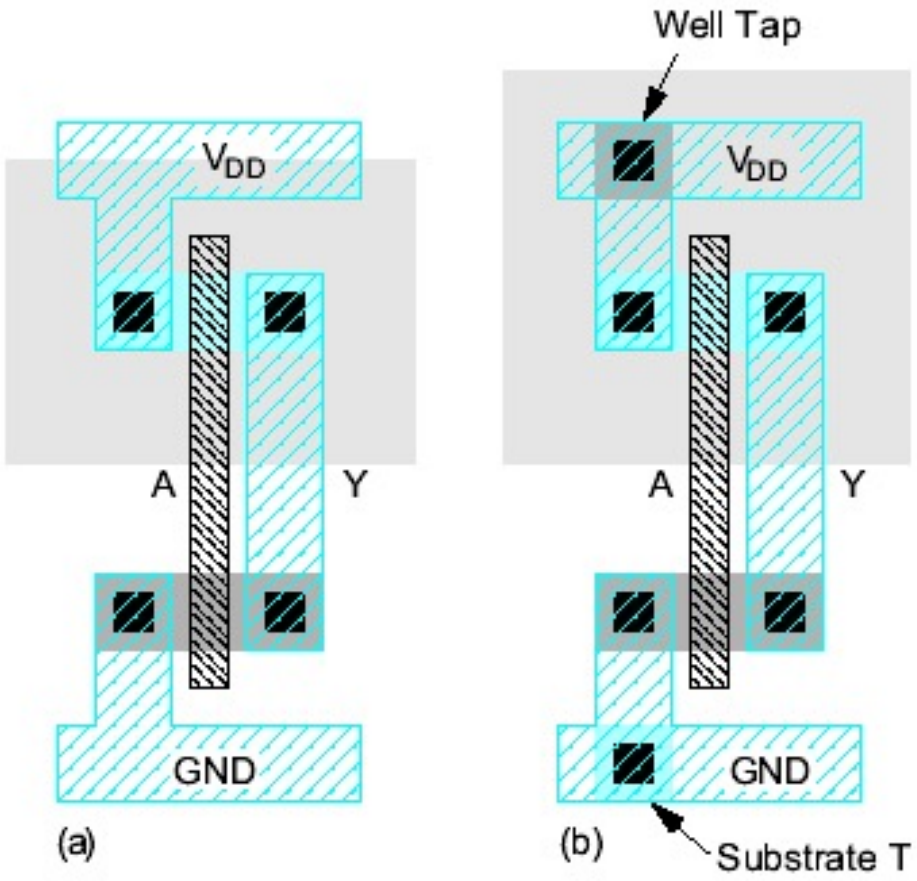
Figure 3.32 Alternate layout for a NOT gate

Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

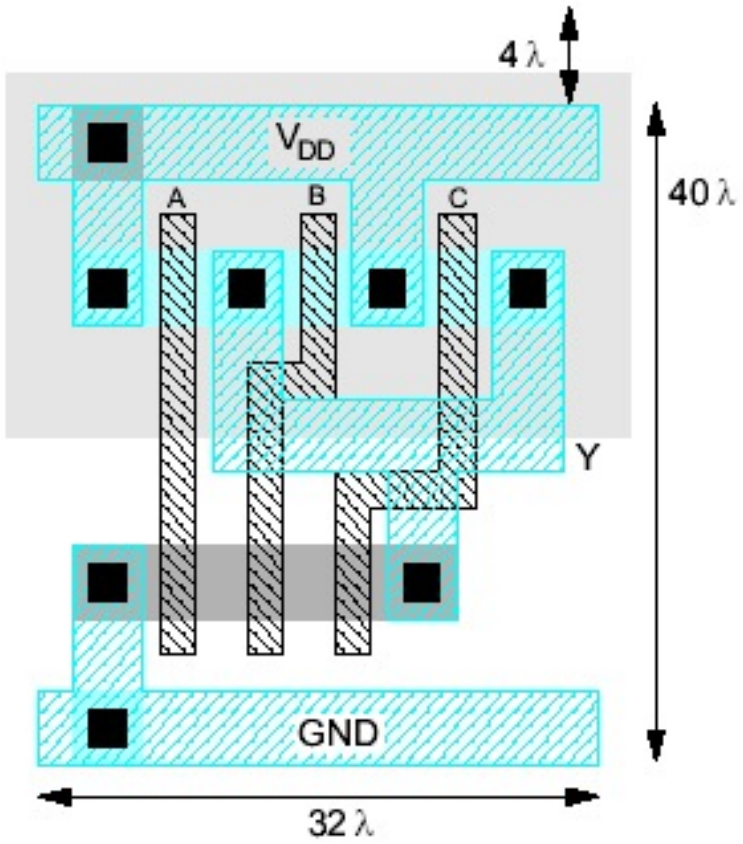


Example: Inverter



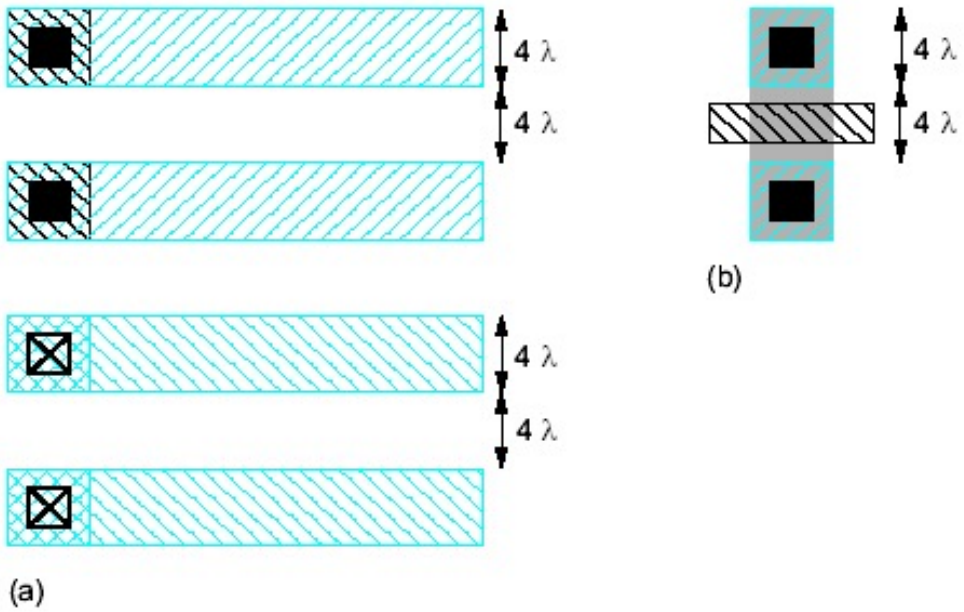
Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom
- 32 λ by 40 λ



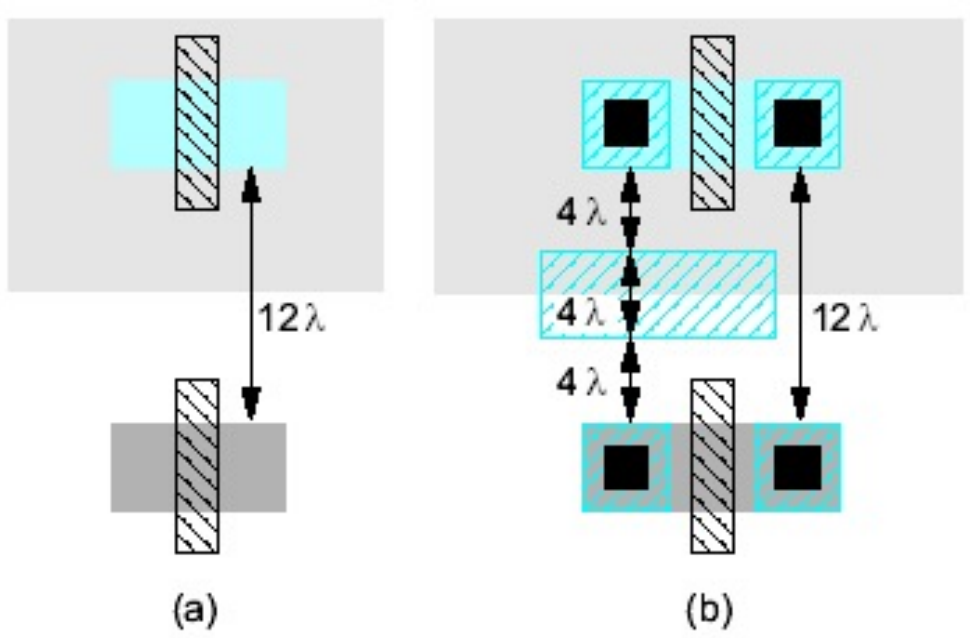
Wiring Tracks

- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbor = 8 λ pitch
- Transistors also consume one wiring track



Well spacing

- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



- In Figure 3.33. Two NOT circuits share the same power supply and ground to reduce area.

=>盡量把polysilicon做成直的比較容易做share

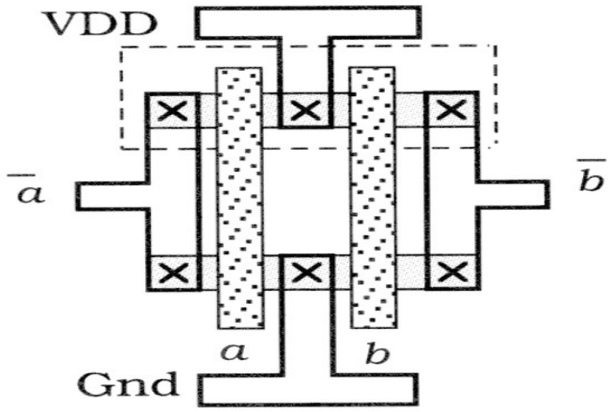
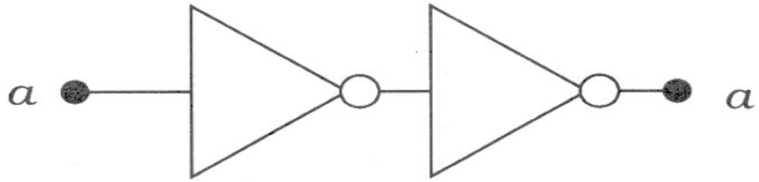
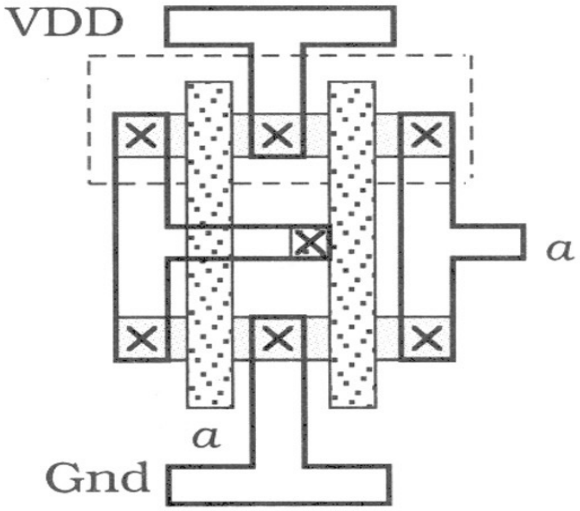


Figure 3.33 Two NOT gates that share power supply and ground



(a) Logic diagram



(b) Layout

Figure 3.34 Non-inverting buffer

- Interconnect routing problems in layout.

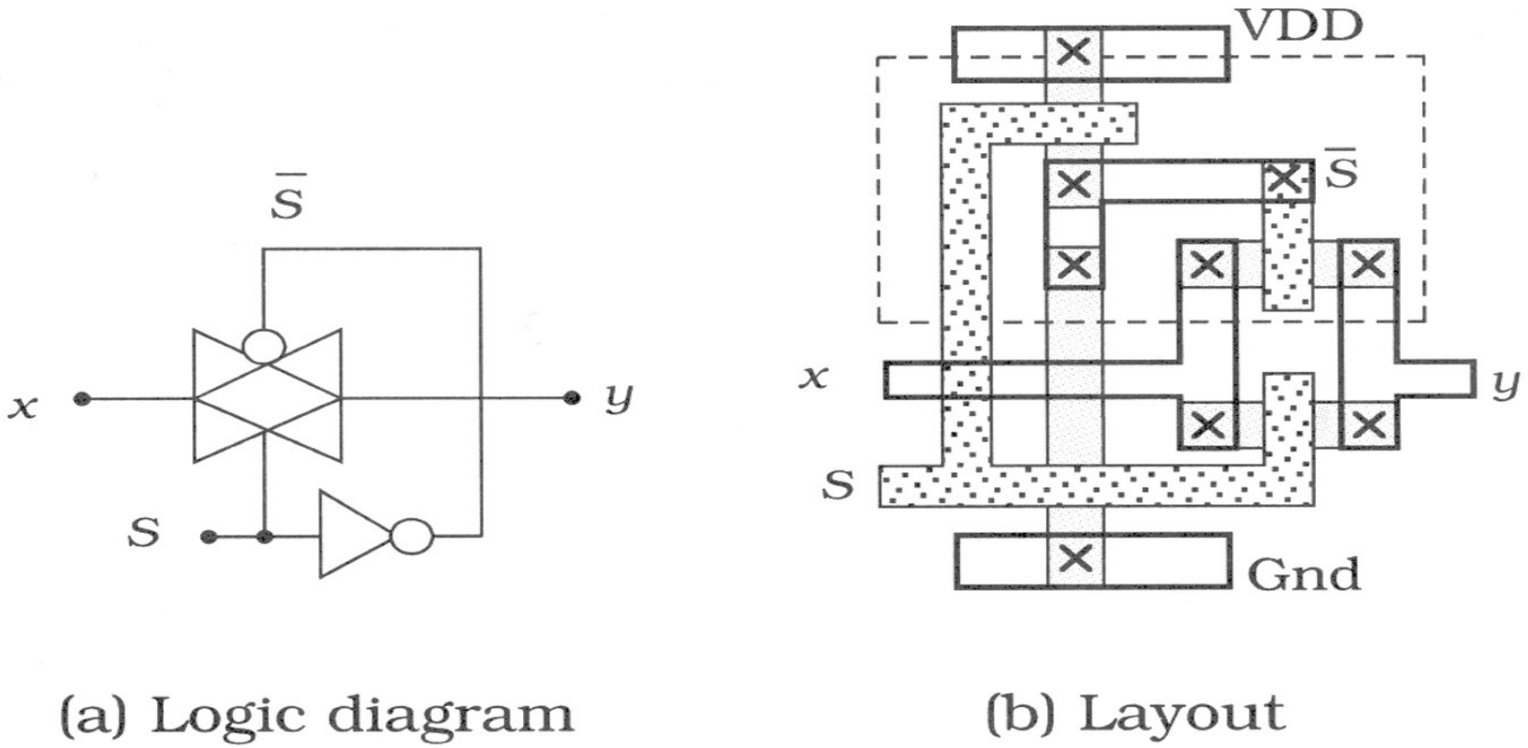
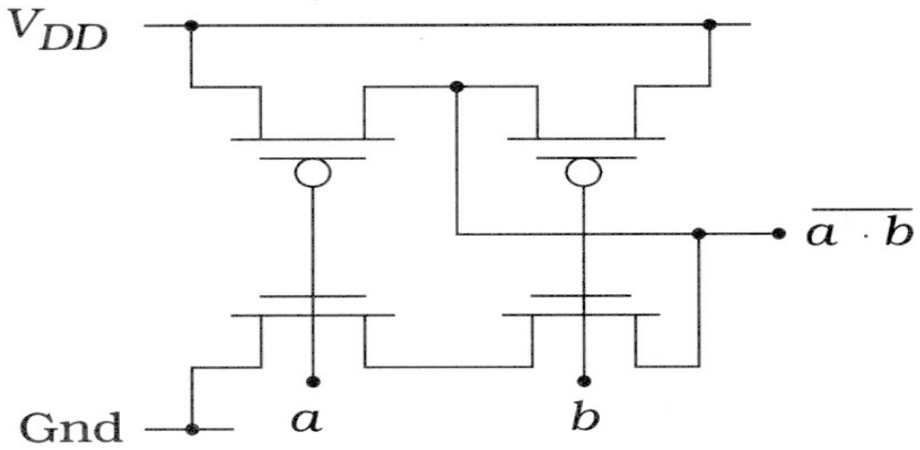
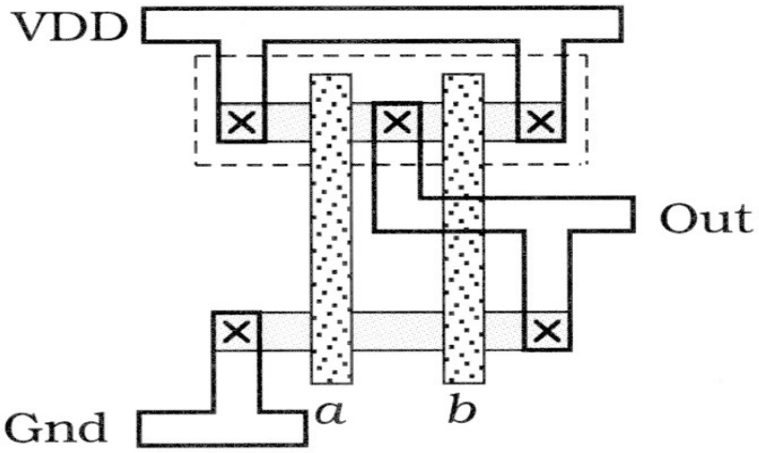


Figure 3.35 Layout of a transmission gate with a driver



(a) Circuit



(b) Layer design

Figure 3.36 NAND2 layout

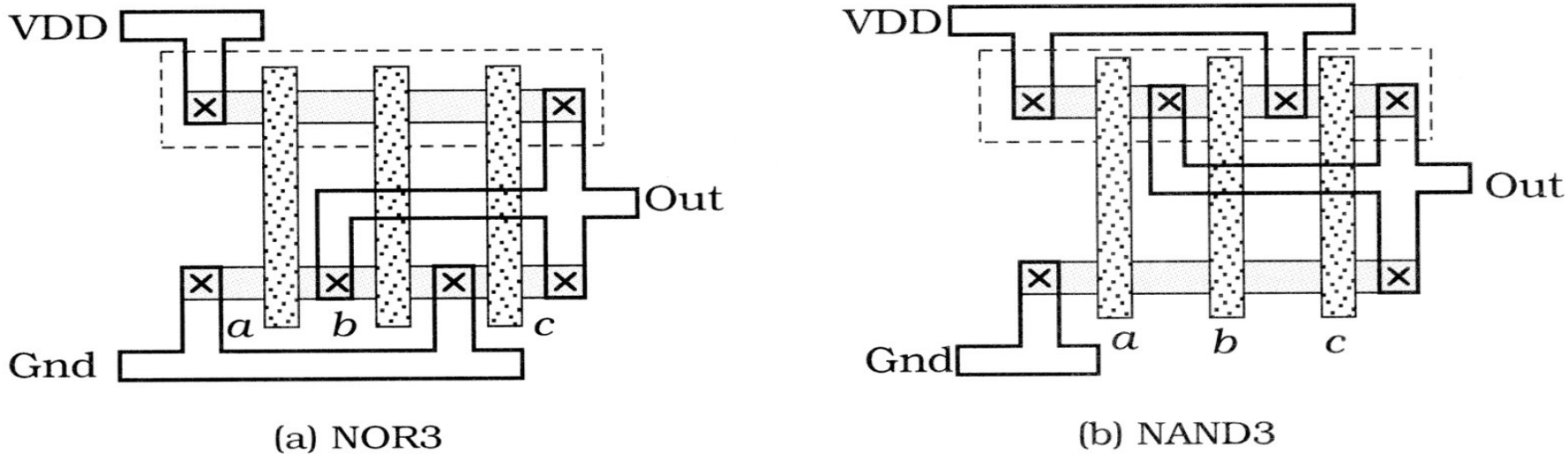


Figure 3.39 Layout for 3-input gates

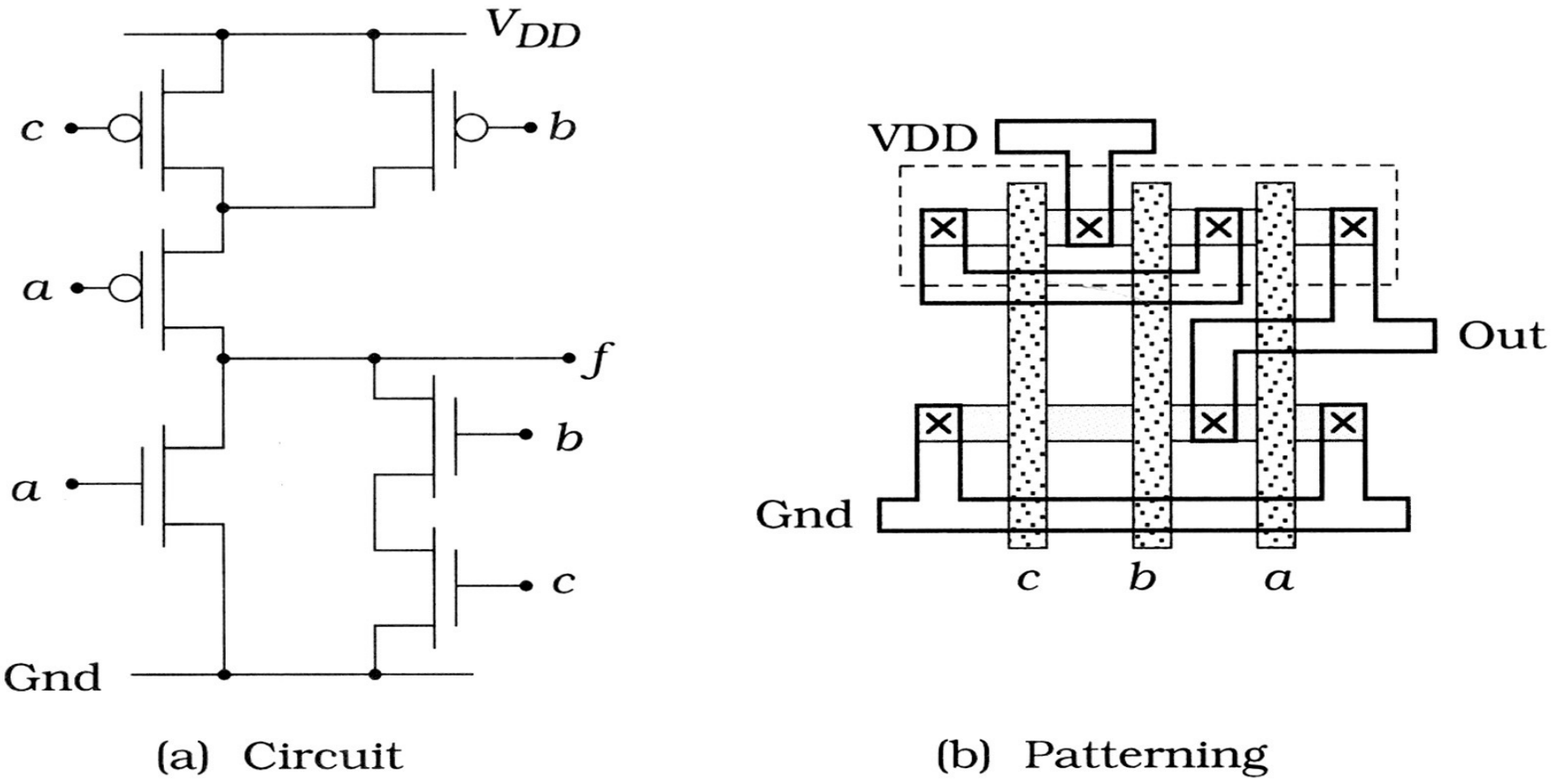
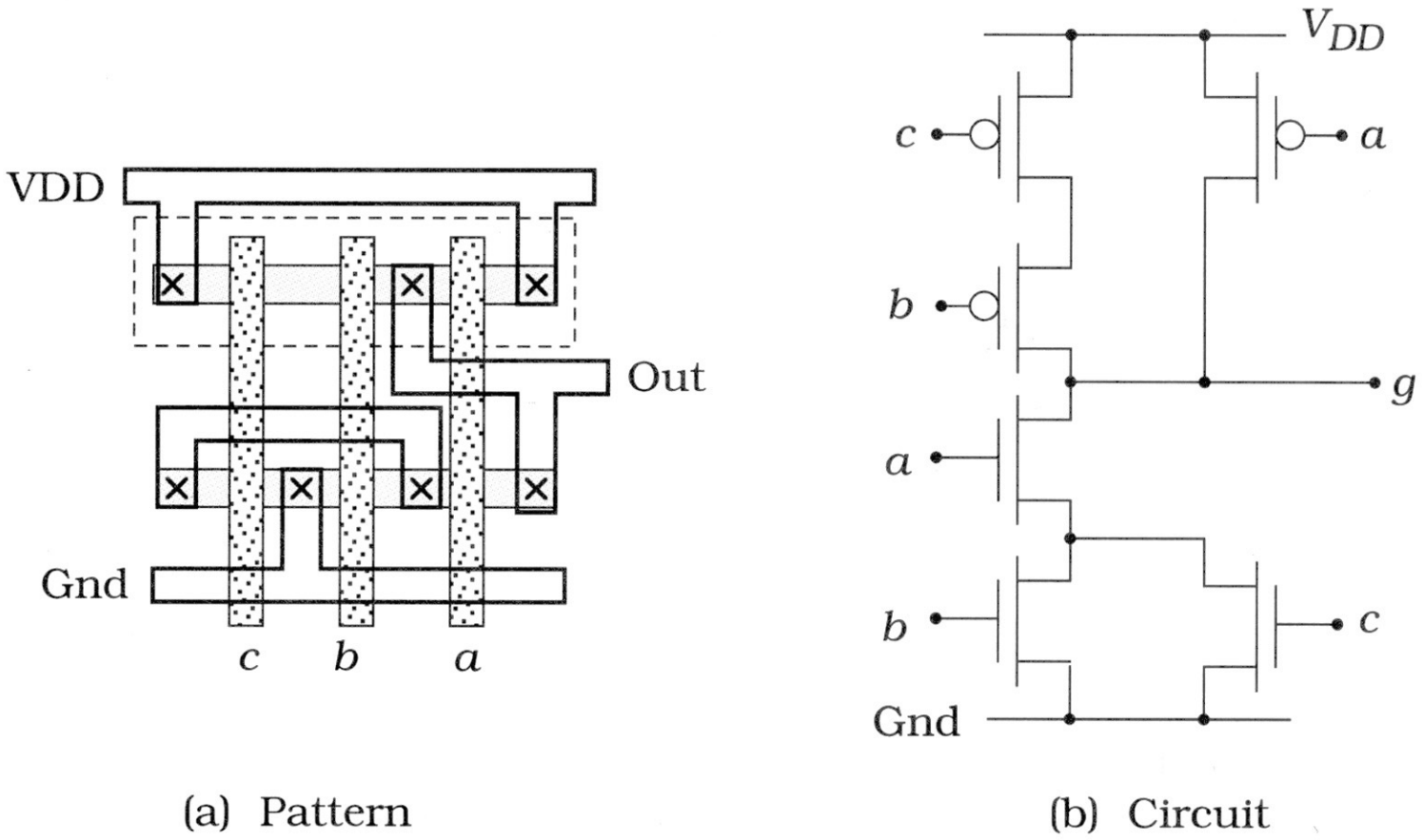


Figure 3.40 Extension of layout technique to a complex logic gate



(a) Pattern (b) Circuit

Figure 3.41 Creation of the dual network

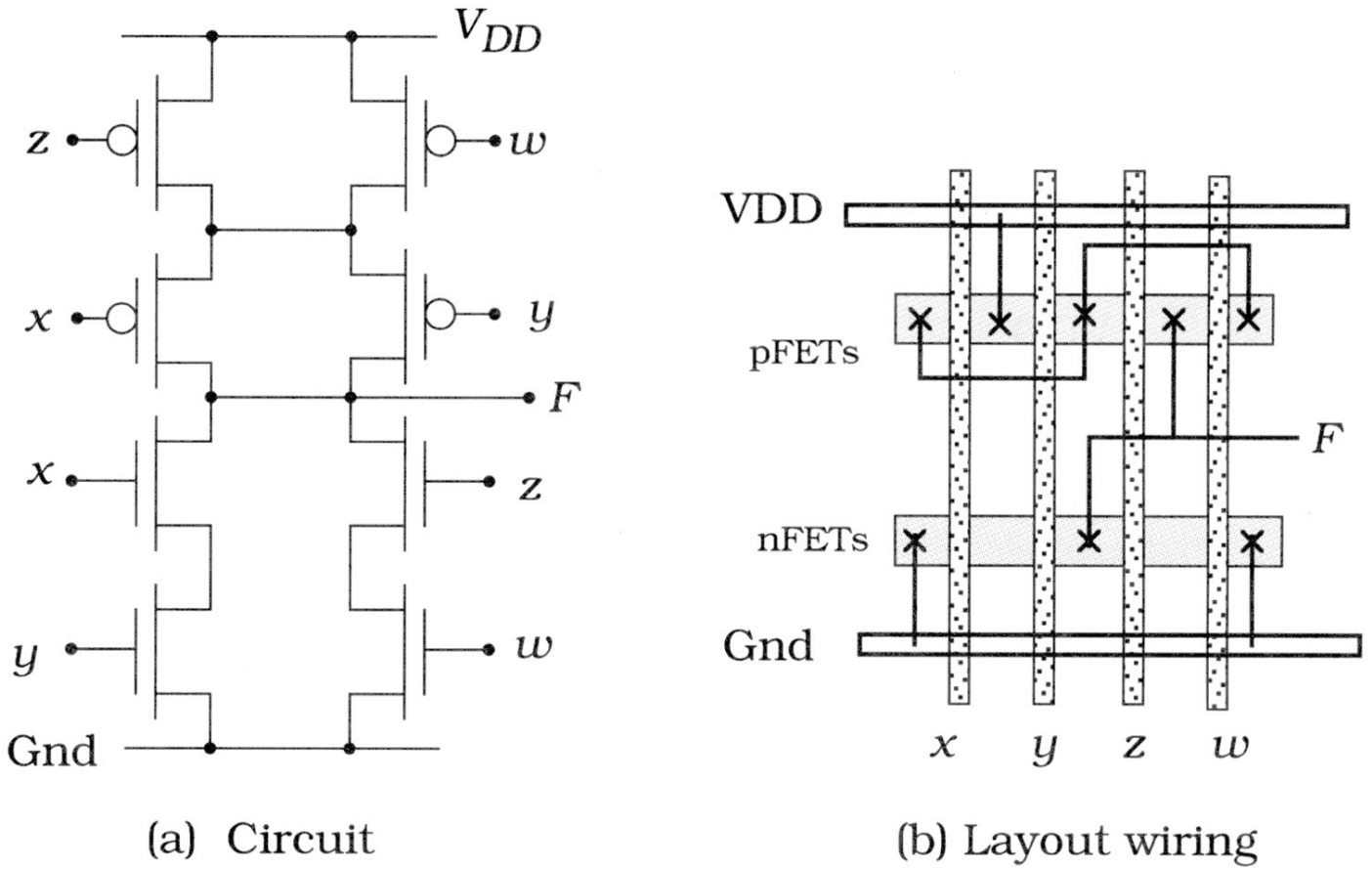
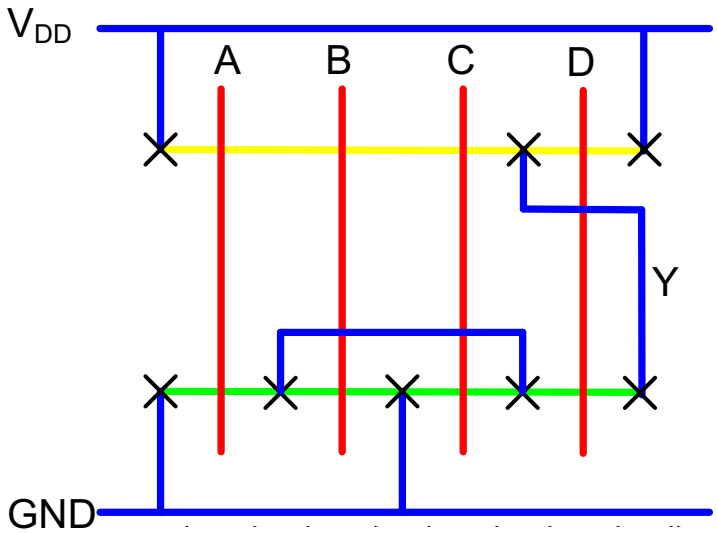


Figure 3.42 A general 4-input AOI gate

Example: O3AI

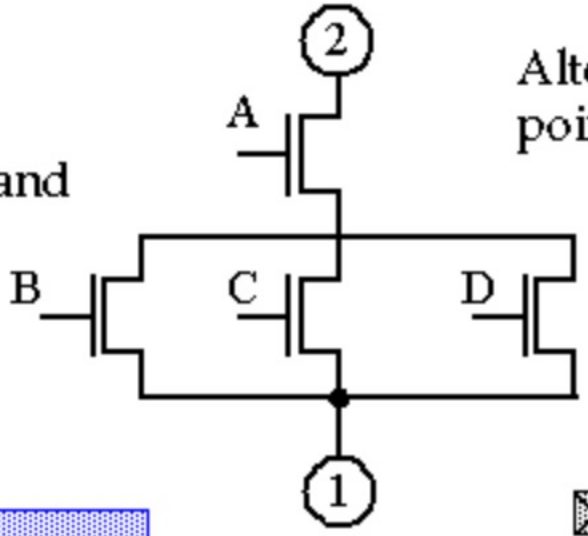
- Sketch a stick diagram for O3AI and estimate area

$$\overline{Y = (A + B + C) \bullet D}$$



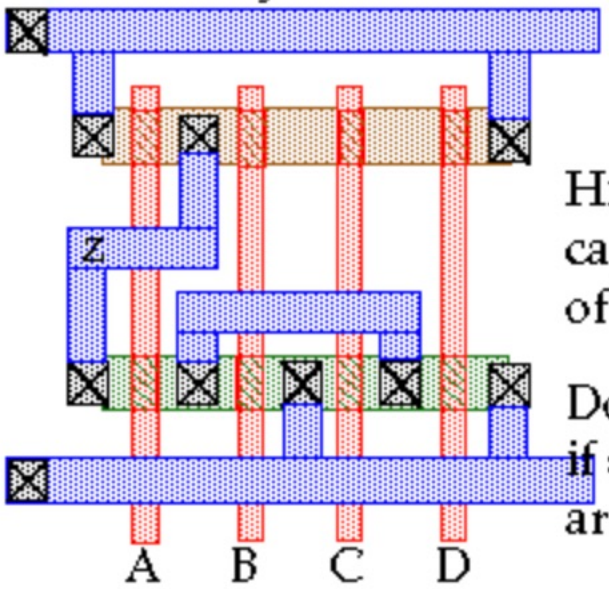
$F = \overline{(A+B+C).D}$

What layout is faster and why?



Alternatively, do we connect point 1 or point 2 to GND?

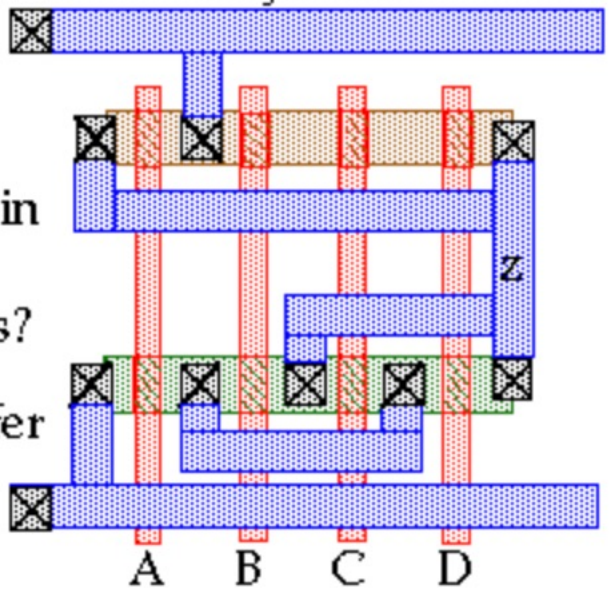
Layout 1



Hint: How many drain capacitances do each of the layouts possess?

Does your choice differ if signal A is the first arriving signal?

Layout 2



Summary

- MOS transistors are stacks of gate, oxide, silicon
- Act as electrically controlled switches
- Build logic gates out of switches
- Draw masks to specify layout of transistors

- Now you know everything necessary to start designing schematics and layout for a simple chip!

Questions?