Google **S**ummer **o**f **C**ode 2019
Apertus Organization

Subject: 1st Evaluation Documentation.

Submitted to: Apertus Organization.
Project name: **Bidirectional Packet Protocol for FPGA communication**

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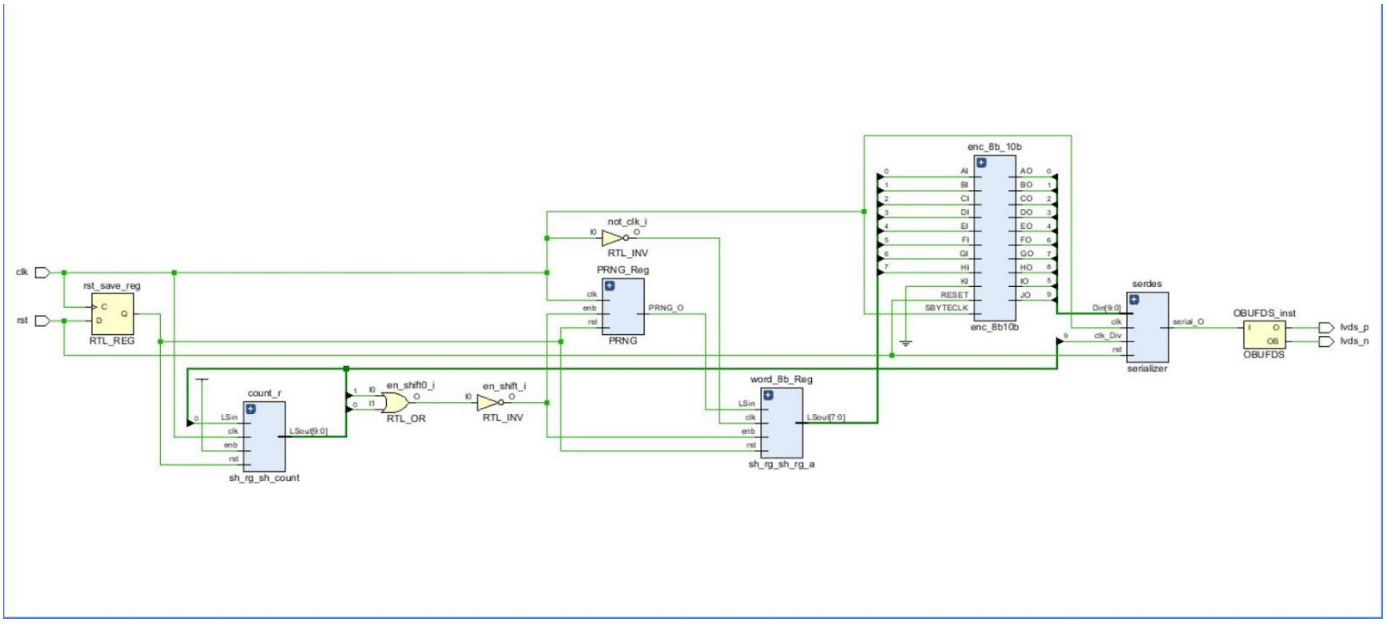
1. Creating projects and design flow on Xilinx Vivado:
   - Software version: Xilinx Vivado 2017.4
   - Product Family: Zynq-7000
   - Target Device: xc7z020clg400-1
   - Language: VHDL

2. Creating projects and design flow on Lattice Diamond:
   - Software version: Lattice Diamond
   - Product: MachXO2
   - Target Device: LCMXO2-1200HC
   - Package: “TQFP100”
   - Grade: 4
   - Language: VHDL

3. Link training between ZYNQ and MachXO2:

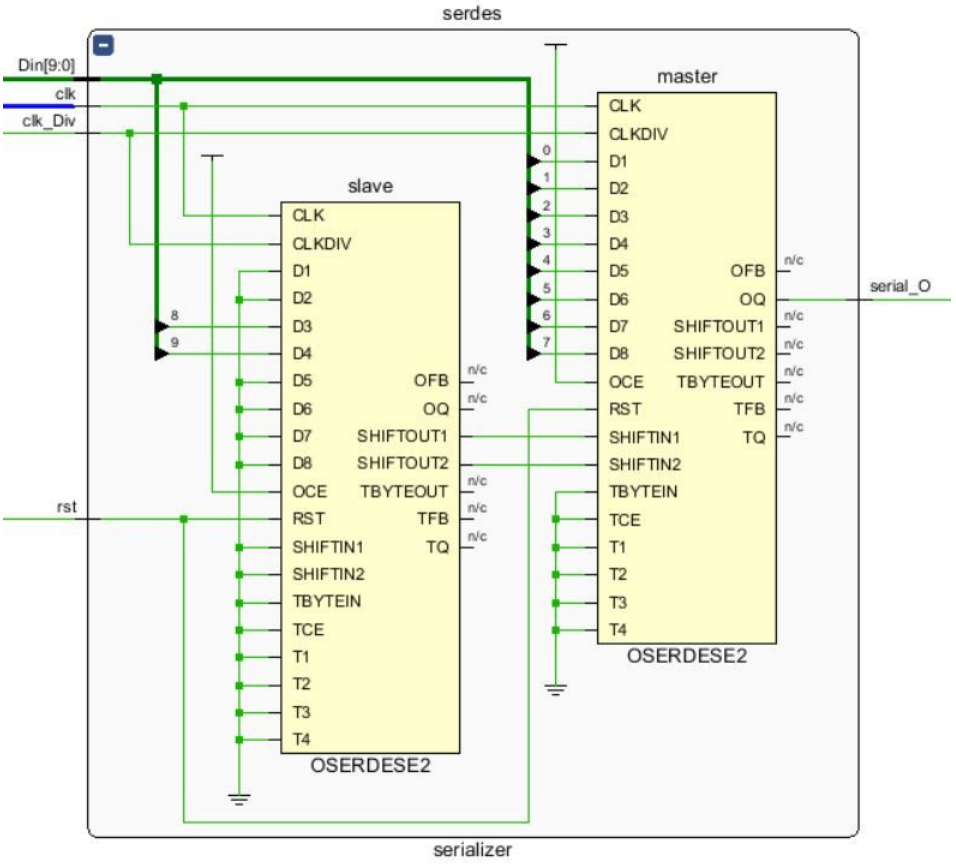
First, By considering the ZYNQ side it has 3 main modules:



1- **PRNG**: Pseudo Random Number Generation which has a Fibonacci LFSR of polynomial 5.3.2.0 of the xor-ed bits with a seed of “11100111” that gives a 255 generated words and loops again. The only word that didn’t generate is “00000000” as its the reset value of the receiver, sending it once the rest signal of Transmitter is fired(after encoding).

2- **enc_8b_10b**: Its an open source code based on IBM encoding that encodes the eight bits generated from PRNG into 10 bits that have a balanced no. of zeros and ones and can make the receiver to regenerate the clock from the received data.

3- **Serializer**: a pair of OSERDESE2 primitives are used in a master & slave configuration in SDR mode for 10:1 serialization ratio, it takes the 10 bits encoded from 8b_10b as input to be serialized.



Rest of modules and signals:

- **OBUFDS**: The output of the serializer is converted into a differential signal (LVDS) by the primitive OBUFDS.
- **count_r** : synchronous counter of size 10 bits that shifts a value of ‘1’ every clk cycle that enables PRNG to shift the new value at the first 8 counts and disable it for 2 cycles to calculate the encoded 10 bits.
  Also count(9) enables serdes to capture the new value to send it for the 10 cycles of the counter

- **rst_save_reg**: register of 1 bit that save the value of the input reset to my module to be last for one cycle after the reset input is set to '0'