# **FOBOS**

Release 2.0

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#### FOBOS Documentation

The Flexible Opensource workBench fOr Side-channel analysis FOBOS is an SCA platform.

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#### INTRODUCTION

The Flexible Opensource workBench fOr Sidechannel analysis (FOBOS) is a platform that can be used for side channel analysis. You can perform trace collection (Data Acquisition) and attacks (Data Analysis). The system is suitable for educational and research purposes.

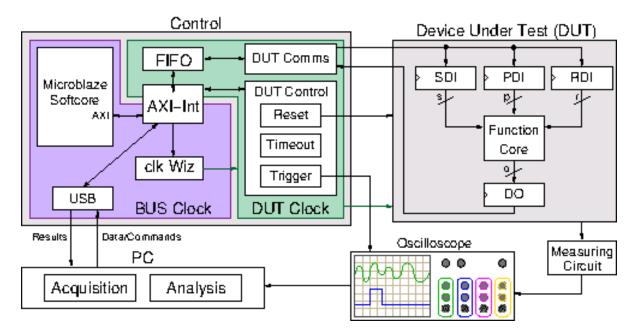


Fig. 1: FOBOS Block Diagram

#### 1.1 Feature Overview

- Separate control and (Design Under Test) boards allowing addition of new DUTs easily.
- Uses commercial over-the-shelf boards to when possible to reduce cost.
- Digilent Basys3 and Nexys A7 control board.
- DUT support includes Diginelt Nexys3 board (Xilinx Spartan6) and compatible with NewAE CW305 (Xilinx Artix7 boards).
- Adjustable DUT clock.
- Adjustable trigger signal.
- Scripts to perform Deferential Power Analysis (DPA).

• Leakage assessment using t-test.

**CHAPTER** 

**TWO** 

### **QUICK START**

Below, we describe how to setup FOBOS hardware and software and test that everything is working.

### 2.1 Requirements

- 1. Digilent Basys3 board
- 2. A PC with Linux installed
- 3. Python2 installed
- 4. Xilinx Vivado 2017.2

### 2.2 Software Installation

Note: The following installation procedure is tested on Linux Ubuntu 16.04.

- 1. Download FOBOS from the FOBOS home page.
- 2. Extract the archive into the directory of your choice

```
$ tar xvfz fobos-v2.0.tgz
```

3. Use the following commands to install the necessary Python packages:

```
$ sudo apt-get install python-pip
$ sudo pip install numpy
$ sudo pip install pyserial
$ sudo pip install matplotlib
$ sudo pip install scipy
$ sudo pip install configuration
```

### 2.3 Hardware Setup

1. Build the control board Vivado project.

```
$ cd path-to-fobos/capture/ctrl/basys3ctrl/vivado
$ make
```

2. Open the project created using Vivado

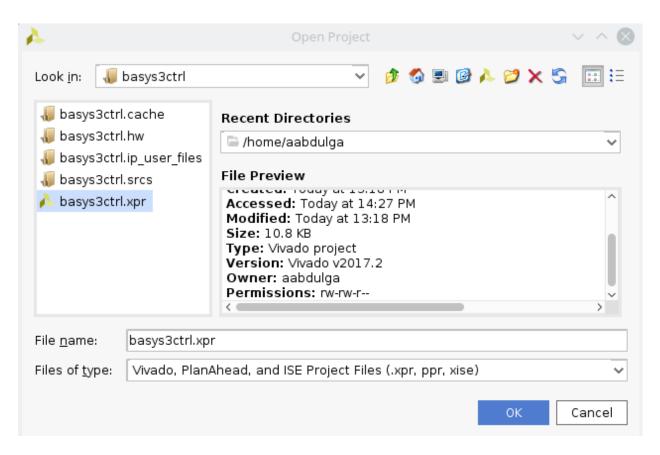


Fig. 1: Open Vivado project

- 3. In the Flow Navigator window, click 'Generate Bitstream'.
- 4. After bitstream is generated, click File > Export > Export Hardware ... make sure to select 'Include bitstream'.

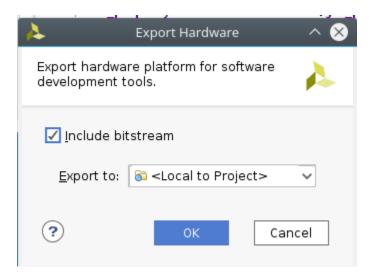


Fig. 2: Export Hardware

5. Launch the Xilinx SDK (File > Launch SDK).

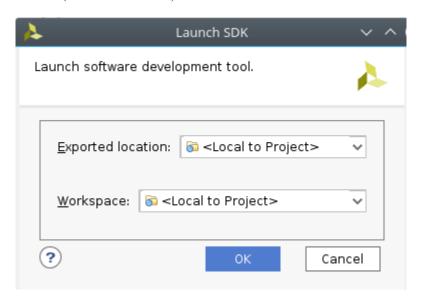


Fig. 3: Launch SDK

- 6. In the SDK, create a new empty project(File> New application project). You will need to select the hardware platform. SDK will create the BSP project from the hardware platform and create the empty project.
- 6. Link all the .c and .h files in the fobos/sources/basys3ctrl/sdk/src to the project (right-click on (project/src) > Import -> General-> file system -> browse to file). make sure to check "Advanced-> Create links in the workspace" and "Create virtual folders".
- 7. Right-click on the project you just created and select Build Configurations > Set Active > Release. Then right-click again and select Build Project.
- 8. Make sure that there are no debug flags. Right-click the release folder under the project and select Properties. In

2.3. Hardware Setup

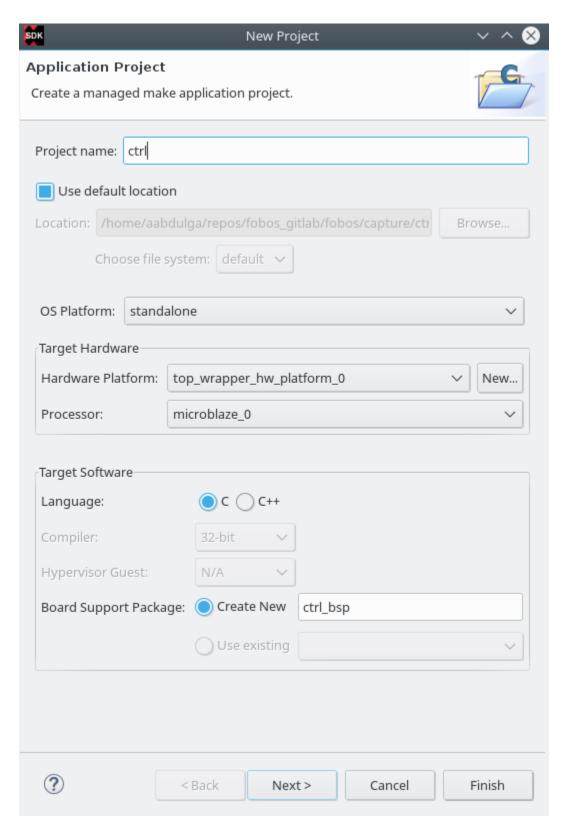


Fig. 4: Create Project

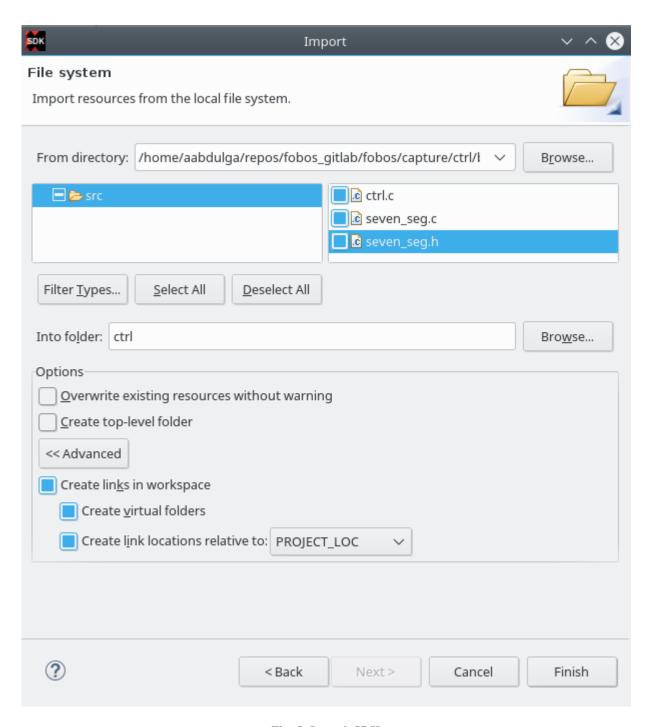


Fig. 5: Launch SDK

2.3. Hardware Setup

the window that appears select C/C++ Build > Settings > Microblaze gcc Compiler > Debugging and set Debug Level to 'None'.

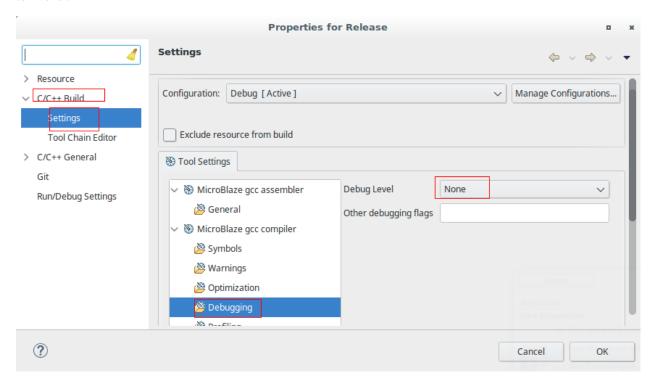


Fig. 6: Remove Debugging

**CHAPTER** 

**THREE** 

## **INSTALLATION**

### 3.1 The controller

To install FOBOS you need to download the package from: and run \$ setup fobos

### **CHAPTER**

## **FOUR**

## **INDICES AND TABLES**

- genindex
- modindex
- search