Lab 4 – Bitwise Operations

Bitwise operations are operations that are executed for each bit (bit-by-bit).

We have:

- logical bitwise operations
- shift operations
- rotate operations

Boolean op -> logical bitwise operations

Operand1 – op1	Operand2 – op2	And op1, op2	Or op1, op2	Xor op1, op2	Not op1
0	0	0	0	0	1
0	1	0	1	1	1
1	0	0	1	1	0
1	1	1	1	0	0

The IA-32 assembly instructions that perform these logical bitwise operations are detailed below:

and operand1, operand2

or operand1, operand2

xor operand1, operand2

not operand1

where *operand1* and *operand2* are either registers, memory references (i.e. variables) or constants (*operand1* can not be a constant!) both of the same size/type: byte, word, doubleword.

Each single bit of *operand2* is and/or/xor with each corresponding bit from *operand1*.

The result is in all cases saved in operand1

The not operation is a unary operation, so the bits of operand1 are modified directly

General rules for OR and AND

X or 0 = X

X or 1 = 1

X and 0 = 0

X and 1 = X

Examples:

Data segment: a db 0000.1111b

Code segment:

and byte[a], 0000.0101b; => 0000.1111b and

0000.0101b => a=0000.0101b

or byte[a], 0000.1101b; => 0000.0101b or

0000.1101b =>a=0000.1101b

xor byte[a], 0000.0110b; => 0000.1101b xor

0000.0110b =>a=0000.1011b

Xor allows us to save value 0 in a register (instead of using mov eax, 0): Xor eax, eax => eax = 0

not byte[a] ; => not 0000.1011b =>a=1111.0100b

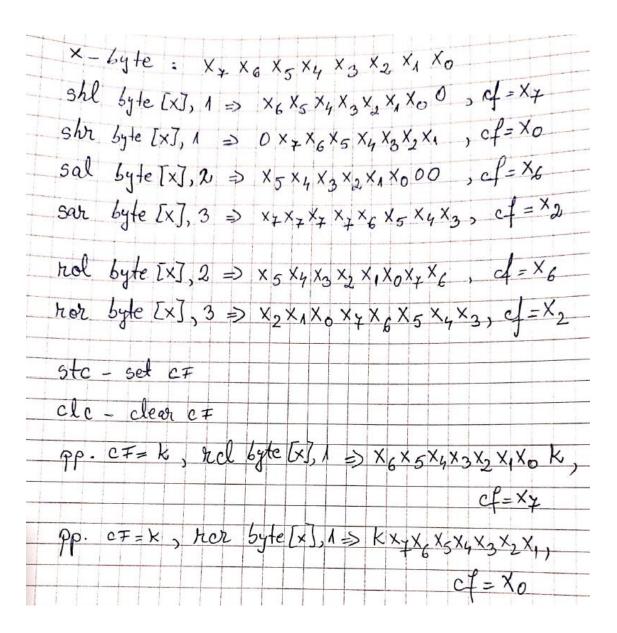
Shift instructions and operations

SHL destination, count	The SHL (shift logic left) instruction	mov dl, 0000.1111b
	performs a logical left shift on the	shl dl, 3; dl = 0111.1000b
destination: reg, mem	destination operand, filling the lowest bit	
count: imm8, or CL reg	with 0. The highest bit is moved to the Carry	
	flag, and the bit that was in the Carry flag is	
	discarded.	
SHR destination, count	The SHR (shift logic right) instruction	mov bl, 1010.1010b
	performs a logical right shift on the	shr bl, 4; bl = 0000.1010b
destination: reg, mem	destination operand, replacing the highest	
count: imm8, or CL reg	bit with a 0.	
	The lowest bit is copied into the Carry flag,	mov eax, 12340000h
	and the bit that was previously in the Carry	shr eax, 16; eax = 00001234h
	flag is lost.	
SAL destination, count	The SAL (shift arithmetic left) instruction	mov al, 1110.0011b
	works the same as the SHL instruction. For	sal al, 1; al=1100.0110b, cf=1
destination: reg, mem	each shift count, SAL shifts each bit in the	
count: imm8, or CL reg	destination operand to the next highest bit	
	position. The lowest bit is assigned 0.	mov bl, 0000.1111b
	The highest bit is moved to the Carry flag,	sal bl, 2; bl = 0011.1100b
	and the bit that was in the Carry flag is	
	discarded.	
SAR destination, count	The SAR (shift arithmetic right) instruction	mov al, 1110.0011b
	performs a logical right shift on the	sar al, 1; al=1111.0001b, cf
destination: reg, mem	destination operand, filling all the positions	=1
count: imm8, or CL reg with the most significant bit (bit sign).		
	The lowest bit is copied into the Carry flag,	
	and the bit that was previously in the Carry	mov bl, 10101010b
	flag is lost.	shr bl, 4; bl = 11111010b

Rotate instructions and operations

ROL destination, count	The ROL (rotate left) instruction shifts	mov bl, 0111.1000b
	each bit to the left.	rol bl, 4; bl = 1000.0111b, cf = 1
destination: reg, mem	The highest bit is copied into the Carry	
count: imm8, or CL reg	flag and the lowest bit position.	
		mov bl, 1111.0000b
		rol bl, 6 ; bl = 0011.1100b
ROR destination, count	The ROR (rotate right) instruction shifts	mov al, 1010.1110b
	each bit to the right and copies the	ror al, 3 ; al=1101.0101b, cf=1
destination: reg, mem	lowest bit into the Carry flag and the	
count: imm8, or CL reg	highest bit position.	

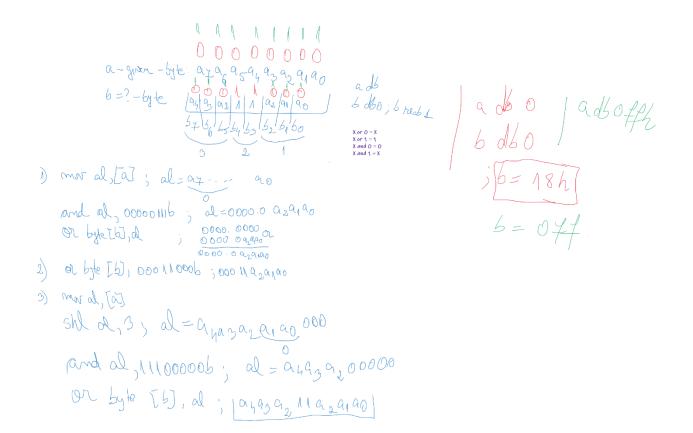
		mov al, 1111.0000b
		ror al, 5; al=1000.0111b
RCL destination, count	The RCL (rotate carry left) instruction	mov al, 0
1102 1101111111111111111111111111111111	shifts each bit to the left, copies the Carry	stc
destination: reg, mem	flag to the LSB, and copies the MSB into	rcl al, 1; al=0000.0001b, cf = 0
count: imm8, or CL reg	the Carry flag.	Ter al, 1 , ar occolocolo, er c
22.10	the curry ring.	
		mov al, 0
		stc
		rcl al, 2; al=0000.0010b, cf=0
		mov al, 0
		stc
		rcl al, 3 ;al = 0000.0100b, cf=0
RCR destination, count	The RCR (rotate carry right) instruction	mov bl, 0
	shifts each bit to the right, copies the	stc
destination: reg, mem	Carry flag into the MSB, and copies the	rcr bl, 1; bl=1000.0000b, cf = 0
count: imm8, or CL reg	LSB into the Carry flag.	
		mov bl, 0
		stc
		rcr bl, 2 ;bl=0100.0000b, cf=0
		mov bl, 0
		stc
		rcr bl, 3, bl =0010.0000b, cf=0



Prob1:

Being given a byte A, construct a new byte B in the following way:

- bits 0-2 of B should be equal to bits 0-2 of A
- bits 3-4 of B should be set to 1
- bits 5-7 of B should be equal to bits 2-4 of A



Prob 2: Generate value 13 in al.

$$\frac{d=13}{|Shf++no-lade|} = d=0000.11015$$

MAR al, 0

Stc; $f=1$
 $ncl al_{1}$; $al=0000.00016$, $cf=0$

Stc

 $ncl al_{1}$; $al=0000.00116$, $cf=0$
 shc
 shc
 $ncl al_{1}$; $al=0000.00116$, $cf=0$
 shc
 $ncl al_{1}$; $al=0000.00106$, $cf=0$
 shc
 $ncl al_{1}$; $al=0000.11016$, $cf=0$
 $ncl al_{1}$; $al=0000.11016$, $cf=0$

Prob 3. Identify the numbers a and b from 2 doubleword X and Y: a is represented of bits 11-16 of X b is represented of bits 26-31 of Y Compute then a*b.

