CSR Module

CSR is a Ucie Adapter registers memory, with APB3 Salve.

Data is exchanged between Protocol layer and internal memory through APB3 protocol.

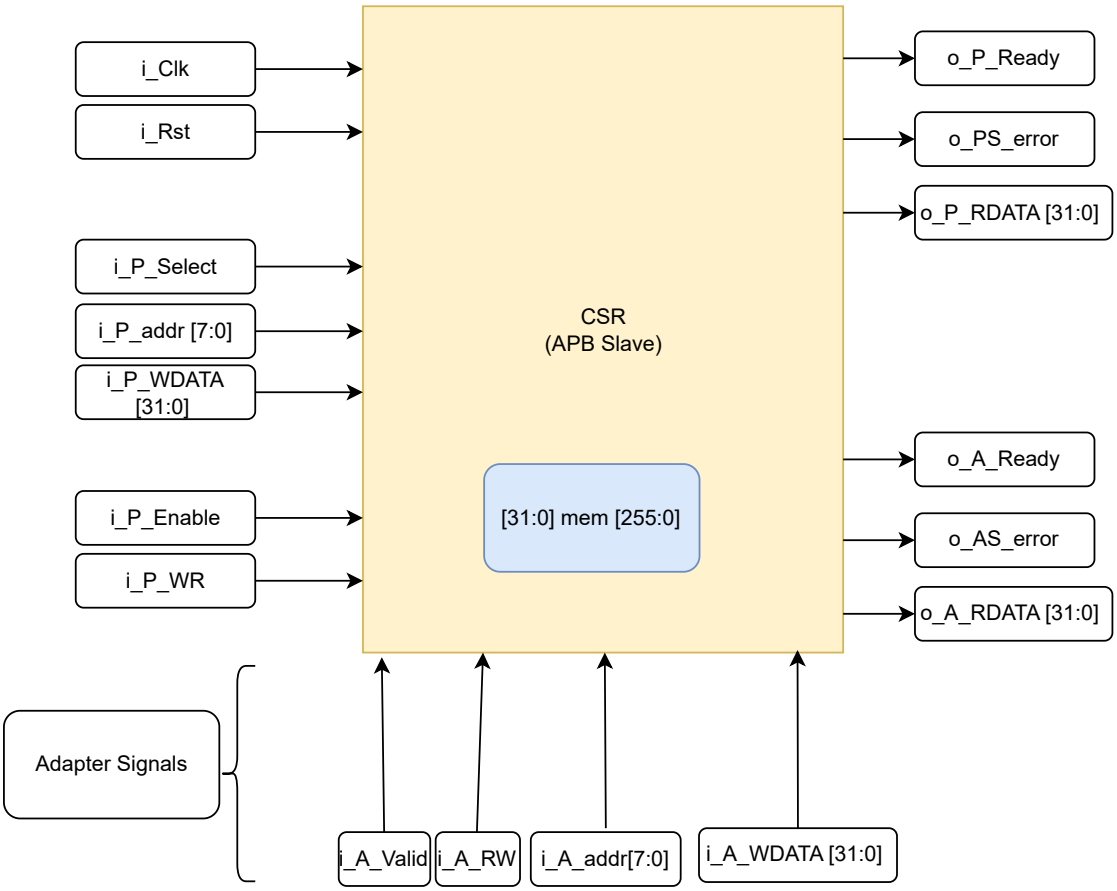
Data is also exchanged between Adapter and internal memory through A_WR , A_Valid and A_Ready signals.

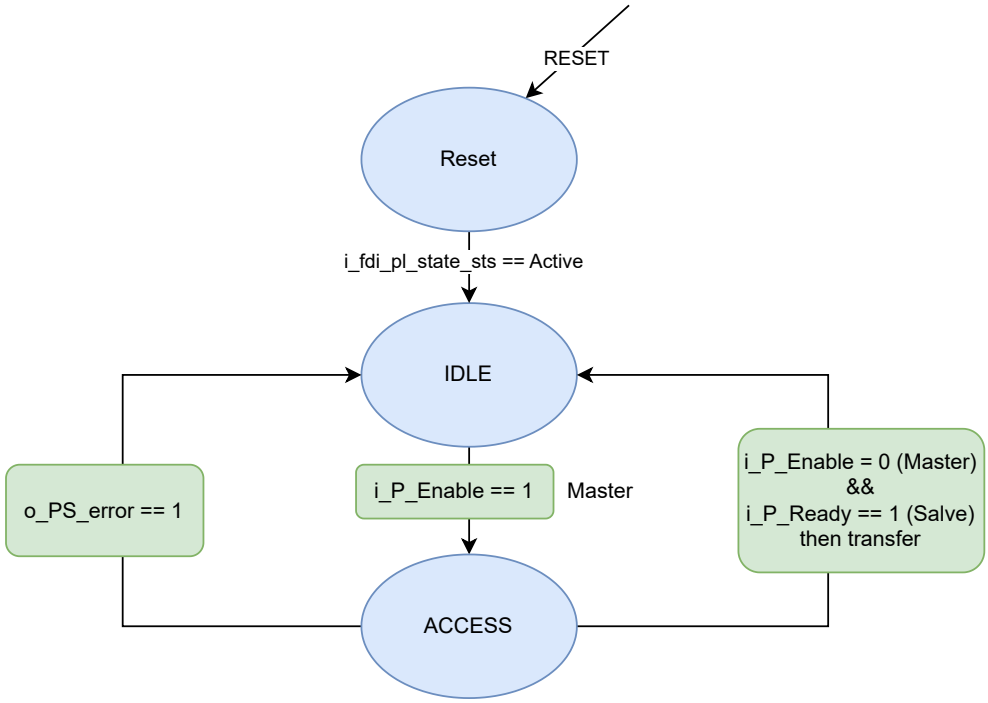
Signal	Direction	Width	Description
i_clk	Input	1 bit	Input clk to the system.
i_rst	Input	1 bit	Synchronous Reset.
i_P_Select	Input	1 bit	Used to initiate a request from Protocol layer (may be used to Select peripheral).
i_P_addr	Input	8 bit	Address of the needed location from the Protocol.
i_P_WDATA	Input	32 bit	Write Data bus from Protocol.
i_P_Enable	Input	1 bit	Enable signal from Protocol.
i_P_WR	Input	1 bit	Read/Write control signal from protocol. 0→Read, 1→Write
o_P_Ready	Output	1 bit	Ready to Transfer signal from internal APB Slave to Protocol.
o_PS_error	Output	1 bit	Error signal from internal APB Slave to Protocol. Ex:(*1)
o_P_RDATA	Output	32 bit	Read Data bus to Protocol.
i_A_WR	Input	1 bit	Read/Write control signal from Adapter. 0→Read, 1→Write
i_A_addr	Input	8 bits	Address of the needed location from Adapter.

i_A_WDATA	Input	32 bit	Write Data bus from Protocol.
i_A_Valid	input	1 bit	Used to initiate a request from Adapter layer.
o_A_Ready	Output	1 bit	Ready to Transfer signal from internal APB Slave to Adapter.
o_AS_error	Output	1 bit	Error signal from internal APB Slave to Adapter. Ex:(*1)
o_A_RDATA	Output	32 bit	Read Data bus to Protocol.

Note:

- Signals start with P is related to Protocol to CSR transfers.
- Signals start with P is related to Adapter to CSR transfers.
- (*1) Error examples:
    1. Trying to Access Reserved part of memory.
    2. Trying to write Read-only location in memory.


i_Clk
i_Rst
i_P_Select
i_P_addr [7:0]
i_P_WDATA [31:0]
i_P_Enable
i_P_WR
CSR
(APB Slave)
[31:0] mem [255:0]
o_P_Ready
o_PS_error
o_P_RDATA [31:0]
o_A_Ready
o_AS_error
o_A_RDATA [31:0]
Adapter Signals
i_A_Valid
i_A_RW
i_A_addr[7:0]
i_A_WDATA [31:0]


RESET
Reset
i_fdi_pl_state_sts == Active
IDLE
i_P_Enable == 1
Master
ACCESS
o_PS_error == 1
i_P_Enable = 0 (Master)
&&
i_P_Ready == 1 (Salve)
then transfer