

Module Signal Table Documentation

Block role:

Rx block is inside the adapter connected to 2 interfaces RDI and FDI, where to receive the data from RDI and send it to FDI according to state and signals that shown below.

1. ucie_rx_buffer Module

Signal Name	Type	Width	Description
i_clk	Input	1	Clock signal
i_rst	Input	1	Reset signal
i_rdi_pl_data	Input	[NBYTES-1:0][7:0]	Data input to the buffer (from RDI)
i_rdi_pl_valid	Input	1	Valid signal for rx_data (from RDI)
o_fdi_data	Output	[NBYTES-1:0][7:0]	Data output from the buffer
o_fdi_data_valid	Output	1	Valid signal for data_out
i_buffer_enable	Input	1	Enable signal for the buffer
o_overflow_detected	Output	1	Overflow detection signal

2. ucie_rx_fsm Module

Signal Name	Type	Width	Description
i_clk	Input	1	Clock signal
i_rst	Input	1	Reset signal
i_state_request	Input	3	Current state of the system (from control unit)
i_overflow_detected	Input	1	Overflow detection signal from buffer
o_buffer_enable	Output	1	Enable signal for buffer
o_overflow_error	Output	1	Overflow error signal (to control unit)

3. ucie_adapter_rx_block (Top-Level) Module

Signal Name	Type	Width	Description
i_clk	Input	1	Clock signal
i_rst	Input	1	Reset signal
i_state_request	Input	3	Current state of the system (from control unit)
i_rdi_pl_data	Input	[NBYTES-1:0][7:0]	Data received (from RDI)
i_rdi_pl_valid	Input	1	Valid signal for rx_data (from RDI)
o_fdi_data_out	Output	[NBYTES-1:0][7:0]	Data output to the protocol layer
o_fdi_data_valid	Output	1	Valid signal for data_out
o_overflow_error	Output	1	Overflow error signal (to the control unit)





