SB module

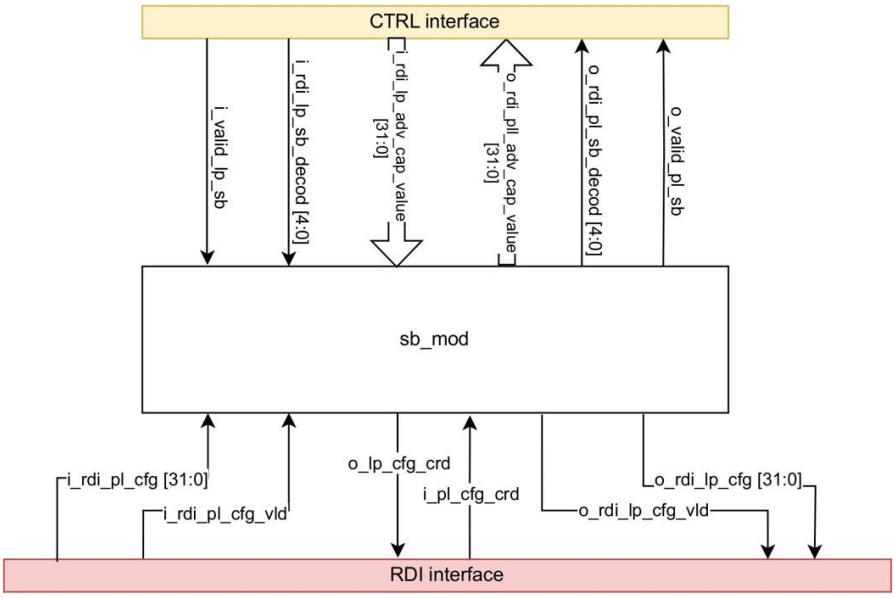
Block Role

This module facilitates communication between the adaptor layer and the PHY layer by handling the transmission and reception of messages. Additionally, it interfaces with the CTRL module through decoded messages to identify and construct the required message content. The module is responsible for re-decoding received messages and providing corresponding responses to the CTRL module. It also manages flow control with the PHY layer using a credit-based mechanism, with one credit allocated for each message type.

The messages processed by the module are categorized into two types: messages without data and messages with data. Messages with data are related to advertising capability messages at which a data is forwarded in parallel with the decoded headers to be sent on their specific phase on the SB – PHY message link after building the message, same happened in the receiving after re-building the decoded message back to send both in parallel again to CTRL as an another die response. However in the messages without data it is assumed to zero padding the message data phases and will be ignored in the receiving.

In summary, this module serves as a critical intermediary for message exchange between the adaptor and PHY layers while ensuring efficient interaction with the CTRL module. By managing message decoding, encoding, and flow control with an optimized way.

Top level Architecture



IO Top level interfacing signals

Signal	Direction	Width	Functionality
i_rdi_lp_sb_decode	form CTRL	5 bits	Input decoded message sent from ctrl mod to determine the message needed to be sent by the side band.
i_valid_lp_sb	from CTRL	1 bit	A valid signal for the decoded message sent from ctrl module.
i_rdi_adv_cap_value	From CTRL	32 bit	Data signals carrying message data of AdvCap register.
i_pl_cfg_crd	from PHY	1 bit	Credit return for sideband packets from the Physical Layer to the Adapter for sideband packets. Each credit corresponds to 64 bits of header and 64 bits of data. Even transactions that don't carry data or carry 32 bits of data consume the same credit and the Physical Layer returns the credit once the corresponding transaction has been processed or deallocated from its internal buffers. Because the advertised credits are design parameters, the Adapter transmitter updates the credit counters with initial credits on domain reset exit, and no initialization credits are returned over the interface.
i_pl_cfg [31:0]	from PHY	32 bits	This is the sideband interface from the Physical Layer to the Adapter.
i_pl_cfg_vld	from PHY	1 bit	When asserted, indicates that pl_cfg has valid information that should be consumed by the Adapter.
o_rdi_pl_sp_decode	TO CTRL	5 bits	Output decode message sent to the ctrl module determining the other die response and comparison result for the AdvCap messages.
o_valid_pl_sb	To CTRL	1 bit	A valid signal for the decoded message sent to ctrl module.

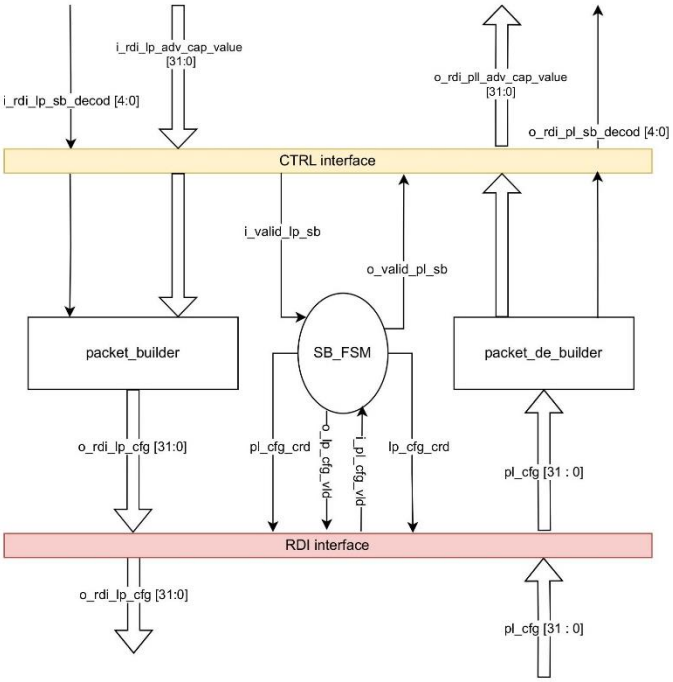
o_rdi_lp_adv_cap_value	To CTRL	32 bit	Data signals carrying message data for AdvCap register received for other die.
o_lp_cfg_crd	To PHY	1 bit	Credit return for sideband packets from the Adapter to the Physical Layer for sideband packets. Each credit corresponds to 64 bits of header and 64 bits of data. Even transactions that don't carry data or carry 32 bits of data consume the same credit and the Adapter returns the credit once the corresponding transaction has been processed or deallocated from its internal buffers. Because the advertised credits are design parameters, the Physical Layer transmitter updates the credit counters with initial credits on domain reset exit, and no initialization credits are returned over the interface.
o_lp_cfg [31:0]	To PHY	32 bits	This is the sideband interface from Adapter to the Physical Layer.
o_lp_cfg_vld	To PHY	1 bit	When asserted, indicates that lp_cfg has valid information that should be consumed by the Physical Layer.

Module Sub blocks

1) Packet Builder sub-block

2) Packet de-builder sub-block

3) SB_FSM



1) Packet Builder sub-block

This sub-block is responsible for building messages on four phases based on decode message from the ctrl module command. It contains a decode analyser message that ouputs a control signals for selecting certain message parts: op_code, msg_code, msg_sub_code, msg_info... etc. Depending the received decode message is start choosing the message parts and concatenating on four phases.

Messages with data																													
Bytes	3								2								1								0					
Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header / Data	Header																															
Phase0	srcid			rsvd		rsvd			msgcode[7:0]								rsvd								opcode[4:0]							
Phase1	dp	cp		rsvd		dstid			MsgInfo[15:0]																MsgSubcode[7:0]							
Header / Data	Data																															
Phase2	data[31:0]																															
Phase3	data[63:32]																															

1.1) Decode Analyser block

Decode bits devider to determine the selection of message parts **(refer to full arch)**

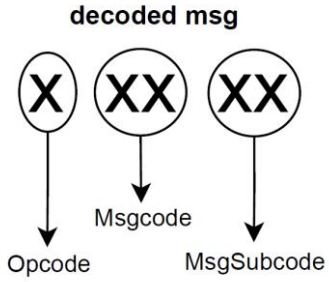
Signal	Width	Values	Functionality
w_op_sel	1 bit	i_rdi_lp_sb_decode [4]	Selects the message op_code part
w_msg_sel	2 bits	i_rdi_lp_sb_decode [1:0]	Selects the msg_code part
w_sub_sel	2 bits	i_rdi_lp_sb_decode [3:2]	Selects the sub_msg_code part
w_Sel_adv2	1 bit	i_rdi_lp_sb_decode [4]	Select the third phase data: padding for no data message and data for messages with data (AdvCap).
w_Sel_adv3	1 bit	i_rdi_lp_sb_decode [4]	Select the fourth phase data: padding for no data message and data for messages with data (AdvCap).

2) Packet de-builder sub-block

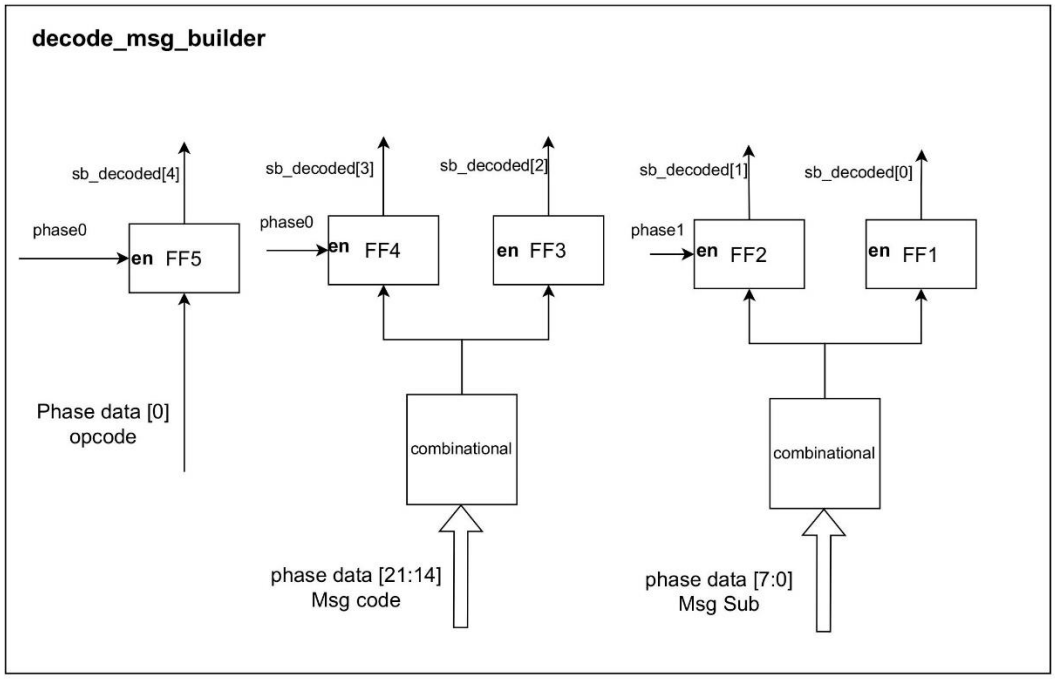
This sub-block is responsible for receiving messages from PHY layer and rebuilding the decode message to be sent to the ctrl module. It receives message phase on a 32 bit buffer and starts extracting message needed parts for determining the decode message. Extracting and building the decode message back is mainly the function of the decode builder.

2.1) Decode_msg_builder block

Extracting message Opcode, Msgcode, and MsgSubcode and building decoded message back based on the received header message phases according to the following decoding pattern:



Block internal Architecture

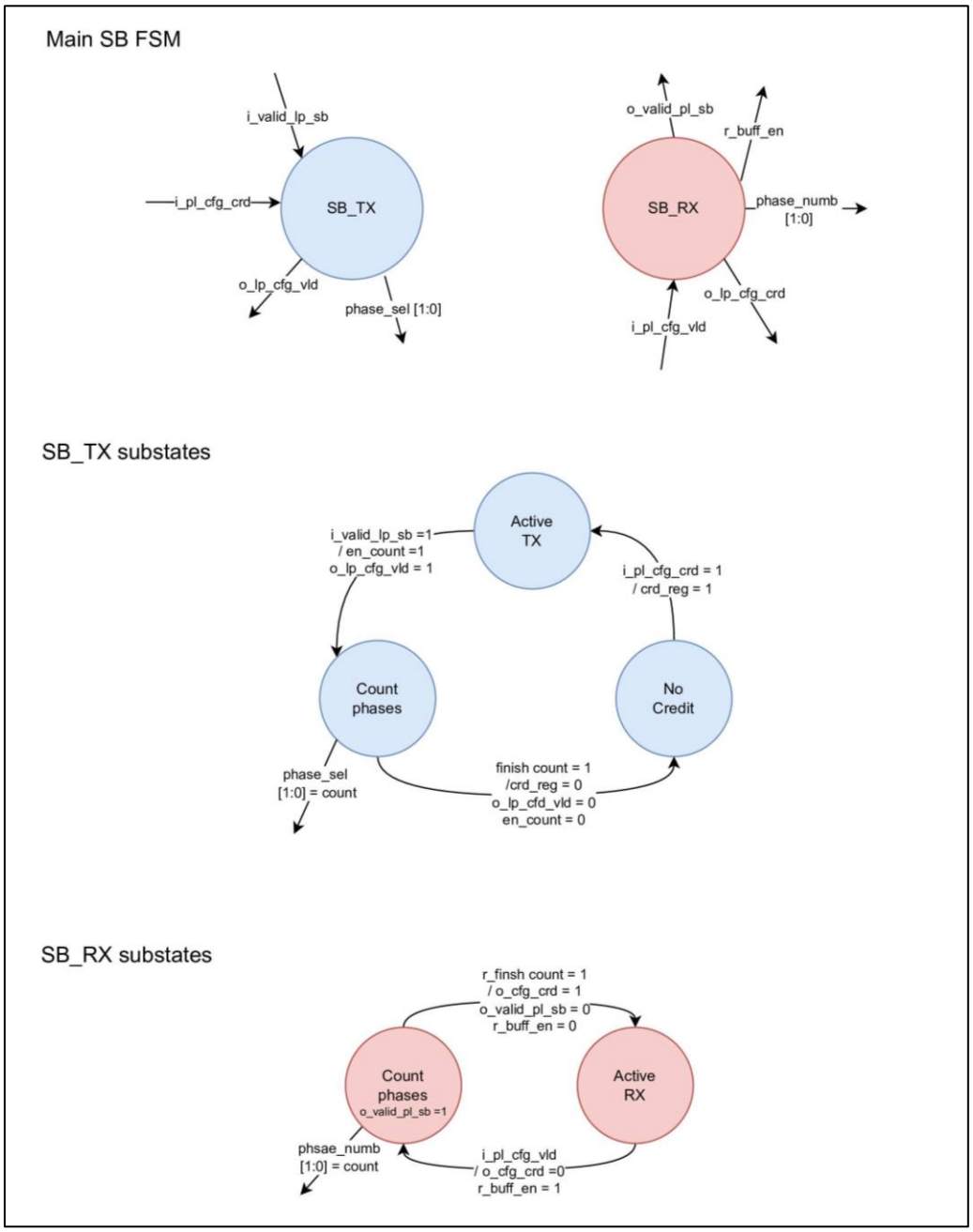


Control Signals

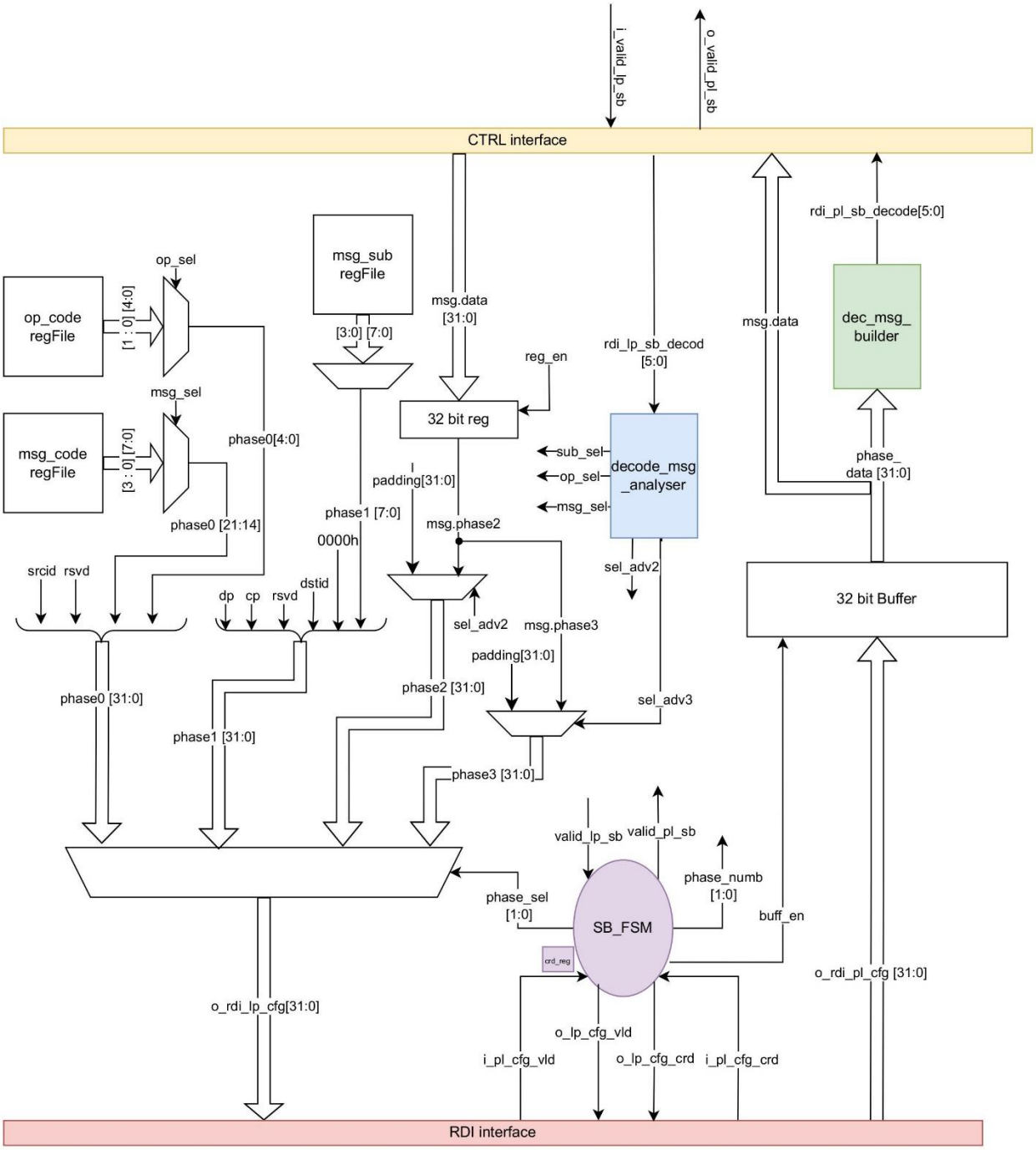
Signal	width	Functionality
Phase_number	2 bits	Determine the phase number that the extraction will be based upon.

3) SB_FSM

This FSM is sending control signals for operating the whole block. It sends phase counter for transmitting messages, enable signal for receiving buffer, increment/decrement credit register based for flow control and sending/receiving valid signals to/from ctl module and the PHY layer.



Full level 2 Architecture



CTRL – SB Message Dictionary

Message	Decoded	Function
ADV_CAP	00000b	Advertising Capability message between dies.
LINK_MGMT_ADAPTER0_REQ_ACTIVE	10101b	Request Active state to/from sb adaptor.
LINK_MGMT_ADAPTER0_REQ_LINK_RESET	10111b	Request Link Reset state to/from sb adaptor.
LINK_MGMT_ADAPTER0_RSP_ACTIVE	11001b	Response Active state to/from sb adaptor.
LINK_MGMT_ADAPTER0_RSP_LINK_RESET	11011b	Response Link Reset state to/from sb adaptor.
ERROR_CORRECTABLE	11100b	Correctable Error messages.
ERROR_NON_FATAL	11101b	Non- fatal Error messages.
ERROR_FATAL	11110b	Fatal Error messages.