UCIe TX

Module Role

TX module is mainly responsible for transmitting Raw format data bytes from protocol layer to PHY layer. It is controlled by FSM_TX internal block at which two signals an adaptor state status is received from ctrl module to be active for transaction only is the received status is active. An Overflow error is also forwarded in according to the TX FIFO status and the protocol requests for transmitting data.

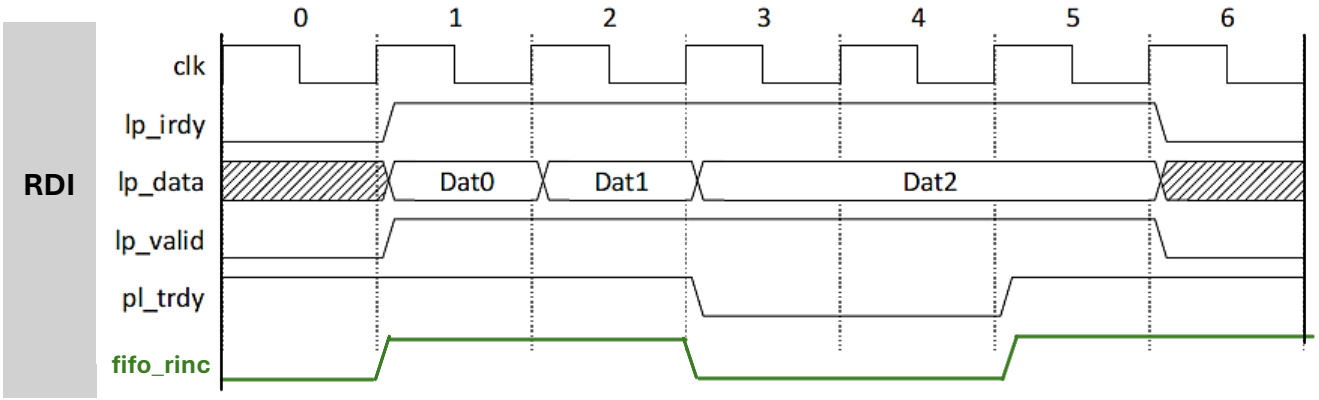
IO Top level interface signals

Signal	direction	width	Functionality
i_fdi_pl_state_sts	Input from crl_mod	4 bits	An input signal determining the status state of the adaptor for which the TX_mod is only active when i_fdi_pl_state_sts == Active.
o_tx_overf_err	Output to crl_mod	1 bit	This is a signal indicating that the tx_fifo is overflowing data, triggered high when the fifo_full ,fdi_lp_valid and fdi_lp_irdy are asserted.
i_fdi_lp_data	Input from protocol layer	NBYTES * 8 bits	Data to be captured from protocol layer. NBYTES = 8B. (8 lanes with 8 bits width for each).
i_fdi_lclk	Input from FDI clock domain	1 bit	Higher speed clock of the FDI.
i_fdi_lp_valid	Input from protocol layer	1 bit	Input signal indicating that protocol layer has a valid data to send.
i_fdi_lp_irdy	Input from protocol layer	1 bit	Input signal indicating that protocol layer is ready to send data, only asserted if i_fdi_lp_valid is asserted.
o_fdi_pl_trdy	Output to protocol layer	1 bit	Indicating that TX_mod is ready to accept data to be send over PHY. Asserted if fifo_full is deasserted.
i_rdi_pl_trdy	Input from PHY layer	1 bit	Indicating PHY layer is ready to accept data to be send.
i_rdi_lclk	Input from RDI clock domain	1 bit	Lower speed clock of the FDI.
o_rdi_lp_valid	Output to PHY layer	1 bit	Output signal indicating that adaptor layer has a valid data to send to PHY.

o_rdi_lp_irdy	Output to PHY layer	1 bit	Output signal indicating that adaptor layer is ready to send data to PHY, only asserted if i_rdi_lp_valid is asserted.
i_fdi_lp_data	Output to PHY layer	NBYTES * 8 bits	Data to be send to PHY layer. NBYTES = 8B. (8 lanes with 8 bits width for each).

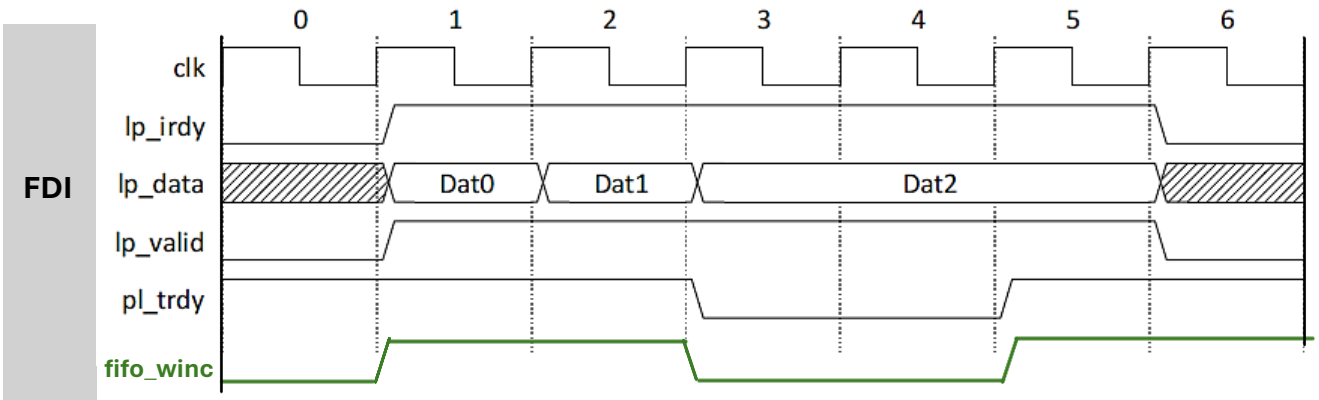
Data Transfer Wave form showing Standard Case at RDI

Based in the standard case for data transfer from Adaptor layer over the PHY layer data is transferred when lp_irdy, pl_trdy, lp_valid are all asserted. Thus a FIFO signal to increment FIFO read address is sent to the FIFO block and the data transfer starts. It is also considered to have bubbles also during the flit transfer as a back pressure response for the PHY layer pl_trdy signal de-assertion.

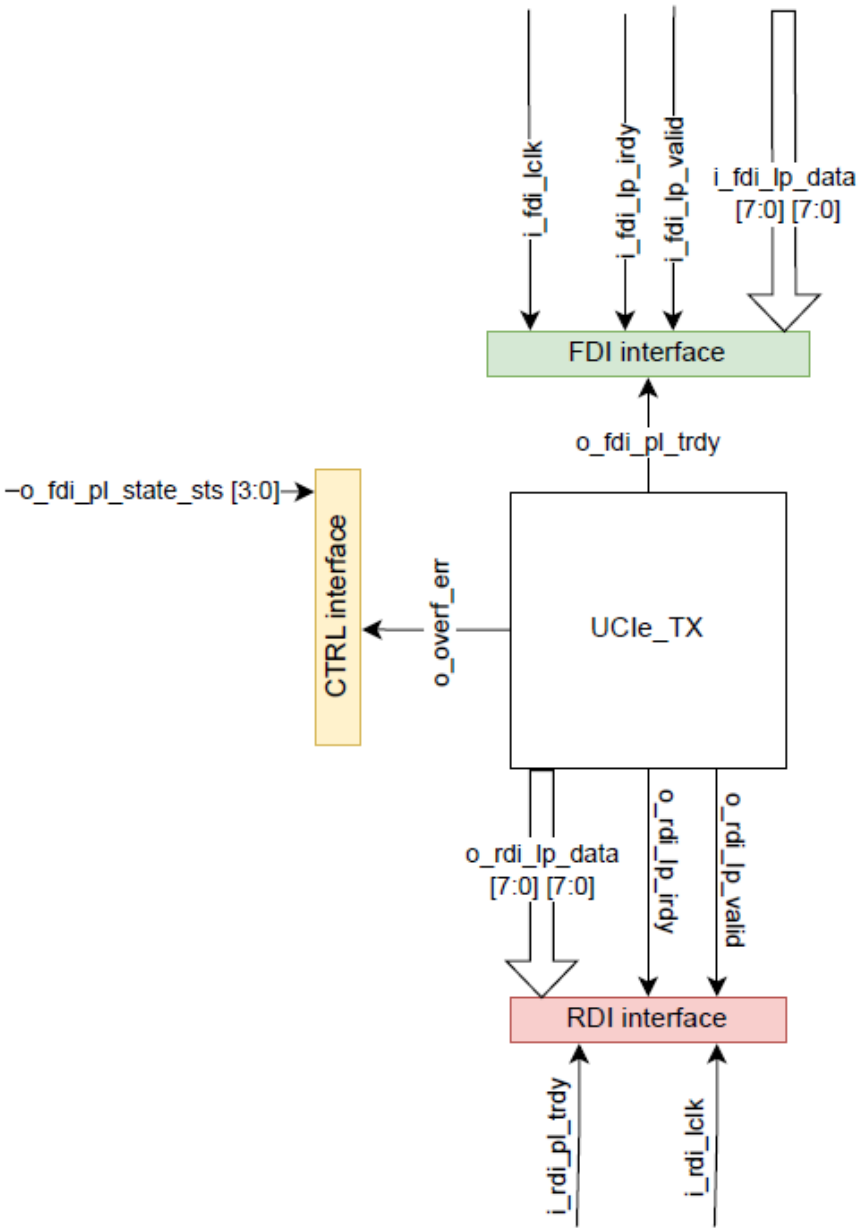


Data Transfer Wave form showing Standard Case at FDI

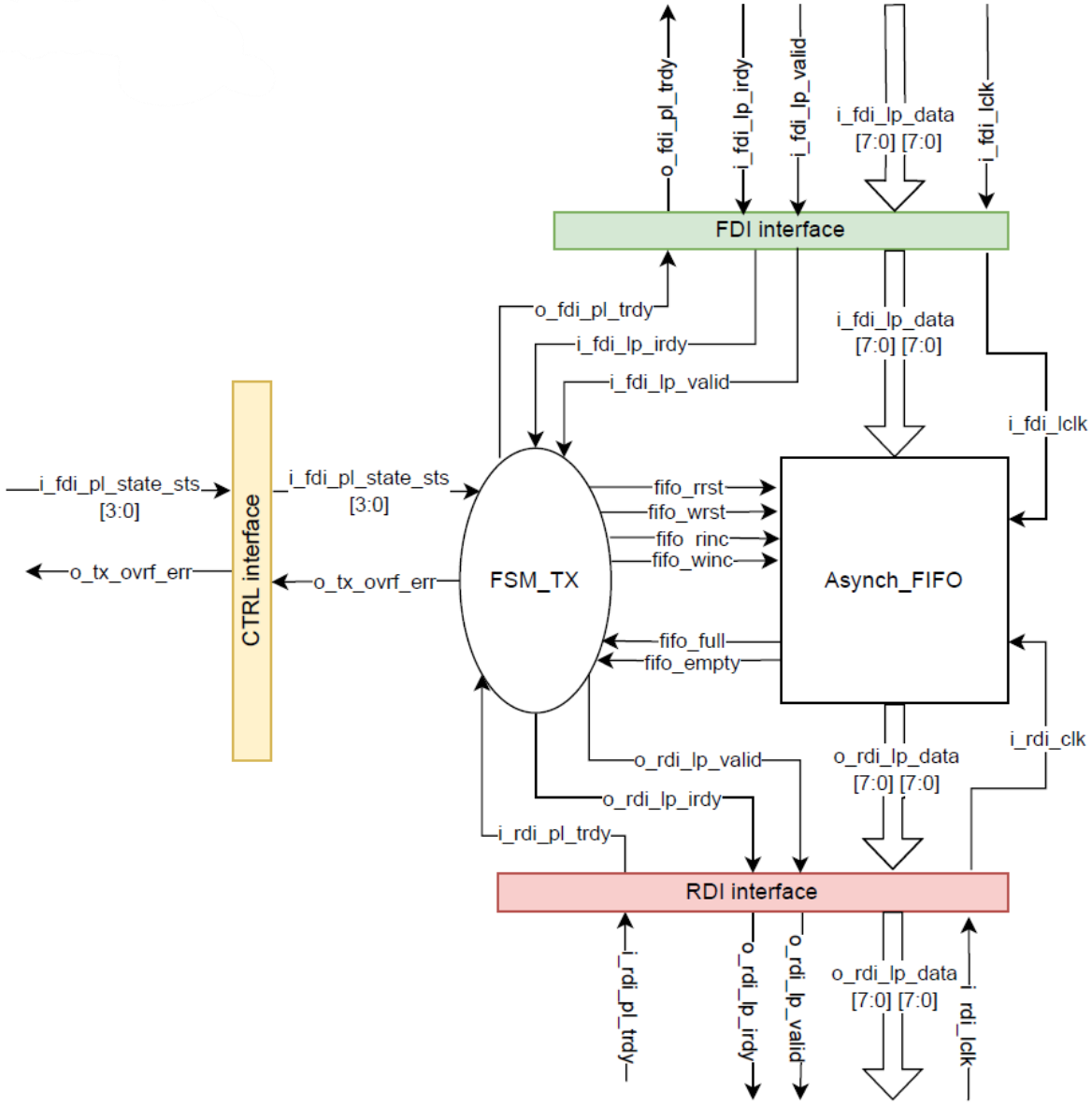
Based in the standard case for data transfer from Protocol layer over the Adaptor layer data is transferred when lp_irdy, pl_trdy, lp_valid are all asserted. Thus a FIFO signal to increment FIFO write address is sent to the FIFO block and the data transfer starts. It is also considered to have bubbles also during the flit transfer as a back pressure response for the Adaptor TX pl_trdy signal de-assertion.



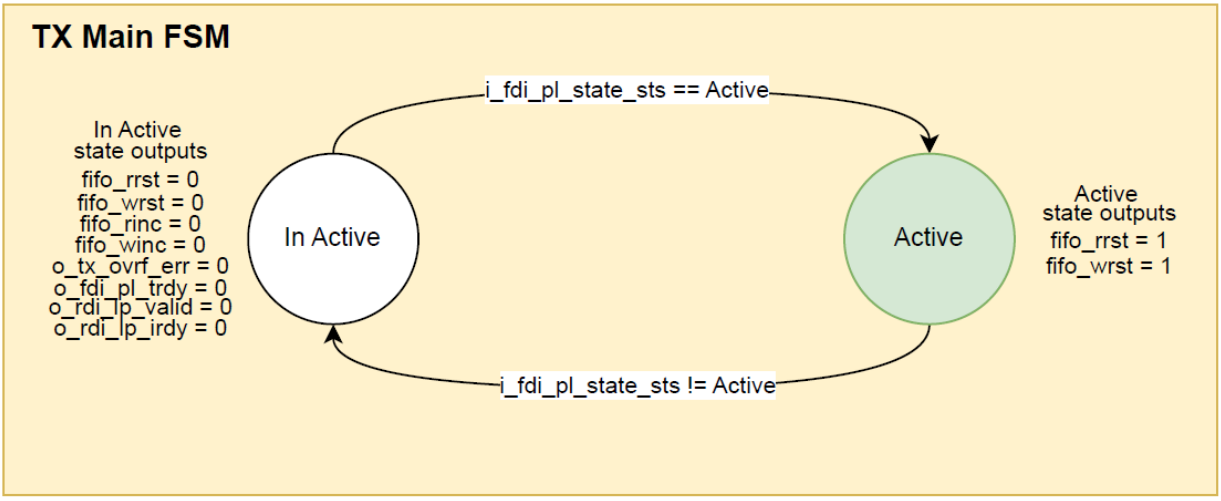
Top Level Architecture

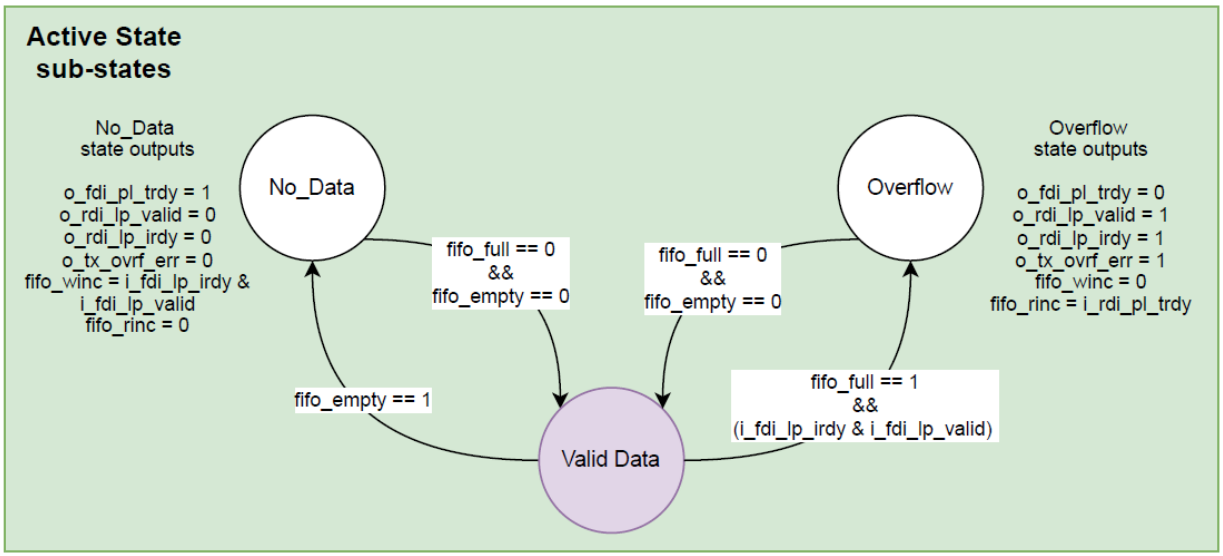


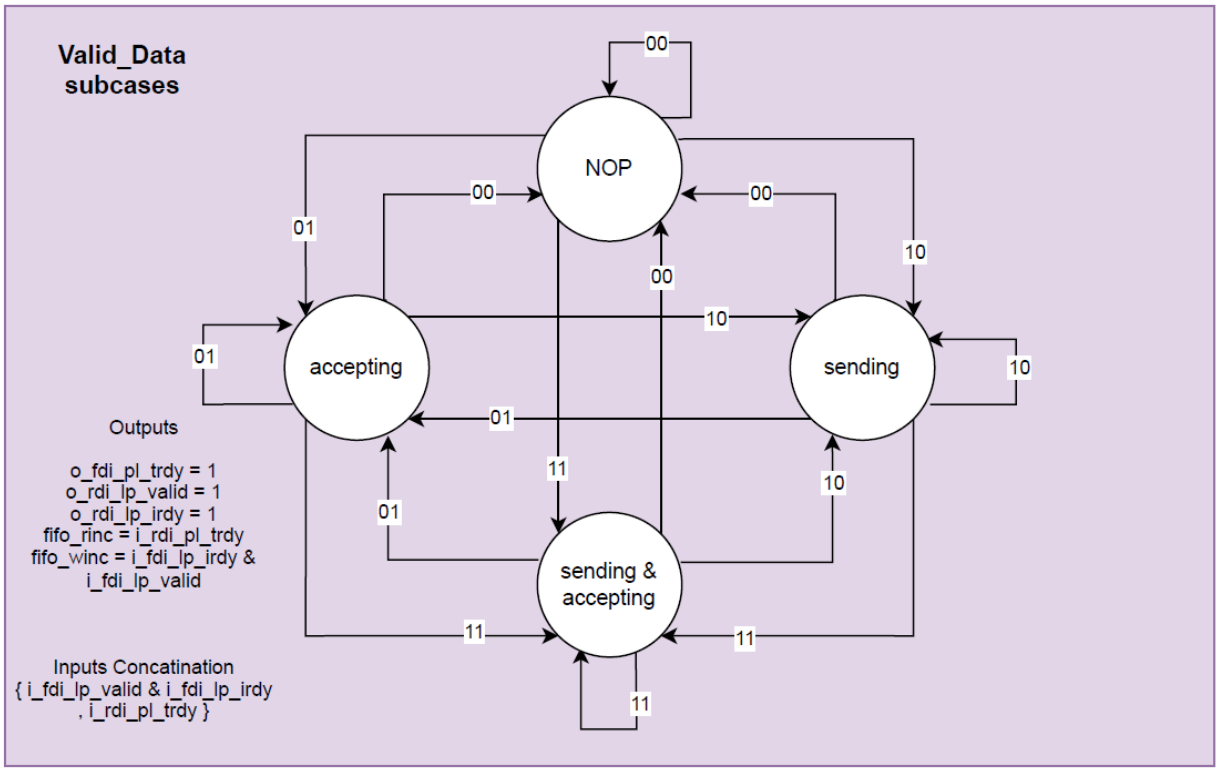
Level-1 Architecture



TX Finite State Machines






Valid_Data
subcases
NOP
accepting
sending
sending &
accepting
00
01
10
11
Outputs
o_fdi_pl_trdy = 1
o_rdi_lp_valid = 1
o_rdi_lp_irdy = 1
fifo_rinc = i_rdi_pl_trdy
fifo_winc = i_fdi_lp_irdy &
i_fdi_lp_valid
Inputs Concatination
{ i_fdi_lp_valid & i_fdi_lp_irdy
, i_rdi_pl_trdy }