Ainshams university

UCIe_PHY_RX Team

Si-Vision Graduation Project

Phy model

1-FSM Controller: the role of this module is to manage the Finite State Machine (FSM) that controls the UCIE link training and associated control states , Error handling with adapter and Sideband messages with two PHY Dies

2- Data transfer: to handle when Adapter is sending data to the Physical Layer and vice versa

3- Sideband interface: is to transfer the sideband messages between two adapter Dies

UCIE_ctl_fsm_control Signal Table

Name	Width/value	Type	Functionality
COUNTER_TIME_OUT	3	Parameter	Timeout value for training/retraining operations.
i_clk	1	Input	Clock signal for the FSM.
i_rst_n	1	Input	Global reset
i_rdi_lp_state_req	4	Input	State request signal from the adapter interface.
i_rdi_lp_linkerror	1	Input	Indicates a link error from the adapter interface.
i_sb_msg_in	4	Input	Sideband message input from the second DUT.
i_start_ucie_link_training	1	Input	Signal to initiate UCIE link training.
i_phy_req_trainerror	1	Input	Indicates a training error from the PHY.
i_phy_req_nferror	1	Input	Indicates a non-fatal error from the PHY.
i_phy_req_cerror	1	Input	Indicates a critical error from the PHY.
i_phy_req_pl_error	1	Input	Indicates a protocol-level error from the PHY.
o_rdi_pl_state_sts	4	Output	Current state status output to the adapter.
o_rdi_pl_error	1	Output	Protocol-level error status output.
o_rdi_pl_cerror	1	Output	Critical error status output.
o_rdi_pl_nferror	1	Output	Non-fatal error status output.
o_rdi_pl_trainerror	1	Output	Training error status output.
o_rdi_pl_phyinrecenter	1	Output	Indicates PHY in re-center mode.
o_rdi_pl_speedmode	3	Output	Speed mode output configuration to the adapter.
o_rdi_pl_lnk_cfg	3	Output	Link configuration output to the adapter.

o_rdi_pl_inband_pres	1	Output	Indicates in-band presence detection.
o_sb_msg_out	4	Output	Sideband message output to the second DUT.
r_current_state	4	Internal	Current state of the FSM.
w_next_state	4	Internal	Next state of the FSM.
r_enable	1	Internal	Enable signal for internal operations.
r_linkreset_flag	1	Internal	Flag indicating a link reset is required.
r_linkerror_flag	1	Internal	Flag indicating a link error is detected.
r_nop_detected_flag	1	Internal	Flag for detecting NOP state.
r_nop_active_flag	1	Internal	Flag for NOP active state.
r_timeout_cntr	2	Internal	Counter for timeout handling.
r_training_cntr	2	Internal	Counter for training operations.

UCIE_ctl_phy_data_transfer Table

Parameters

Parameter Name	Width	Description
NBYTES	Integer	Number of data bytes (default: 32).

Inputs

Signal Name	Width	Description
i_clk	1-bit	Clock signal.
i_rst_n	1-bit	Global reset
i_rdi_lp_irdy	1-bit	Indicates Adapter (LP) is ready.
i_rdi_lp_valid	1-bit	Valid signal from Adapter (LP).
i_rdi_lp_data	[NBYTES -1:0][7:0]	Data from Adapter (LP).
i_data_received	[NBYTES -1:0][7:0]	Data received from Second DUT.
i_data_valid	1-bit	Indicates validity of received data.
i_enable	1-bit	FSM enable control input.
i_phy_req_data_error	1-bit	Error injection signal for test bench.

Outputs

Signal Name	Width	Description
o_rdi_pl_trdy	1-bit	Indicates readiness for data transfer to Adapter (LP).
o_rdi_pl_valid	1-bit	Valid signal for Adapter (LP) output data.
o_rdi_pl_data	[NBYTES -1:0][7:0]	Data sent to Adapter (LP).
o_data_sent	[NBYTES -1:0][7:0]	Data sent to the Second DUT.
o_data_valid	1-bit	Indicates validity of data sent to Second DUT.

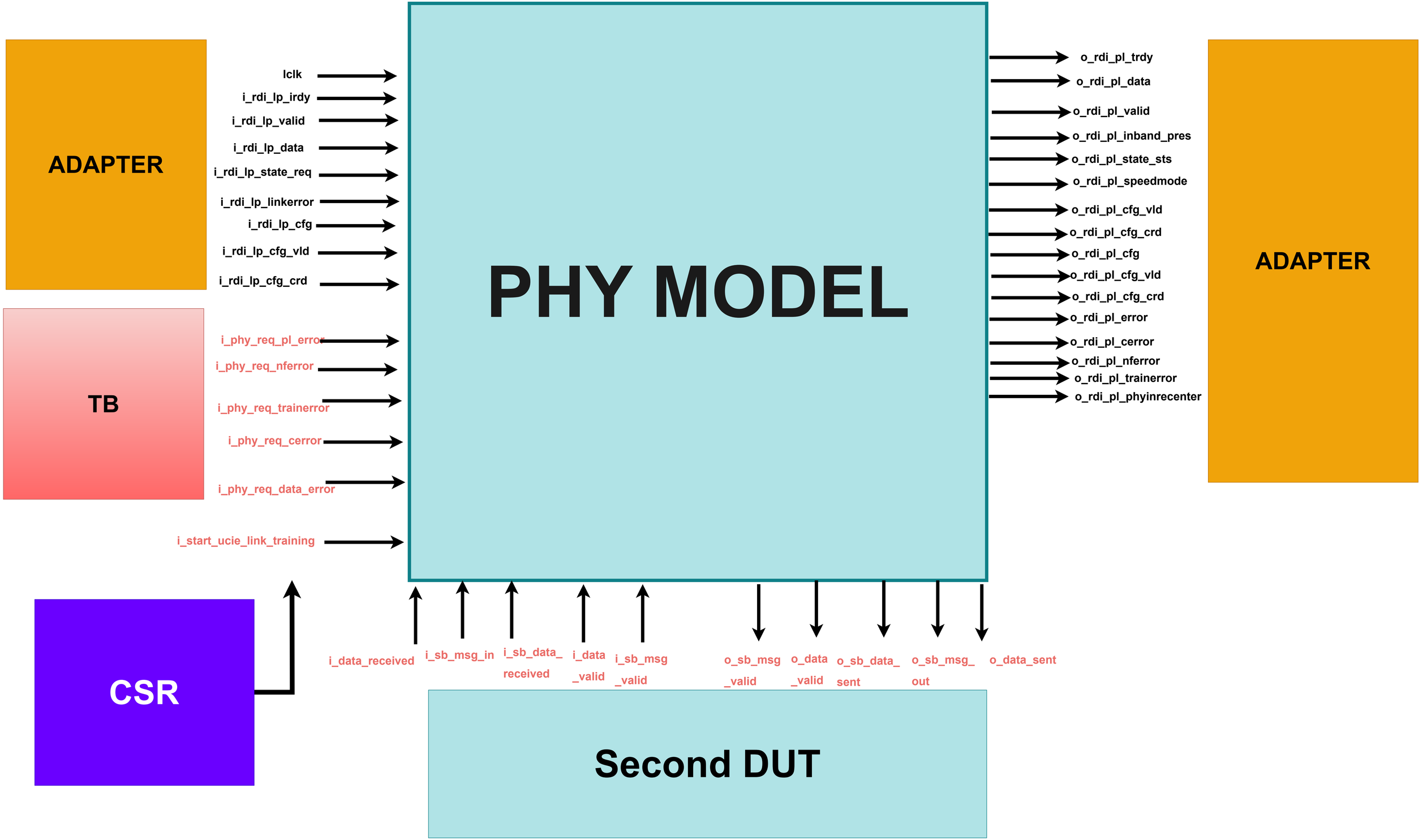
Internal Signals

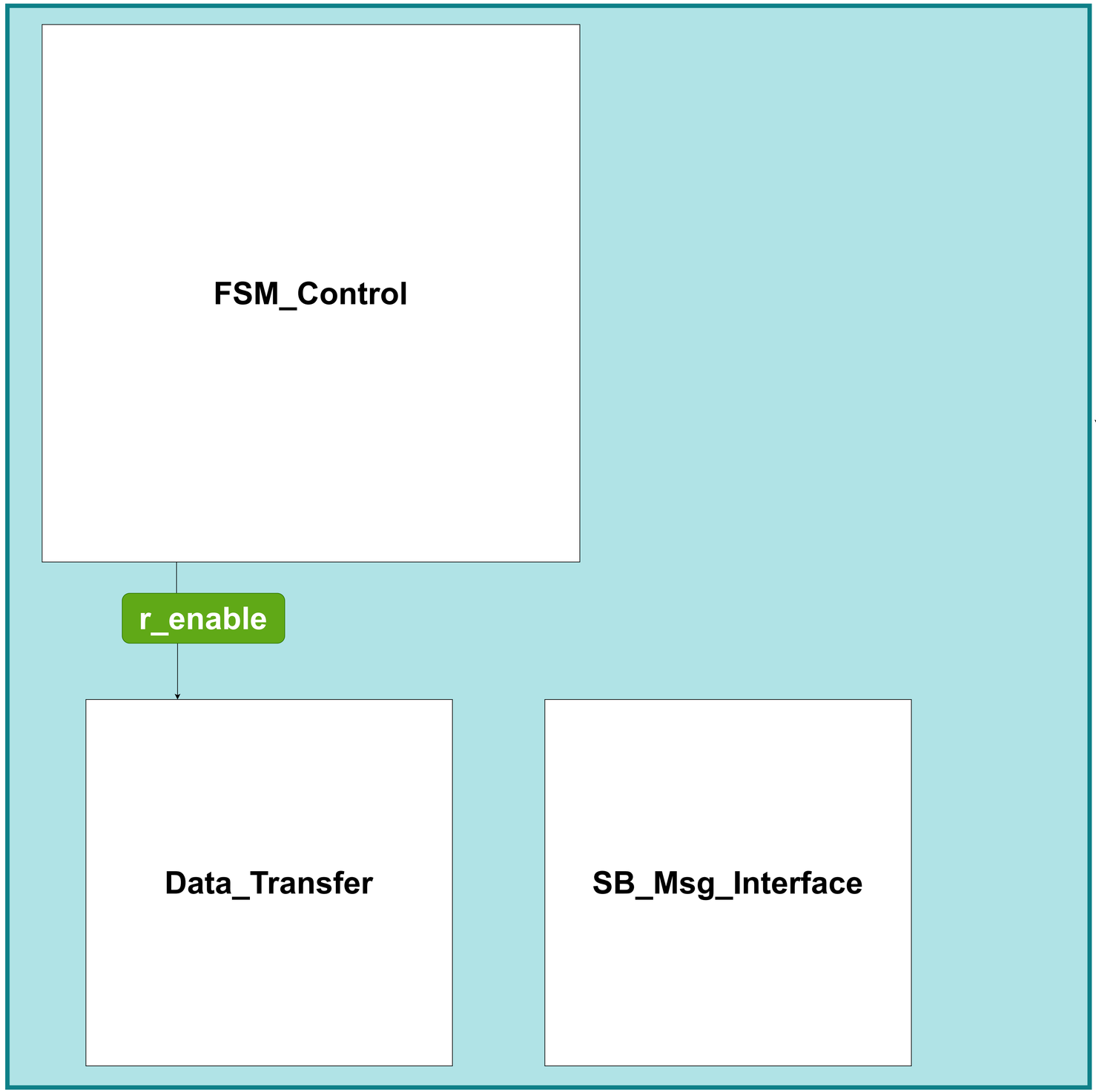
Signal Name	Width	Description
r_current_state	2-bit	Current state of the FSM.
w_next_state	2-bit	Next state of the FSM.

UCIE_ctl_phy_sb_msg_interface Table

Signal Name	Width	Type	Functionality
i_clk	1-bit	Input	Clock signal for synchronization.
i_rst_n	1-bit	Input	Active-low reset signal for initializing the system.
i_rdi_lp_cfg_crd	1-bit	Input	Credit signal for receiving data from LP adapter.
i_rdi_lp_cfg_valid	1-bit	Input	Valid signal indicating the availability of LP configuration data.
i_sb_data_valid	1-bit	Input	Valid signal indicating the availability of sideband data.
i_data_received_sb	NC bits	Input	Sideband data received from PHY.
i_rdi_lp_cfg	NC bits	Input	Configuration data received from LP adapter.
o_rdi_pl_cfg_crd	1-bit	Output	Credit signal indicating availability to send data to LP adapter.
o_rdi_pl_cfg_vld	1-bit	Output	Valid signal indicating the validity of configuration data to LP adapter.

o_sb_data_valid	1-bit	Output	Valid signal indicating the availability of sideband data for PHY.
o_rdi_pl_cfg	NC bits	Output	Configuration data sent to LP adapter.
o_data_sent_sb	NC bits	Output	Sideband data sent to PHY.
r_current_state	2 bits	Internal	Current state of the state machine.
w_next_state	2 bits	Internal	Next state of the state machine based on current conditions.
r_internal_counter	1-bit	Internal	Counter indicating PHY credit availability.
r_data_received_sb	NC bits	Internal	Latches the sideband data received from PHY.
r_rdi_lp_cfg	NC bits	Internal	Latches the configuration data received from LP adapter.


ADAPTER
TB
CSR
PHY MODEL
Second DUT
ADAPTER
lclk
i_rdi_lp_irdy
i_rdi_lp_valid
i_rdi_lp_data
i_rdi_lp_state_req
i_rdi_lp_linkerror
i_rdi_lp_cfg
i_rdi_lp_cfg_vld
i_rdi_lp_cfg_crd
i_phy_req_pl_error
i_phy_req_nferror
i_phy_req_trainerror
i_phy_req_cerror
i_phy_req_data_error
i_start_ucie_link_training
o_rdi_pl_trdy
o_rdi_pl_data
o_rdi_pl_valid
o_rdi_pl_inband_pres
o_rdi_pl_state_sts
o_rdi_pl_speedmode
o_rdi_pl_cfg_vld
o_rdi_pl_cfg_crd
o_rdi_pl_cfg
o_rdi_pl_cfg_vld
o_rdi_pl_cfg_crd
o_rdi_pl_error
o_rdi_pl_cerror
o_rdi_pl_nferror
o_rdi_pl_trainerror
o_rdi_pl_phyinrecenter
i_data_received
i_sb_msg_in
i_sb_data_received
i_data_valid
i_sb_msg_valid
o_sb_msg_valid
o_data_valid
o_sb_data_sent
o_sb_msg_out
o_data_sent


FSM_Control
r_enable
Data_Transfer
SB_Msg_Interface

input output internal wire

Global reset

o_pl_state_sts == Reset

Reset

i_start_ucie_link_training

o_rdi_pl_phyinrecenter

Link_Training

Text

r_training_cntr =done

o_rdi_pl_inband_pres transition 0 > \

Wait_For_Adapter

i_SB msg_in == ACT_REQ

i_rdi_lp_state_req == Active

o_SB_msg_out == ACT_REQ

REQ_Active

i_SB msg_in == ACT_RSP

o_rdi_pl_status_sts == Active

r_enable== 1'b1

Active

RSP_Active

i_rdi_lp_state_req == Active

o_SB_msg_out == ACT_RSP

RDI bring up flow

Retrain_TX

i_SB_msg_in == Rtn_RSP

o_rdi_pl_state_sts = Retrain

Retrain

i_pl_error_retrain

o_rdi_pl_phyinrecenter

o_rdi_pl_error

i_SB_msg_in == Active_REQ

i_lp_status_req == Retrain

o_SB_msg_out == Rtn_REQ

i_SB_msg_in == Rtn_REQ

o_rdi_pl_state_sts = Retrain

o_rdi_pl_phyinrecenter

Retrain_RX

Active

i_rdi_lp_status_req == NOP -> Active

o_SB_msg_out == Active_REQ

i_rdi_lp_status_req == NOP -> Active

o_SB_msg_out == Active_REQ

o_SB_msg_out == Active_RSP

i_SB_msg_in == Active_RSP

o_rdi_pl_state_sts = Active

NOP

Retrain

Link Reset

Link_Training

i_start_ucie_link_training

o_rdi_pl_phyinrecenter

if (r_linkreset_flag== 1'b0)

Reset

i_rdi_lp_state_req == NOP -> Active | | Start UCIe Link training

if (r_linkreset_flag== 1'b1)

o_rdi_pl_phyinrecenter

if (r_linkreset_flag== 1'b0 && r_timeout_cntr == done)

o_pl_state_sts == Reset

r_training_cntr =done

o_rdi_pl_inband_pres transition 0 > \

i_rdi_lp_state_req == Active

if (r_linkreset_flag== 1'b1)

o_pl_state_sts == Reset

Wait_For_Adapter

i_SB msg_in == ACT_REQ

r_linkreset_flag== 1'b1

o_rdi_pl_status_sts == Active

Lnk_rst_TX

i_rdi_lp_state_req == LinkReset

o_SB_msg_out == LNKRST_REQ

r_linkereset_flag== 1'b1

o_SB_msg_out == LNKRST_RSP

o_pl_state_sts == LinkReset

Any state

Active/Retrain /Reset

Link Reset

I_SB_msg_out == LNKRST_REQ

o_pl_state_sts == LinkReset

o_SB_msg_out == LNKRST_RSP

Link_Training

o_rdi_pl_phyinrecenter

i_start_ucie_link_training

if (r_linkerror_flag== 1'b0)

Reset

i_rdi_lp_state_req == NOP -> Active | | Start UCIe Link training

if (r_linkerror_flag== 1'b1)

o_rdi_pl_phyinrecenter

r_training_cntr =done

o_rdi_pl_inband_pres transition 0 > \

i_rdi_lp_state_req == Active

r_linkerror_flag== 1'b1

o_pl_state_sts == Reset

if (r_linkrerror_flag== 1'b0 && r_timeout_cntr == done)

o_pl_state_sts == Reset

Wait_For_Adapter

Lnk_err_TX

i_SB msg_in == ACT_REQ

if (r_linkerror_flag== 1'b1)

o_rdi_pl_status_sts == Active

i_phy_req_train_error

i_rdi_lp_linkerror

o_SB_msg_out == LNKERR_REQ

r_linkerror_flag== 1'b1

I_SB_msg_out == LNKERR_RSP

o_pl_state_sts == LinkError

Any state

Link Error

i_SB_msg_in == LNKERR_REQ

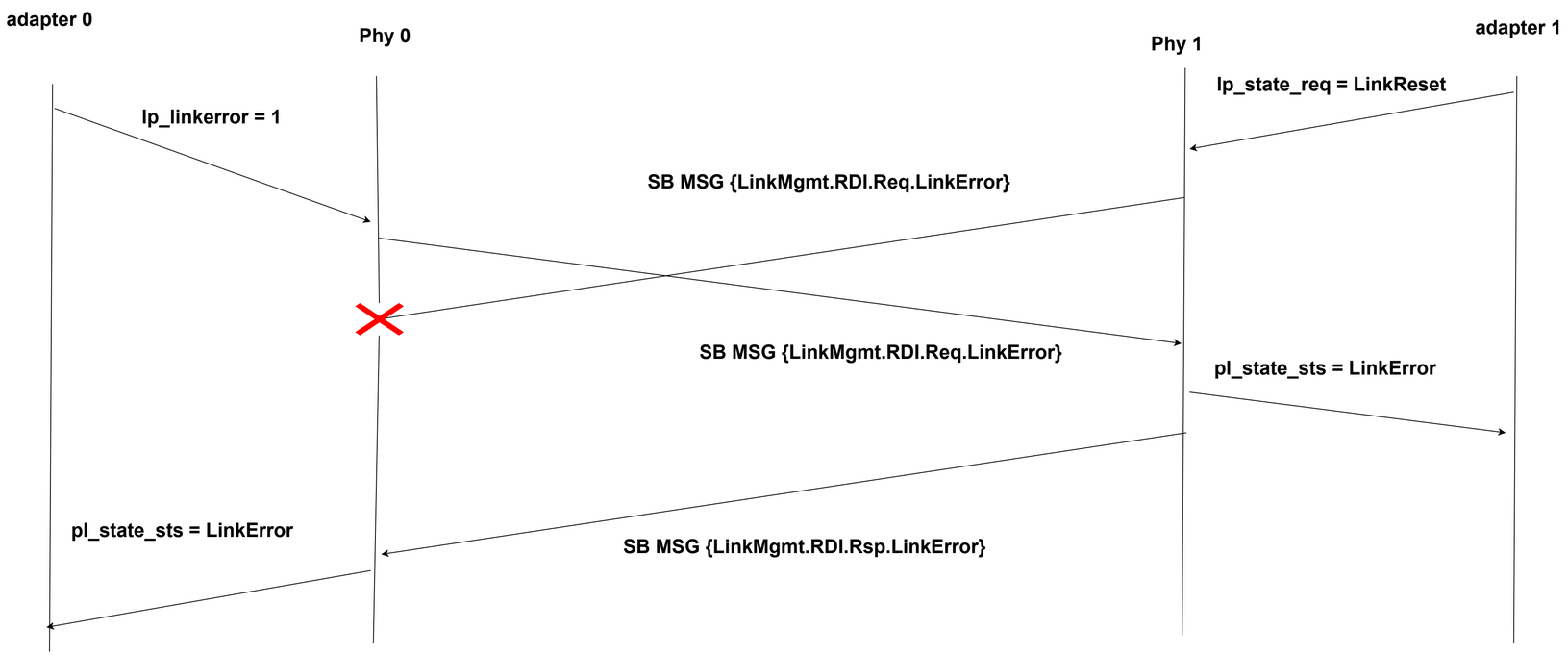
o_pl_state_sts == LinkError

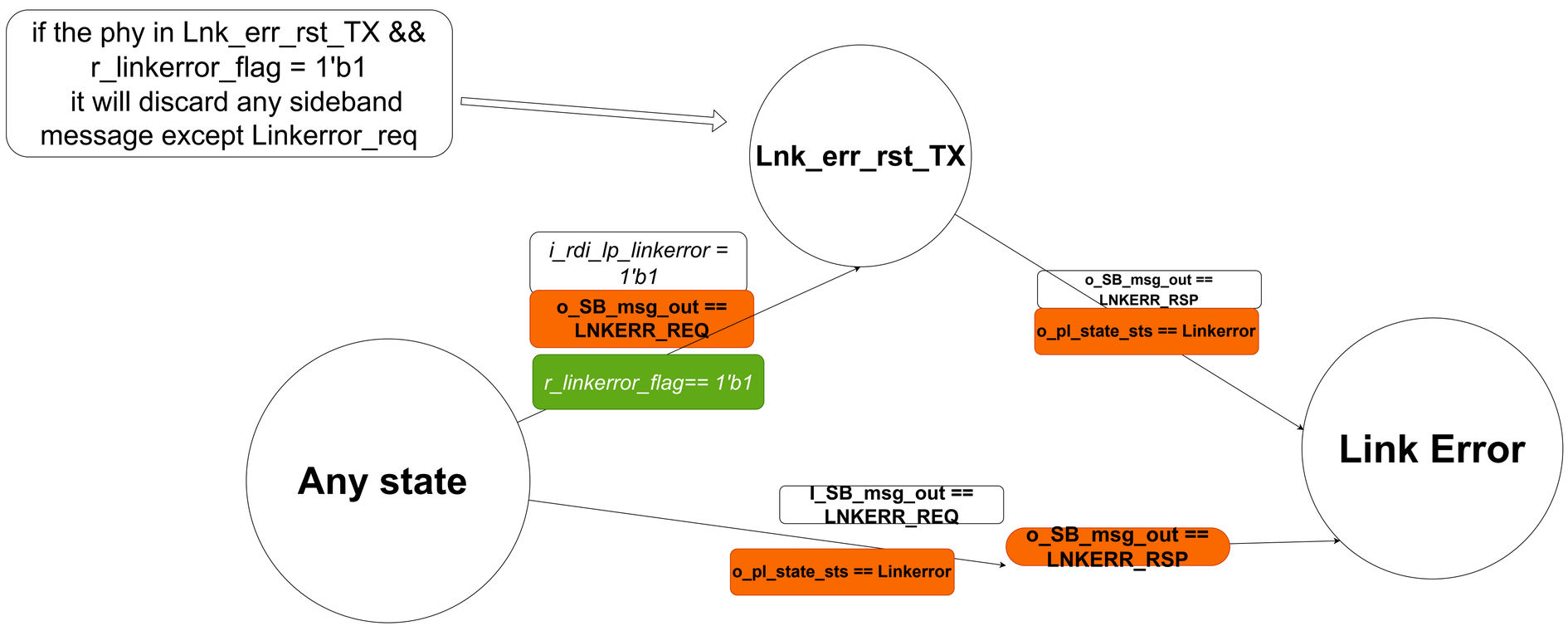
o_SB_msg_out == LNKERR_RSP

Link Error

Corner Case 1

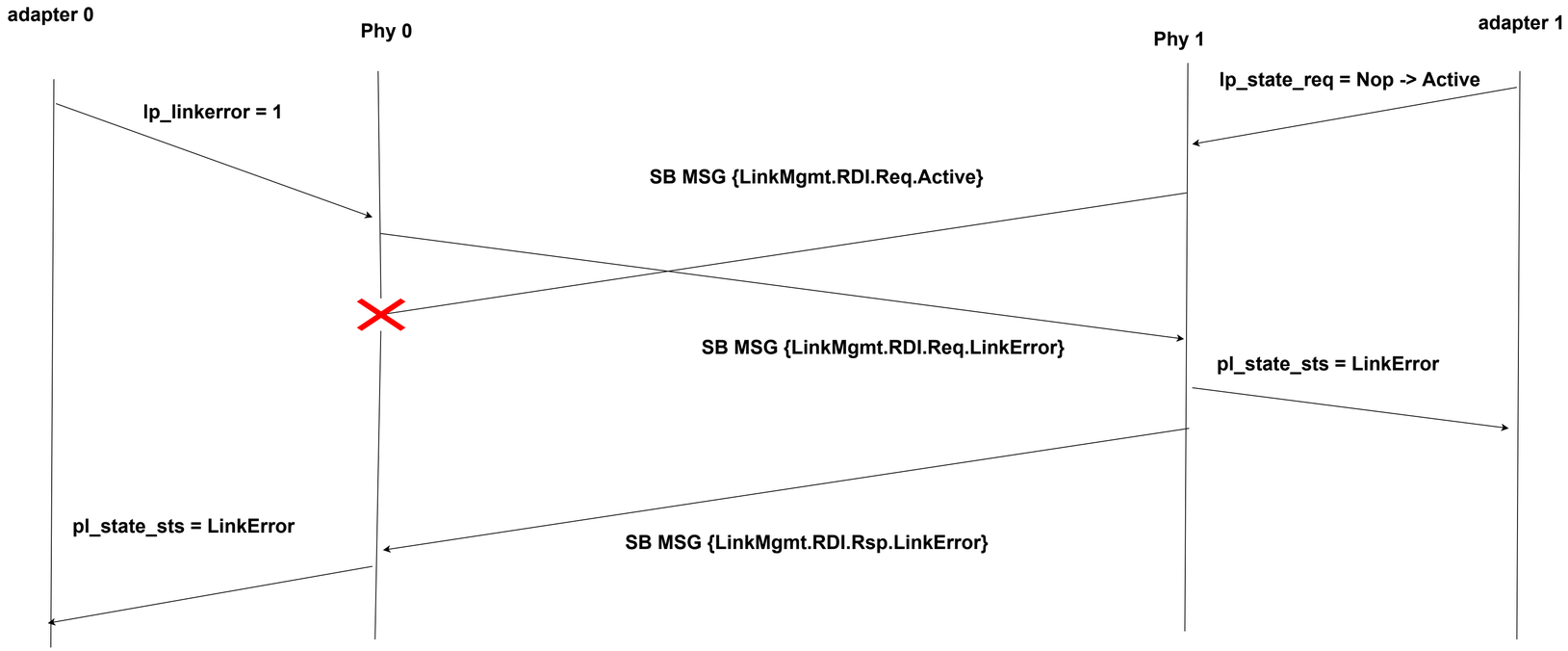
Link Error has Prioirty than Link reset

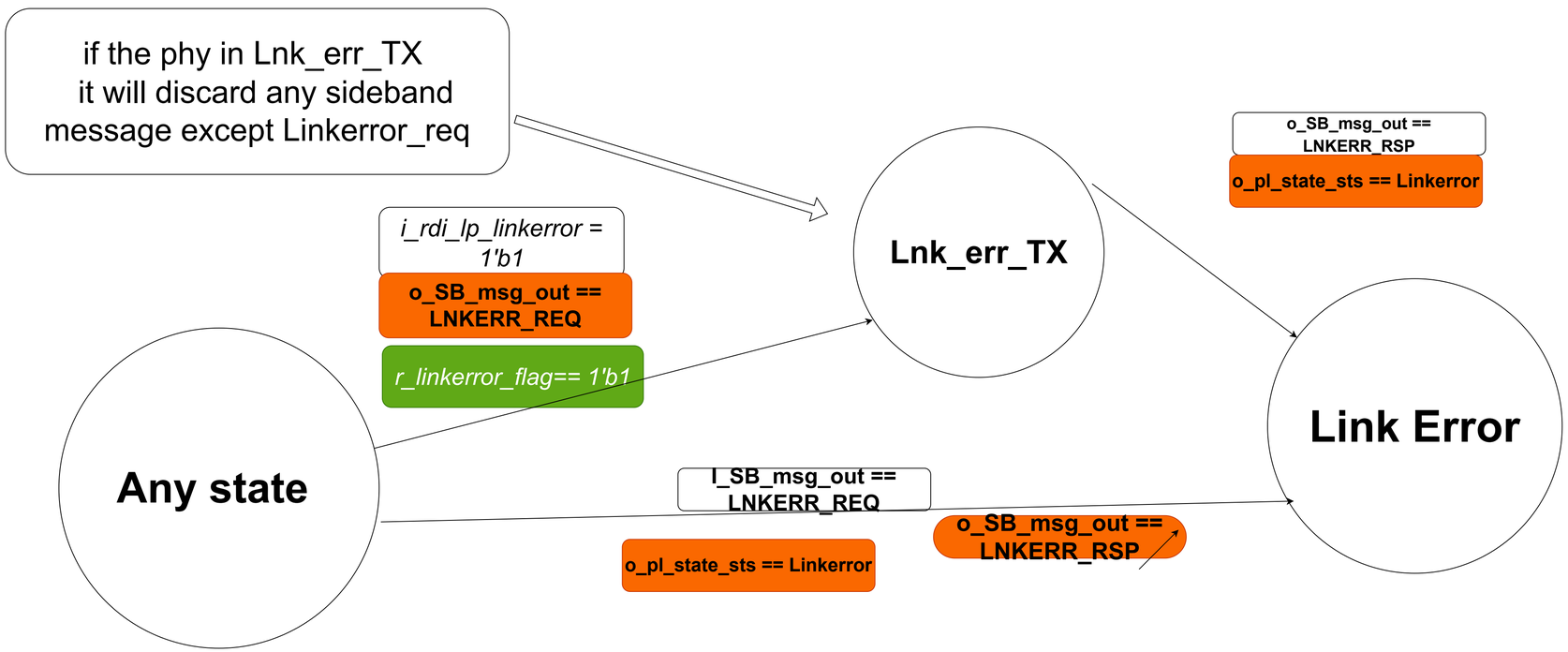




Corner Case 2

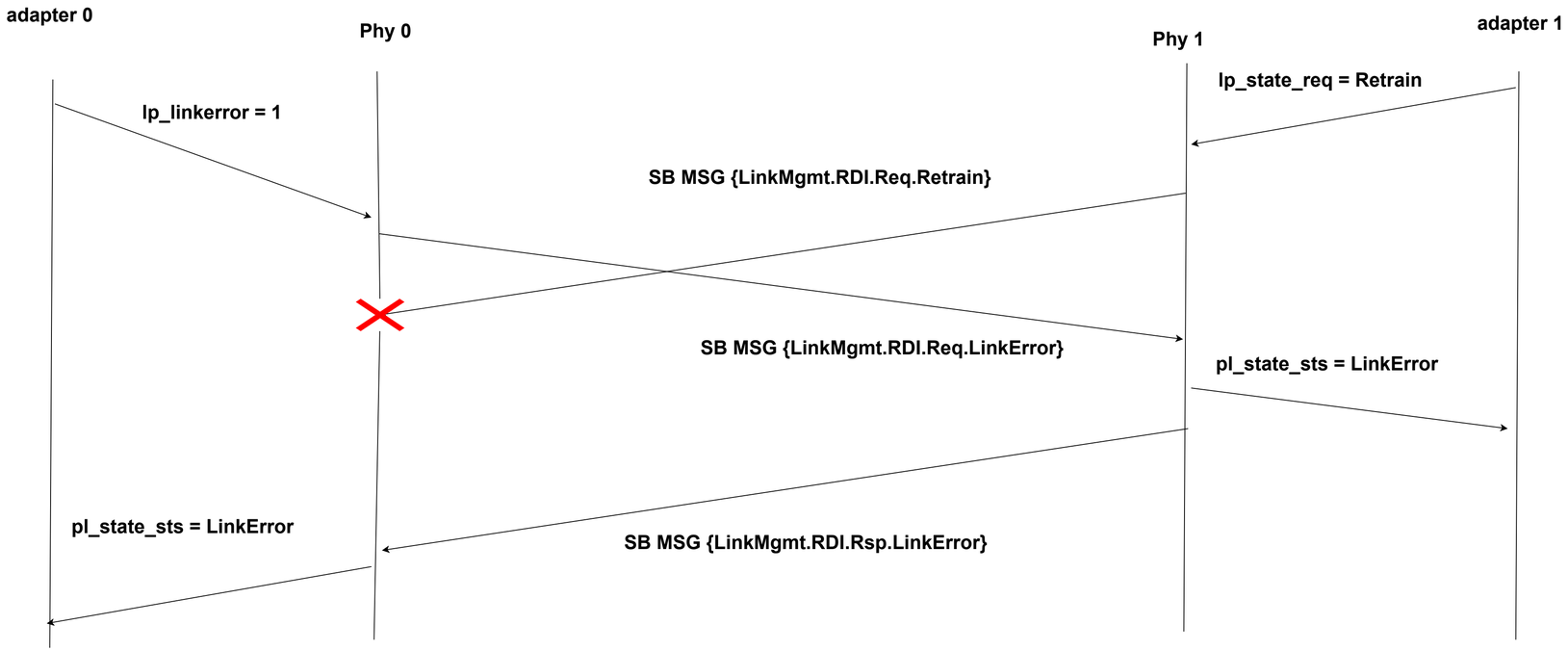
Link Error has Prioirty than Active

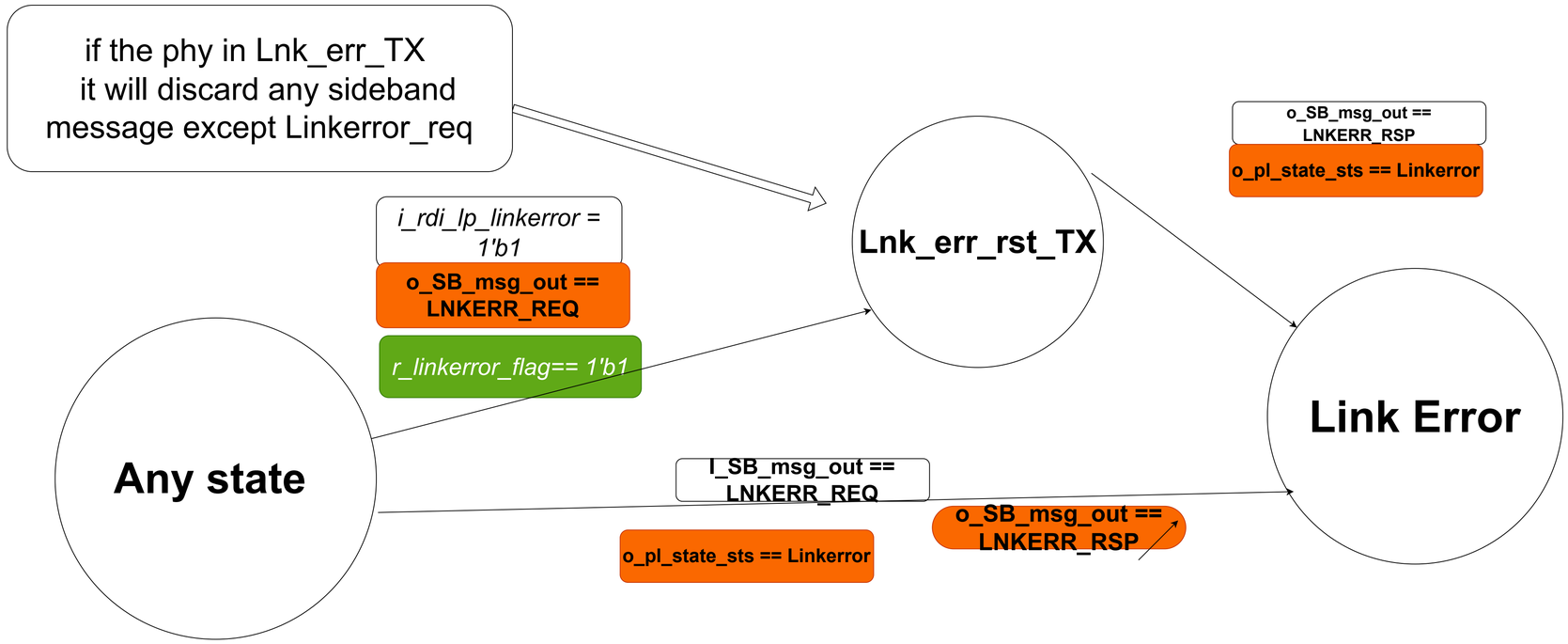




Corner Case 3

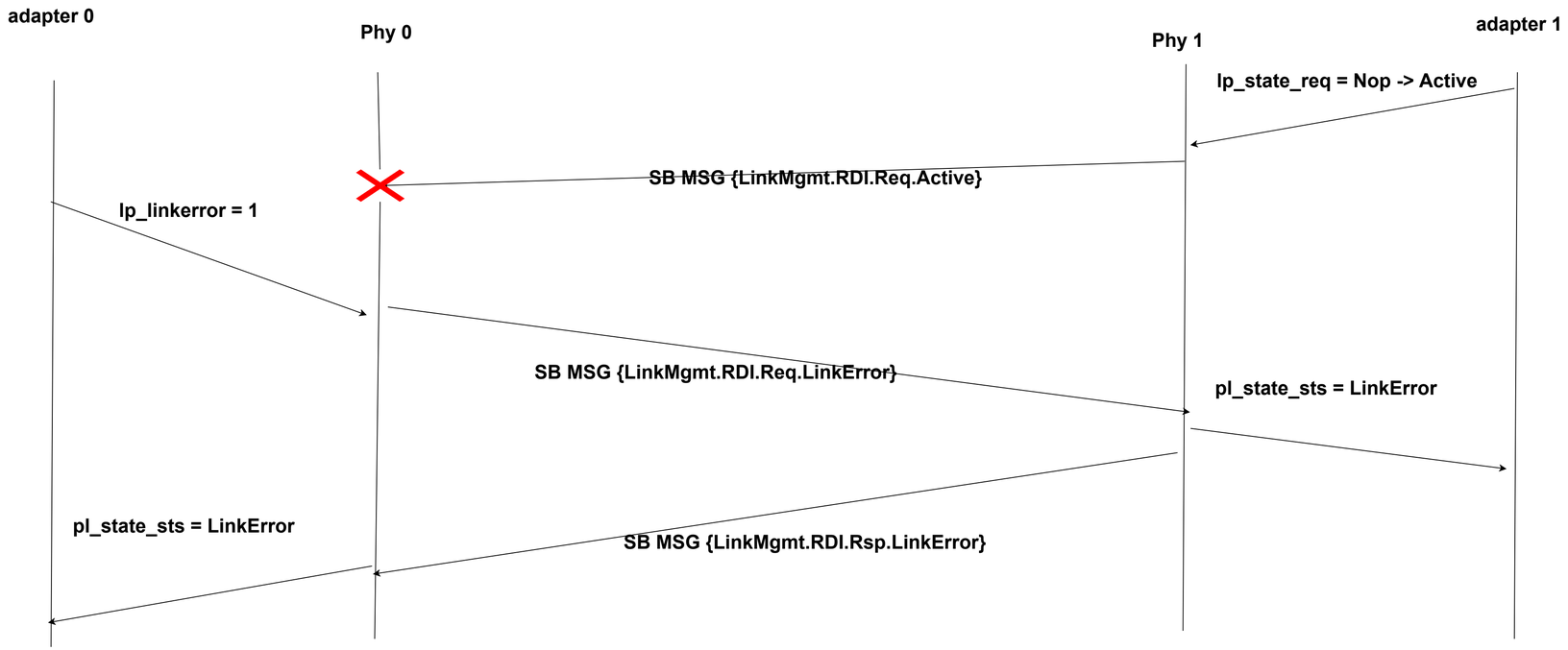
Link Error has Prioirty than Retrain

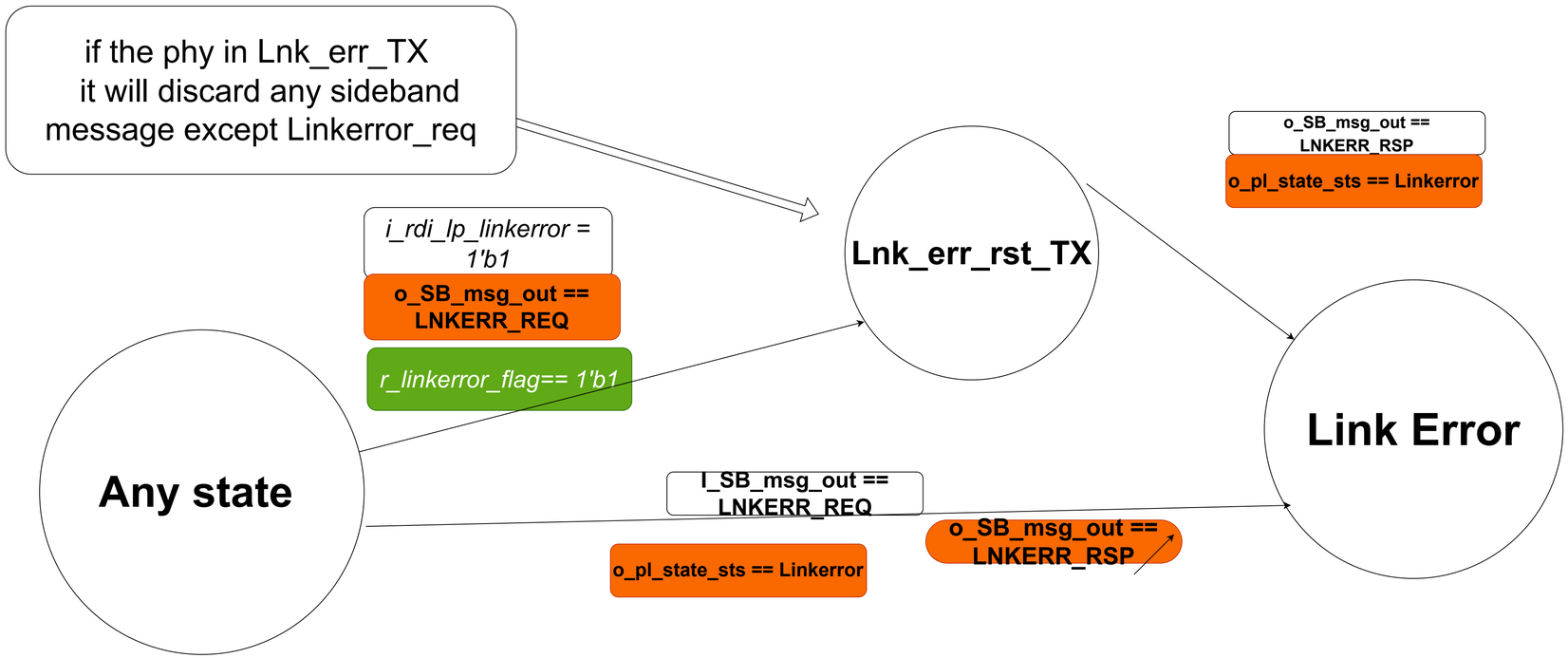




Corner Case 4

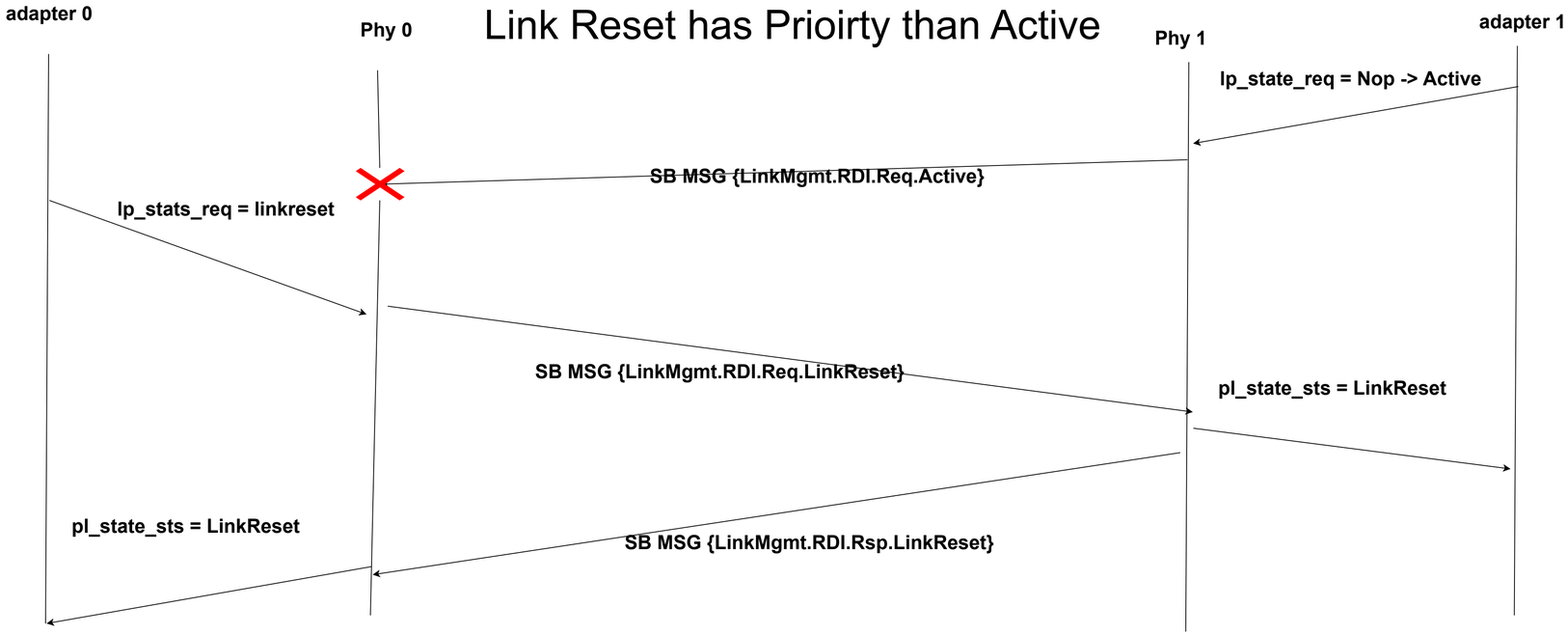
Link Error has Prioirty than Retrain

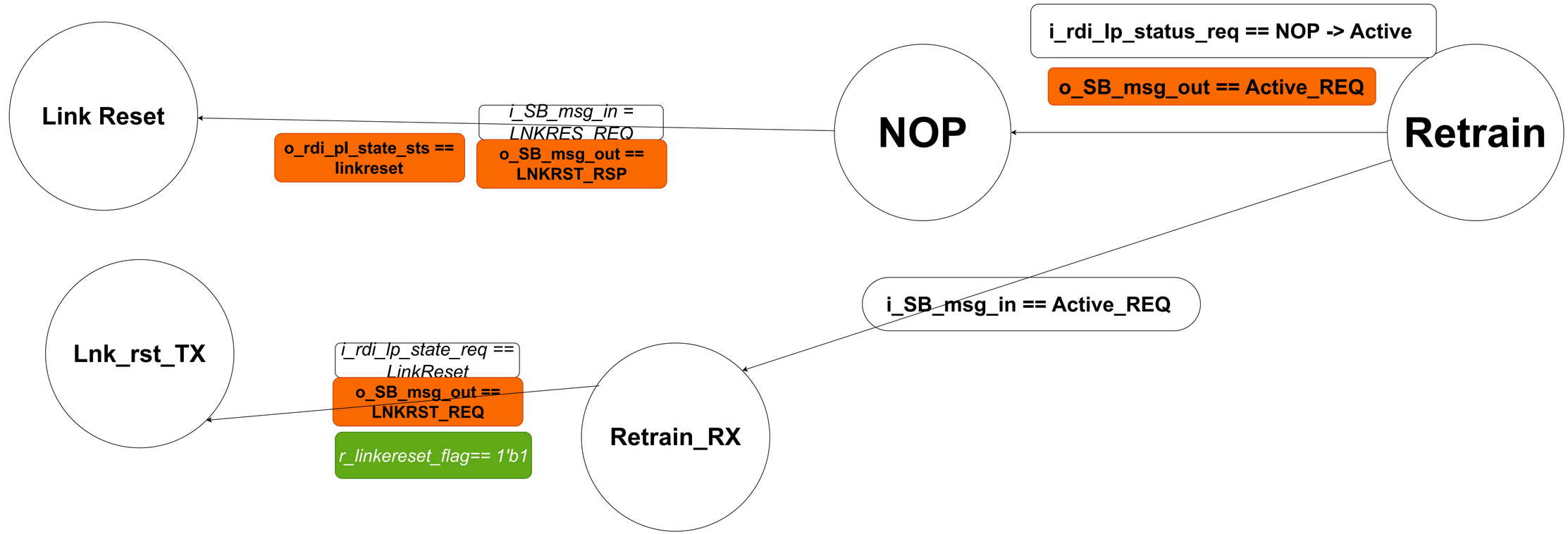


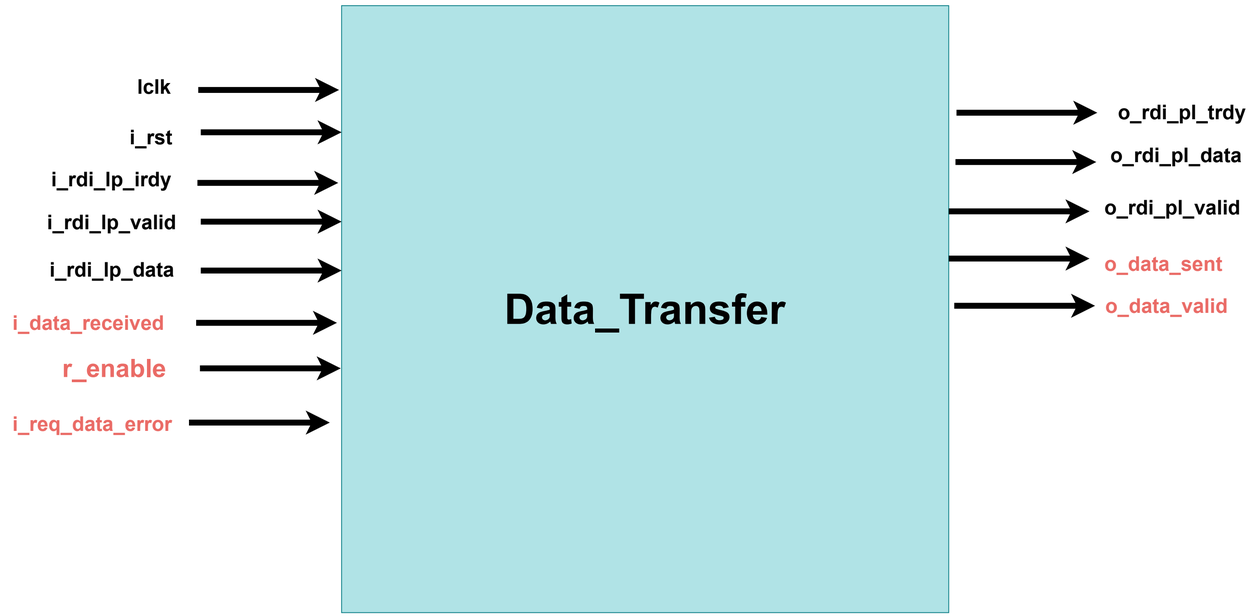


Corner Case 5

Link Reset has Prioirty than Active

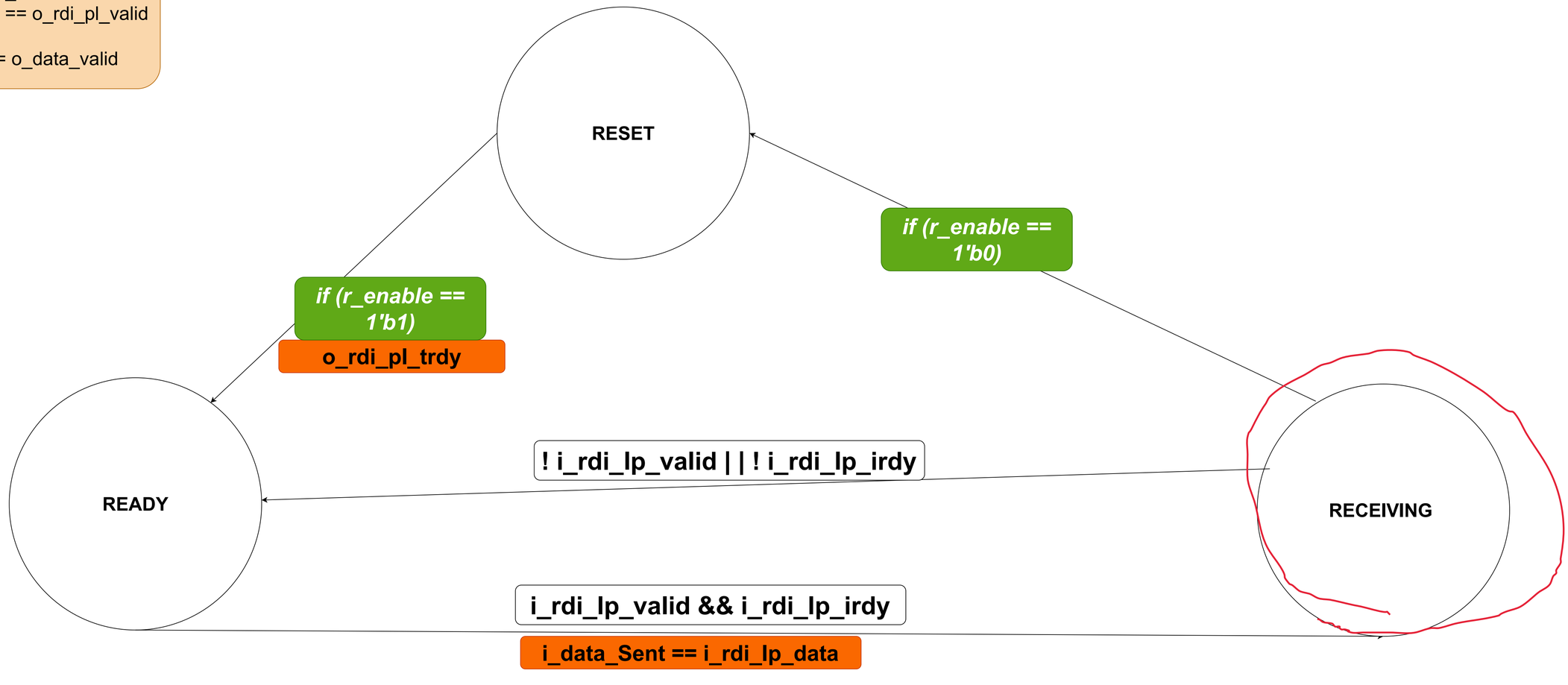


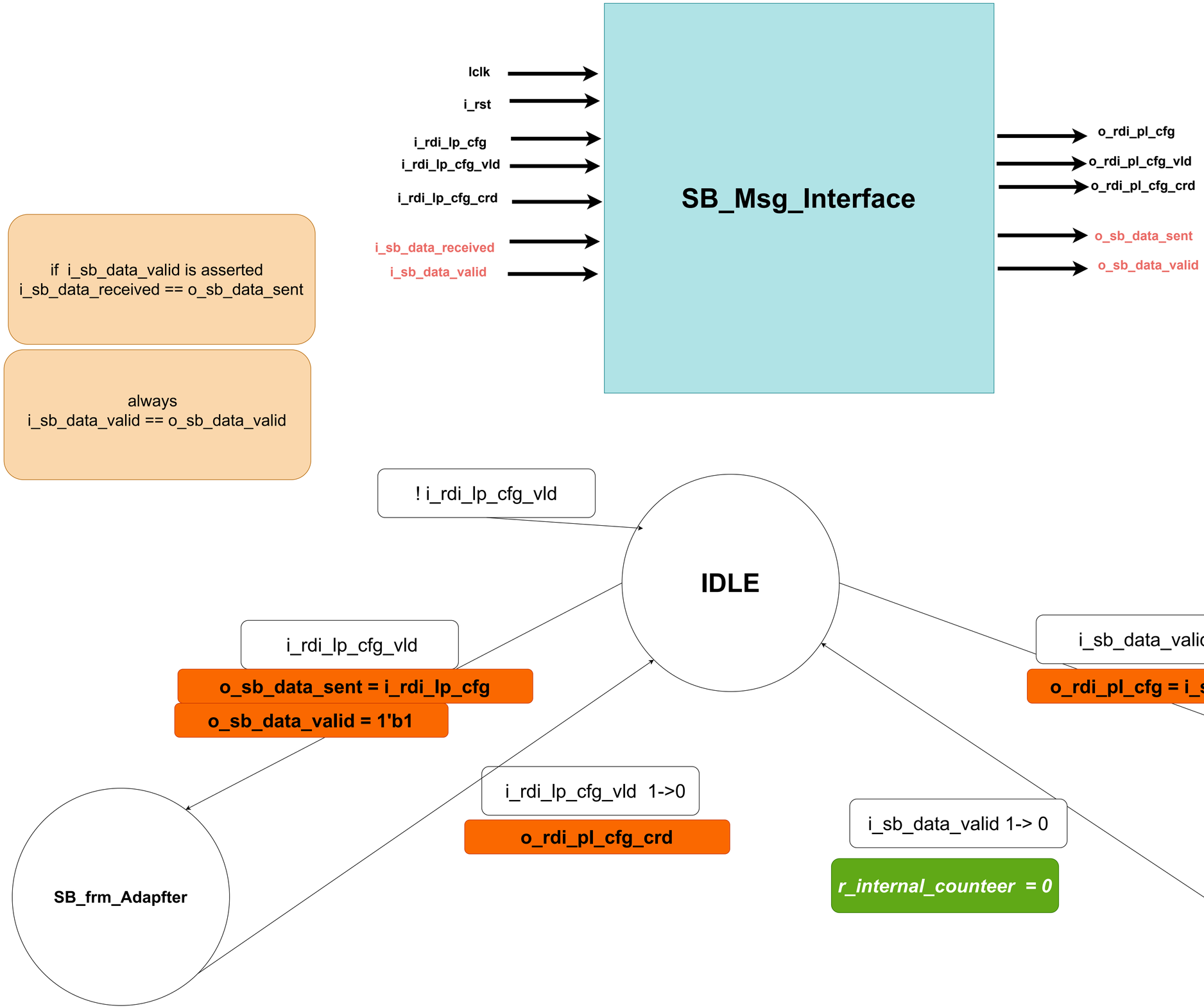




if r_enable is asserted and whenever o_rdi_pl_valid is asserted i_data_Received == o_rdi_pl_valid

i_data_valid = o_data_valid




lclk
i_rst
i_rdi_lp_cfg
i_rdi_lp_cfg_vld
i_rdi_lp_cfg_crd
i_sb_data_received
i_sb_data_valid
SB_Msg_Interface
o_rdi_pl_cfg
o_rdi_pl_cfg_vld
o_rdi_pl_cfg_crd
o_sb_data_sent
o_sb_data_valid
if i_sb_data_valid is asserted
i_sb_data_received == o_sb_data_sent
always
i_sb_data_valid == o_sb_data_valid
! i_rdi_lp_cfg_vld
IDLE
i_rdi_lp_cfg_vld
o_sb_data_sent = i_rdi_lp_cfg
o_sb_data_valid = 1'b1
i_sb_data_valid
o_rdi_pl_cfg = i_sb_data_recevied
SB_frm_Adapfter
i_rdi_lp_cfg_vld 1->0
o_rdi_pl_cfg_crd
i_sb_data_valid 1-> 0
r_internal_counteer = 0
SB_frm_PHY