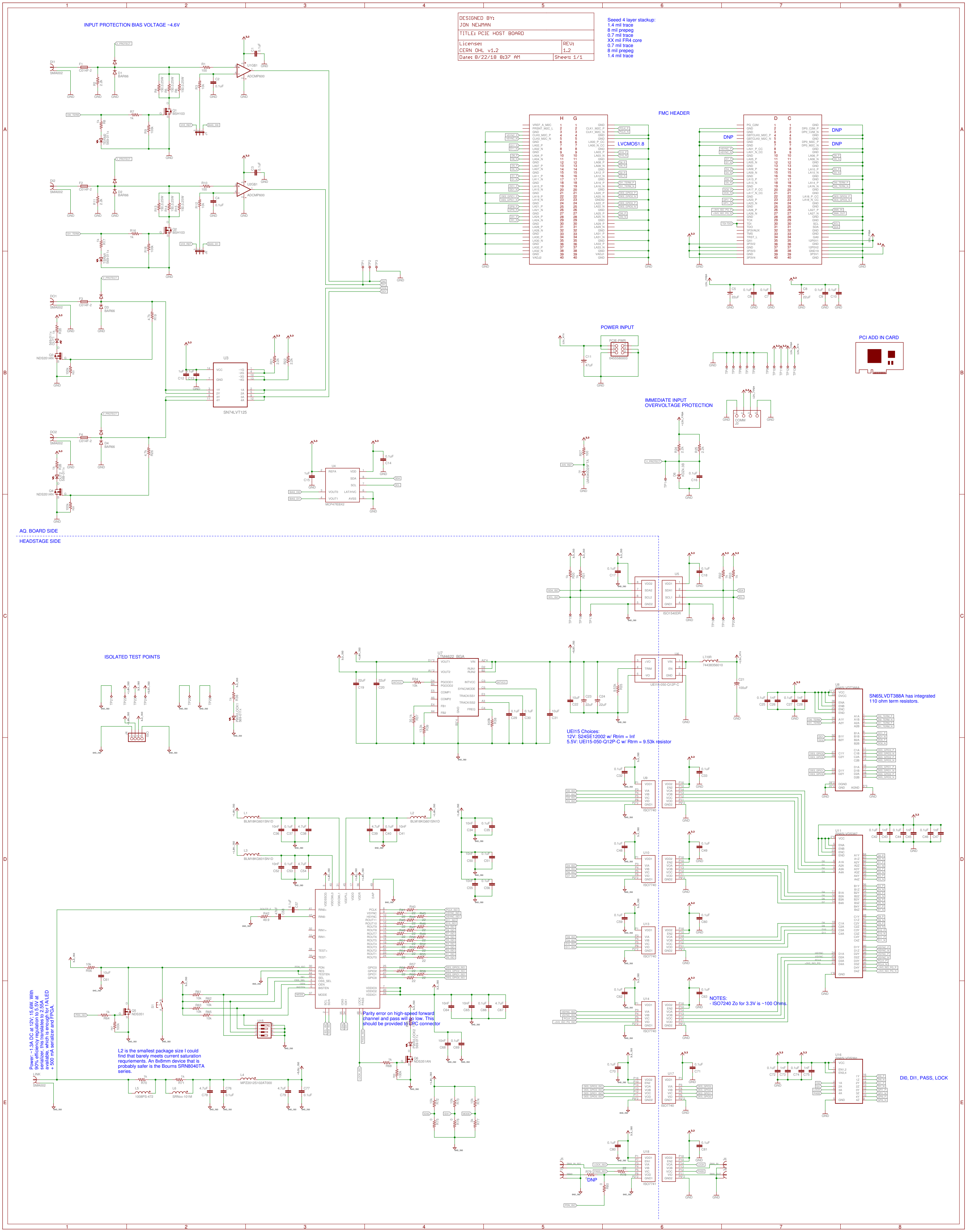

DESIGNED BY:
JON NEWMAN
TITLE: PCIE HOST BOARD
License:
CERN OHL v1.2
REV:
1.2
Date: 8/22/18 8:37 AM
Sheet: 1/1
Seeed 4 layer stackup:
1.4 mil trace
8 mil prepeg
0.7 mil trace
XX mil FR4 core
0.7 mil trace
8 mil prepeg
1.4 mil trace
INPUT PROTECTION BIAS VOLTAGE ~4.6V
FMC HEADER
LVCMOS1.8
DNP
POWER INPUT
PCI ADD IN CARD
IMMEDIATE INPUT OVERVOLTAGE PROTECTION
AQ. BOARD SIDE
HEADSTAGE SIDE
ISOLATED TEST POINTS
UEI15 Choices:
12V: S24SE12002 w/ Rtrim = Inf
5.5V: UEI15-050-Q12P-C w/ Rtrim = 9.53k resistor
SN65LVDT388A has integrated 110 ohm term resistors.
NOTES:
- ISO7240 Zo for 3.3V is ~100 Ohms.
DI0, DI1, PASS, LOCK
Parity error on high-speed forward channel and pass will go low. This should be provided to SPC connector
Power: ~1.3A DC at 12V; 15.6W. With 90% efficiency regulation to 5.5V at serializer, this translates to 2.55A available, which is enough for 1A/LED + 500 mA serializer and FPGA.
L2 is the smallest package size I could find that barely meets current saturation requriements. An 8x8mm device that is probably safer is the Bourns SRN8040TA series.