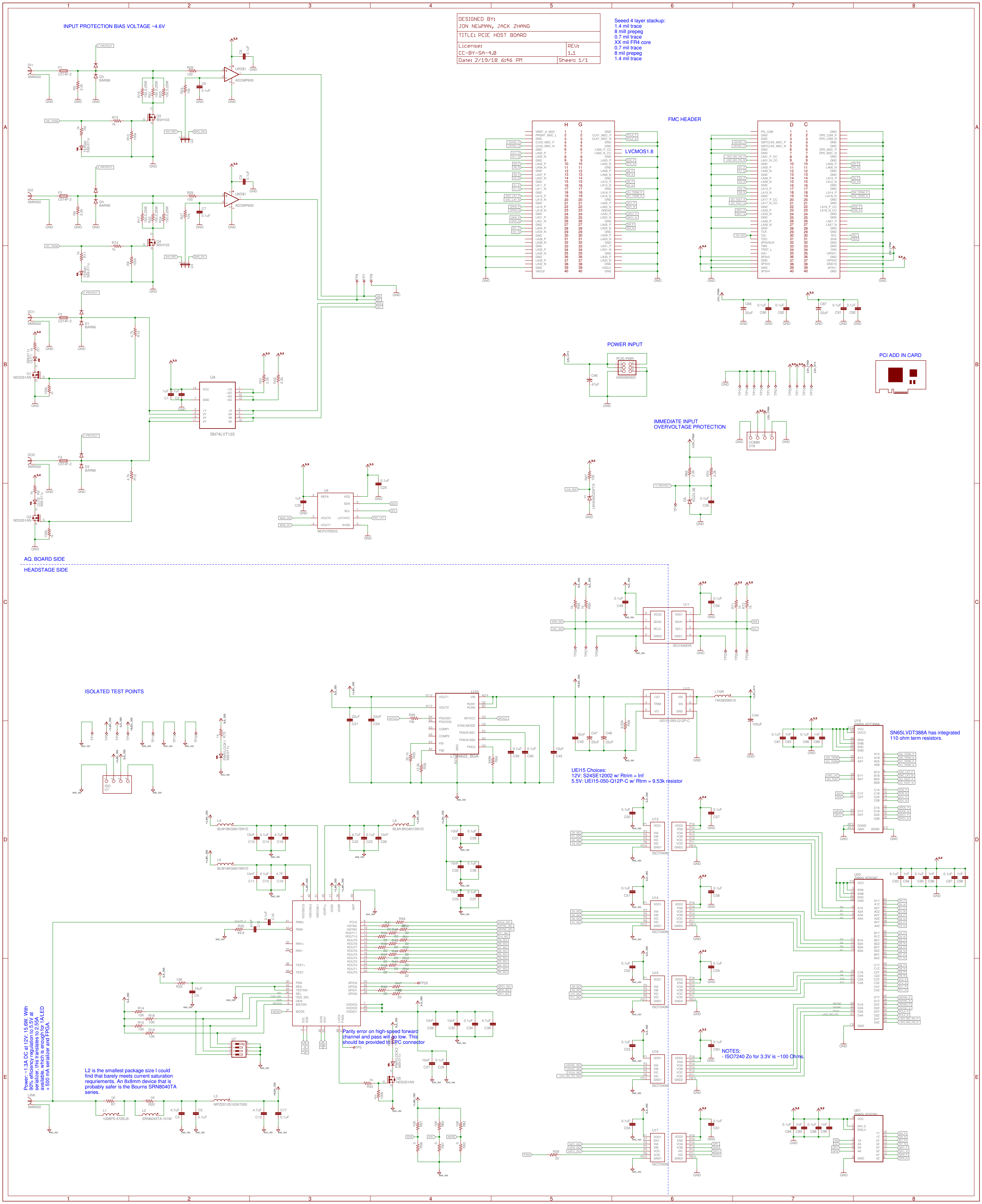
DESIGNED BY:
JON NEWMAN, JACK ZHANG
TITLE: PCIE HOST BOARD
License:
CC-BY-SA-4.0
REV:
1.1
Date: 2/19/18 6:46 PM
Sheet: 1/1
Seeed 4 layer stackup:
1.4 mil trace
8 mill prepeg
0.7 mil trace
XX mil FR4 core
0.7 mil trace
8 mil prepeg
1.4 mil trace
INPUT PROTECTION BIAS VOLTAGE ~4.6V
FMC HEADER
LVCMOS1.8
POWER INPUT
PCI ADD IN CARD
IMMEDIATE INPUT
OVERVOLTAGE PROTECTION
AQ. BOARD SIDE
HEADSTAGE SIDE
ISOLATED TEST POINTS
SN65LVDT388A has integrated
110 ohm term resistors.
UEI15 Choices:
12V: S24SE12002 w/ Rtrim = Inf
5.5V: UEI15-050-Q12P-C w/ Rtrm = 9.53k resistor
Parity error on high-speed forward
channel and pass will go low. This
should be provided to LPC connector
NOTES:
- ISO7240 Zo for 3.3V is ~100 Ohms.
L2 is the smallest package size I could
find that barely meets current saturation
requriements. An 8x8mm device that is
probably safer is the Bourns SRN8040TA
series.
Power: ~1.3A DC at 12V; 15.6W. With
90% efficiency regulation to 5.5V at
serializer, this translates to 2.55A
available, which is enough for 1A/LED
+ 500 mA serializer and FPGA.
U4
SN74LVT125
U8
MCP47FEBXX
U10
LTM4622_BGA
U12
UEI15-050-Q12P-C
U11
ISO1540DR
U13
ISO7240M
U14
ISO7240M
U15
ISO7240M
U16
ISO7240M
U17
ISO7242M
U19
SN65LVDT388A
U20
SN65LVDS387
U21
SN65LVDS391
L1
1008PS-472KLB
L2
SRN6045TA-101M
L3
MPZ2012S102AT000
L7/0R
74438356010
L4
BLM18KG601SN1D
L5
BLM18KG601SN1D
L6
BLM18KG601SN1D