Status LEDs

Headstage Ports

Power

CLK Feedthrough

Analog IO

HARP Bus

FPGA

NB: Jumper wire to pin 25 on bottom of TinyFPGA

IO Expander

Host AUX

NB: P,N order matches SDR datasheet spec.

Buttons

Digital IO

Open Ephys

Use JLC2313 Stackup:
https://jlcpcb.com/client/index.html#/impedance. 0.2 mm prepeg