# System Driven Hardware Design (SDHD),SS2020

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# Bandpass Test Assignment

Report submitted by:

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**12.07.2020**

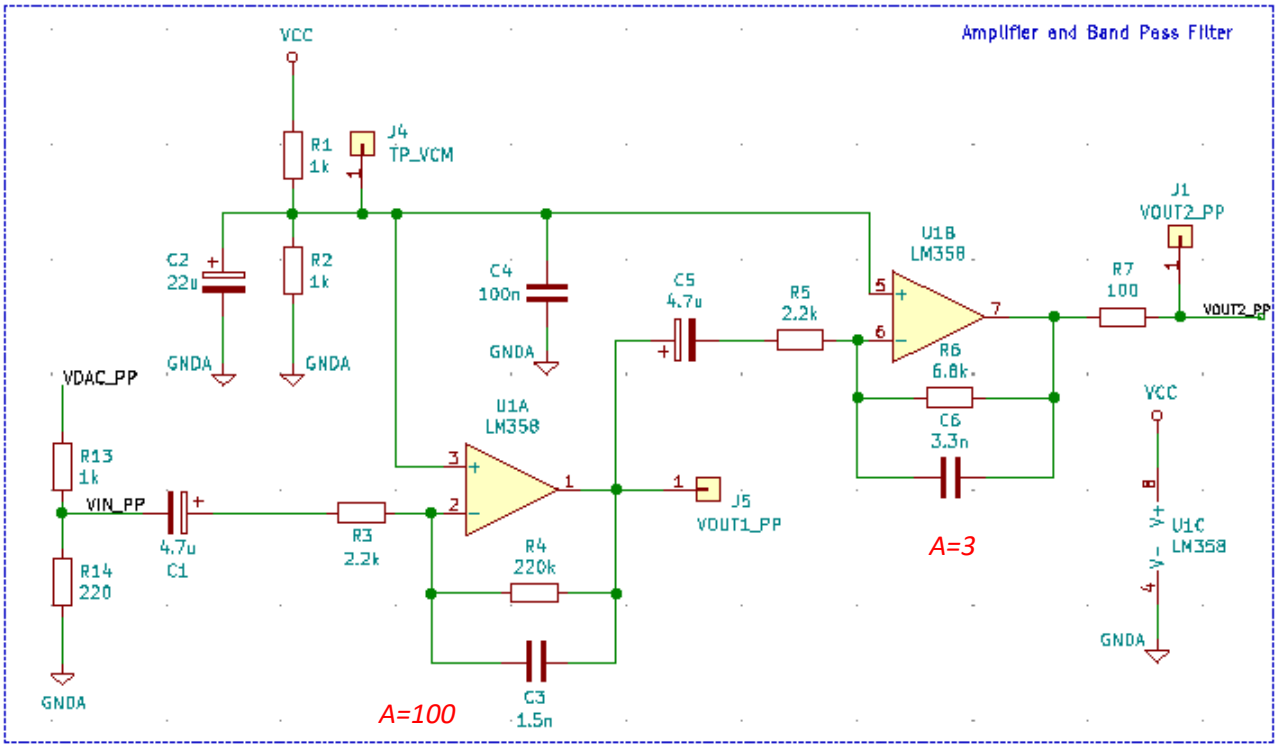
# Contents

# 1. Introduction

The aim of the assignment is to validate the bandpass amplifier with a test signal. The DAC peripheral in the FreeSoC board is used as signal generator to generate the test signal. The output of the amplifier is sampled by the ADC and the output data is transmitted via UART. Matlab Script is used as to observe the sampled ADC data in the form of graph. ADC data at each sample number is converted into voltage and graph is plotted (Voltage vs Sample Number). We also perform FFT on the sampled ADC data and plot the graph (magnitude in dB vs Frequency).

# 2. Concept

The final objective of the assignment was to detect the movements using a 24 GHz Doppler radar sensor. The output of the radar sensor is an AC signal which ranges from minimum of 300uV to 1 mV. For processing the sensor signal, we use the ADC peripheral in the FreeSoC board. The ADC works in range of 100mV to 4.75 V, hence the AC signal coming from the radar sensor has to be amplified before ADC sampling is performed. Hence, we design a 2- stage bandpass amplifier to amplify the sensor signal such that it comes in the range of ADC peripheral for sampling. The schematic of the designed 2-stage amplifier is attached below:




2.1. Figure 1: Schematic of 2-stage amplifier circuit

The radar sensor signal is emulated using a test signal generated from DAC peripheral of FreeSoC2, the amplitude of this test signal is fixed as 40mV, in the schematic label VDAC_PP, the overall gain of the 2-stage amplifier is 300. This has been decided so that after amplification the signal lies in the

ADC range of the 100mV to 4.75 V. The values of the resistances and capacitances in the above circuit were fixed using the below equations for each stage of amplification. For 1st stage of amplification these equations were used.

$$\text{Low cut off freq} = \frac{1}{2 * \pi * R3 * C1}, \text{High cut off freq} = \frac{1}{2 * \pi * R4 * C3}, \text{Amplification} = \frac{R4}{R3},$$

For stage 2 amplification:

$$\text{Low cut off freq} = \frac{1}{2 * \pi * R5 * C5}, \text{High cut off freq} = \frac{1}{2 * \pi * R6 * C6}, \text{Amplification} = \frac{R6}{R5},$$

At stage 1 the amplification was 100 and at stage 2 the amplification was as a factor of 3. We obtain the resistance and the capacitance with these equations for these values of the gain.

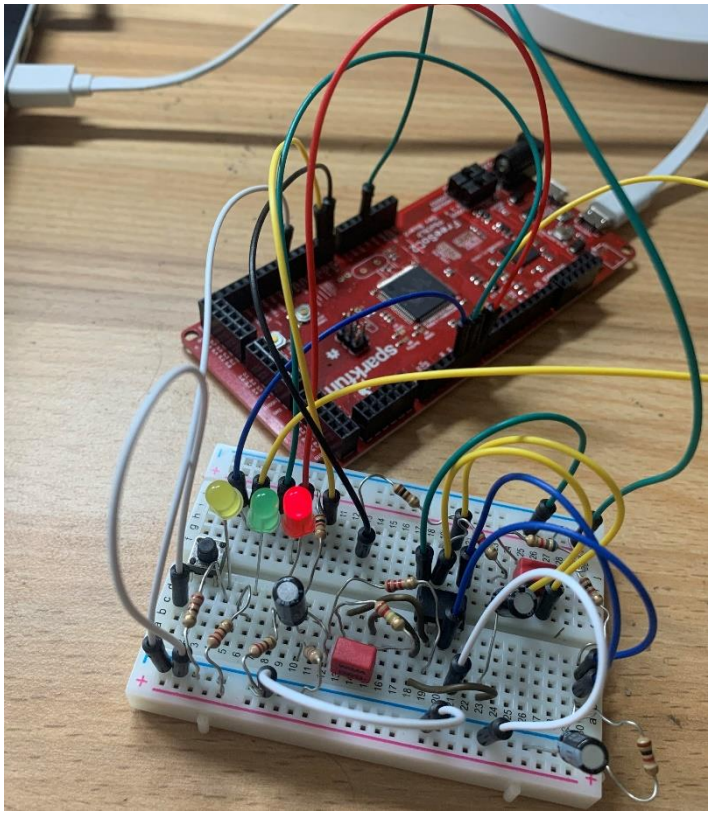
Reason for using voltage divider circuit with the VDAC signal was: The voltage divider circuit was used in the beginning since the amplitude of the test signal is 40mV when it is amplified with a factor of 300, the expected output will be 12V which is outside the range of ADC hence a voltage divider is used to lower the input frequency by a factor, with my circuit the factor is (220/1000+220), hence the output voltage after amplification would be around 2.5 V which is in the range of ADC.

# 3. Implementation and Testing

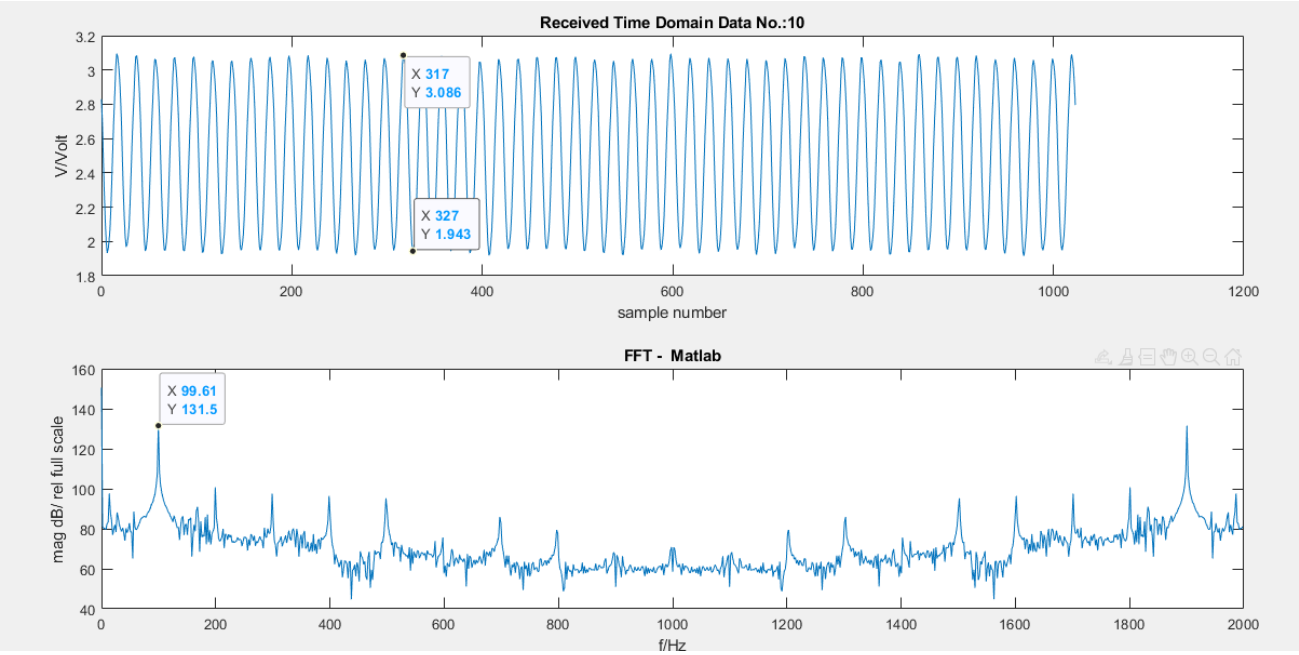
The schematic shown above was built on the breadboard. To test the circuit, the test signal from VDAC was generated with various frequencies between the lower and higher cut off frequencies which is 20 Hz and 520 Hz respectively for the 2-stage amplifier obtained from the circuit. This signal was given as the input, the signals at the test points VDACpp, VINpp, Vout1pp, and Vout2pp were given to the ADC of the FreeSoC. The sampled ADC values were sent to Matlab script. The ADC values were converted into volts. The ADC conversion rate is 2000 samples/seconds and it is a 16-bit ADC hence using these voltages was calculated. For each of the corresponding signals FFT was performed and the results were plotted against frequency.

| S No | Fsine | Udac_pp | Vin_pp | Vout1_pp | Vout2_pp | A1 | A2 | A | A_LTSPICE |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 10 Hz | 0.0229 V | 0.00439 V | 0.235 V | 0.399 V | 53.54 | 1.697 | 90.88 | 90.26097 |
| 2 | 30 Hz | 0.0224 V | 0.00403 V | 0.359 V | 0.9589 V | 89.081 | 2.68 | 237.94 | 242.661 |
| 3 | 50 Hz | 0.02279 | 0.00389 V | 0.379 V | 1.123 V | 97.429 | 2.963 | 288.68 | 267.916 |
| 4 | 80 Hz | 0.0223 V | 0.00381 V | 0.372 V | 1.156 V | 97.6377 | 3.1075 | 302.617 | 279.576 |
| 5 | 100 Hz | 0.0227 V | 0.00382 V | 0.369 V | 1.132 V | 96.59 | 3.06775 | 296.335 | 280.866 |
| 6 | 125 Hz | 0.0224 V | 0.00373 V | 0.363 V | 1.121 V | 97.319 | 3.088 | 300.536 | 279.2544 |
| 7 | 150 Hz | 0.02259 V | 0.00366 V | 0.357 V | 1.079 V | 97.54 | 3.0224 | 294.808 | 276.37 |
| 8 | 200 Hz | 0.0218 V | 0.00358 V | 0.316 V | 0.988 V | 88.268 | 3.126 | 275.977 | 267.60 |
| 9 | 350 Hz | 0.0201 V | 0.00312 V | 0.275 V | 0.831 V | 88.14 | 3.02 | 266.346 | 233.07 |
| 10 | 500 Hz | 0.016 V | 0.00279 V | 0.163 V | 0.468 V | 58.422 | 2.87 | 167.741 | 198.83 |
| 11 | 600 Hz | 0.011 V | 0.00183 V | 0.091 V | 0.282 V | 49.72678 | 3.098901 | 154.09 | 174.1801 |

3.1 Table 1: Measurement Value at test points for each of your frequencies



3.2 Figure 2: Picture of the Breadboard Setup for bandpass amplifier



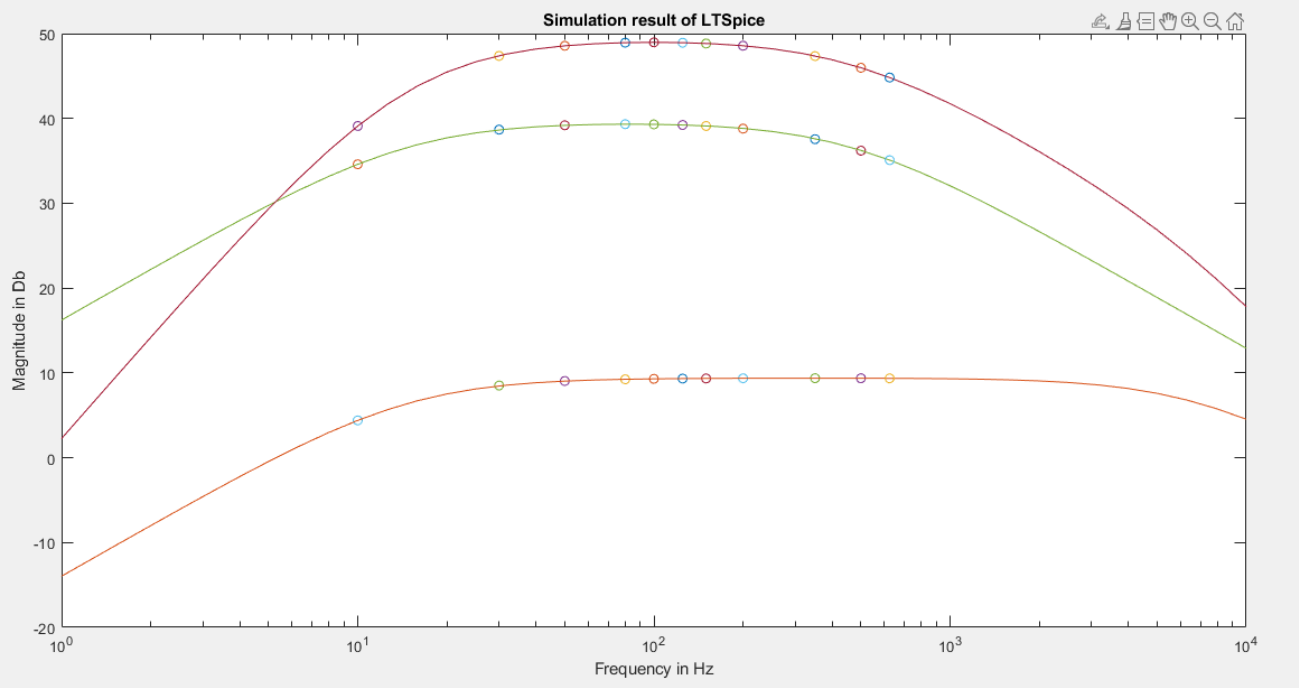

3.3 Figure 3: Output from the breadboard

3.4 Graph 1: Final Output Voltage(V) vs sample number

3.5 Graph 2: FFT of the output voltage (mag in DB) vs frequency (Hz)

# 4. Observation

- The Figure 3.2 shows the breadboard setup which was built and the figure 3.3 and the plots shows the output result for the test signal with f =100 Hz.
- We see from the FFT vs Frequency plot that at f=100 Hz we obtain the peak ADC output in frequency domain which signifies that, the obtained output corresponds to frequency of 100Hz. The expected frequency is 100 Hz, obtained frequency is 99.61, error = 0.39.
- We change the frequency of the test signal between the corner frequencies 20 Hz (Lower cut off frequency) and 520 Hz (Upper cut off frequency). We measure all the signals at test points (VDACpp, VINpp, Vout1pp, and Vout2pp) using ADC and make a table as shown in Table 1.
- We compare the output with the simulation result obtained from the LT-spice circuit. The raw file from the LT-Spice is taken as input and fed to MATLAB script to obtain the output gain of total amplification, 1-stage amplification and 2-stage amplification at various frequency.




4.1 Figure 4: Simulation result of LT- Spice

For the above graph red line corresponds to Total amplification gain in dB vs Frequency, green line corresponds to 1-stage amplification gain in dB vs Frequency and orange line corresponds to 2-stage amplification gain in dB vs Frequency.

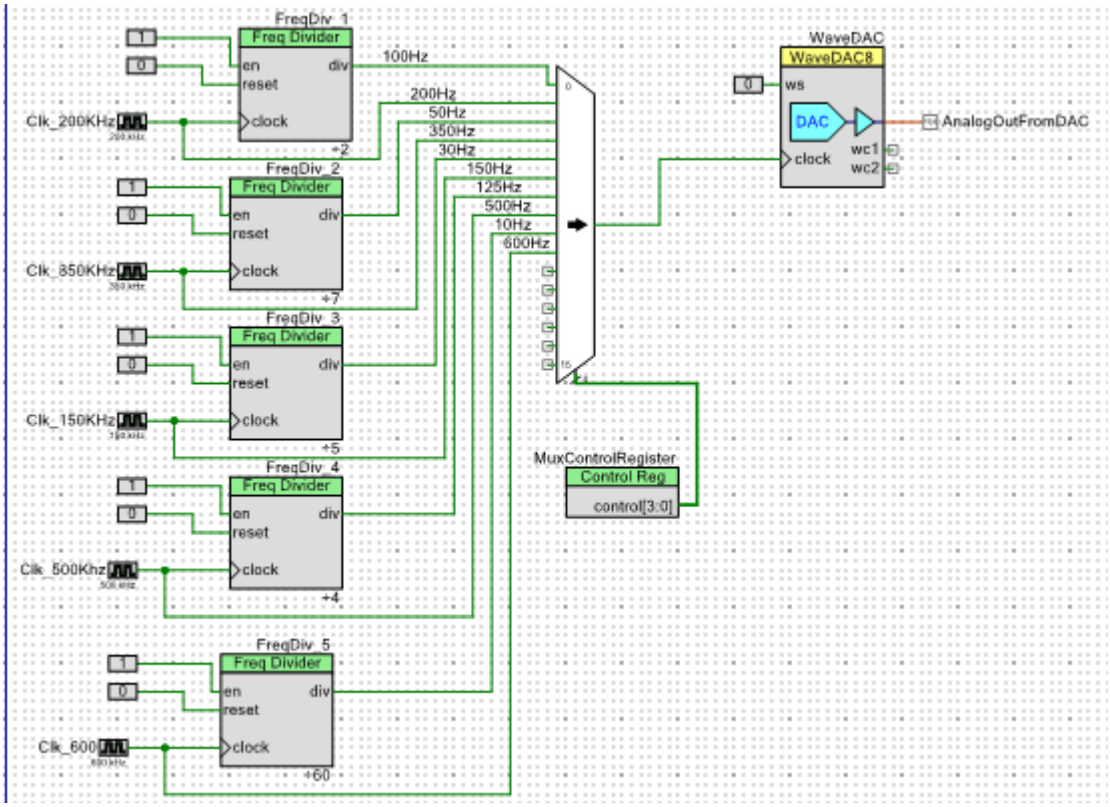
# 5. Analysis and Conclusion:

- we use 5V supply from the FreeSoC to power LMV385 but we don't receive exactly 5 V, it has a tolerance. This happens because FreeSoC is powered using USB and the USB output fluctuates, as it is unstable, we receive certain tolerance.
- The DAC used to generate test signals at various frequency is not ideal waveform generator as it has a high resistor connected to it in series, which could affect the test signal which is generated.

- We observe that the obtained output gain and the simulated output gain differs this happens because of the tolerances of resistors, capacitors and non – ideal characteristics of the OpAmp. Also, since we are doing connections on bread board using wires. Using a PCB instead can result in more stable and accurate system but it is costing more than that of breadboard.

## 5. Ideas for Improvement / Outline:

- The test signal frequency has to be changed every time to prepare the table manually, so we can make a test setup and the software such that it does change automatically. This has been implemented and the setup is attached below:




5.1 Figure 5: Change frequency on button press, implemented in SW as improvement

- We could use Zener diode to avoid the voltage fluctuations of VCC being supplied to the LMV385 so that we get same supply voltage irrespective of the current.
- DAC peripheral is not an ideal source of waveform generator; hence we could use a signal generator to provide the input to the breadboard circuit.
- Use of PCB instead of Breadboard so that we have a stable circuitry instead of using wires in the breadboard.