NEW LUMBINI PUBLICATION

Advance Electronics

1st Edition

Suraj Agrahari :: Arjun Chhetri

For BEI / BEX Engineering

Book: Advance Electronics

II Year / II Part (TU, PU, KU, PoU

Authors
Suraj Agrahari
Arjun Chhetri

Publisher : **New Lumbini Books**
Mob: 9851166694, 9864277554
Near Thapathali Engineering Campus
Maitighar, Kathmandu

Copyright : **Publication & Authors**

First Edition : **2022/023**

Price : **Rs. 400.00**

Printed in Nepal

...✍ Preface

With the aim to provide electronics knowledge in simple, effective and conceptual way a reference book on "advance electronics" is written for student studying in undergraduate level in electronics, communication and IT engineering field in IOE, Tribhuvan University. This book presents all the topics in a simple and lucid way with the help of definition, derivation, numerical and necessary examples so that theoretical and real-world problem can be visualize, analyzed and solved. In addition, there are few short notes, practice questions and past question along with their solution so that student can practice what they have learned and score a better academic score. We have left no stone unturned for developing an efficient understanding of the subject matter but as it said "better than a thousand days of diligent study is one day with a great teacher" so this book will be more effective along with teacher lectures.

We are eternally grateful to Er. Devendra Kathayat (Senior Lecturer at Thapathali Engineering Campus, Himalayan Engineering College), our parents and everyone who have paved the way toward accomplishing this fine project. Special mention to an anomalous PDF with has been a beam of light in the darkness of nowhere. Writing a book is harder than we thought and more rewarding than we could have ever imagined. We are highly indebted and thankful to everyone who have supported and helped us directly and indirectly in bringing this book so that we could serve future engineer and nation.

Before pen down, we want suggest a life lesson "Expect for the best but Prepare for the worst". Any comments and suggestion will be highly appreciated from the bottom of our heart. With the hope every student and concerned person will be benefited from our book, fulfilling the sole meaning of life to serve humanity.

Authors

Table of Contents

1. Operational Amplifier Circuit 1 – 28

1.1 Bias Circuit Suitable for IC Design 1
1.2 Types of Circuit Model 2
1.3 The Differential Amplifier 10
1.4 BJT Differential Amplifier with Active Load 17
1.5 Output Stage 21
Numerical Problems 21
Old Questions with Solution 22

2. Fluid Operational Amplifier Characterization 29–60

2.1 Input Offset Voltage 30
2.2 Input Basis and Input Offset Current 32
2.3 Output Impedance 35
2.4 Differential And Common Mode Input Resistance 36
2.5 DC Gain, Bandwidth, Bandwidth Product 38
2.6 Common Mode and Power Supply Rejection Ratio 41
2.7 Higher Frequency Pole Setting Time 42
2.8 Slew Rate 42
2.9 Noise in Operational Amplifier Circuit 43
Numerical Problems 45
Old Questions with Solution 45

3. Digital to Analog and Analog to Digital 61–92

3.1 The R-2R Ladder Circuit 66
3.2 Unipolar and Bipolar D/A Converters 70
3.3 Count Up and Tracking A/D based on DAC 71
3.4 Successive Approximation A/D Converters 74
3.5 Integrating A/D Converter 76
3.6 Sigma Delta A/D Converters 79
3.7 Flash A/D Converter 80
Old Questions with Solution 82

4. Instrumentation and Isolation Amplifier 93–108

4.1 Types of I.A. 93
4.2 There Op-amp Instrumentation Amplifier 99
4.3 Consideration of Non-ideal Prosperities 100
4.4 Isolation Amplifier Principles and Realization 100
Old Questions with Solution 102

5. Operational Amplifier-Bipolar Transistor Logarithmic Amplifier 109 – 132

5.1 Log amplifier 109
5.2 Non-ideal Effects 112
5.3 Stability Consideration 117
5.4 Anti-logarithmic operations 118
Old Questions with Solution 125

6. Log-Antilog Circuit Application 133 – 154

6.1 Analog Multiplier Based on Log Antilog Principle 133
6.2 The Multifunction Converter Circuit 142
6.3 Proportional to Absolute Temperature (PTAT) Devices 145
Old Questions with Solution 146

7. Introduction to Power Electronics 155 – 208

7.1 Introduction 155
7.2 Controlled Rectifier Circuits 175
7.3 Inverters 181
7.4 Choppers 184
7.5 DC-DC Conversion 188

7.6 AC to AC Conversion 19
Numerical Problems 19
Old Questions with Solution 20

8. Switched Power Supplies 209 – 256

8.1 Buck Regulators 210
8.2 Boost Regulators 217
8.3 Buck-Boost regulators 223
8.4 Filtering Considerations 229
8.5 Control Circuits, IC Switched 230
Numerical Problems 231
Old Questions with Solution 239

Short Notes 248 – 256

Question Bank (2068 to 2078) 257 – 287

References 288

Syllabus

Advanced Electronics is continuation of Electronic Devices & Circuits which is included in BE Electronics and Communication course for III Year – I part with emphasis on data conversion, instrumentation and power circuits. The subject code of Advanced Electronics is _ and following syllabus, practicals list, references and marking scheme are as per the latest update of IOE Syllabus.

1. Operational Amplifier Circuits (6 hours)

1. Bias circuits suitable for IC Design
2. The Widlar current source
3. The differential amplifier
4. Active loads
5. Output stages

2. Operational Amplifier Characterization (6 hours)

1. Input offset voltage
2. Input bias and input offset currents
3. Output impedance
4. Differential and common-mode input impedance
5. DC gain, bandwidth, gain-bandwidth product
6. Common-mode and power supply rejection ratios
7. Higher frequency poles settling time
8. Slew rate
9. Noise in operational amplifier circuits

3. Digital-To-Analog and Analog-To-Digital Conversion (8 hours)

1. The R-2R ladder circuit
2. Unipolar and bipolar D/A converters
3. Count-up and Tracking A/D's based on D/A's
4. Successive approximation A/D converters

5. Integrating voltage-to-time conversion A/D converter dual and quad slope types
6. Sigma delta A/D converters
7. Flash A/D converters

4. Instrumentation and Isolation Amplifiers (4 hours)

1. One and two operational amplifier instrumentation amplifiers
2. The three operational amplifier instrumentation amplifier
3. Consideration of non-ideal properties
4. Isolation amplifier principles and realization
5. Consideration of non-ideal properties

5. Operational Amplifier-Bipolar Transistor Logarithmic Amplifier (3 hours)

1. The basic logarithmic amplifier
2. Non-ideal effects
3. Stability consideration
4. Anti-logarithmic operations

6. Log Antilog Circuit Application (5 hours)

1. Analog multiplier based on log-antilog principles
2. The multifunction converter circuit
3. Proportional to absolute temperature (PTAT) devices
4. RMS to dc conversion

7. Introduction to Power Electronics (7 hours)

1. Diodes, thyristors, triacs, IGBT
2. Controlled rectifier circuits
3. Inverters
4. Choppers
5. DC-to-DC conversion
6. AC-to-AC conversion

8. Switched Power Supplies (4 hours)

1. Voltage step-down regulators
2. Voltage step-up regulators
3. Step-up/step-down regulators
4. Filtering considerations
5. Control circuits, IC switched

Laboratory:

- Characteristics of operational amplifier
- 4 bit D to A converter
- Differential amplifier, Instrumentation amplifier
- Logarithmic amplifier
- Study of switched voltage regulator
- Study of Silicon-controlled-rectifier (SCR) and TRIAC circuit

Reference:

- A.S. Sedra and K.C. Smith, "Microelectronic Circuits", 6th Edition, Oxford University Press.
- W. Stanely, "Operational Amplifiers with Linear Integrated Circuits", Charles
- Merrill Publishing Company, Toronto, 1984.
- Jacob Millman and Christos C. Halkias, "Integrated Electronics", TATA McGRAW- Hill Edition 1991.
- Muhammad H. Rashid, "Power Electronics: Circuits, Devices and Applications", 3rd Edition, Pearson Education, 2003.
- Ramakant A. Gayakwad, "Operational Amplifiers with Linear Integrated Circuits", 4th Edition, Prentice Hall, New Delhi, 2004.
- Robert F. Coughlin and Frederick F. Driscoll, "Operational Amplifiers and Linear Integrated Circuits", 4th Edition, Prentice Hall, New Delhi, 1996.

- C.W. Lander, "Power Electronics", 2nd Edition, McGraw-Hill Book Company, New York,1987.
- J.G. Graeme, "Application of Operational Amplifiers: Third Generation Techniques", The Burr-Brown Electronics Series, McGraw-Hill, New York,
- N. Mohan, T. M. Undeland and W. P, Robbins, : Power Electronics: Converters, Applications and Design", John Willey and Sons, New York,

Evaluation Scheme:

There will be 12 Questions covering all the chapters in the syllabus. The evaluation scheme for the questions will be indicated in the table below:

Unit	Hour	Number of questions	Marks distribution
1	6	1	7
2	8	2	14
3	8	2	14
4	4	1	7
5	3	1	4
6	5	1	7
7	7	2	14
8	4	1	7
1, 4, 5, 6, 8		1	6
Total	**45**	**12**	**80**

Chapter 1 Operational Amplifier Circuit

An operational amplifier circuit is a DC- coupled high gain electronics voltage amplifier with a differential input and usually single ended output. It is a three terminal device which have all the properties required for nearly ideal DC amplification. Therefore it is used for extensively in a signal conditioning filtering or to perform mathematical operation such as add subtract integration and differentiation.

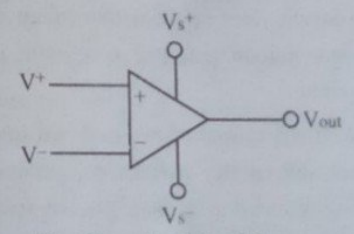


Fig: Operational amplifier

1.1 Bias Circuit Suitable for IC Design

A Bias circuit is a portion of the device circuit which supplies the steady current or voltage Bias circuit are used to Bias discrete BJT because it is not suitable as they need large number of resistor as well as large coupling and by pass capacitor. With the current technology it is almost impossible to fabricate large capacitor and it is uneconomical to manufactory large resistance. It is based on constant current source.

On an IC chip with number of amplifier stage. A constant dc current is generated at one location and then if it reproduced at various other location. Major advantage of this approach is Bias current of various track each other in case at change in power supple voltage or temperature.

Constant current source is characterized by:

- Very high output resistance
- Very high voltage resistance

1.2 Types of Circuit Model

There are different circuit model some of them are given below:

(a) Simple current mirror circuit

(b) Current steering circuit

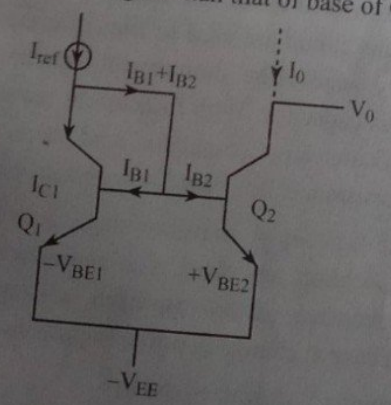
(c) Improved current mirror circuit

(d) Wilson current mirror circuit

(e) Wildar current source

(a) Simple current mirror circuit: This simple current mirror circuit simply known as current mirror circuit is designed to copy the current through one active device by controlling the current in another active device. Keeping the output circuit constant regardless of loading. Output current is forced to be equal to input current in current mirror circuit.

Current mirror circuit consist of two matched transistor Q_1 and Q_2 with their bases and emitter connected together Q_1 connected as diode by shorting collector to its base. A reference current source I_{ref} is fed to the collection of Q_1 and output current is taken from the collector of Q_2. The circuit fed by the collector of Q_2 should ensure the active mode of operation of Q_2 at all times that is collector voltage of Q_2 will be higher than that of base of Q_2.



Since, both transistor are matched and $V_{BE1} = V_{BE2}$

$V_{E1} = V_{E2}, \beta_1 = \beta_2 = \beta$

Using KCL,

$$I_{ref} = I_{c1} + I_{B1} + I_{B2}$$

$$I_{ref} = \frac{\beta}{\beta+1} I_{E1} + \frac{2 I_{E1}}{\beta+1} \qquad \left(\because I_B = \frac{I_E}{\beta+j} I_c = \frac{\beta}{\beta+1} I_E\right)$$

$$I_{ref} = \left(\frac{2+\beta}{\beta+1}\right) I_{E1} \rightarrow \text{(i)}$$

Similarly,

$$I_0 = I_{c2} = \frac{\beta}{\beta+1} I_{E1} \qquad \text{... ... ... (ii)}$$

Dividing equation (ii) by (i) we get

$$\frac{I_0}{I_{ref}} = \frac{\beta}{2+\beta} = \frac{1}{1+2/\beta}$$

Which approaches unity i.e. $I_0 \approx I_{ref}$ when $\beta \gg 1$

This shows that I_0 varies according to the change in β., Hence we can conclude that I_0 is not exactly equal to I_{ref} because,

(i) β has finite value

(ii) Q_2 has finite value of output resistance

Useful defination Early effect: Early effect is the variation in the width of base in BJT due to variation in applied base to the collector for example; voltage in C – B has greater bias the C – B depletion width increases and width of B decreases.

(b) Current steering circuit: In order to reproduce, current for biasing various circuit current mirror are used.

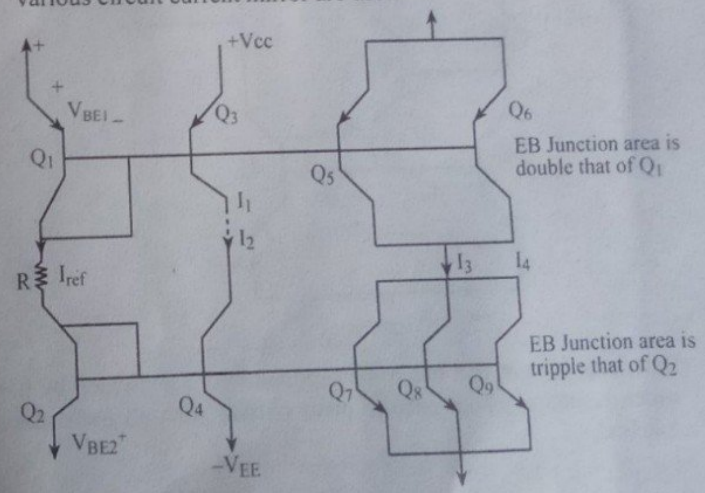


Fig: Current steering circuit

Generalization of number of constant current source using KVL,

$$I_{ref} = \frac{V_{CC} + V_{EE} - V_{BE1} - V_{BE2}}{R}$$

Assuming the transistor has high β and neglecting early effect $I_{ref} = I_1$ Q_3 can supply the load as long as the Q_3 can operate in active region i.e. voltage ($V_{cE} = 0.3$ V) to generate a dc current twice the value of I_{ref} 2 transistor Q_5 and Q_6 are connected in parallel and combination forms mirror with Q_1. Thus $I_3 = 2\ I_{ref}$.

Parallel combination of Q_5 and Q_6 is equivalent to the transistor whose EBJ area is double that of Q_1. In IC fabrication the BJT area is double if the current has to be double.

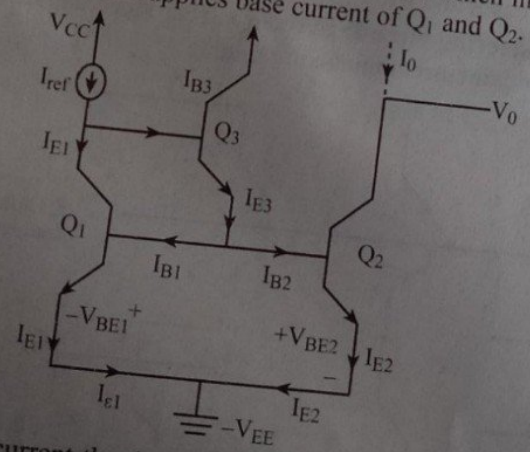
The effect of finite β becomes more server as the number of output of the mirror, is increased. This is because the addition of more transistor means that their base current has to be supplied by the reference source.

(c) Improved current source: There are two parameter of the BJT current source that need improvement.

(i) Dependence of I_0 on β results in the error of mirror current gain introduced by finite β.

(ii) Output resistance of current source which is found to be equal to r_0 of BJT and thus limited to order of 100 kΩ.

Assuming a improved current mirror circuit which include transistor Q_3 whose emitter supplies base current of Q_1 and Q_2.



Here base current that has to be supplied by I_{ref} is divided by β + 1 which results in much smaller error circuit. Also all transistor are matched,

$$\beta_1 = \beta_2 = \beta_3 = \beta$$

$\therefore$ $V_{BE1} = V_{BE2}$ then $I_{E1} = I_{E2} = I_{E3}$

Using KCL at note x,

$$I_{ret} = I_{c1} + I_{B3}$$

$$= \left(\frac{\beta}{\beta+1}\right) I_E + \left(\frac{I_E}{\beta+1}\right) \qquad \left(\because I_c = \frac{\beta}{\beta+1} I_{E1},\ I_E = (\beta+1)\, I_B\right)$$

$$= \left(\frac{\beta}{\beta+1}\right) I_E + \frac{(2/I_E)\,(\beta+1)}{\beta+1}$$

$$= \frac{I_E}{\beta+1} + \frac{I_E}{\beta+1} = \frac{2I_E}{\beta+1}$$

$$I_{ref} = \frac{\beta I_E}{\beta+1} + \frac{2I_E}{(\beta+1)^2} \quad \ldots\ldots\ldots \text{(i)}$$

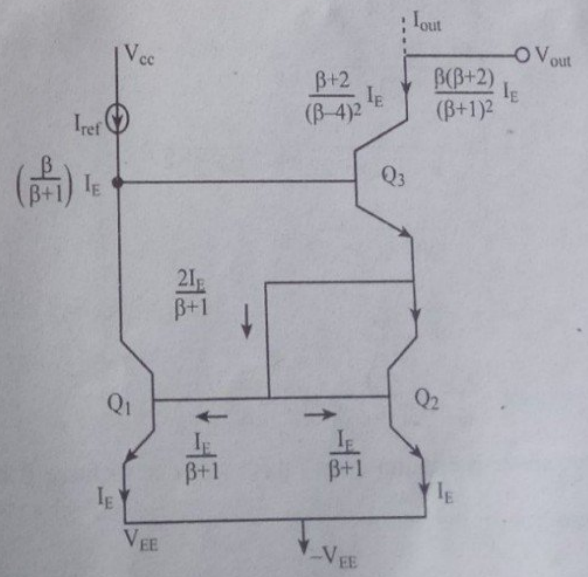
Then, $I_0 = I_{c2} = \left(\frac{\beta}{\beta+1}\right) I_E \rightarrow$ (ii)

Dividing equation (ii) by equation (i) we get

$$\frac{I_0}{I_{ret}} = \frac{1}{1 + \frac{2}{\beta(\beta+1)}} \approx \frac{1}{1 + \frac{2}{\beta^2}}$$

From the above equation, we can conclude that error due finite β has been reduced from $\frac{2}{\beta}$ to $\frac{2}{\beta^2}$ which is tremendous improvement.

(d) Wilson current mirror circuit: Wilson current mirror circuit achieves both current compensation and increased output resistance.



From figure,

$$I_{out} = \frac{\beta(\beta+2)}{(\beta+1)^2} I_E \rightarrow (i)$$

$$I_{ref} = \left(\frac{\beta}{\beta+1} + \frac{\beta+2}{(\beta+1)^2}\right) I_E$$

$$I_{ref} = \left(\frac{\beta^2+\beta+\beta+2}{(\beta+1)^2}\right) I_E$$

$$\therefore \quad I_{ref} = \left(\frac{\beta^2+2\beta+2}{(\beta+1)^2}\right) I_E \rightarrow (i)$$

$$I_E = \frac{(\beta+1)^2}{\beta^2+2\beta+2} I_{ref} \rightarrow (ii)$$

From equation (i) and (ii)

$$I_{out} = \frac{\beta(\beta+1)}{(\beta+1)^2} \cdot \frac{(\beta+1)^2}{(\beta^2+2\beta+2)} I_{ref}$$

$$= \frac{1}{1+\frac{2}{\beta(\beta+2)}} I_{ref}$$

From equation (iv)

$$I_{out} = \frac{\beta(\beta+2)}{\beta^2+2\beta+2} I_{ref}$$

$$= \left(\frac{\beta^2+2\beta+2-2}{\beta^2+2\beta+2}\right) I_{ref}$$

$$= \left(1-\frac{2}{\beta^2+2\beta+2}\right) I_{ref} \approx \frac{1}{1+2/\beta^2}$$

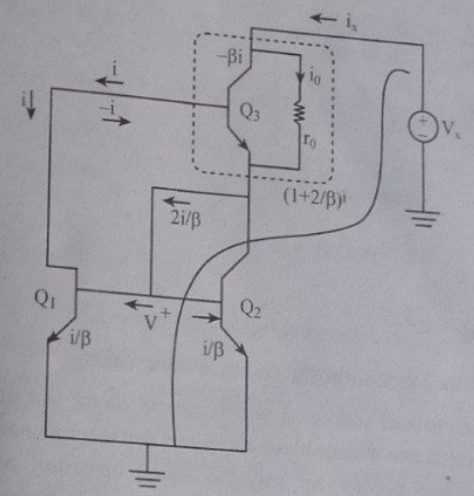
$$= \left(1-\frac{2}{\beta(\beta+2)+2}\right) I_{ref}$$

$$= \left(1-\frac{2}{\beta^2}\right) I_{ref}$$

$$\text{Current gain} = \frac{I_{out}}{I_{ref}} = \frac{1}{1+2/\beta^2} = 1-\frac{2}{\beta^2}$$

Hence, above derivation shows that error due to finite β has been reduced from $\frac{2}{\beta}$ to $\frac{2}{\beta^2}$

For output resistant



From figure,

$$i_X = 1 + \left(1+\frac{2}{\beta}\right) i = 2\left(1+\frac{1}{\beta}\right) i$$

$$V = \left(\frac{\beta+1}{\beta}\right) i \times re$$

Applying KVL at collector of Q_3

$$i_0 = i_X - (-\beta i)$$

$$= 2i + \frac{2i}{\beta} + \beta i$$

$$= \left(\beta + 2 + \frac{2}{\beta}\right) i$$

Again on applying KVL,

$$V_x = i_0 r_0 + V$$

$$= \left(\beta+2+\frac{2}{\beta}\right) i r_0 + \left(1+\frac{1}{\beta}\right) i r_0$$

$$V_x \approx \left(\beta+2+\frac{2}{\beta}\right) i r_0$$

Now,

$$\frac{V_x}{i_x} = \frac{(\beta + 2 + 2/\beta)}{2(1 + 1/\beta)} r_0$$

$$R_0 = \left(\frac{\beta}{2(1 + 1/\beta)} + 1\right) r_0$$

$$= \left(\frac{\beta^2}{2(\beta + 1)} + 1\right) r_0$$

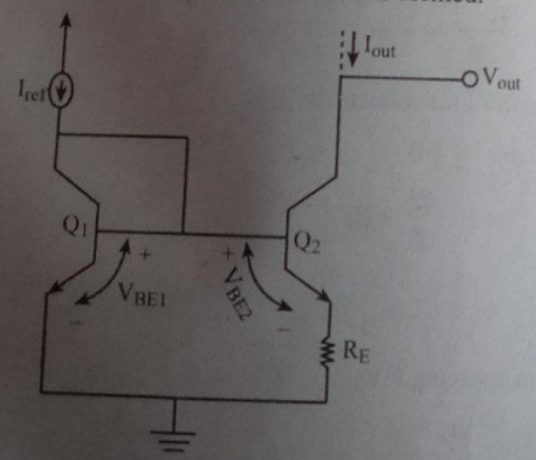
$$= \frac{\beta r_0}{2} \text{ from } \beta \gg 1$$

$$R_0 = \frac{\beta r_0}{2}$$

This shows that output impedance is increased

(e) **Wildar current source:** A wildar current source is a modification of the basic two transistor current mirror that incorporates an emitter degeneration resistor for only the output transistor, enabling the current source to generate low current using only moderate resistor value.

In simple terms when R_E is introduced in emitter terminal of Q_2 is basic current mirror then Wildar current is formed.



Let us suppose two transistor Q_1 and Q_2 are used and base current one negligible then.

$$V_{BE1} = V_T \ln\left(\frac{I_{ref}}{I_s}\right)$$

And,

$$V_{BE2} = V_T \ln\left(\frac{I_0}{I_s}\right)$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{ref}}{I_0}\right)$$

Again, from the circuit we have,

$$V_{BE1} = V_{BE2} + I_0 R_E \text{ (neglecting base current)}$$

Thus,

$$I_0 R_E = V_T \ln\left(\frac{I_{ref}}{I_0}\right)$$

Benefits of using wildar oven simple current source

(i) Wildar current source allows generation of small constant current using relatively small resistance which results in considerable saving in chips area.

(ii) It has high output resistance due to the presence of emitter resistance, R_E.

Determination of output resistance

In order to determine the output resistance of Q_2 transistor let us replace BJT with it's π model and apply test voltage V_x to the collector.

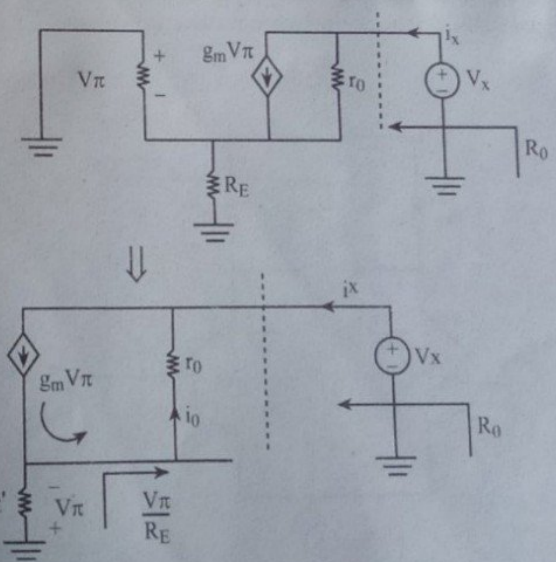


Fig : determination of output resistance of Wildars circuit source.

From the diagram,

$$R_E' = R_E // r_\pi,\ i_0 = g_m V\pi + \frac{V_\pi}{R_E} = \left(g_m + \frac{1}{R_E'}\right) V\pi$$

Applying KVL,

$$V_x = -V\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi\, r_0$$

And, $ix = g_m V_\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi$

∴ The output resistance is,

$$R_0 = \frac{V_x}{ix} = \frac{-V_x - \left(g_m + \frac{1}{R_E'}\right) V\pi\, r_0}{g_m V\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi} = \frac{-1 - \left(g_m + \frac{1}{R_E'}\right) r_0}{g_m - g_m - \frac{1}{R_E'}}$$

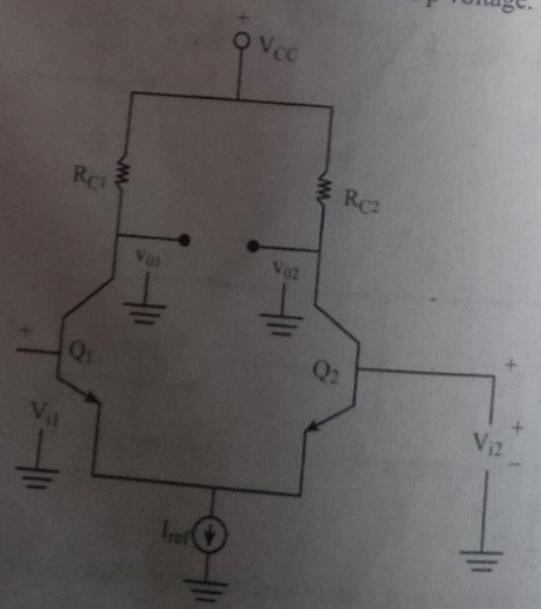
$$= R_E' + R_E' \left(g_m + \frac{1}{R_E'}\right) r_0 = R_E' + (1 + g_m R_E')\, r_0$$

$$R_0 \approx (1 + g_m R_E')\, r_0$$

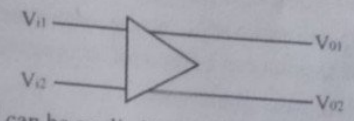
As a result, output resistance is increased by the factor of $(1 + g_m R_E')$

1.3 The Differential Amplifier

It is circuit that can accept two input signal and amplify. The difference between these input signals. The output of an differential amplifier is proportional to the difference between the two i/p voltage.



Symbolically,



Here , input signal can be applied by two ways.

(a) Signal is applied to any one of the transistor and other input is grounded-single ended input arrangement.

(b) Signal are applied to both the input of DA-double ended input arrangement.

Also output can be taken in two ways

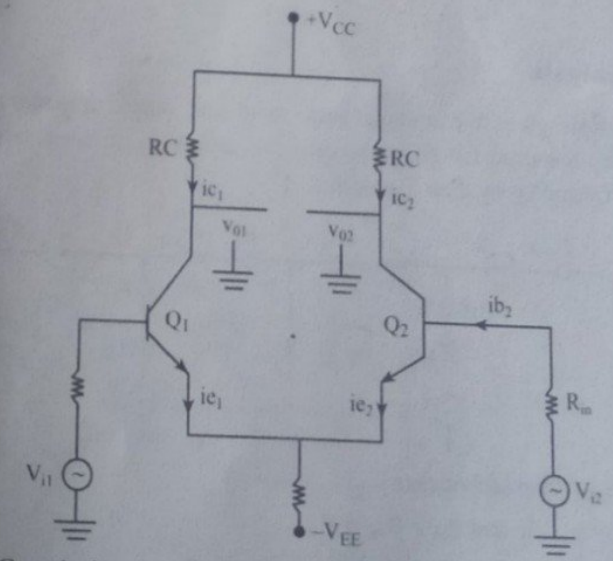
(a) Output signal is taken from any one of the output terminal and other output is grounded single ended output arrangement.

(b) Output signal is taken between two output terminal between the collector of Q_1 and Q_2 double ended input arrangement.

Example: Show that $V_0 \propto V_{i1} - V_{i2}$.

Solution:

Analysis of differential amplifier.



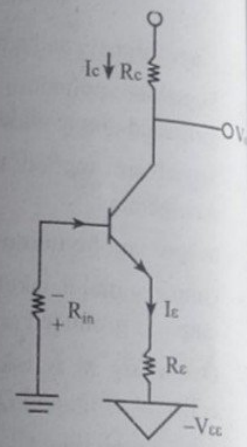
DC analysis

DC analysis is done for the determination of operating point (I_{c0} and V_{cEq}) when no signal is applied.

So, input signal $V_{i1} = V_{i2} = 0$ (Gnd)

Also, Q_1 and Q_2 are matched so, we can determine the Q-point for only. The same Q-point can be used for transistor Q_2.

Applying KVL to base emitter loop.



$$-I_B R_{in} - V_{BE} - I_E R_E + V_{EE} = 0$$

or, $$\frac{I_E R_{in}}{\beta + 1} - V_{BE} - I_E R_E + V_{EE} = 0$$

or, $$-I_E\left(\frac{R_{in}}{\beta + 1} + R_E\right) = -(V_{EE} - V_{BE})$$

or, $$I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_{in}}{\beta + 1}}$$

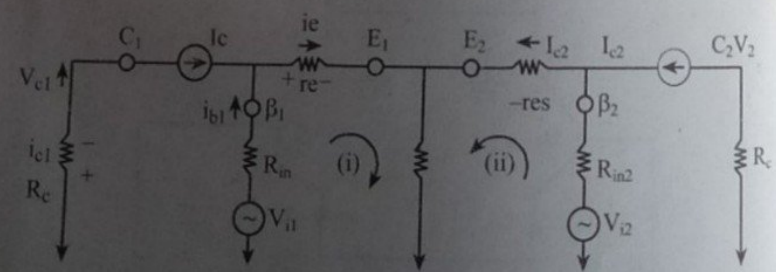
$$\approx \frac{V_{EE} - V_{BE}}{R_E}$$

or, $$\left(\frac{\beta + 1}{\beta}\right) I_c = \frac{V_{EE} - V_{BE}}{R_E}$$

$$\therefore \quad I_c \approx \frac{V_{EE} - V_{BE}}{R_E}$$

AC analysis

AC analysis gives the voltage gain, input and output impedance and frequency response for AC analysis + V_{cc} and V_{EE} are set at zero and replace Q_1 and Q_2 by their T-models.



It Q_1 and Q_2 are matched then,

$$re_1 = re_2 = re \text{ and } R_{in1} = R_{in2} = R_{in}$$

While applying KVL in loop I and loop II we get,

$$V_{i2} = ib_1 R_{in1} + ie_1 re_1 + (ie_1 + ien) R_E$$

$$V_{i2} = ib_2 R_{in2} + ie_2 re_2 + (ie_1 + ie_2) R_E$$

So, $$V_{i1} - V_{i2} = (ib_1 - ib_2) R_{in} + (ie_1 - ie_2) R_E$$

$$= (ib_1 - ib_2) R_{in} + (\beta + 1) re (ib_1 - ib_2)$$

$$= (ib_1 - ib_2)(R_{in} + (\beta + 1) re)$$

$$\therefore \quad ib_1 - ib_2 = \frac{V_{i1} - V_{i2}}{R_{in} + (\beta + 1)re}$$

$$\frac{V_0}{V_{i1} - V_{i2}} = \frac{-\beta R_c}{R_{in} + (\beta + 1)re}$$

$$\approx \frac{-\beta R_c}{(R + 1)re}$$

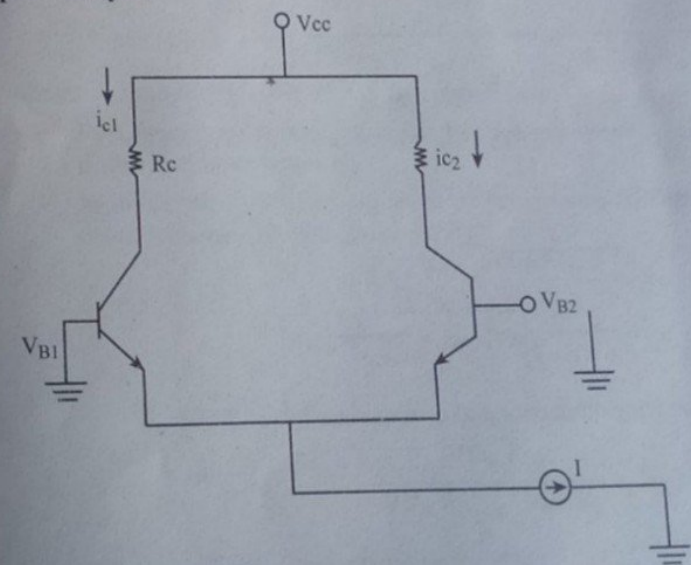
$$\approx \frac{-\beta R_c}{\beta R_e}$$

$$\approx \frac{-R_c}{r_e}$$

$$Ad = \text{differential gain} = \frac{V_0}{V_{id}} = \frac{-R_c}{V_e}$$

From the above derivation it is clear that Ad is directly proportional to the collector resistance R_c i.e. load.

Complete analysis



Consider V_{B1} and V_{B2} are two signal input to differential amplifier V_{01} and V_{02} are two collector outputs do the differential input voltage is $V_{B1} - V_{B2}$ and voltage is $V_{01} - V_{02}$.

For BJT,

$$i_{E1} = \frac{I_s}{\alpha} e^{\frac{V_{BE}}{V_T}}$$

or, $$i_{E1} = \frac{I_s}{\alpha} e^{(V_{B1} - V_E)/V_T} \quad \text{..... (i)}$$

And, $$i_{E2} = \frac{I_s}{\alpha} e^{(V_{B2} - V_E)/V_T} \quad \text{..... (ii)}$$

So, $$\frac{i_E}{i_{E2}} = e^{(V_{B1} - V_{B2})/V_T} \quad \text{..... (iii)}$$

$$1 + \frac{i_{E1}}{i_{E2}} = 1 + e^{(V_{B1} - V_{B2})/V_T}$$

or, $$\frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{-(V_{B1} - V_{B2})/V_T}}$$

So, $$i_{E2} = \frac{I}{1 + e^{V_{id}/V_T}} \quad (\because I_E + I_{E2} \neq I \text{ and } V_{id} = V_{B1} - V_{B2})$$

Similarly,

$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{-(V_{B1} - V_{B2})/V_T}}$$

So, $$i_{E2} = \frac{I}{1 + e^{(V_{id}/V_T)}} \quad (\because I_E + I_{E2} \neq I \text{ and } V_{id} = V_{B1} - V_{B2})$$

Similarly,

$$I_E = \frac{I}{1 + e^{(-V_{id}/V_T)}}$$

So, $$ic_1 = \frac{\alpha I}{1 + e^{(-V_{id}/V_T)}}, \; ic_2 = \frac{\alpha I}{1 + e^{(V_{id}/V_T)}}$$

Multiplying numerator and denumerator by $e^{V_{id}/2V_T}$.

$$I_{c1} = \alpha \frac{I_c \, V_{id}/2V_T}{e^{V_{id}/2V_T} + e^{-V_{id}/2V_T}}$$

$$\frac{\alpha I(1 + V_{id}/2V_T) + \left(\frac{V_{id}}{2V_T}\right)^2 / 2! + \ldots\ldots}{\left(1 + \frac{V_{id}}{2V_T} + \ldots\ldots\right) + \left(1 - \frac{V_{id}}{2V_T} + \ldots\ldots\right)}$$

$$= \frac{\alpha I + \frac{V_{id}}{2V_T} \cdot \alpha I}{2}$$

$$= \frac{\alpha I}{2} + \frac{\alpha I}{2V_T}\left(\frac{V_{id}}{2}\right) = I_{c1} + ic_1$$

Similarly,

$$ic_2 = \frac{\alpha I}{2} - \frac{\alpha I}{2V_T} \cdot \frac{V_{id}}{2}$$

So, $$ic_1 = \frac{\alpha I}{2V_T}\left(\frac{V_{id}}{2}\right) = \frac{I_c}{V_T} \cdot \frac{V_{id}}{2}$$

$$= g_m \cdot \frac{V_{id}}{2} \text{ and } ic_2 = -\frac{g_m V_{id}}{2}$$

Thus, $V_{01} = V_{cc} - ic_1 R_c$

$V_{02} = V_{cc} - icR_c$

So, $V_0 = V_{02} - V_{01} = ic_1 R_c - ic_2 R_c$

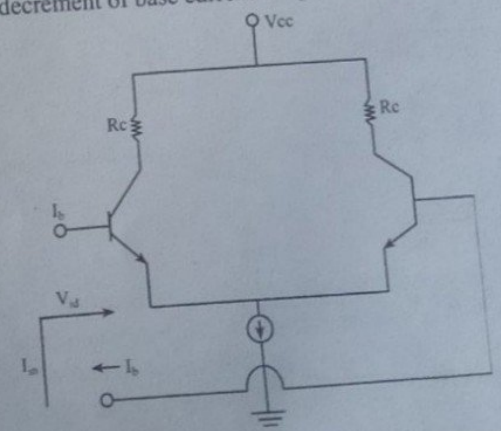
$$= \left(g_m \frac{V_{id}}{2} + g_m \frac{V_{id}}{2}\right) R_c$$

$\therefore \quad V_0 = g_m V_{id} R_c$

$$\frac{V_0}{V_{id}} = Ad = g_m R_c$$

Differential input resistance in term of circuit parameter.

- Resistance seen between the two bases i.e. resistance seen by differential input signal V_{id}.
- In differential amplifier increment of base current Q_1, result in equal decrement of base current of Q_2.



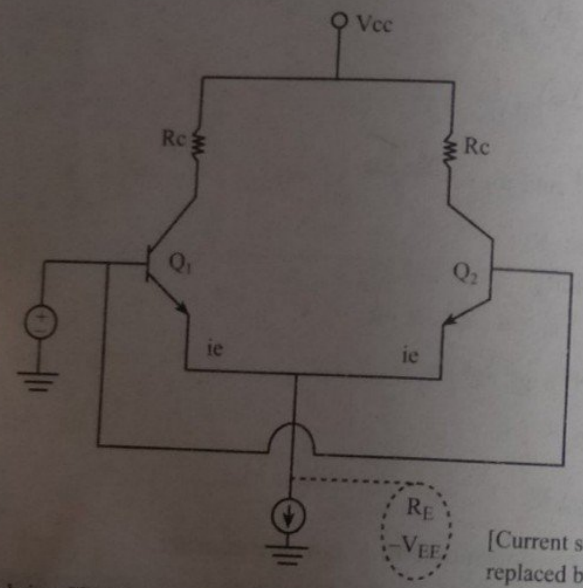
From the figure

$V_{id} = 2ie\ re$ (for AC; I = 0

$= 2(B + 1)\ ib\ re$ (∵ i.e. = (B + 1) ib)

or, $\frac{V_{id}}{i_b} = 2(B + 1)r/e$

Common mode voltage gain,



[Current source is replaced by R_E and $-V_{EE}$]

Applying KVL,

$V_{cm} = ie\ re + 2i\ e_1\ R_E$

$= ie_1\ (re + 2R_e)$

$ie_1 = \frac{V_{cm}}{re + 2R_E}$

or, $ic_1 = \frac{\alpha\ V_{cm}}{re + 2R_E}$

Similarly,

$ic_2 = \frac{\alpha\ V_{cm}}{re + 2R_E}$

$V_{c1} = (-ic_1)\ R_c = \left(\frac{-\alpha V_{cm}}{re + 2R_E}\right) R_c$

$V_{c2} = (-ic_2) R_c = \left(\frac{-\alpha V_{cm}}{re + 2R_E}\right) R_c$

Single ended common mode voltage gain

$A_{cm} = \frac{V_{c1}}{V_{cm}} = \frac{-\alpha R_c}{r_e + 2R_E} = \frac{-R_c}{2R_E}$

Common mode rejection ratio (CMRR)

$CMRR = 20 \log \left(\frac{Ad(x)}{A\ CM(x)}\right)$

Ad – differential mode voltage gain

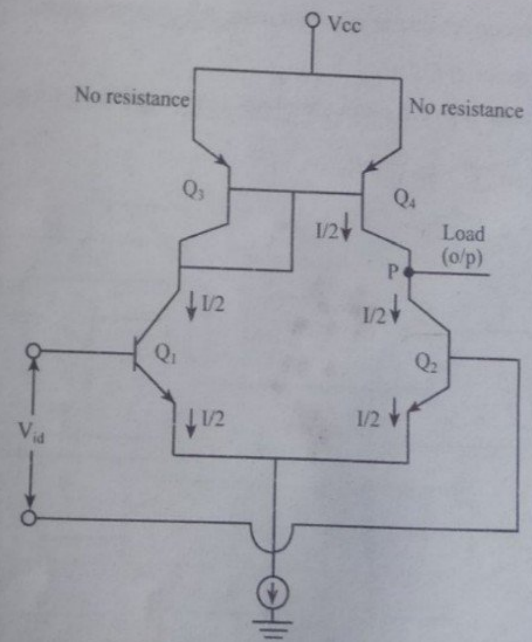
ACM – common mode voltage gain

x = S for single ended

x = D for double ended

CMRR = 80 dB to 100 dB for single ended.

1.4 BJT Differential Amplifier with Active Load



BJT Differential Amplifier with active load is used because Amplifier that ultilize active load can achieve higher voltage gain that those with passive loads for Active loads. BJT as a mirror current source is used which has very high output resistance.

In figure Q_3 and Q_4 together makes a load circuit connected in a current mirror configuration and the output is taken from the collector of Q_2 (single ended output).

Case I

If the no input signal is applied to the base of Q_1 and Q_2 (i.e. two terminal are grounded). The bias current I is divided equally between Q_1 and Q_2. The current of Q_1 is fed to the Q_3 transistor (i.e. input transistor of mirror circuit so, the replicate of the current is provided by the output transistor of mirror Q_4. Hence at output node P. The current I/2 balance each other out leaving a zero current to the load.

Case II

When the diff signal V_{id} is applied at the input the current signal $\frac{g_m V_{id}}{2}$ will result in the collector of Q_1 and Q_2 with polarities indicated in figure.

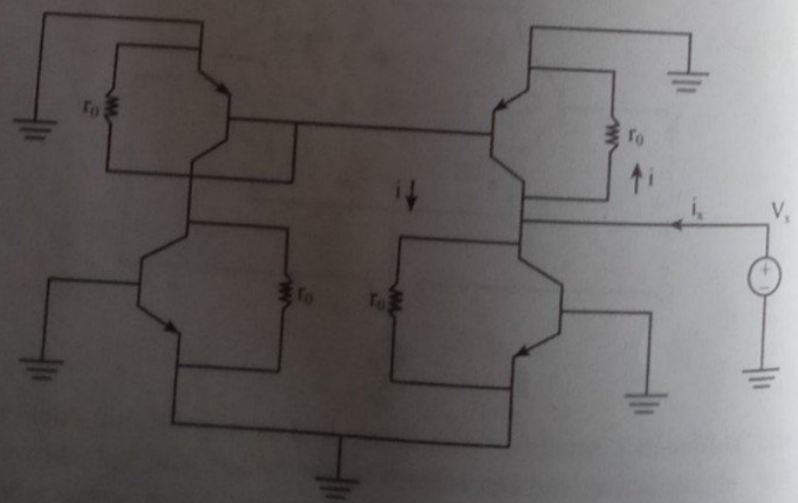
Also, due to current mirror configuration, the current signal $\frac{g_m \text{ vid}}{2}$ flows through collector of Q_4.

Now, resistance between output terminal and ground is R_0 then,

$$V_0 = \left(g_m \frac{V_{id}}{2} + g_m \frac{v_{id}}{2}\right) R_0$$

$$= g_m V_{id} R_0$$

To find R_0,



$$V_0 = g_m V_{id} \frac{r_0}{2}$$

So, Voltage gain $= \frac{V_0}{V_{id}} = \frac{g_m r_0}{2}$ ..... (i)

Substituting $g_m = \frac{I_C}{V_t}$, $r_0 = \frac{V_A}{I_C}$

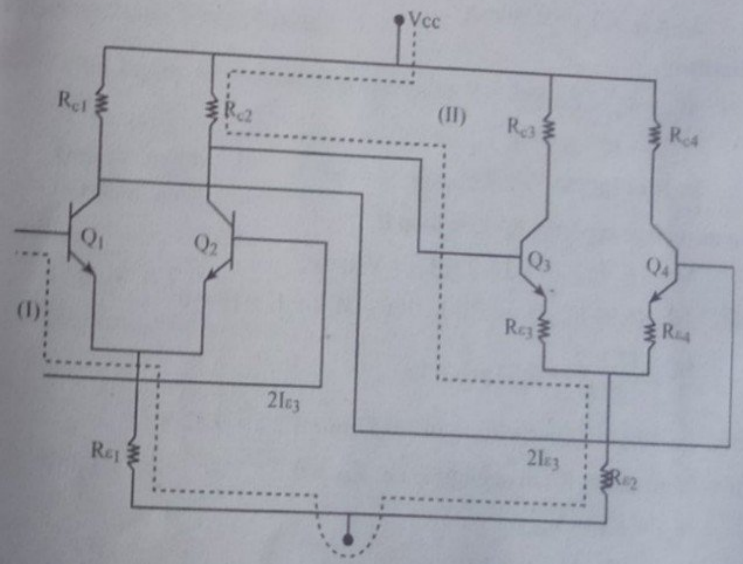
$$g_m r_0 = \frac{V_A}{V_t} = \text{constant for given transistor.}$$

Typically V_A= 100 V, leading to $g_m r_0$ = 4000 and a stage voltage a gain of about 2000. Without the current mirror the voltage gain would be half the value found above.

If passive load is used, $V_0 = g_m \frac{V_{id}}{2} R_0$

So, voltage gain $= \frac{V_0}{V_{id}} = \frac{g_m r_0}{4}$ ..... (ii)

Cascaded Differential Amplifier



The output of first section differential amplifier is fed to the section (Which is also differential amplifier) which provides the best common mode rejection and differential voltage gain.

Consider the following value of the differential resistor used.

$R_{c1} = R_{c2} = 2.2k, V_{cc} = 10$ V

$R_{c3} = R_4 = 1.2k$

$R_{E3} = R_{E4} = 100\Omega$

$R_{E1} = 4.7$ k

$R_{E2} = 15$ k

From DC analysis

Applying KVL in loop (I)

$$0 - V_{BE1} - 2\, I_{E1} R_{E1} + V_{EE} = 0$$

$$I_{E1} = \frac{V_{EE} - V_{BE}}{2R_{E1}}$$

$$= \frac{10 - 0.7}{2 \times 4700}$$

$$= 0.99 \text{ mA}$$

$$I_{c1} \approx I_{E1} \approx I_{c2} = 0.99 \text{ mA}$$

Similarly,

$$V_{c1} = V_{cc} - I_{c1} R_{c1}$$

$$= 10 - 0.99 \text{ m} \times 2.2 \text{ k}$$

$$= 7.82 \text{ V}$$

In next stage applying KVL in loop II,

$$V_{cc} - I_{c2} R_{c2} - V_{BE3} - 2\, I_3 R_{E2} + V_{EE} = 0$$

or, $10 - (0.99 \times 2.2) - 0.7 - I_E . 100 - 30 \text{ k} + I_3 + 10 = 0$

$$\frac{I_B}{3} = \frac{17.122}{30.1} = 0.57 \text{ mA} = I_{c3}$$

So, $V_{c4} = V_3 = V_{cc} - I_{c3} R_{c3} = 10 - 0.57 \text{ m} \times 1.2 \text{ k} = 9.32$ V

If voltage across R_{in} in negligible i.e. $V_{B1} \approx 0$,

$$V_{E1} = V_{B1} - V_{BE1}$$

$$= 0 - V_{BE} = 0.7 \text{ V}$$

Now,

$$V_{cE1} = V_{cE2} = V_{c1} - V_{E1} = (7.82 - (-0.7)) \text{ V}$$

$$= 8.52 \text{ V}$$

$$V_{cE3} = V_{cE4} = V_{c4} - V_{E4}$$

$$= V_{c4} - (V_{B4} - V_{BE4})$$

$$= V_{c4} - (7.84 - 0.7)$$

$$= 9.32 - 7.12$$

$$= 2.2 \text{ V}$$

Voltage at emitter of Q_1 and Q_2 at first stage is 0.7 V out of Q_3 and Q_4 of 2 V. Stage is 7.12 V.

Thus the increase in emitter voltage of second stage and in turn change in Q – point are due to cascading of differential amplifier.

1.5 Output Stage

The purpose of the output stage is to provide the amplifier with a low output resistance. In addition, the output stage should be able to supply relatively large load current without dissipating a large amount of power in the IC.

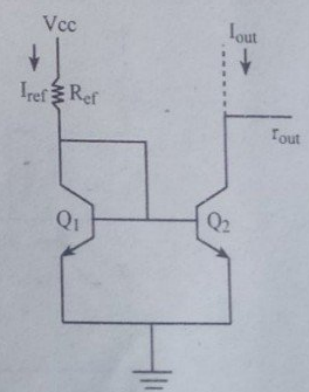
Numerical Problems

1. **Find Ic_2 for the following given value B = 200, $V_{CC} = 5$ V, $R_f = 5$ kΩ.**

   Determine the value of B_{min} and B_{max} which result change in I_{c2} to be no longer then 1%.

Solution:

I^st part



Neglecting the effect of ro

$$I_{c2} = \frac{1}{1 + 2/B} I_{ref}$$

But, $I_{ref} = \dfrac{V_{cc} - V_{BE1}}{R_{ref}}$

$$\therefore \quad I_{c2} = \frac{1}{1 + 2/B}\left(\frac{V_{cc} - V_{BE1}}{R_{ref}}\right)$$

$$= \frac{200}{202}\left(\frac{5 - 0.7}{5 \text{ k}}\right)$$

$$= 0.85 \text{ mA5}$$

IInd part

Collector current can change by 1%

$$I_{c2}^{1} = I_{c2} \pm I_{c2} * 1\%$$

$$= 0.8585 \text{ mA}$$

or, 0.8415 mA.

For B_{max}, $0.8585 \text{ m} = \frac{1}{1 + 2/B_{max}} \left(\frac{5 - 0.7}{5 \text{ k}}\right)$

$\therefore$ $B_{max} = 1143$

Similarly,

$B_{min} = 91$

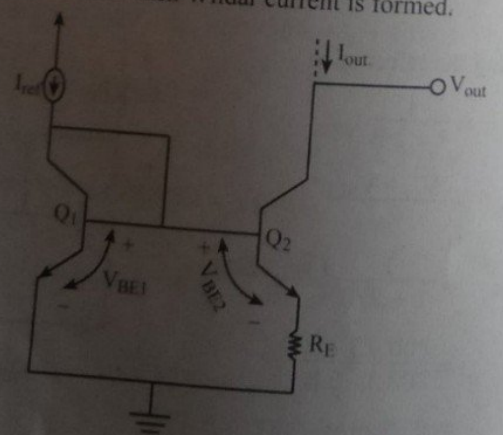
Old Questions with Solution

1. What are the benefits of widlar current source as compared to simple current source? Derive an expression for an output resistance of wildlar current source.

[2074 Ashwin, 2074 Chaitra, 2073 Sharwan, 2073 Chaitra, 2072 Kartik, 2071 Sharwan, 2070 Chaitra]

A wildar current source is a modification of the basic two transistor current mirror that incorporates an emitter degeneration resistor for only the output transistor, enabling the current source to generate low current using only moderate resistor value.

In simple terms when R_E is introduced in emitter terminal of Q_2 is basic current mirror then Wildar current is formed.



Let us suppose two transistor Q_1 and Q_2 are used and base current one negligible then.

$$V_{BE1} = V_T \ln\left(\frac{I_{ref}}{I_s}\right)$$

And, $V_{BE2} = V_T \ln\left(\frac{I_0}{I_s}\right)$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{ref}}{I_0}\right)$$

Again, from the circuit we have,

$V_{BE1} = V_{BE2} + I_0 R_E$ (neglecting base current)

Thus, $I_0 R_E = V_T \ln\left(\frac{I_{ref}}{I_0}\right)$

Benefits of using wildar oven simple current source

(i) Wildar current source allows generation of small constant current using relatively small resistance which results in considerable saving in chips area.

(ii) It has high output resistance due to the presence of emitter resistance, R_E.

Determination of output resistance

In order to determine the output resistance of Q_2 transistor let us replace BJT with it's π model and apply test voltage V_x to the collector.

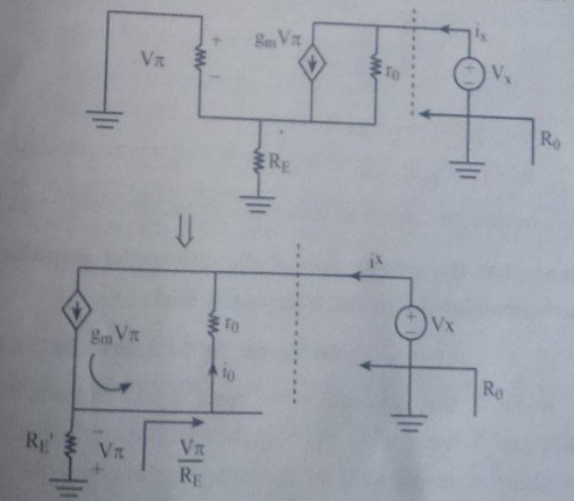


Fig : determination of output resistance of Wildars circuit source.

From the diagram,

$$R_E' = R_E // r_\pi,\ i_0 = g_m V\pi + \frac{V_T}{R_E}$$

$$= \left(g_m + \frac{1}{R_E'}\right) V\pi$$

Applying KVL,

$$V_x = -V\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi\, r_0$$

and, $ix = g_m V_\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi$

∴ The output resistance is,

$$R_0 = \frac{V_x}{ix} = \frac{-V_x - \left(g_m + \frac{1}{R_E'}\right) V\pi\, r_0}{g_m V\pi - \left(g_m + \frac{1}{R_E'}\right) V\pi}$$

$$= \frac{-1 - \left(g_m + \frac{1}{R_E'}\right) r_0}{g_m - g_m - \frac{1}{R_E'}}$$

$$= R_E' + R_E' \left(g_m + \frac{1}{R_E'}\right) r_0$$

$$= R_E' + (1 + g_m R_E')\, r_0$$

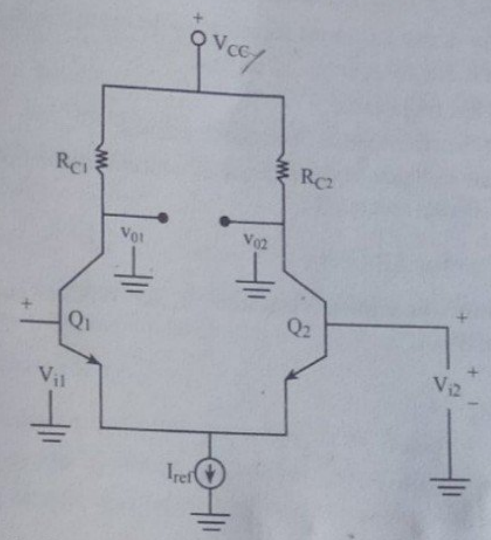
$$R_0 \approx (1 + g_m R_E')\, r_0$$

As a result, output resistance is increased by the factor of $(1 + g_m R_E')$

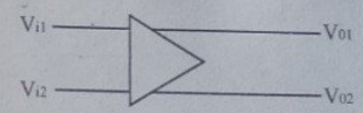
2. Show that the voltage gain of the differential amplifier with active load is twice to that with passive load.

[2078 Kartik, 2077 Chaitra, 2072 Chaitra]

It is circuit that can accept two input signal and amplify. The difference between these input signals. The output of an differential amplifier is proportional to the difference between the two i/p voltage.



Symbolically,



Here , input signal can be applied by two ways.

(a) Signal is applied to any one of the transistor and other input is grounded-single ended input arrangement.

(b) Signal are applied to both the input of DA-double ended input arrangement.

Also output can be taken in two ways

(a) Output signal is taken from any one of the output terminal and other output is grounded single ended output arrangement.

(b) Output signal is taken between two output terminal between the collector of Q_1 and Q_2 double ended input arrangement.

3. Why output current of simple minor circuit is not exactly equal to reference current? [2072 Kartik, 2071 Chaitra, 2069 Chaitra]

The output current of simple mirror circuit is given by,

$$I_0 = \frac{1}{1 + 2/\beta} I_{ref}$$

This shows that I_{out} varies according to the change in β.

I_{out} is not exactly equal to I_{ref} because.

(a) β has finite value

(b) Q_2 has finite value of output resistance

(c) Due to linear of dependence of collector current of Q_2 (I_{out}) collector voltage Q_2

$$I_{c2} = \left(\frac{1}{R}\right) V_{c2}$$

4. Determine the emitter resistance R_e for Wildars current whic applies 10 μA.

Solution:

Here, $R_E = ?$

$I_{ref} = 10$ mA

$I_0 = 10$ μA

We have,

$$I_0 R_E = V_T \ln\left(\frac{I_{ref}}{I_0}\right)$$

$$10 \times 10^{-6} \times R_E = 25 \times 10^{-3} \ln\left(\frac{10^{-3}}{10 \times 10^{6}}\right)$$

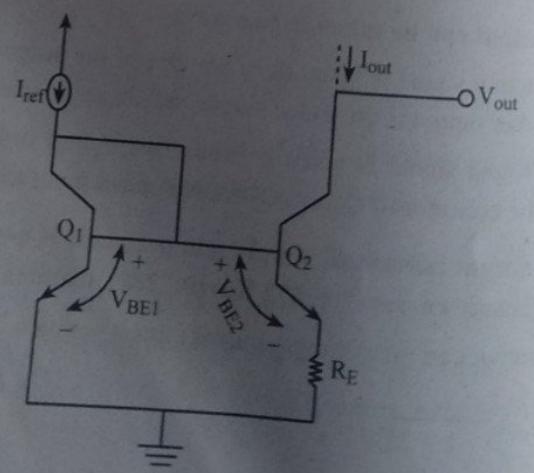
$$R_E = 11.512\Omega$$

5. What are the benefits of Widlar current source as compared t simple current source? Derive an expression for an outpu resistance of Widlar Current Source. **[2075 Ashwin**

Solution:

Part I: Refer to Theory

Part II:



This emitter resistor effectively reduces the current across the Q_2 compared with the Q_1. This is done by the voltage drop across this resistor, this voltage drop reduces the base-emitter voltage of the output transistor which further results in reduced collector current across the Q_2.

6. Draw clearly the differential amplifier with active load. Show that its voltage gain is doubled in compare to the differential amplifier with passive load (R_c). **[2075 Chaitra]**

Solution: Refer to theory

7. Why are current mirrors important in IC design? Describe how it is possible to obtain an output current that is twice the amount of reference current by using a current mirror circuit?

[2076 Ashwin]

Solution:

Part I: A Bias circuit is a portion of the device circuit which supplies the steady current or voltage Bias circuit are used to Bias discrete BJT because it is not suitable as they need large number of resistor as well as large coupling and by pass capacitor. With the current technology it is almost impossible to fabricate large capacitor and it is uneconomical to manufactory large resistance. It is based on constant current source.

On an IC chip with number of amplifier stage. A constant dc current is generated at one location and then if it reproduced at various other location. Major advantage of this approach is Bias current of various track each other in case at change in power supple voltage or temperature.

Constant current source is characterized by:

- Very high output resistance
- Very high voltage resistance

Part II: Refer to theory

8. Explain the operation of current steering circuit with necessar circuit diagram and its application. What are the advantages amplifier using active load than using passive load in IC?

[2078 Kartik

Solution:

Part I: Refer to theory part

Part II: This circuit is mainly applicable in integrated circu design, where one resistor R is used to make multiple curre sources. In other words, if each transistor is identical to, then eac current will equal reference current

Part III: BJT Differential Amplifier with active load is use because Amplifier that ultilize active load can achieve highe voltage gain that those with passive loads for Active loads. BJT as mirror current source is used which has very high output resistance.

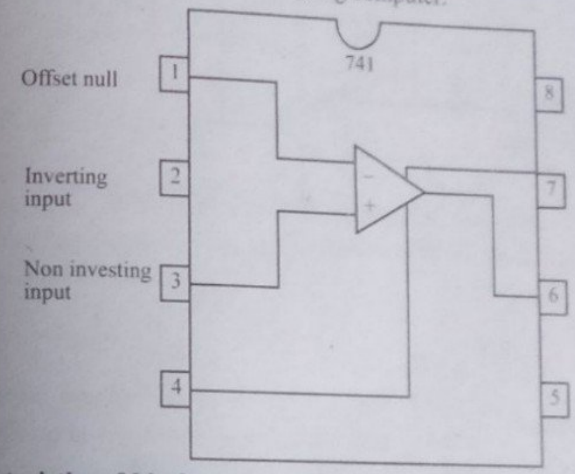
❖❖❖

Chapter 2

Operational Amplifier Characterization

Op-Amp characteristics

An op-amp is a high gain direct-coupled amplifier which is often powered by both a positive and a negative supply voltage. The name operational amplifier is derived from one of the original uses of op-amp circuit to perform mathematical operation in analog computer.



Characteristics of Ideal op-amp and typical op-amp.

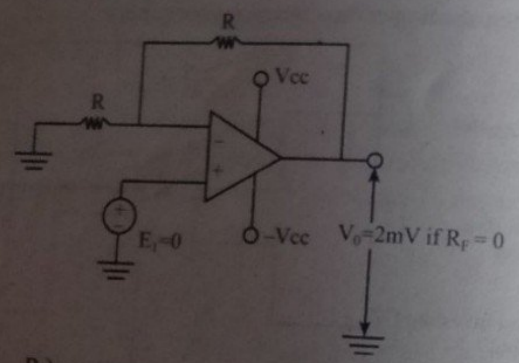
Parameter	Ideal op-amp	Typical op-amp
1. Input Impedance (Z_{in})	∞	2MΩ
2. Output Impedance (z_{out})	0	75Ω
3. Open loop voltage gain (A_{0l})	∞	10^5
4. Band width (B)	∞	1MHz
5. Slew rate (S.R)	∞	0.7V/μs
6. CMRR	∞	100dB
7. Input offset voltage (V_{io})	0	2mA
8. Input offset current (I_0)	0	20nA
9. Virtual short between input terminal	Yes	No

2.1 Input Offset Voltage

When the input voltage to an ideal op-amp is zero, the o/p is zero. This is not true for an actual op-amp. The input offset voltage is defined as the input voltage required to make an o/p voltage equal to zero.

It can be negative or positive with typical magnitude of ± 2mV. This offset voltage is caused by the mismatched input stages.

The output voltage produced when the zero input voltage is applied is called output offset voltage.

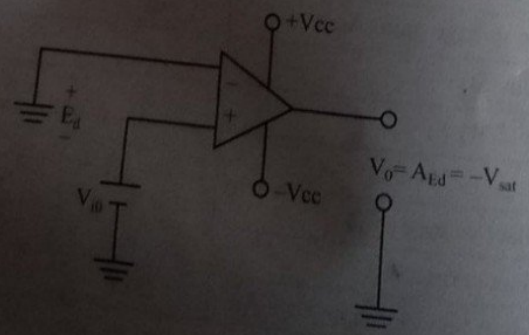


$$V_0 = \left(1 + \frac{R_f}{R}\right) \varepsilon_i = V_{i0}$$

Thinks to know:

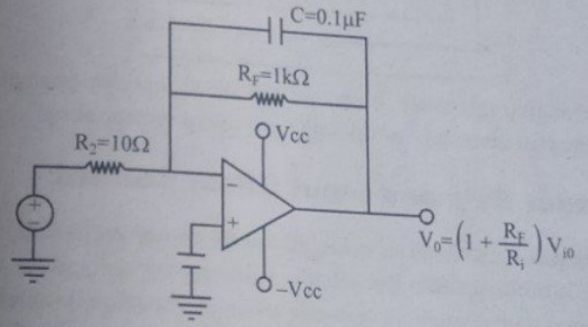
- Effect of input offset voltage on output voltage.
- Measurement of input offset voltage
- Method of reducing effect of input offset voltage

2.1.1 Effect of input offset voltage on output



In figure input offset voltage V_{i0} and large value of open-loop voltage gain of op-amp combinely act to drive output voltage V_0 to the negative saturation.

The magnitude and polarities of V_{i0} varies from op-amp to op-amp So, negative V_{i0} here act to drive the V_0 to V_{sat} may act to drive V_{sat} in other op-amp.



The circuit describe the method to predict the magnitude of error in output voltage caused by the input offset voltage V_{i0} since V_{i0} is applied to non-inverting input.

$$V_0 = V_{i0}\left(1 + \frac{R_f}{R_i}\right)$$

V_{i0} is the reason behind this voltage error. Since, ε_1 = OV so the V_0 should also be OV but in instead actual case $V_0 \neq 0$

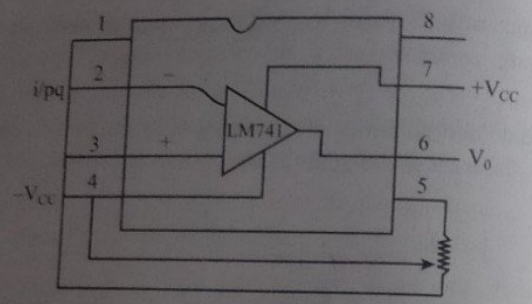
$$V_0 = V_{i0}\left(1 + \frac{R_f}{R_1}\right)$$

$$\therefore V_{i0} = \frac{V_0}{\left(1 + \frac{R_f}{R_1}\right)}$$

Here, The capacitor C is used to minimize the poise in V_0 and R_f is used with small value to minimize the effect of bias current.

2.1.2 Method of reducing effect of input offset voltage

A non-zero value of V_{i0} is undesirable, since the op-amp amplify any input offset which causes large dc output error. So, to reduce the effect of V_{i0} in LM741 a variable resistor is used as follow:



Here by changing resistance, it counter acts the asymmetry present in the input differential amp stage of op-amp making o/p voltage zero.

2.2 Input Bais and Input Offset Current

If the op-amp is Ideal then it is assumed that the no current is flowing into the terminals of the op-amp But actually when biasing voltage are applied to the op-amp then a small amount of current used to flow through these terminal and these current are known as the input bias current of the op-amp. Also it is defined as the average value of input bias current following in the two terminals of the op-amp (inverting and non-inverting terminal).

Mathematically,

$$I_{bais} = \frac{I_{B1} + I_{B2}}{2}$$

Where,

$I_{B1} \rightarrow$ bais current at transistor 1

$I_{B2} \rightarrow$ bais current at transistor 2

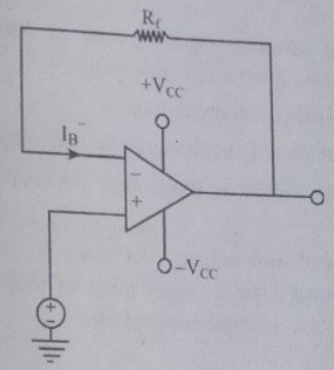
Ideally both bias current (I_{B1} and I_{B2}) should be identical but in practically because of slight mismatch between two transistor of the differential amplifiers. These current are slightly different and the difference between the two input bias current is defined as the input offset current.

Mathematically

$$I_{i0} = (I_{B1} - I_{B2})$$

Typically, it's value is in few nano ammeter. Being very small current it's effect is negligible in most application but, the application where a very precise output is required at that time input bais current and voltage becomes a critical parameter.

2.2.1 Effect of input bais current

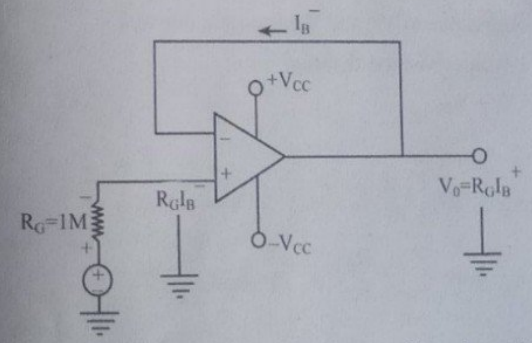


Let us assume the input offset voltage is zero for the op-amp as shown in figure. If the zero input voltage is supplied. Output voltage along with differential input voltage must be zero.

But I_B^- current flows as inverting input bias current as shown in figure so V_0 must rise to supply the voltage drop across R_f. Thus the voltage error due to I_B^- is,

$$V_0 = I_B^- \times R_f$$

Effect of (+) input bias current



This case is also similar to (–) input bias current, Here Input bias current is assumed to be zero as a result of the input voltage and differential input voltage becomes zero.

Ideally, the output voltage should also be zero volt but due to the current I_B^+ which follows through internal resistance of signal generator modeled as R_G, output is affected.

The voltage across non-inverting input = $R_G I_s^+$ with polarity as shown in figure.

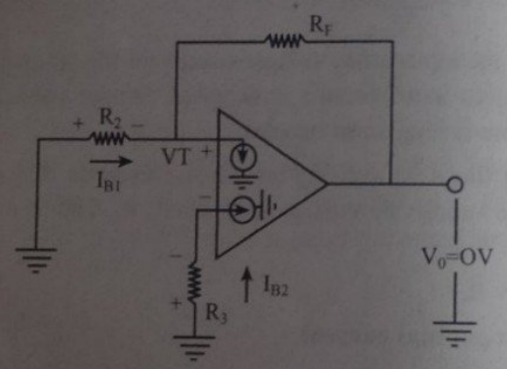
The voltage across inverting input = $R_G I_B^+$ = Voltage across non-inverting input (because differential input = 0)

Since, there is no resistor in feedback loop

So, $V_0 = -R_G I_B^+$ with polarity as shown in the above figure.

Method of reducing effect of input bias current and input offset voltage.

This method consist of introducing a resistance R_3 in series with non-inverting input terminal from a signal point of view has a negligible effect. The value of R_3 is determined as follow:



Let V_{01} is output due to V^- and V_{02} is output due to V^+

So, Applying superposition theorem,

$$V_0 = V_{01} + V_{02}$$

Here,

$$V_{01} = (-I_{B1}R_1)\left[\frac{-R_f}{R_1}\right] \qquad [\because V^- = -I_{B1}R_1]$$

$$V_{02} = (-I_{B2}R_3)\left[1 + \frac{R_f}{R_1}\right] \quad V^+ = -I_{B2}R_3$$

So,

$$V_0 = -I_{B2}\frac{R_3}{R_1}(R_1 + R_f) + I_{B1}R_f$$

Let $I_{B1} = I_{B2} = I_B$ then,

$$V_0 = -I_B\frac{R_3}{R_1}(R_1 + R_f) + I_B R_f$$

For the best output $V_0 = 0$

$$-I_B\frac{R_3}{R_1}(R_1 + R_f) + I_B R_f = 0$$

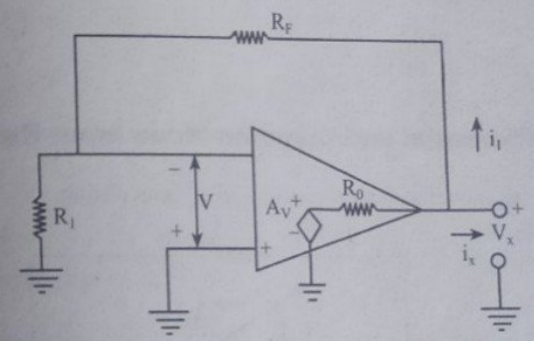
or, $R_1R_3 + R_F R_3 = R_1R_f$

$$R_3 = \frac{R_1R_f}{R_1 + R_f} = R_1//R_f$$

Which is required expression

2.3 Output Impedance

For the output impedance R_{out} the test voltage V_x is applied at output.



Here,

$$ix = i_1 + i_z$$

Also,

$$i_1 = \frac{V_x - o}{R_1 + R_f} \quad \ldots\ldots (i)$$

$$i_2 = \frac{V_x - AV}{R_0} \quad \ldots\ldots (ii)$$

We know that,

$$V_x = -\left(1 + \frac{R_f}{R_1}\right)V$$

$$\therefore \quad V = -\left(\frac{R_1 + R_f}{R_1}\right)V_x = -\beta V_x$$

From equation (ii)

$$i_2 = \frac{V_x + A\beta V_x}{R_0} = \frac{V_x(1 + A\beta)}{R_0}$$

Thus,

$$i_x = \frac{V_x}{R_1 + R_f} + \frac{V_x(1 + A\beta)}{R_0}$$

$$\frac{i_x}{V_x} = \frac{1}{R_1 + R_f} + \frac{(1 + A\beta)}{R_0}$$

or, $$\frac{1}{R_{out}} = \frac{1}{R_1 + R_f} + \frac{1}{R_0/(1 + A\beta)}$$

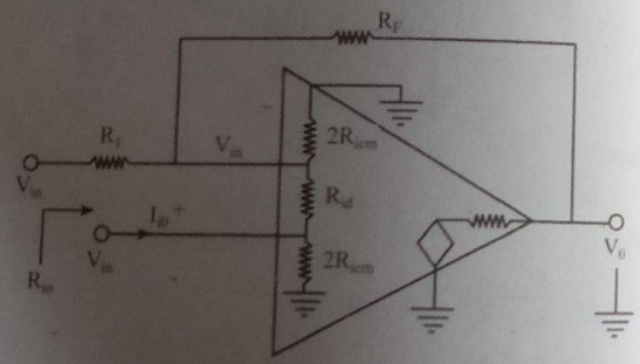
$$\therefore \quad R_{out} = (R_1 + R_f)//R_0/(1 + A\beta)$$

$$\approx \frac{R_0}{(1 + A\beta)} \qquad [\because R_0 \ll (R_1 + R_2)]$$

$$\therefore \quad R_{out} = \frac{R_0}{(1 + A\beta)}$$

2.4 Differential and Common Mode Input Resistance

Input resistance of closed loop configured op-amp circuit.



Here, $R_{icm} \rightarrow$ common mote input resistance

$R_{id} \rightarrow$ differential mode input resistance

Example; Equivalent circuit for studing R_{in}

Let us assume the output resistance of op-amp four determining the input resistance of closed loop configured op-amp.

There are two cases

(a) When op-amp is acting as inverting amplifier

b) When op-amp acts as non-inverting amplifier

(a) As inverting amplifier

Let the current flowing at input of op-amp be In.

$$I_{in} = \frac{V^- - V_0}{R_f} + \frac{V^-}{R_{id}} \qquad (\because V_0 = AV_{id})$$

$$= \frac{V^- + AV^-}{R_f} + \frac{V^-}{R_{id}} \qquad (\because V_{id} = -V)$$

$$= \left(\frac{1 + A}{R_f} + \frac{1}{R_{id}}\right) V^-$$

$$= \left(\frac{1 + A}{R_f}\right) V^- \qquad (\because R_{id} \gg 1; \text{ normally range of } M\Omega)$$

$$\therefore \quad \text{Input resistance } R_{in} = R_1 + \frac{V^-}{in}$$

$$= R_1 + \frac{R_f}{1 + A}$$

$$= R_1$$

Also from figure,

$$R_{in} = R_1 || R_{id} || 2R_{icm} = R_i$$

(b) non-inverting amplifier

Here, $V_0 = \left(1 + \frac{R_f}{R_1}\right) V^+$

$$V^+ = \left(\frac{R_1}{R_1 + R_f}\right) V_0 = \beta V_0$$

And

$$V_{in} = V_{id} + V^+$$

or, $$V_{in} = V_{id} + \beta V_0$$

$$V_{in} = V_{id} + \beta . A V_{id} \qquad (\because V_0 = A V_{id})$$

Dividing both sides by I_{in}, we get.

$$\frac{V_{in}}{I_{in}} = \frac{V_{id}}{I_{in}} + A\beta \frac{V_{id}}{I_{in}}$$

$$R_{in} = \frac{V_{id}}{id} (1 + A\beta)$$

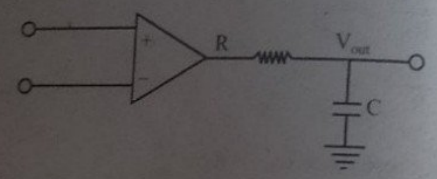
$$= R_{id} (1 + A\beta)$$

If effect of R_{icm} is also included

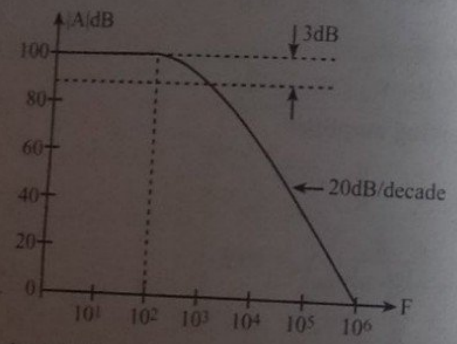
$$R_{in}' = R_{in}//2R_{icm}$$

2.5 DC Gain, Bandwidth, Bandwidth Product

(a) DC Gain and Bandwidth: Differential open loop gain of op-amp is finite and decreases with the increase in frequency. However the network (low pass circuit) within a op-amp is responsible for the role off in gain as frequency increase.



Despite of low frequencies and high gain at DC it starts to fall off at higher frequencies. In order to internally compensated op-amp. The gain decreases uniformly with-20dB/decade as shown in figure,



To insure the stability of op-amp circuit open loop gain is modified by the process called frequency compensation. It is implemented by, modifying the gain and phase characteristics of the amplifiers open loop output or it's feedback network or both in such a way as to avoid the condition leading to oscillation.

(b) Open loop bandwidth: The frequency range between the point where the gain is 3d less than mid-range gain is called bandwidth of an amplifier.

$B|\alpha| = f_{CH} - f_{CL}$

Op-amp, $f_{CL} = OH_z$

$B|\alpha| = f_{CH}$

(c) Unit gain bandwidth: The unit bandwidth of an amplifier is simply the frequency of an input signal at which the open loop gain is equal to 1.Note that open-loop gain is measured maximum gain of the amplifier when no components are present in the feedback loop gain value ranges on the order of 100,000 and above at DC for a typical op-amp it is $10^6 H_z = 1MH_z$.

(d) Gain bandwidth product: Relation between closed loop gain and in bandwidth is inversely proportional so. An increase in closed bop gain causes decrease in bandwidth and vice versa such that product between them remain constant. This is true as long as role off rate is fired.

Let $A_{CC} \rightarrow$ Closed loop gain

$f_C \rightarrow$ Closed loop critical frequency

$A_{OL} \rightarrow$ Open loop gain

fc (OL) $\rightarrow$ Open loop critical frequency

Then,

$A_{CL} f_C (CL) = A_{OL} f_C (OL) =$ Unity gain bandwidth.

The gain bandwidth product of the op-amp is always equal to the frequency at which the op-amp open loop gain is unity.

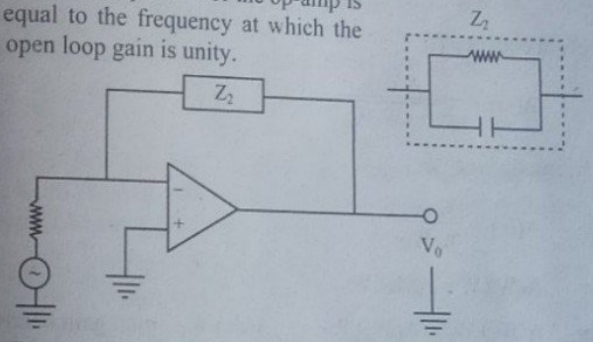


Fig: inter ting amplifier ckt for studying GBP.

From figure,

$$Z_2 = \frac{R_2 X_c}{\sqrt{R_2^2 + X_c^2}} = \frac{R_z}{\sqrt{(1 + R_2/X_c)^2}} = \frac{R_2}{\sqrt{1 + (R_2 wc)^2}}$$

For inverting amplifier voltage gain at any frequency W is,

$$A(w) = \frac{-Z_2}{R_1}$$

$$\therefore \quad A(w) = \frac{-R_2/R_1}{\sqrt{1 + (R_2 wc)^2}} \qquad \text{..... (i)}$$

For dc, w = 0

$$A(dc) = \frac{-R_2}{R_1} \quad \text{..... (ii)}$$

At cut-off frequency W_C

$$A(W_C) = \frac{A_{dc}}{\sqrt{2}} \quad (\because W_C \text{ is frequency where gain is 0.707 of dc gain})$$

Also,

$$A(W_C) = \frac{-R_2/R_1}{\sqrt{(1 + W_C R_{2C})^2}}$$

$$\frac{-R_2/R_1}{\sqrt{(1 + W_C R_{2C})^2}} = \frac{-R_2}{R_1\sqrt{2}}$$

or, $\sqrt{1 + (W_C R_2 c)^2} = \sqrt{2}$

or, $1 + (W_C R_2 c)^2 = 2$

$$w_c = \frac{1}{R_2 c} \quad \text{..... (iii)}$$

From equation (i),

$$A(w) = \frac{A(dc)}{\sqrt{1 + (W/W_C)^2}}$$

Normally $w/w_c \gg 1$,

$$\therefore \quad A(w) = \frac{A(dc)}{W/W_C}$$

$$\therefore \quad A(W).W = A(dc).W_C$$

or, $A/W_1).W_1 = A(W_2).W_2 = \ldots A(dc).W_C$ = unit gain bandwidth

Here,

$A(W).W = A_1(W_1).W_1 = A_2(W_2).W_2$ = finite and constant

i.e. $A(W).W$ = constant

Gain × bandwidth = constant

∴ GBP = constant

∴ Gain bandwidth product is constant.

2.6 Common Mode and Power Supply Rejection Ratio

Common Mode Rejection Ratio (CMRR)

If the same input voltage is applied to the both terminal of an op-amp. The op-amp is said to be operating in a common mode configuration and voltage is known as common mode voltage.

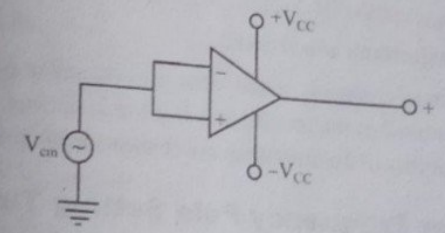


Fig: Common mode configuration of op-amp

The output voltage of op-amp in common mode configuration V_{0cm} should be zero because an op-amp amplifies only the differential input voltage is zero so, V_{ocm} should be zero. However there will be some voltage at output so, the common mode voltage gain can be defined as ratio of output common mode voltage V_{ocm} to input mode voltage.

$$\text{i.e. } A_{cm} = \frac{V_{ocm}}{V_{cm}}$$

If there is a perfect matching between two input terminal the value of A_{cm} will be zero so, to measure the degree of matching between two input terminal the term CMRR is defined as .

$$CMRR = \frac{Ad}{A_{cm}} = \frac{\text{differential mode gain}}{\text{common mode gain}}$$

$$\text{In dB, } CMRR = 20 \log\left(\frac{Ad}{A_{cm}}\right)$$

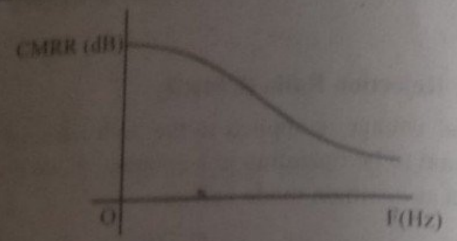
CMRR is also expressed as the ratio of change in offset voltage to total change in common mode voltage.

$$\text{i.e. } CMRR = \frac{V_{i0}}{V_{cm}}$$

$$\text{In dB, } CMRR = 20 \log\left(\frac{V_{i0}}{V_{cm}}\right)$$

Matching between two terminal α value of CMRR so it the matching between two terminal is more, value of CMRR will be high.

CMRR is the function and decrease as frequency increases.



Power supply rejection ratio (PSRR)

PSRR is the ratio of change is output voltage to change in power voltage. It is usually expressed in microvolt per voltage or in decibel. Also it is the measure of the ability of op-amp to ignore change supply voltage.

2.7 Higher Frequency Pole Setting Time

Setting time is the time elapsed from the application of an ideal instantaneous step input to the time at which the closed loop amplifier output has entered and remained within a specified error band usually symmetrical about the final value.

Setting time includes a very brief propagation delay plus the time required for the output to slew to riclmty of the final value recover from the over load condition associated with slewing and finally settle to within the specified error.

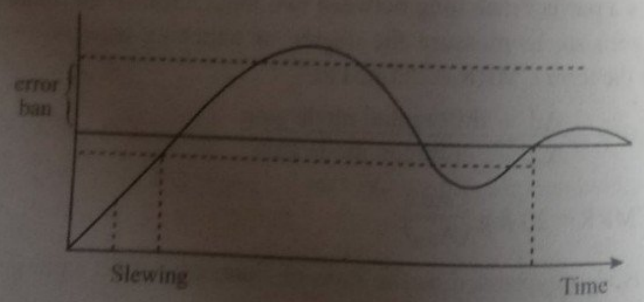


Fig: Illustration of setting time

2.8 Slew Rate

When the op-amp is driven by a step or pulse type signal to track the input signal by o/p signal the capacitor must charge and discharge rapidly. This lead to limit on the rate at which the o/p voltage change.

The maximum possible rate at which an amplifier output voltage can change is called slew rate it is measured in volts per microsecond (V/μsec)

For very high frequency input signal the resulting output is delayed As a result.

(a) input sine wave turn into triangular wave at output

(b) Input square wave turns into trapezoidal wave at output.

Mathematically,

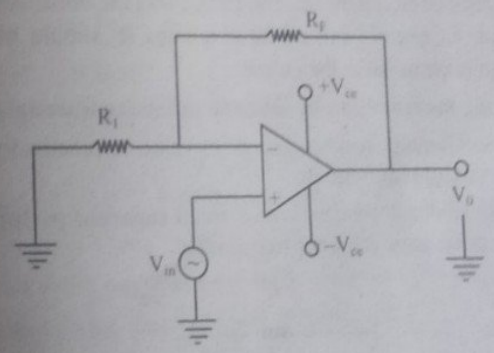
$$\text{Slew rate} = \frac{dV_0}{dt}\Big|_{max}$$

Consider a circuit as shown in figure

Let $V_{in} = V_m \sin 2\pi ft$

$$\text{Gain (A)} = 1 + \frac{R_f}{R_1}$$

and $V_0 = AV_m \sin 2\pi ft$



$$SR = \frac{dV_0}{dt}\Big|_{max}$$

$$= \frac{d}{dt}[AV_m \sin 2\pi ft]_{max}$$

$$= AV_m\, 2\pi f \cos 2\pi ft\,|_{max}$$

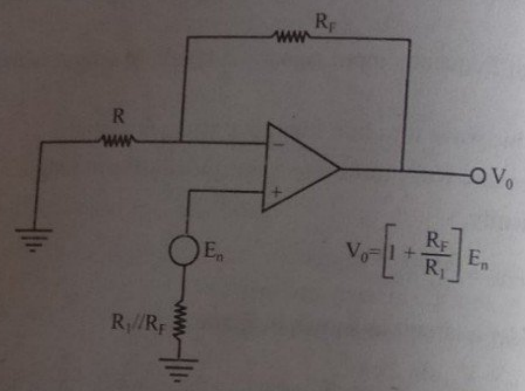
$$= AV_m.\, 2\pi\,.\,f\,.\,|$$

$$\therefore \quad SR = AV_m\, 2\pi f$$

2.9 Noise in Operational Amplifier Circuit

Electronics circuit are susceptible to noise and op-amp is not exception. Apart from extend noise op-amp has internal noise source like bias

current, drift and internal components noise is also amplified by op-amp just as offset voltage and signal voltage.

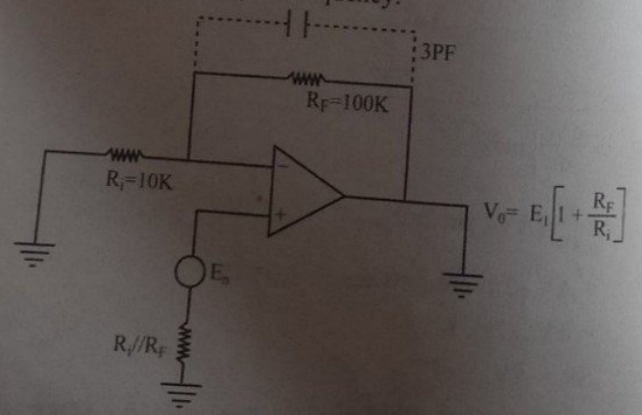


This internal op-amp noise is modeled most simply by a voltage source E_n. E_n is placed in series with non-inverting (+) input. The 741 op-amp has 2μV of noise over a frequency of 10 kH_z. This noise voltage is valid for source resistor (R_1) between 100 Ω to 20kΩ the noise voltage goes up directly with R_1 one R_1 exceed 20 kΩ. Thus R_1 should be kept below 20kΩ to minimize noise in the output.

The following measure can be taken to minimize internal noise.

(a) Keep series input resistor as low in value as practically possible to satisfy circuit requirements.

(b) By pass feedback resistor with a small capacitor (≈ 3pf) which will reduce noise gain at higher frequency.



c) Never connect a capacitor across the input resistor or from (–) input to ground. There will always be a few PF. of stray capacitance from (–) input to ground due to wiring.

Numerical Problems

1. **The inverting input configuration has a feedback resistance of 470k and on input resistance of 10k. If the input signal is V_{in}= 0.1 sin (200000 t). Determine when there the output will be distorted due to slew rate limitation of op-amp. If so, find remedy the op-amp has a slew rate of 0.5 V/μs.**

[2073 Sharwn, 2073 Chaitra, 2069 Chaitra]

Solution:

$R_f = 470k$

$R_{in} = 10k$

$A = \frac{-R_f}{R_{in}} = -47$

and $|A| = 47$

$V_{in} = 0.1 \sin(200000\ t)$ hence $V_m = 0.1$

∴ $V_{out} = 47 \times 0.1 \sin(200000\ t)$

$SR = 0.5\ V/\mu s$

Now, $2\pi f = 200000$

So, S.R will be S.R' $= V_m\, 2\pi f A$

$= 0.1 \times 200000 \times 4.7$ V/s

$= 0.94 \times 10^6$ V/s

$= 0.94$ V/μs

Here, SR < SR' So, signal will be distorted so remedies are.

(a) Use op-amp with slew rate ≥ 0.94 V/μs

(b) Reduce op-amp gain such that

$S.R = 0.5\ V/\mu s \geq 2\pi f\, V_m\, A'$ $A' \leq 25$

Old Questions with Solution

1. **Explain slew rate of an operational amplifier. An inverting configuration op-amp feedback resistor 470 kΩ and output resistor 10 kΩ. If input signal is 0.1 sin (200000 t). determine when there the output will be distorted due to slew rate limiting of op-amp. Find remedy. The op-amp has slew rate of 0.5 V/μs.**

[2074 Chitra, 2073 Chaitra, 2073 Shrawan, 2070 Chaitra, 2068 Chaitra]

Solution:

The maximum possible rate at which an amplifier output voltage change is called slew rate. It is measured in volt per microseconds.

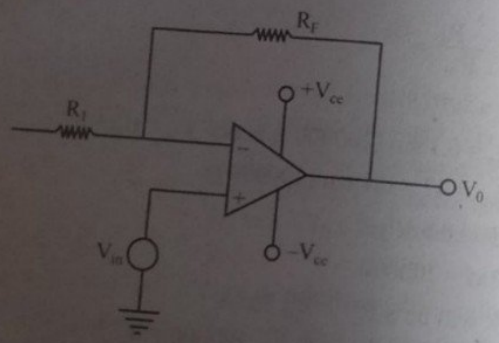
Mathematically,

$$\text{Slew rate} = \frac{dV_0}{dt}\Big|_{min}$$

Consider a circuit as shown in fig

Let $V_{in} = V_m \sin 2\pi ft$

$$\text{Gain} = \frac{R_f}{R_1}$$



And,

$$V_0 = A\, V_m \sin 2\pi ft$$

$$\therefore \quad SR = \frac{dV_0}{dt}\Big|_{max}$$

$$= \frac{d}{dt}\,[A\, V_m \sin 2\pi ft]\Big|_{max}$$

$$= A\, V_m \cdot 2\pi f \cos 2\pi ft\Big|_{max}$$

$$= A\, V_m \cdot 2\pi f \cdot 1$$

$$\therefore \quad SR = A\, V_m \cdot 2\pi f$$

$R_f = 470\ k$

$R_{in} = 10\ k$

$$A = \frac{-R_f}{R_{in}} = -47$$

$$\therefore \quad |A| = 47$$

$V_{in} = 0.1 \sin (200000\ t)$

$V_m = 0.1\ V$

$$\therefore \quad V_{out} = 47 \times 0.1 \sin (200000\ t)$$

$$= 4.7 \sin (200000\ t)$$

$SR = 0.5\ V/\mu s$

Now, $2\pi f = 200000$

So, SR will be $S.R' = V_m\, 2\pi fA$

$$= 0.1 \times 200000 \times 47\ V/s$$

$$= 0.94 \times 10^6\ V/s$$

$$= 0.94\ V/\mu s$$

Here SR < SR' so signal will be distorted remedies are:

(a) Use of op-amp with slew rate $\geq 0.94\ V/\mu s$

(b) Reduce of op-amp gain such that

$$S.R = 0.5\ V/\mu s \geq 2\pi f\, V_m A'$$

$$\therefore \quad A' \leq 25$$

2. Describe relationship of gain and bandwidth of op-amp and prove gain bandwidth product is constant.

[2074 Chaitra, 2073 Shrawan, 2072 Kartik, 2071 Shrawan, 2070 Ashad]

Solution:

Relation between closed loop gain and in bandwidth is inversely proportional so. An increase in closed bop gain causes decrease in bandwidth and vice versa such that product between them remain constant. This is true as long as role off rate is fired.

Let $A_{CC} \rightarrow$ Closed loop gain

$f_C \rightarrow$ Closed loop critical frequency

$A_{OL} \rightarrow$ Open loop gain

$fc\ (OL) \rightarrow$ Open loop critical frequency

Then,

$A_{CL} f_C\ (CL) = A_{OL}\ f_C\ (OL) =$ Unity gain bandwidth.

The gain bandwidth product of the op-amp is always equal to the frequency at which the op-amp open loop gain is unity.

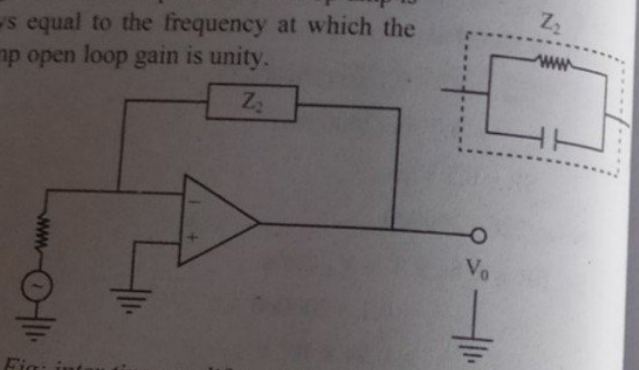


Fig: inter ting amplifier ckt for studying GBP.

From figure,

$$Z_2 = \frac{R_2 X_c}{\sqrt{R_2^2 + X_c^2}} = \frac{R_Z}{\sqrt{(1 + R_2/X_c)^2}} = \frac{R_2}{\sqrt{1 + (R_2 wc)^2}}$$

For inverting amplifier voltage gain at any frequency W is,

$$A(w) = \frac{-Z_2}{R_1}$$

$$\therefore \quad A(w) = \frac{-R_2/R_1}{\sqrt{1 + (R_2 wc)^2}} \qquad \text{..... (i)}$$

For dc, w = 0

$$A(dc) = \frac{-R_2}{R_1} \qquad \text{..... (ii)}$$

At cut-off frequency W_C

$$A(W_C) = \frac{A_{dc}}{\sqrt{2}} \quad (\because W_C \text{ is frequency where gain is 0.707 of dc gain})$$

Also,

$$A(W_C) = \frac{-R_2/R_1}{\sqrt{(1 + W_C R_{2C})^2}}$$

$$= \frac{-R_2/R_1}{\sqrt{(1 + W_C R_{2C})^2}} = \frac{-R_2}{R_1\sqrt{2}}$$

or, $\sqrt{1 + (W_C R_2 c)^2} = \sqrt{2}$

or, $1 + (W_C R_2 c)^2 = 2$

$$w_c = \frac{1}{R_2 c} \qquad \text{..... (iii)}$$

From equation (i),

$$A(w) = \frac{A(dc)}{\sqrt{1 + (W/W_C)^2}}$$

Normally $w/w_c \gg 1$,

$$\therefore \quad A(w) = \frac{A(dc)}{W/W_C}$$

$\therefore \quad A(W).W = A(dc).W_C$

or, $A/W_1).W_1 = A(W_2).W_2 = \ldots A(dc).W_C$ = unit gain bandwidth

Here, $A(W).W = A_1(W_1).W_1 = A_2(W_2).W_2$ = finite and constant

i.e. $A(W).W$ = constant

Gain × bandwidth = constant

$\therefore$ GBP = constant

$\therefore$ Gain bandwidth product is constant.

3. In a closed loop inverting configuration of an op-amp the input resistance and the feedback resistance of 1 kΩ and 33 kΩ respectively.

(a) Determine the value of V_p for an undistorted output if an input to the current in V/n = V_p sin (2πft), where f = 1 kH_z and slew rate = 0.6 V/μs.

(b) If the value of V_p is assumed to be 5 V show two possible remedies in the circuit to have an undistorted output.

[2072 Chaitra, 2071 Sharwan, 2070 Chaitra]

Solution:

Case (I)

$R_p = 33\ k\Omega$

$R_{in} = 1\ k\Omega$

$$A = \frac{-R_f}{R_{in}} = \frac{-33}{1}$$

$\therefore \quad |A| = 33$

$V_p = ?$

$F = 1\ kH_z$

$S.R = 0.6\ V/\mu s$

$S.R = V_p 2\pi f A$

$0.6 \times 10^6 = V_p \times 2.\pi \times 1 \times 10^3 \times 33$

$V_p = 2.89\ V$

Case (II)

$V_p = 5V$

Then,

$$S.R' = V_p \cdot 2\pi f.A$$
$$= 5 \times 2\pi \times 10^3 \times 33$$
$$= 1.036 \times 10^6 \text{ V/}\mu\text{s}$$
$$= 1.036 \text{ V/}\mu\text{s}$$

SR' > S.R so signal will be distorted remedies are:

(a) Use of op-amp with S.R ≥ 1.036 V/μs

(b) Reduce op-amp gain such that

$S.R = 0.5 \text{ V/}\mu\text{s} \geq 2\pi V_m f.A'$

$\therefore \quad A' \leq |5.9|$

4. What do you understand by input bias and input offset current of op-amp? What are the effects of input bias currents on output voltage? How do you reduce the effect of input bias current?

[2075 Ashwin, 2074 Chaitra, 2073 Chaitra, 2072 Chaitra, 2071 Shrawan, 2070 Chaitra, 2069 Ashad]

Solution: 1st part

If the op-amp is Ideal then it is assumed that the no current is flowing into the terminals of the op-amp But actually when biasing voltage are applied to the op-amp then a small amount of current used to flow through these terminal and these current are known as the input bias current of the op-amp. Also it is defined as the average value of input bias current following in the two terminals of the op-amp (inverting and non-inverting terminal).

Mathematically,

$$I_{bais} = \frac{I_{B1} + I_{B2}}{2}$$

Where,

$I_{B1} \rightarrow$ bais current at transistor 1

$I_{B2} \rightarrow$ bais current at transistor 2

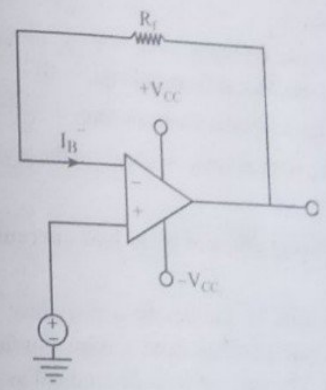
Ideally both bias current (I_{B1} and I_{B2}) should be identical but in practically because of slight mismatch between two transistor of the differential amplifiers. These current are slightly different and the difference between the two input bias current is defined as the input offset current.

Mathematically

$I_{io} = (I_{B1} - I_{B2})$

Typically, it's value is in few nano ammeter. Being very small current, it's effect is negligible in most application but, the application where a very precise output is required at that time input bais current and voltage becomes a critical parameter.

2nd part

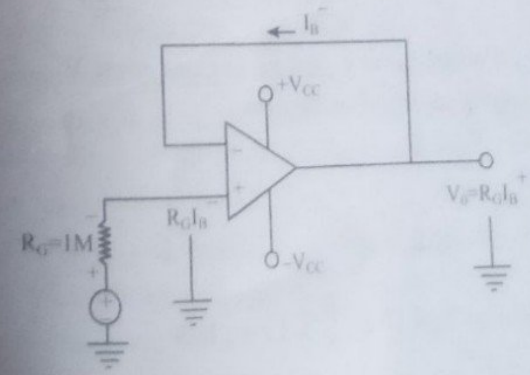


Let us assume the input offset voltage is zero for the op-amp as shown in figure. If the zero input voltage is supplied. Output voltage along with differential input voltage must be zero.

But I_B^- current flows as inverting input bias current as shown in figure so V_0 must rise to supply the voltage drop across R_f. Thus the voltage error due to I_B^- is,

$V_0 = I_B^- \times R_f$

Effect of (+) input bias current



This case is also similar to (–) input bias current, Here Input bias current is assumed to be zero as a result of the input voltage and differential input voltage becomes zero.

Ideally, the output voltage should also be zero volt but due to the current I_B^+ which follows through internal resistance of signal generator modeled as R_G, output is affected.

The voltage across non-inverting input = $R_G I_s^+$ with polarity as shown in figure.

The voltage across inverting input = $R_G I_B^+$ = Voltage across non-inverting input (because differential input = 0)

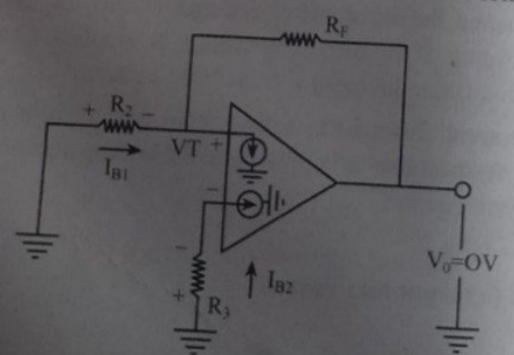
Since, there is no resistor in feedback loop

So, $V_0 = -R_G I_B^+$ with polarity as shown in the above figure.

3rd part

Method of reducing effect of input bias current and input offset voltage.

This method consist of introducing a resistance R_3 in series with non-inverting input terminal from a signal point of view has a negligible effect. The value of R_3 is determined as follow:



Let V_{01} is output due to V^- and V_{02} is output due to V^+

So, Applying superposition theorem,

$$V_0 = V_{01} + V_{02}$$

Here,

$$V_{01} = (-I_{B1}R_1)\left[\frac{-R_f}{R_1}\right] \qquad [\because V^- = -I_{B1}R_1]$$

$$V_{02} = (-I_{B2}R_3)\left[1 + \frac{R_f}{R_1}\right] \quad V^+ = -I_{B2}R_3$$

So, $V_0 = -I_{B2}\frac{R_3}{R_1}(R_1 + R_f) + I_{B1}R_f$

Let $I_{B1} = I_{B2} = I_B$ then,

$$V_0 = -I_B\frac{R_3}{R_1}(R_1 + R_f) + I_B R_f$$

For the best output $V_0 = 0$

$$-I_B\frac{R_3}{R_1}(R_1 + R_f) + I_B R_f = 0$$

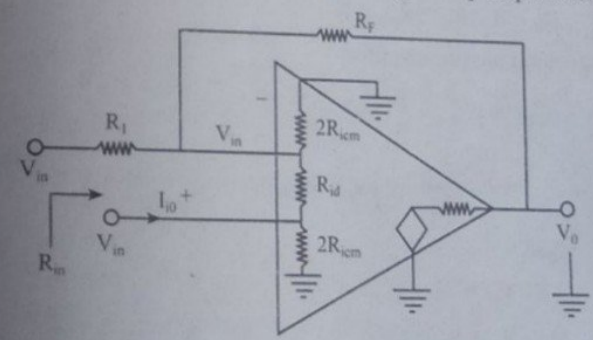
or, $R_1R_3 + R_F R_3 = R_1R_f$

$$R_3 = \frac{R_1R_f}{R_1 + R_f} = R_1//R_f$$

Which is required expression.

5. Draw a circuit diagram of inverting op-amp and derive the expression of input impedance. **[2072 Kartik, 2069 Chaitra]**

Solution: Input resistance of closed loop configured op-amp circuit.



Here, R_{icm} → common mote input resistance

R_{id} → differential mode input resistance

Example; Equivalent circuit for studing R_{in}

Let us assume the output resistance of op-amp four determining the input resistance of closed loop configured op-amp.

There are two cases

(a) When op-amp is acting as inverting amplifier

(b) When op-amp acts as non-inverting amplifier

(a) As inverting amplifier

Let the current flowing at input of op-amp be In.

$$I_{in} = \frac{V^- - V_0}{R_f} + \frac{V^-}{R_{id}} \qquad (\because V_0 = AV_{id})$$

$$= \frac{V^- + AV^-}{R_f} + \frac{V^-}{R_{id}} \qquad (\because V_{id} = -V)$$

$$= \left(\frac{1+A}{R_f} + \frac{1}{R_{id}}\right) V^-$$

$$= \left(\frac{1+A}{R_f}\right) V^- \qquad (\because R_{id} \gg 1; \text{ normally range of } M\Omega)$$

$\because$ Input resistance $R_{in} = R_1 + \frac{V^-}{in}$

$$= R_1 + \frac{R_f}{1+A}$$

$$= R_1$$

Also from figure,

$$R_{in} = R_1 || R_{id} || 2R_{icm} = R_1$$

(b) non-inverting amplifier

Here, $V_0 = \left(1 + \frac{R_f}{R_1}\right) V^+$

$$V^+ = \left(\frac{R_1}{R_1 + R_f}\right) V_0 = \beta V_0$$

And

$$V_{in} = V_{id} + V^+$$

or, $V_{in} = V_{id} + \beta V_0$

$$V_{in} = V_{id} + \beta . A V_{id} \qquad (\because V_0 = A V_{id})$$

Dividing both sides by I_{in}, we get.

$$\frac{V_{in}}{I_{in}} = \frac{V_{id}}{I_{in}} + A\beta \frac{V_{id}}{I_{in}}$$

$$R_{in} = \frac{V_{id}}{id} (1 + A\beta)$$

$$= R_{id} (1 + A\beta)$$

If effect of R_{icm} is also included

$$R_{in}' = R_{in} // 2R_{icm}$$

6. Define input offset voltage for a given op-amp prove that Gain Bandwidth Product (GBP) is constant.

Solution:

The input offset voltage is the voltage that must be applied between two input terminal of an op-amp to null the output.

Second part: Refer to theory,

7. The op-amp in the given figure has slew rate of 0.5 V/μs. The input signal are as follow:

$V_1 = 0.1 \sin 10^6 t$

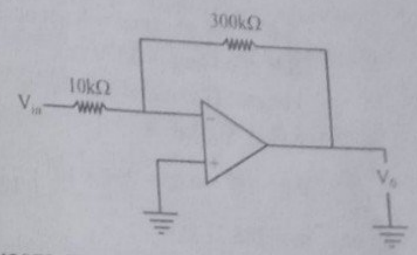
$V_2 = 0.5 \sin (350 \times 10^3) t$

$V_3 = 0.1 \sin (200 \times 10^3) t$

$V_4 = 0.1 \sin (50 \times 10^3) t$

$R_f = 330\ k\Omega$

$R_{in} = 10\ k\Omega$



[2073 Chaitra, 2070 Chaitra, 2069 Ashad]

Solution:

$$A = \frac{-R_f}{R_{in}} = \frac{-330}{10} = -33$$

$\therefore$ $|A| = 47$

Case I:

$V_1 = 0.01 \sin 10^6 t$

$V_p = 0.01$ V

$2\pi k = 10^6$

$S.R' = A . 2\pi f V_p = 33 \times 10^6 \times 0.01$

$= 0.33$ V/μs

S.R > S.R' so signal will not be distorted

Case II:

$V_2 = 0.05 \sin (350 \times 10^3) t$

$SR' = 0.05 \times 350 \times 10^3 \times 33$

$= 0.577 \times 10^6$ V/s

$= 0.577$ V/μs

S.R' > S.R so signal will be distorted

Case III:

$V_3 = 0.1 \sin (200 \times 10^3) t$

$SR' = 0.1 \times 200 \times 10^3 \times 33$

$= 0.66\ V/\mu s$

$SR' > S.R$ so signal will be distorted

Case IV:

$V_4 = 0.1 \sin (50 \times 10^3)\, t$

$S.R' = 0.1 \times 50 \times 10^3 \times 33$

$= 0.165 \times 10^6\ V/s$

$= 0.165\ V/\mu s$

$S.R' < S.R$ so signal will not be distorted

S.R of op-amp = 0.5 V/μs

For case II to remove distortion

$S.R = V_p.\ 2\pi f.\ A$

$$0.5 \times 10^6 = 0.05 \times 350 \times 10^3 \times \frac{R_f}{10 \times 10^3}$$

or, $R_f = 285.71\ k\Omega$

In equation to remove distortion

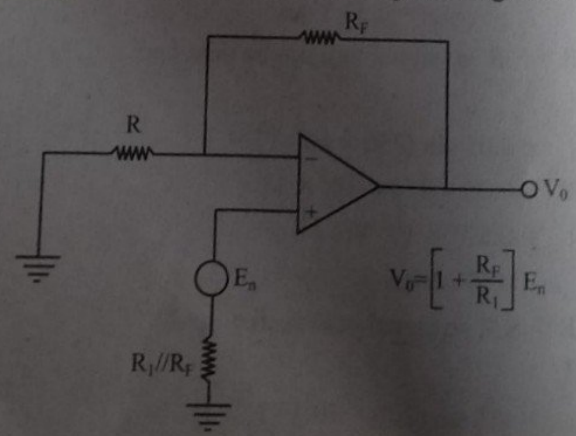
$$0.5 \times 10^6 = 0.1 \times 200 \times 10^3 \times \frac{R_f}{10 \times 10^3}$$

$\therefore\ R_f = 250\ k\Omega$

8. Discuss noise in operational amplifier circuit with necessary diagram and suggest the measure to be taken to minimize the interval noise. 2078 Kartik, 2075 Chaitra, 2071 Chaitra

Solution:

Electronics circuit are susceptible to noise and op-amp is not exception. Apart from extend noise op-amp has internal noise source like bias current, drift and internal components noise is also amplified by op-amp just as offset voltage and signal voltage.

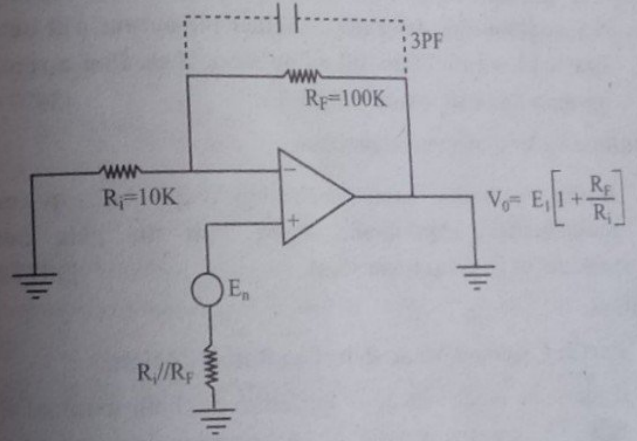


This internal op-amp noise is modeled most simply by a voltage source, E_n. E_n is placed in series with non-inverting (+) input. The 741 op-amp has 2μV of noise over a frequency of 10 kH_z. This noise voltage is valid for source resistor (R_1) between 100 Ω to 20kΩ the noise voltage goes up directly with R_1 one R_1 exceed 20 kΩ. Thus R_1 should be kept below 20kΩ to minimize noise in the output.

The following measure can be taken to minimize internal noise.

(a) Keep series input resistor as low in value as practically possible to satisfy circuit requirements.

(b) By pass feedback resistor with a small capacitor (≈ 3pf) which will reduce noise gain at higher frequency.



(c) Never connect a capacitor across the input resistor or from (–) input to ground. There will always be a few PF. of stray capacitance from (–) input to ground due to wiring.

9. What is input offset voltage and input offset current of an operational amplifier? Find the output resistance of closed loop op-amp. [2070 Chaitra]

Solution: The input offset voltage is the voltage that must be applied between two input terminal of an op-amp to the null the output.

The input offset current (I_{i0}) is defined as the difference between separated current entering input terminal of a balanced differential amplifier. $I_{i0} = |I_{B1} - I_{B2}|$

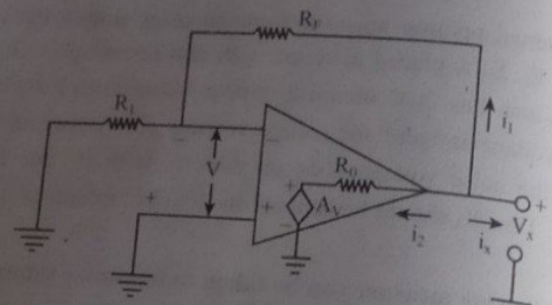


Fig: Equivalent ckt for finding round

- Please refer output impedance for 2nd part.

10. The inverting op-amp configuration has a feedback resistance 470 kΩ and input resistance of 10 kΩ. If the input signal 0.1 sin(200000t), determine whether the output will be distor due to slew rate limitation of op-amp. If so, find a remedy. T op-amp has a slew rate of 0.5V/μs. [2077 Chait

Solution: Refer to numerical problem

11. Define common mode rejection ratio of op-amp wi mathematical expressions. Prove that the gain bandwid product of op-amp is constant. [2077 Chaitr

Solution:

Part I: Common Mode Rejection Ratio (CMRR)

If the same input voltage is applied to the both terminal of an o amp. The op-amp is said to be operating in a common mo configuration and voltage is known as common mode voltage.

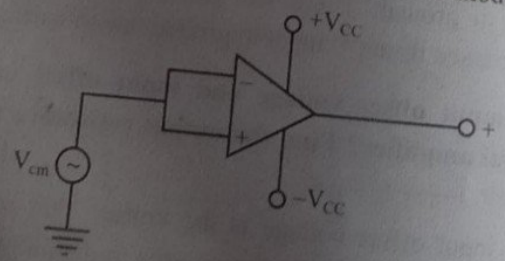


Fig: Common mode configuration of op-amp

The output voltage of op-amp in common mode configuration V_{oc} should be zero because an op-amp amplifies only the differenti

input voltage is zero so, V_{ocm} should be zero. However there will be some voltage at output so, the common mode voltage gain can be defined as ratio of output common mode voltage V_{ocm} to input mode voltage.

$$\text{i.e. } A_{cm} = \frac{V_{ocm}}{V_{cm}}$$

If there is a perfect matching between two input terminal the value of A_{cm} will be zero so, to measure the degree of matching between two input terminal the term CMRR is defined as

$$\text{CMRR} = \frac{Ad}{A_{cm}} = \frac{\text{differential mode gain}}{\text{common mode gain}}$$

$$\text{In dB, CMRR} = 20 \log\left(\frac{Ad}{A_{cm}}\right)$$

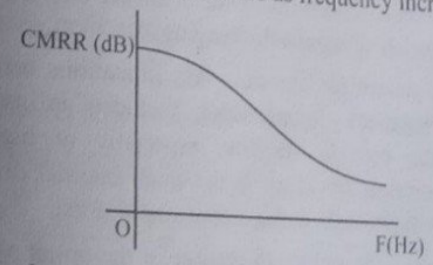
CMRR is also expressed as the ratio of change in offset voltage to total change in common mode voltage.

$$\text{i.e. CMRR} = \frac{V_{i0}}{V_{cm}}$$

$$\text{In dB, CMRR} = 20 \log\left(\frac{V_{i0}}{V_{cm}}\right)$$

Matching between two terminal α value of CMRR so it the matching between two terminal is more, value of CMRR will be high.

CMRR is the function and decrease as frequency increases.



Power supply rejection ratio (PSRR)

PSRR is the ratio of change is output voltage to change in power voltage. It is usually expressed in microvolt per voltage or in decibel. Also it is the measure of the ability of op-amp to ignore change supply voltage.

Part II: Refer to theory

12. **Find the closed loop input impedance of an inverting op-a**
An inverting op-amp with R_1 = 330 KΩ and R_1 = 10 KΩ ha
slew rate of 0.5 V/μs with input signal equal to 0.1 sin(2000
Determine whether the output will be distorted due to slew r
limitation, if so, find a remedy. **[2076 Ashw**

Solution: Refer to theory

13. **Explain the gain-bandwidth product of a practical op-amp. F**
the output resistance of an amplifier that uses a practical
amp. **[2076 Ashw**

Solution: Refer to theory

14. **Design a 4-bit voltage mode R-2R ladder type DAC and deri**
the expression for its analog output. Differentiate betwe
unipolar and bipolar DACS. **[2076 Ashw**

Solution:

Part I: Refer to theory

Part II: Refer to theory

15. **Show the effect of input offset voltage in Op-Amp. How can it b**
minimized? Define power supply rejection ratio of Op-Amp.

Solution: **[2075 Ashwi**

Part I: The slew rate limit is the maximum rate of change of th amplifier's output voltage and is due to the fact that th compensation capacitor inside the amplifier only has finite curren available for charging and discharging.

The chief causes for the slew rate limitations are caused by th internal frequency compensation included in most operation amplifiers to provide stability, especially at high frequencie Another contributory factor is the small internal drive currents, a well as any limitations in the output stage.

The best way is to reduce the power of the op-amp specifically th tail current. When the tail current reduces, you are going to hav lower slew rate, lower burning of power and more gain. You coul also cut down on the compensation caps if area is of more importan to save than power.

Part II: Refer to numerical problems

❖❖❖

Chapter 3

Digital to Analog and Analog to Digital

A signal is a electromagnetic or electrical cured that carries data from one system to another. There are two types of signal.

(a) Analog signal

(b) Digital signal

Analog signal	Digital signal
It is a continuous signal in which one time varying quality represent another time based variable	It is a discrete signal which is used to represent data as a sequence of separate value at any point in time.
Continuous range of value to represent into	It uses discrete 0 and 1 to represent information.
It is suitable for audio and video transmission	It is suited for computing and digital electronics

Advantages of digital signal

(a) Highly immune to noise

(b) Can be stored easily

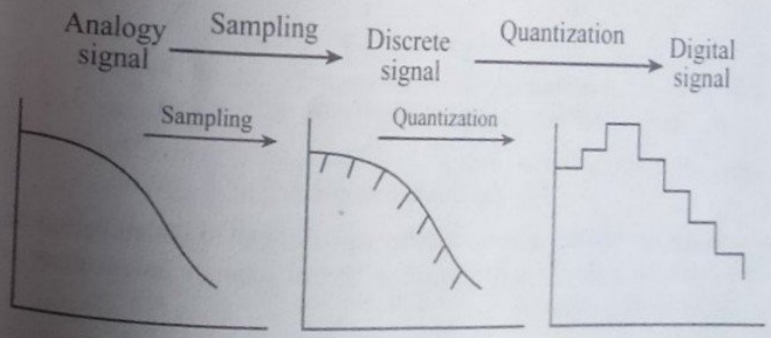
(c) Can be transmitted easily

(d) Easily replicated and highly secured

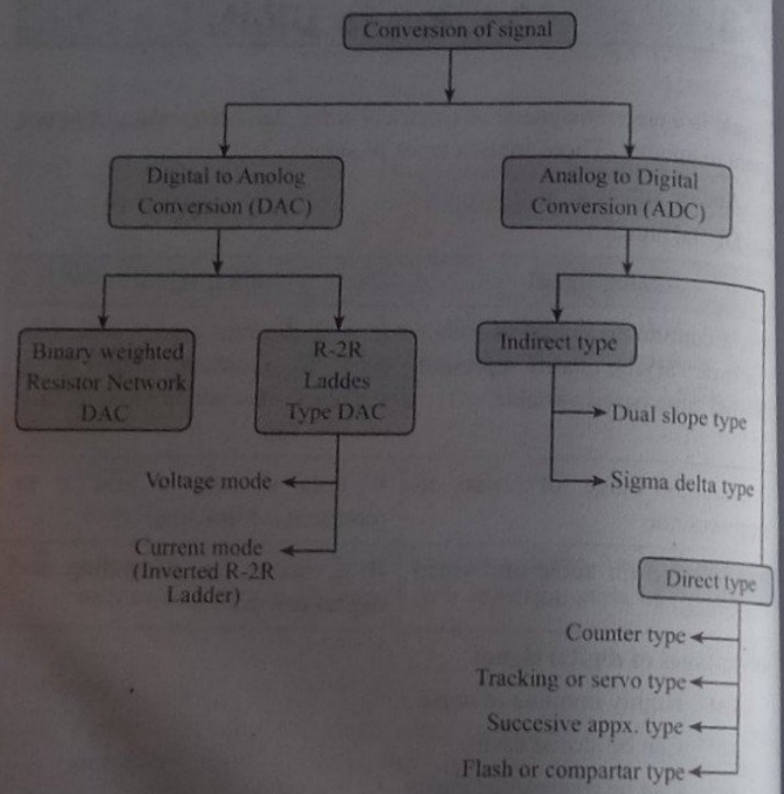
Disadvantage

(a) Requires high bandwidth

(b) System complexity



Signal can be converted from one form to another i.e. analog to digital and vice versa.



Digital to analog conversion

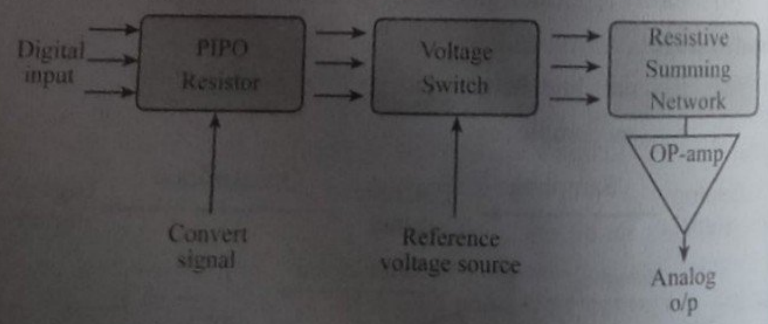
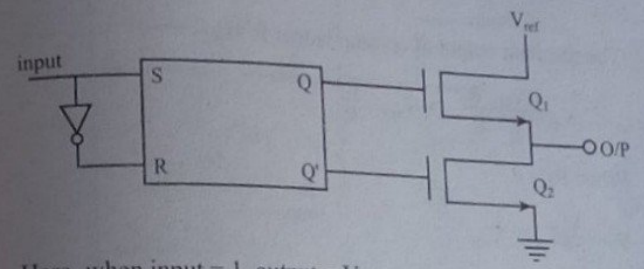


Fig: Block diagram of DAC

(a) Resistor: Initially resistor receives digital signal to be converted on receiving end of resistor which is latched (stored) unless convert command is imitated.

(b) Voltage switch: Normally totempole MOSFET. Switch is used depending upon the nature of input logic i.e. 0 or 1. Voltage switch provides ground or reference voltage (V_{ref}).



Here, when input = 1, output = V_{ref}

When input = 0, output = ground

For, n-bit bipolar DAC diagram is given below:

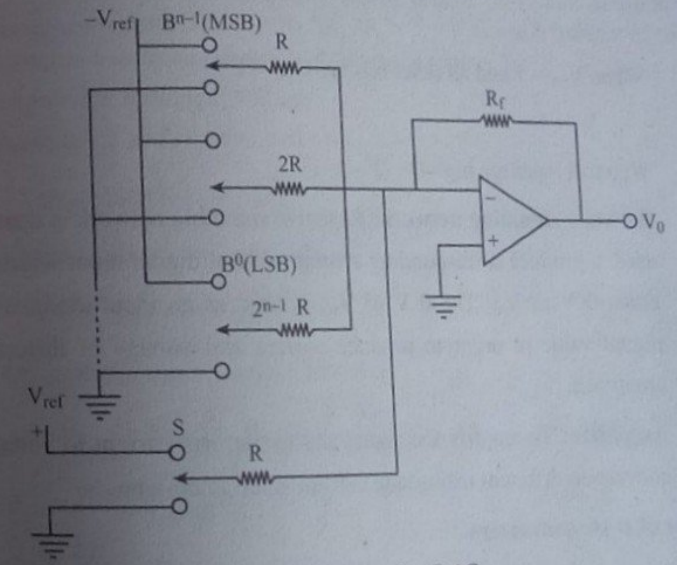


Fig: bit bipolar DAC

When the switch S is connected to the grounded then DAC becomes Uni-polar DAC (binary weighted resistor network DAC) whereas,

When switch is connected to + V_{ref} then output voltage range from – V_{ref} to V_{ref}. So act as bipolar DAC.

The output of op-amp due to binary weighted resistor network is,

$$V_{01} = -\frac{V_{ref}}{2^{n-1}R} \cdot R_f (2^{n-1}B_{n-1} + 2^{n-2}B_{n-2} + \ldots + 2^0 B_0)$$

The output due V_{ref} voltage is,

$$V_{02} = -\frac{V_{ref}}{R} \cdot R_f$$

The resultant output of op-amp ladder is

$$V_0 = \frac{V_{ref} \cdot R_f}{2^{n-1}R} \cdot D. V_{ref} = \frac{R_f}{R}$$

When $R_f = R$

$$V_0 = \frac{V_{ref}}{2^{n-1}} \cdot D. V_{ref}$$

where D = Decimal equation off binary input data

Where all input = 0, D = 0

$\therefore \quad V_0 = V_{ref}$

When $V_{ref} = 1$ and all other bits are $O.D = 2^{n-1}$

$V_0 = 0$

When all input are high $D = 2^n - 1$

(c) **Resistive summing network:** Resistive summing network is mainly used to produce corresponding analog value of digital input which is either 0 V or V_{ref}. The 0 V or V_{ref} is used as an input along with digital value in order to produce current and voltage of different amplitude.

(d) **Amplifier:** To amplify the signal and to perform current to voltage conversion different magnitude current is fed to op-amp.

Types of DAC converters

(a) Binary weighted resistor network DAC

(b) R-2R ladder types DAC.

⇒ Voltage mode

⇒ Current more (inverted R-2R ladder)

(a) Binary weighted resistor Network DAC.

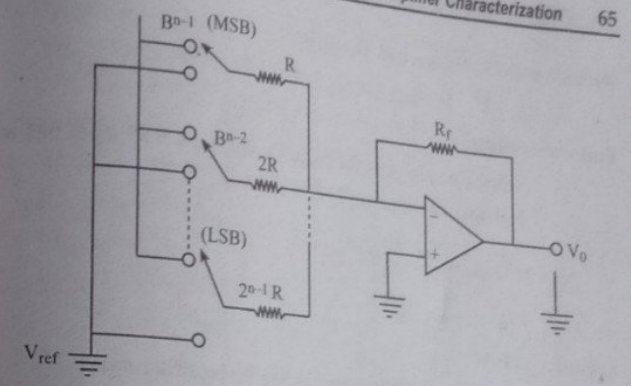


Fig: Binary weighted Resistor DAC

Let us consider a n-bit circuit which consist of n number of binary weighted resistor. Such as R_1 $2R_1$ 4R ... ... $2^{n-1}R$ and n number of SPDT switches and let an op-amp with feedback resistor R_f.

Expression for output voltage.

I_0 MSB = 1 and all other bits = 0

$$V_0(MSB) = (-V_{ref})\frac{R_f}{R}$$

If next MSB = 1 and other bits = 0

$$V_0(LSB) = -(V_{ref})\frac{R_f}{2^{n-1}R}$$

On applying superposition theorem,

$$V_0 = V_{ref} \cdot \frac{R_f}{R} \cdot B_{n-1} + V_{ref}\frac{R_f}{2R} \times B_{n-2} + \dots\dots + V_{ref}\frac{R_f}{2^{n-1}R} \times B$$

$$= V_{ref}\frac{R_f}{2^{n-1}R}(2^{n-1}B_{n-1} + 2^{n-2}B_{n-2} + \dots\dots + 2^0 B_0)$$

$$V_0 = \frac{V_{ref}}{2^{n-1}R} R_f D$$

When D = decimal equivalent of input unit.

Resolution of DAC

➢ Resolution of the DAC is the weight of the LSB. It is also the increment in each stop of bits combination.

$$\therefore \quad \text{Resolution} = \frac{V_{ref}}{2^{n-1}R} \times R_f$$

Relation between $V_{0(MSB)}$ and $V_{0(LSB)}$ is,

$$V_{0(MSB)} = 2^{n-1} V_{0(LSB)}$$

Full scale voltage

- Full scale voltage is the output voltage when all input bits are high and mathematically it is equal to.

$$V_{FS} = V_{0\,max} = \frac{V_{ref}}{2^{n-1}} \cdot \frac{R_f}{R} (2^n - 1)$$

$$= (2^n - 1)\, V_{0(LSB)}$$

Accuracy of DAC

(a) V_{ref} should be constant and praise for better accuracy

(b) Switch on-resistance should be zero

(c) Accuracy depends on precision of resistor so it should be considered properly

Some of the drawback of binary weighted resistor DAC are:

- As bit goes on increasing voltage of resistance increase i.e. There will be wide range of variation of resistance used in DAC which is not suitable for mordent IC manufacturing technology.
- Effect of input bias current is significant for increasing value of n.

3.1 The R-2R Ladder Circuit

There are several drawback in binary weighted register which is solved by R – 2R ladder circuit. It uses only two value resistor R and 2R. It can be operated in two mode i.e. voltage mode and current mode.

(Note: Value of R and 2R ranges from 2.5 kΩ – 10kΩ)

1. **Voltage mode R – 2R ladder DAC:** If the R – 2R ladder network is operated in voltage mode then it is known as voltage mode R – 2R ladder which is used as a current splitting device.

   In this mode resistance at left or right side of the ladder from any made is 2R. As a result this current splits half at each made giving rise to binary weighted Seq. of current.

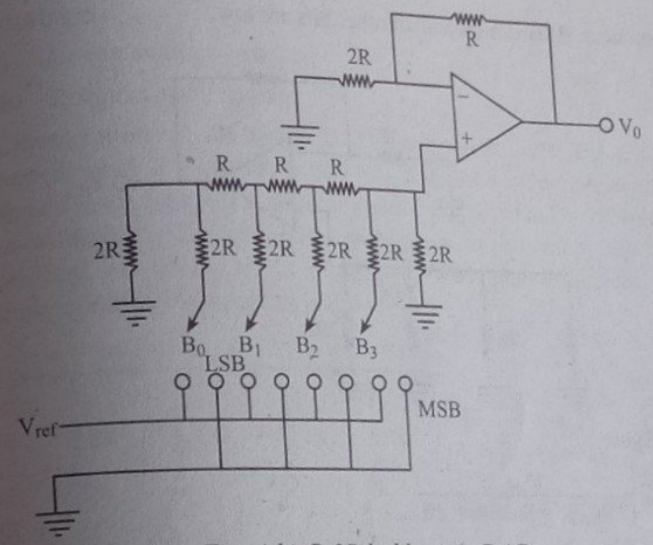
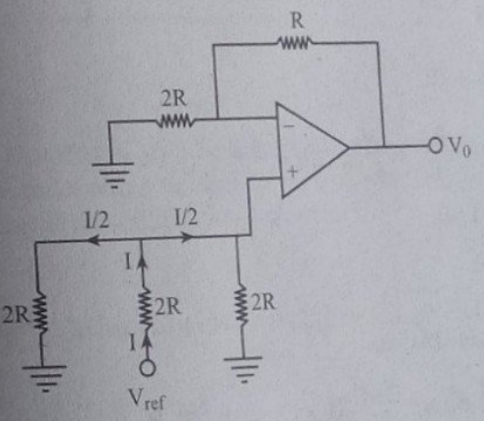


Fig: 4-bit R-2R ladder type DAC

When MSB is high and all other bits are low.

From figure,



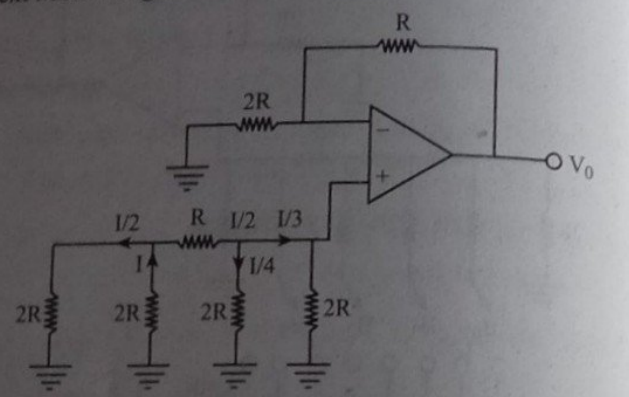
$$I = \frac{V_{ref}}{(2R//2R) + 2R}$$

$$= \frac{V_{ref}}{3R}$$

$$V^+ = \frac{I}{2} \times 2R = \frac{V_{ref}}{3R.2} \cdot 2R = \frac{V_{ref}}{3}$$

and, $V_0 = \left(1 + \frac{R}{2R}\right) V^+ = \frac{V_{ref}}{2}$

When next MSB is high and all other bits are low.



From figure,

$$I = \frac{V_{ref}}{(2R//2R + R)//2R + 2R}$$

$$= \frac{V_{ref}}{3R}$$

and, $V^{+} = \frac{I}{4} \times 2R$

$$= \frac{V_{ref}}{4.3R} \times 2R$$

$$V_0 = \left(1 + \frac{R}{2R}\right) \times \frac{V_{ref}}{4.3R} \cdot 2R = \frac{V_{ref}}{4}$$

Similarly for LSB,

$$V_0 = \frac{V_{ref}}{2^n}$$

So, the output of DAC is,

$$V_0 = \frac{V_{ref}}{2} B_{n-1} + \frac{V_{ref}}{2^2} B_{n-2} + \ldots\ldots + \frac{V_{ref}}{2^n} B_0$$

$$= \frac{V_{ref}}{2^n} [B_{n-1} 2^{n-1} + B_{n-2} 2^{n-2} + \ldots\ldots + B_0 2^0]$$

$$= \frac{V_{ref}}{2^n} D$$

Advantage

(a) Uses only two value of resistor R and 2R.

Disadvantages

(a) Circuit analysis complex.

(b) Requires many resistor.

2. **Current mode R–2R ladder DAC (Inverted R – 2R DAC):** The current mode R – 2R ladder network DAC for 4 bit digital input is shown in the figure. It is also known as inverted mode R – 2R ladder network DAC. The switch here only divert the current to negative terminal of op-amp or to the ground. The network divides the current into two equal parts in each node.

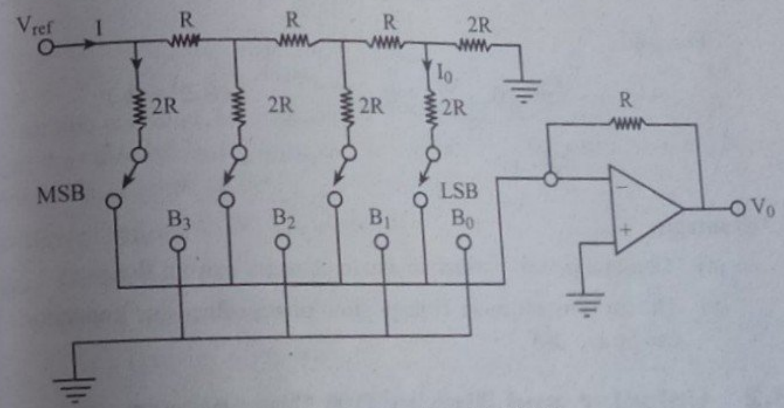


Fig: Inverted R – 2R DAC

When the input bit is low, the switch diverts the current to ground and diverts to inverting terminal of op-amp when input bit is high. Here op-amp as current to voltage converter.

Here,

$$I = \frac{V_{ref}}{R} \text{ (equivalent resistance = R from circuit analysis)}$$

So,

$$I_3 = \frac{I}{2} = \frac{V_{ref}}{2R}$$

$$I_2 = \frac{I}{4} = \frac{V_{ref}}{4R}$$

$$I_1 = \frac{I}{8} = \frac{V_{ref}}{8R}$$

$$I_0 = \frac{I}{16} = \frac{V_{ref}}{16R}$$

If all bits are high

$$V_0 = -I_{total} R$$

$$= -R\left(\frac{V_{ref}}{2R} + \frac{V_{ref}}{4R} + \frac{V_{ref}}{8R} + \frac{V_{ref}}{16R}\right)$$

In general,

$$V_0 = -R\left(\frac{V_{ref}}{2R}B_3 + \frac{V_{ref}}{4R}B_2 + \frac{V_{ref}}{8R}B_1 + \frac{V_{ref}}{16R}B_0\right)$$

$$\therefore \quad V_0 = -\frac{V_{ref}}{2^4}(B_3.\,2^B + B_2.\,2^2 + B_1.\,2^1 + B_0.\,2^0)$$

For n-bil

$$V_0 = -\frac{V_{ref}}{2^n}(B_{n-1}\,2^{n-1} + B_{n-2}\,2^{n-2} + \ldots\ldots + B_1 2^1 + B_0)$$

$$= \frac{-V_{ref}}{2^n}.\,D$$

Advantages

(a) Constant power dissipation due to constant current flow.

(b) Due to constant node voltage slow down effect due capacitor can be avoided.

3.2 Unipolar and Bipolar D/A Converters

(a) Unipolar DAC: It output voltage range of DAC from – 0 to + V_{ref} voltage or from – V_{ref} to 0 voltage. The DAC is called Unipolar DAC.

(B) Bipolar DAC: Bipolar DAC provides both positive as well as negative output voltage.

$$V_0 = \frac{V_{ref}}{2^{n-1}}(2^n - 1) - V_{ref}$$

$$= \frac{V_{ref}}{2^{n-1}}2^n - \frac{V_{ref}}{2^{n-1}} - V_{ref}$$

$$= 2V_{ref} - V_{ref} - \frac{V_{ref}}{2^{n-1}}$$

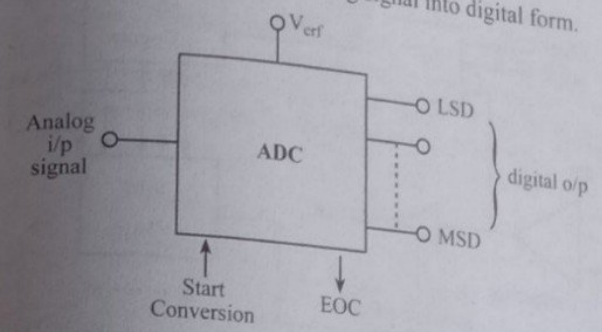
$$= V_{ref} - \frac{V_{ref}}{2^{n-1}}$$

$$= V_{ref} - V_0(LSB \approx 0)$$

$$V_0 = V_{ref}$$

Analog to digital convents

ADC is a device that converts the analog signal into digital form.



A sample and hold circuit is used before analog signal is fed to ADC so that the value of analog input can be kept constant and conversion can be done with constant value.

Different types of ADC are available

(a) Direct type

(i) Counter type

(ii) Tracking servo type

(iii) Successive approximation type

(iv) Flash or comparator type

(b) Indirect type

(i) Dual slope type

(ii) Sigma-Delta type

3.3 Count Up and Tracking A/D based on DAC

3.3.1 Count-Up type/ Staircase Romp type ADC

The count-Up type ADC consists of binary-up counter DAC, comparator and control gates.

Operation

The reset signal reset the counter to zero at the start of conversion. When a reference voltage V_r is less than input analog voltage V_a. The comparator output is 1So, it start signal is also 1. The counter receives the clock pulse and DAC produces staircase reference voltage according to the digital input (output of counter).

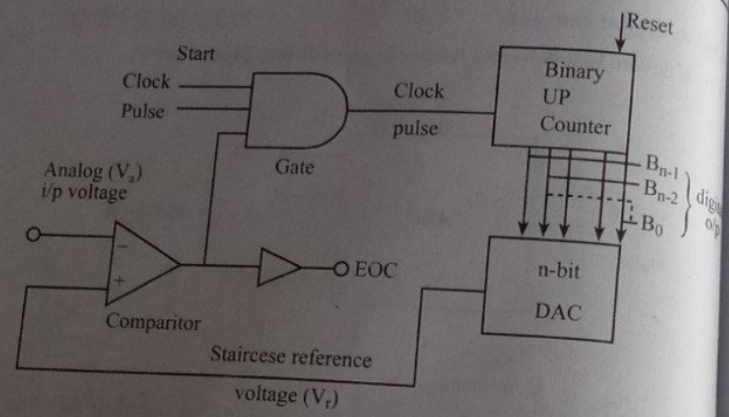


Fig: Count-up type ADC

When $V_r \geq V_a$ the output of comparator is KW and the output of gate is also zero so counter doesn't get clock pulse. So, the value of counter at this stage is the digital output of analog input voltage V_a. For n-bit ADC the maximum number of clock pulses required is 2^{n-1} and maximum time delay is $(2^n - 1)T$. Where T is clock pulse period.

In this type of ADC. The clock period must be high enough (or clock frequency must be low enough) to give sufficient time for DAC to settle and for the comparator to respond. Which times the speed of ADC.

Advantage

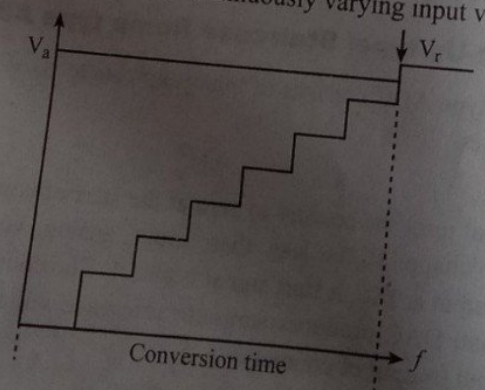
(a) Simple in operation and circuitary

Disadvantage

(a) Conversion speed is very low

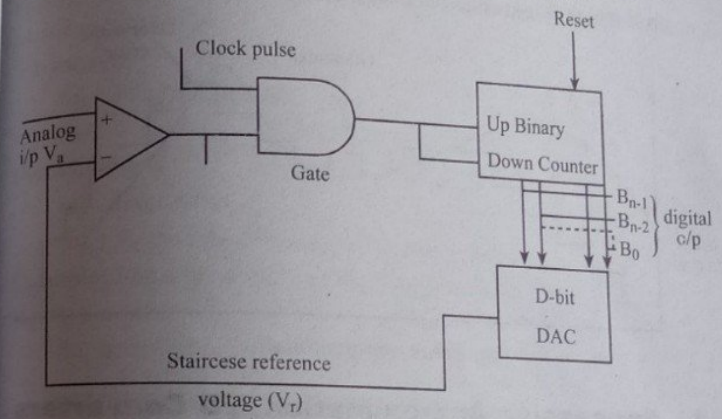
(b) Conversion time varies for different input.

(c) Cannot convert the continuously varying input voltage.

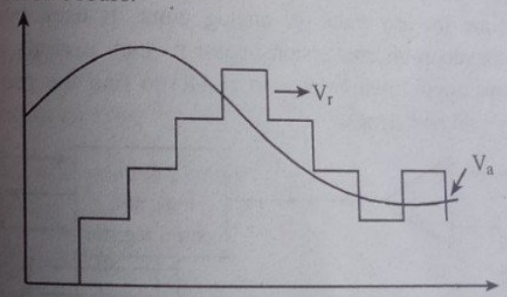


3.3.2 Tracking or servo type ADC

This is improved version of count up type ADC. The counter performs up counting or down counting depending upon the result of comparator the analog output of DAC is compared with analog input value V_a. If $V_a > V_r$. The output of comparator goes high and the counter is caused to count up. If $V_r > V_a$ the counter reverses the direction and count down.



When analog input change rapidly the tracking A/D cannot keep up with change and error occurs.



Advantage

(a) Always close to the input value.

Disadvantages

(a) Requires more time to stabilize.

Error in tracking type ADC

(a) **Start up error:** At time $t = 0$ when the ADC is operated it there is certain analog input value then there is incorrect output for certain time until DAC output reaches close to the value of input. Such error which exist at the start up is termed as start up error.

(b) **Granular noise (or granular error):** When input voltage is nee constant then there exists a fluctuation in binary output this sho that there is an error which lies between 0 to 1 LSB such error termed as granular noise or error.

(c) **Over slope error:** If the input voltage exhibits high level local slo then the binary output could not track the input voltage resulting error which is termed as over slope error.

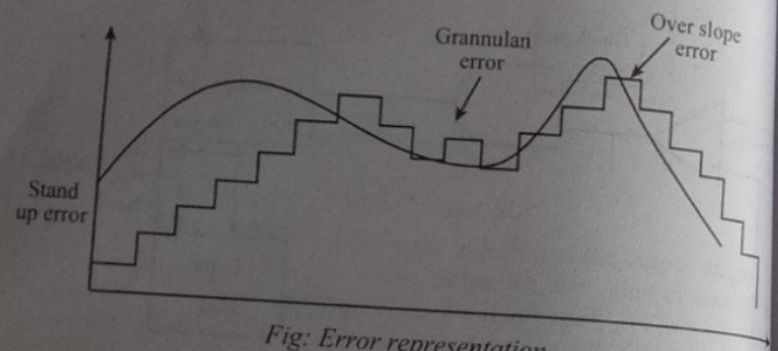


Fig: Error representation

3.4 Successive Approximation A/D Converters

This type of ADC is most widely used A/D converter. It has fixed conversion time for any value of analog input. It uses very efficient strategy to convert n-bit conversion in just n-clock periods. The circuit uses successive approximation register (SAR) to find the required value of each bit by trial and error.

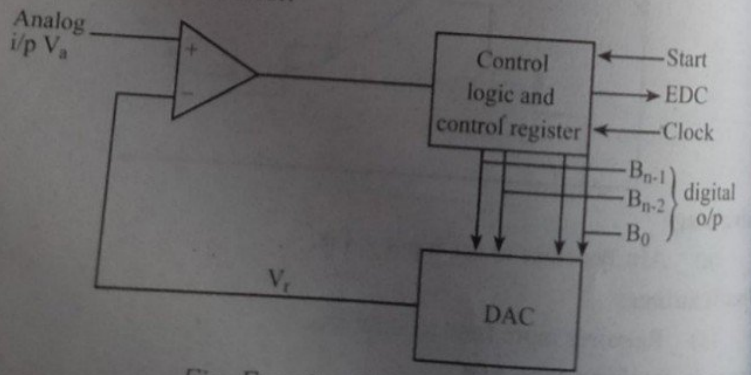


Fig: Functional block diagram

With the arrival of the start commend SAR sets MSB bit = 1 with all other bit zero so that trial code = 10. Then DAC's output will be compared to analog input V_a.

If V_a is greater than DAC's output the MSB is left at 1 and the next lower significant bit is made 1 and further tested.

If V_a is less than DAC's output then SAR resell the MSB to '0' and goes to the nerd lower significant bit.

This procedure is repeated for all sub sequent bits one at time. Unstill all position n bit has been tested.

Finally, DAC' output voltage becomes successively closer to the actual analog input voltage.

Advantages

(a) Easy interfacing.

(b) Conversion time is constant.

Disadvantages

(a) Expensive

(b) V_a must be constant during conversion

Example: For 4 bit ADC, Let V_{ref} = 16 V and V_a = 10.2 V

Step I: Set MSB = 1

So, output of register = 1000

and, output of DAC $= \frac{V_{ref}}{2^4} . D = \frac{16}{16} \times 8 = 8$ V

Here, $V_a > V_r$ So 1 is retained

Step II : Set MSB = 1

So, output of register = 1100

and, output of DAC $= \frac{V_{ref}}{2^4} . D = \frac{16}{16} \times (8+4) = 12$ V

Here, $V_a < V_r$ so, 1 is flipped to 0

Step III : Set next bit = 1

So, output of register = 1010

and, output of DAC $= \frac{V_{ref}}{2^4} . D = \frac{16}{16} \times (8+2) = 10$ V

Here, $V_a > V_r$ so, 1 is retained

Step IV : Set next bit = 1

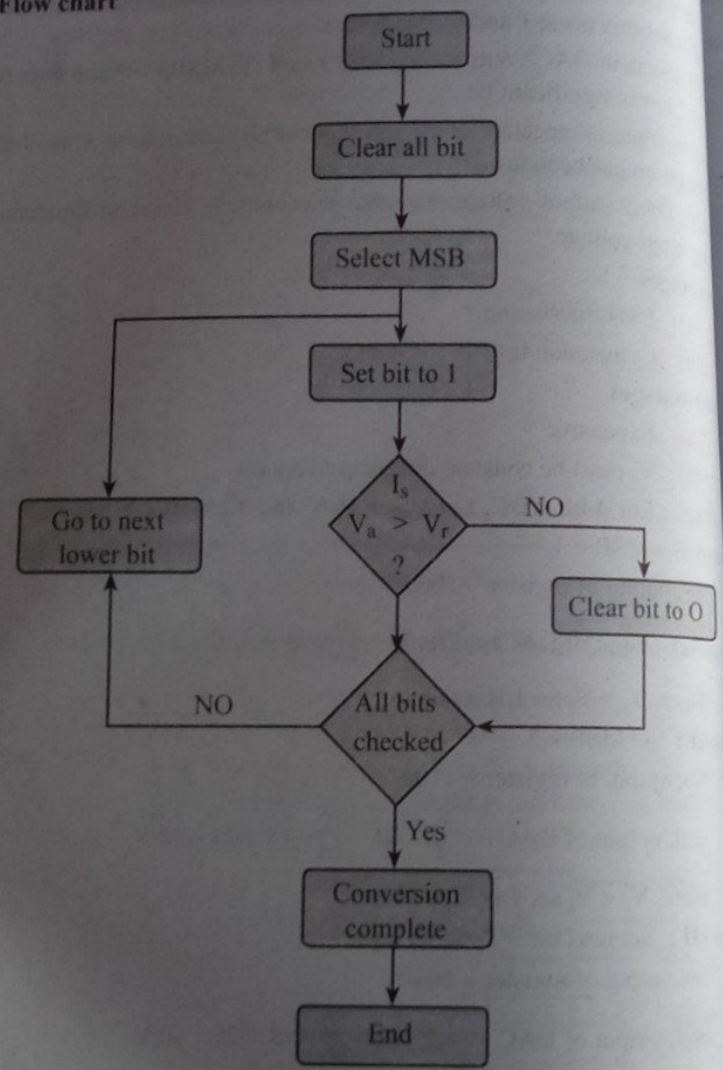
output of register = 1011

output of DAC $= \frac{16}{16}(8+2+1) = 11$ V

Here, $V_a < V_r$ So, 1 is flipped to 0

Hence, final output = 1010

Flow chart

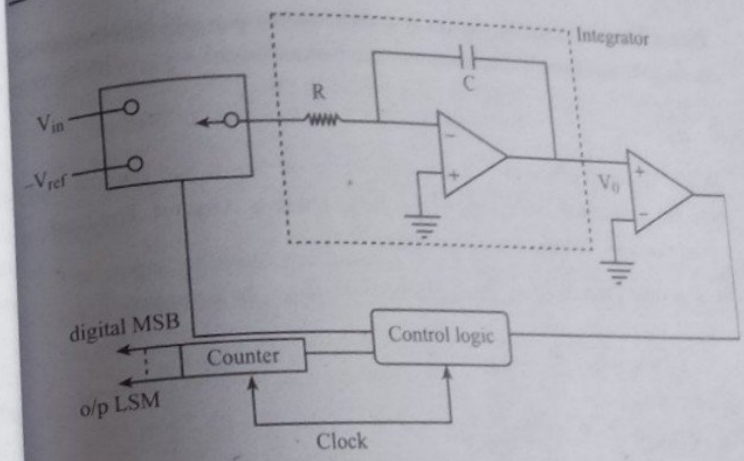


3.5 Integrating A/D Converter

(a) Dual slope ADC

(b) Quad slope ADC

(a) Dual slope ADC: It is used in the digital voltmeter and other types of measuring instruments. A ramp generator is used to produce dual slope characteristics.



Operation

Initially, the capacitor is discharged so, $V_0 = 0$

Phase I

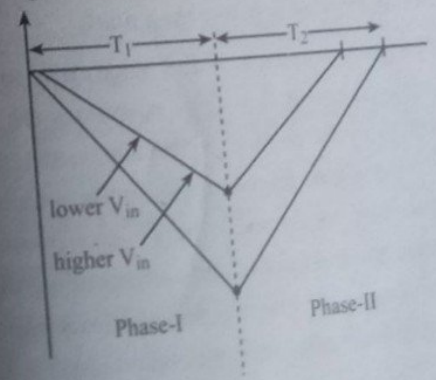
The control logic connects, the switch to V_{in} so that capacitor is charged by V_{in} for fixed time duration by the current $I = \frac{V_{in}}{R}$

So, the output of integrator is

$$V_0 = \frac{-1}{C}\int_{T_1} I dt$$

$$= \frac{-1}{C}\int_{T_1} \frac{V_{in}}{R} dt = \frac{-1}{CR} V_{in} T_1$$

Here, T_1 and RC i.e. constant so V_0 ramp up with slope proportional to V_{in} as shown in figure.



Phase II: After time T_1, switch is connected to $-V_{ref}$ and binary co starts to count from 0. The capacitor discharges toward $-V_{ref}$ with cu

$$-\frac{V_{ref}}{R_1}$$

When V_0 ramp down to 0 V the comparator senses it and control l stop the conversion. The slope of discharge phase is constant. The read of the counter is output for given input.

So, the final value of $V_0 = 0 = V_0$ (after T_1)

$$\frac{-1}{C}\int_{T_2} \frac{-V_{ref}}{R}\, dt$$

or, $$0 = \frac{-1}{RC} V_{in} T_1 + \frac{V_{ref}}{RC}\int_{T_2} dt$$

or, $$V_{in} T_1 = V_{ref} T_2$$

$$T_2 = \frac{V_{in}}{V_{ref}} T_1$$

So, digital output is no. of counts by counter i.e. counter reading $= \frac{T_2}{T_c}$ (clock period of counter)

Advantage

(a) Independent of circuit component so more accurate

(b) Cheaper

Disadvantages

(a) Conversion speed is slow

Quad slope ADC (Why quad is better than dual)

Quad slope is the improved version of dual slope ADC to remove noise. In this type of conversion two dual slope operations are performed for each data conversion cycle. In first conversion actual input signal is removed so that input signal represent only noise which gives digital word as error that must be removed. In 2nd conversion input signal (Which may contains noise) is applied and corresponding digital words is generated the previous digital error is subtracted from equivalent digital word. The resulting words is more accurate and precise.

3.6 Sigma Delta A/D Converters

Sigma delta ADC is mostly used in analog to digital conversion. Particularly in telecommunication which uses audio signals. This method is based on delta modulation where the difference between two successive samples is quantized. Delta modulation is a 1 bit quantization method.

The output of delta modulator is single output bit data stream where the relative number of is and 0'S indicates the level or amplitude of input.

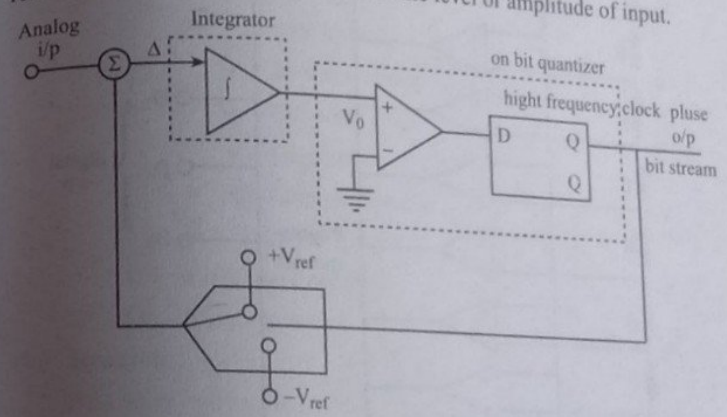


Fig: Block diagram of sigma- Delta ADC

In sigma delta ADC, the analog sigma and analog output of ADC are applied to the summation (Σ) point. So, the delta signal (difference sigma) is generated at summation point integrator generates ramp signal for difference signal Δ. If ramp voltage exceeds threshold 0 V, the one bit quantize output will be 1 other wise output will be 0.

Here 1-bit DAC in feedback path produces $+V_{ref}$ if it's input is 1 and produces $-V_{ref}$ if it's input is 0.

The output of DAC is fed to summing point to generate new Δ.

Advantage

(a) It is much more accurate.

Disadvantage

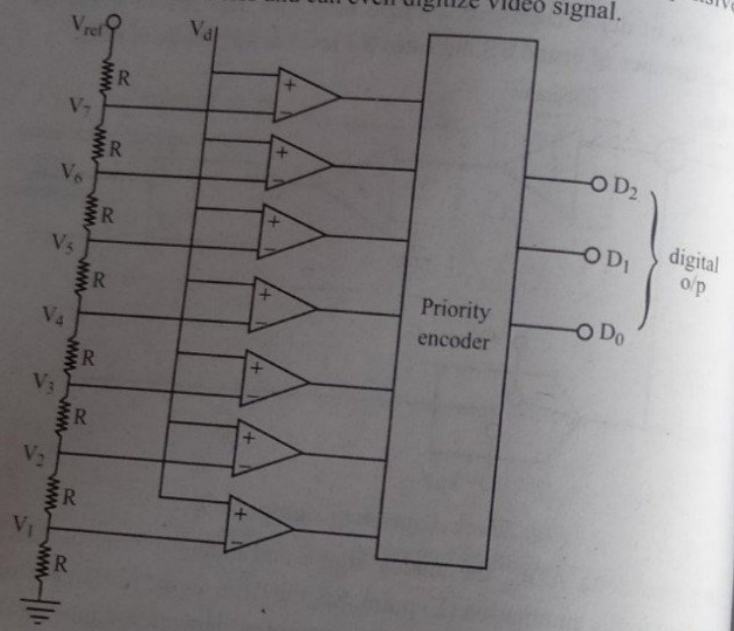
(a) Require high clock frequency.

(b) Complex circulatory required.

3.7 Flash A/D Converter

The flash type ADC (simultaneous ADC) is the fastest ADC that utilizes comparator that compares reference voltage with analog voltage. Along comparators priority encoder is used to convert the output of comparator into the digital output.

For n-bit ADC, 2^{n-1} comparator are required so it' is very expensive. It's conversion time is less and can even digitize video signal.



If $V_{ref} = 8$ V

So, $V_1 = 1V$, $V_2 = 2V$, $V_3 = 3V$, $V_4 = 4V$, $V_5 = 5V$, $V_6 = 6V$ and $V_7 = 7V$

So, If $V_a < 1V$, input to priority encoder = 0000000

If $2 < V_a \leq 1V$, input priority encoder = 000000 1

If you want the output 0 for $V_a < 0.5$ V.

The bottom resistor can be replaced by $\frac{R}{2}$ and the top resistor with $\frac{3R}{2}$

Advantages

(a) Very fast

(b) Clock is not required

Disadvantages

(a) Expensive and high power consumption

(b) Complexity doubles for each additional bits.

Characteristics of D/A A/D converter

(a) Static

(i) resolution

(ii) Linearity

(1) Integral linearity

- Absolute linearity
  - Zero scale error
  - Full scale error
  - Gain error
- Best straight linearity
- End point linearity

(2) Diffential linearity

(3) Monotonously

(b) Dynamic

(i) Conversion time

(ii) Setting time

Some important question

Advantages of R – 2R ladder over binary weight.

It's operation is much more easily analyzed. It uses only two different resistor value. The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.

Advantages of current mode over voltage mode.

Although both mode uses two resistor (R – 2R) current mode is better than voltage mode due to following:

(a) Number of bit can be expanded by adding more section of same R/2R value.

(b) In inverted R/2R, ladder DAC node remain constant with changing input binary words. This avoids any slowdown effects by stray capacitance.

Old Questions with Solution

1. Explain the operation of bipolar DAC. Write disadvantages of weighted resistor DAC.

[2073 Sharwan, 2072 Chaitra, 2071 Sharwan, 2074 Chartra, 2073 Chaitra]

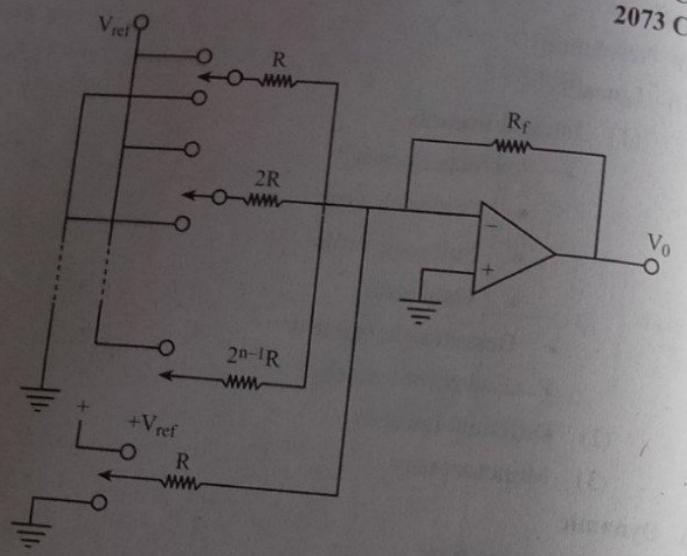


Fig: n-bit bipolar DAC

Solution:

When switch S is connected to ground. DAC becomes Unipolar DAC (binary weighted network resistor network DAC). But if connected to $+V_{ref}$ the output voltage range from $-V_{ref}$ to $+V_{ref}$ so, acts as bipolar DAC.

The output of op-amp due to binary weighted resistor network is.

$$V_0 = \frac{V_{ref}}{2^{n-1}R} . R_f (2^{n-1}B_{n-1} + 2^{n-2} B_{n-2} + \dots + 2^0 B_0)$$

The output due to $+V_{ref}$ voltage is,

$$V_{02} = \frac{-V_{ref}}{R} . R_f.$$

∴ The resultant output of op-amp is,

$$V_0 = \frac{V_{ref}}{2^{n-1}R} . R_f . D - V_{ref} . \frac{R_f}{R}$$

When $R_f = R_f$

$$V_0 = \frac{V_{ref}}{2^{n-1}} D - V_{ref}$$

(where D = decimal equivalent of binary input data)

When all input = 0, D = 0

$$V_0 = -V_{ref}$$

When MSB = 1 and all other bits are 0,

$$D = 2^{n-1}$$

$$V_0 = 0$$

When all input 's are high $D = 2^{n-1}$

$$V_0 = \frac{V_{ref}}{2^{n-1}} (2^n - 1) - V_{ref}$$

$$= \frac{V_{ref}}{2^{n-1}} .2^n - \frac{V_{ref}}{2^{n-1}} - V_{ref}$$

$$= 2V_{ref} - V_{ref} - \frac{V_{ref}}{2^{n-1}}$$

$$= V_{ref} - \frac{V_{ref}}{2^{n-1}}$$

$$= V_{ref} - V_0 \text{ (LSB} \approx 0)$$

∴ $V_0 \approx V_{ref}$

For 4 bit digital input

0000	$-V_{ref}$
1000	0
1111	$+V_{ref}$

The disadvantage of weighted resistor DAC are given below:

(i) Requirement of wide range of resistor

(ii) For n > 4 practically not good

(iii) V_{ref} should be stable and constant

(iv) Resistance of switch must be zero

2. Explain the working principle of dual slope analog to digital convert (ADC) with circuit diagram explain why it's output is accurate.

[2074 Chaitra, 2073 Shrawan, 2073 Chaitra, 2070 Chaitra, 2069 Chaitra]

Solution:

Part I: Please refer theory

Part II: The output of ADC is independent of circuit component so it's output is accurate

3. Why current mode R – 2R ladder type DAC is preferred over voltage mode R – 2R ladder type DAC? Find expression for output voltage of bipolar DAC and justify it's name.

[2078 Kartik, 2077 Chaitra, 2074 Ashwin, 2074 Chaitra, 2072 Kartik, 2071 Sharawan, 2070 Chaitra, 2069 Chaitra, 2068 Chaitra]

Solution:

Part: I: Current mode R – 2R ladder type DAC is preferred over voltage mode R – 2R ladder type DAC because of the following advantages.

(a) Constant power dissipation due to constant current flow.

(b) Due to constant node voltages slow down effect due to capacitor can be avoided.

Part II: Please refer to theory

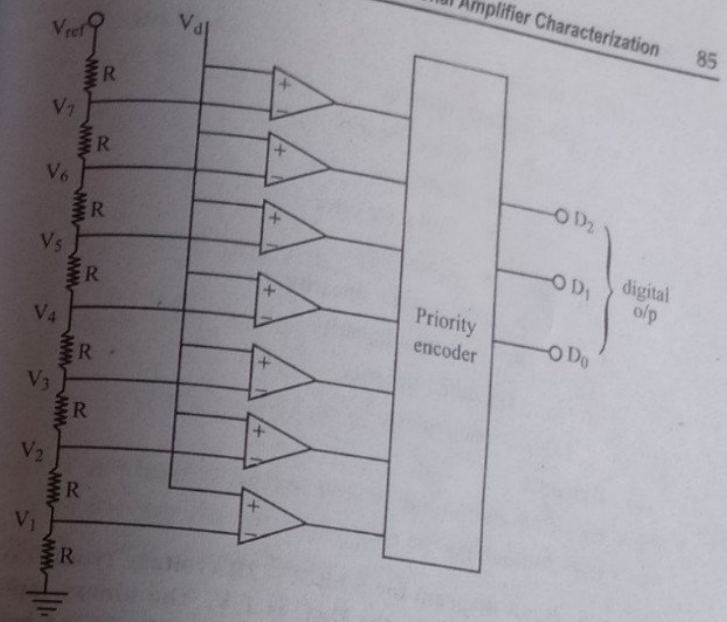
4. Draw and explain the circuit diagram of flash type of ADC. What are the demerits of flash type ADC over other ADC's?

[2078 Kartik, 2075 Ashwin, 2071 Shrawan]

olution:

The flash type ADC (simultaneous ADC) is the fastest ADC that utilizes comparator that compares reference voltage with analog voltage. Along comparators priority encoder is used to convert the output of comparator into the digital output.

For n-bit ADC, 2^{n-1} comparator are required so it' is very expensive. 's conversion time is less and can even digitize video signal.



If $V_{ref} = 8$ V

So, $V_1 = 1V$, $V_2 = 2V$, $V_3 = 3V$, $V_4 = 4V$, $V_5 = 5V$, $V_6 = 6V$ and $V_7 = 7V$

So, If $V_a < 1V$, input to priority encoder = 0000000

If $2 < V_a \leq 1V$, input priority encoder = 000000 1

If you want the output 0 for $V_a < 0.5$ V.

The bottom resistor can be replaced by $\frac{R}{2}$ and the top resistor with $\frac{3R}{2}$

Advantages

(a) Very fast

(b) Clock is not required

Disadvantages

(a) Expensive and high power consumption

(b) Complexity doubles for each additional bits.

Characteristics of D/A A/D converter

(a) Static

(i) resolution

(ii) Linearity

(1) Integral linearity

- Absolute linearity
  - Zero scale error
  - Full scale error
  - Gain error
- Best straight linearity
- End point linearity

(2) Diffential linearity

(3) Monotonously

(b) Dynamic

(i) Conversion time

(ii) Setting time

5. Draw a circuit diagram for 5 bit R – 2R (voltage type) DAC if the reference voltage for the DAC is 1 V. The binary input is 10110, find the output voltage. [2072 Chaitra, 2071 Chaitra]

Solution:

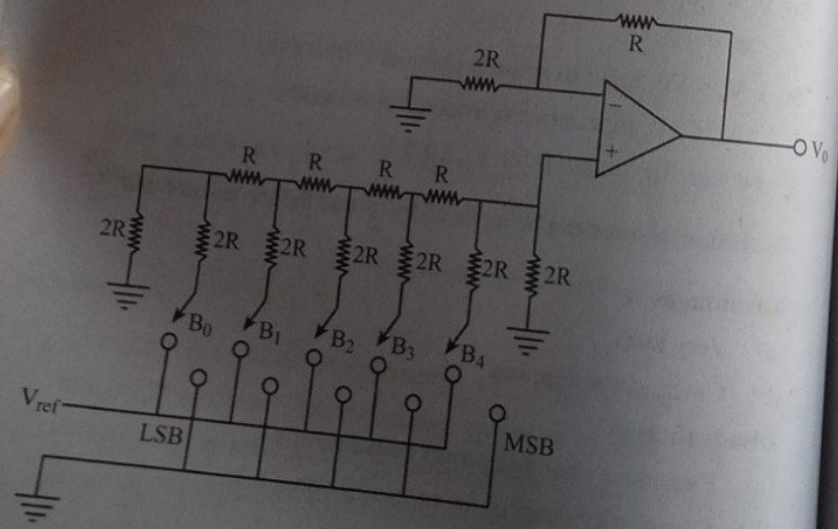


Fig: 5 bit R – 2R ladder type DAC

$V_{ref} = 1$ V

Input = 10110

$V_0 = ?$

$n = 5$

$$V_0 = \frac{V_{ref}}{2^n} D$$

$$= \frac{V_{ref}}{2^5} [B_4 2^4 + B_3 2^3 + B_2 2^2 + B_1 2^1 + B_0 2^0]$$

$$= \frac{1}{2^5} [1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2]$$

$$= \frac{1}{3^2} \times 22 = 0.6875 \text{ V}$$

6. Draw the block diagram of dual-slope type ADC and explain about it's working principle with necessary diagram. Explain briefly about integral linearity of DAC. [2071 Chaitra]

Solution:

Part I: Please refer to theory

Part II: Integral linearity is the maximum derivation of the output of a D/A for any given input code from a straight line drawn from it's ideal maximum to it's actual maximum.

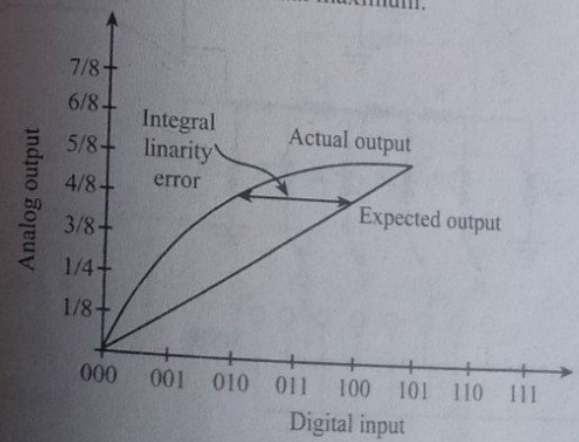


Fig: integral linearity error

(a) Absolute linearity: It is measured by assuming that output of D/A will begin at zero and end at full scale.

(b) **Best straight line linearity:** It depicts the accuracy of a D in term of the derivation from the ideal output range with regard to zero or full is code error.

(c) **End point linearity:** It uses a straight line through the actu end points instead of the ideal points.

7. What are the advantage of R – 2R type DAC? Derive the expression for voltage inverted R – 2R type DAC.

[2074 Ashwin, 2074 Chaitra

Solution:

Part I: The advantages of R – 2R type DAC is given below:

- Uses only two values of resistors R and 2R

Part II: If the R – 2R ladder network is operated in voltage mod then it is known as voltage mode R – 2R ladder which is used as current splitting device.

In this mode resistance at left or right side of the ladder from any made is 2R. As a result this current splits half at each made giving rise to binary weighted Seq. of current.

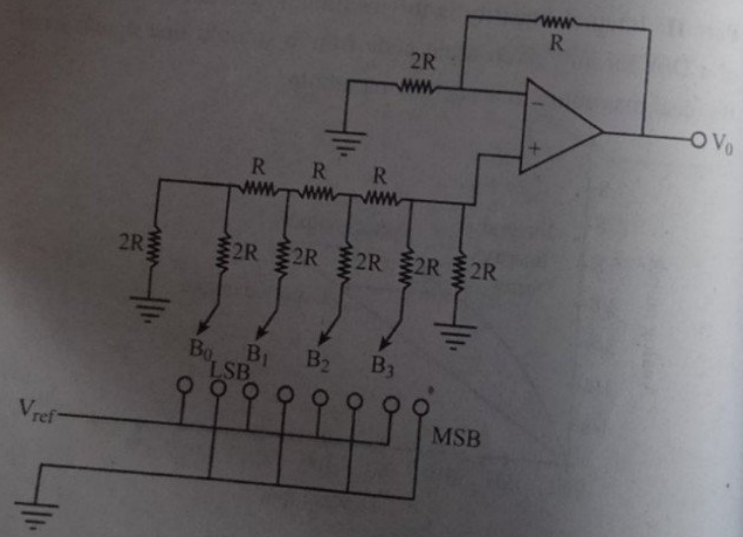
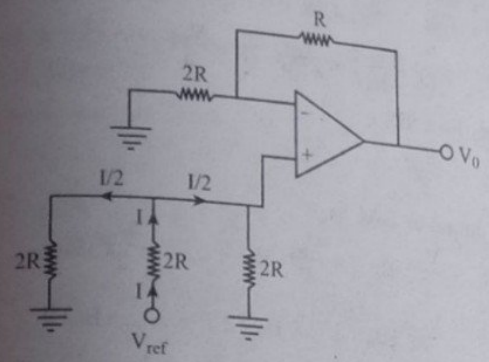


Fig: 4-bit R-2R ladder type DAC

When MSB is high and all other bits are low.

From figure,



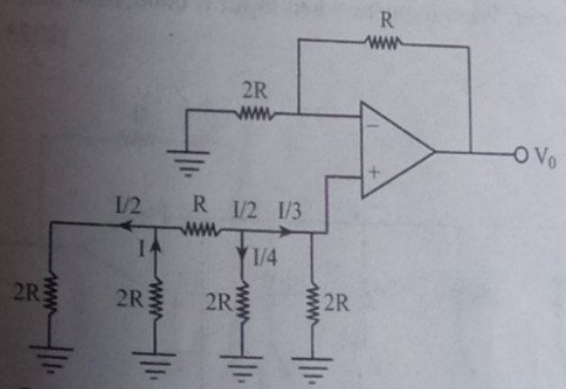
$$I = \frac{V_{ref}}{(2R//2R) + 2R}$$

$$= \frac{V_{ref}}{3R}$$

$$V^{+} = \frac{I}{2} \times 2R = \frac{V_{ref}}{3R.2} \cdot 2R = \frac{V_{ref}}{3}$$

and, $V_0 = \left(1 + \frac{R}{2R}\right) V^{+} = \frac{V_{ref}}{2}$

When next MSB is high and all other bits are low.



From figure,

$$I = \frac{V_{ref}}{(2R//2R + R)//2R + 2R}$$

$$= \frac{V_{ref}}{3R}$$

and, $V^{+} = \frac{I}{4} \times 2R = \frac{V_{ref}}{4.3R} \times 2R$

$$V_0 = \left(1 + \frac{R}{2R}\right) \times \frac{V_{ref}}{4.3R} \cdot 2R = \frac{V_{ref}}{4}$$

Similarly for LSB,

$$V_0 = \frac{V_{ref}}{2^n}$$

So, the output of DAC is,

$$V_0 = \frac{V_{ref}}{2} B_{n-1} + \frac{V_{ref}}{2^2} B_{n-2} + \dots\dots + \frac{V_{ref}}{2^n} B_0$$

$$= \frac{V_{ref}}{2^n} [B_{n-1} 2^{n-1} + B_{n-2} 2^{n-2} + \dots\dots + B_0 2^0]$$

$$= \frac{V_{ref}}{2^n} D$$

8. Draw circuit for 4 bits inverted R – 2R ladder network type DAC. Find the expression for output voltage and explain why inverted R – 2R ladder DAC is better than R – 2R ladder DAC.

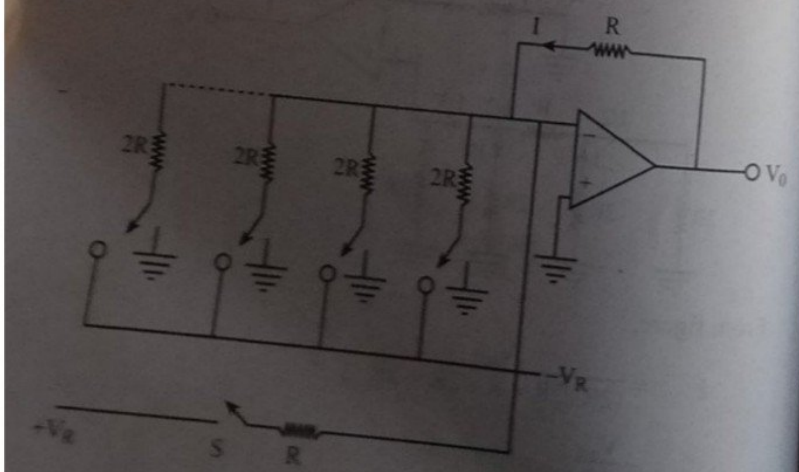
Solution:

Part I: Similar to 2071 Chaitra

Part II: Refer to theory

9. List out the advantages of bipolar D/A converter over binary weighted register. express output voltage of bipolar D/A converter. What happens when input is 0000,1000 and 1111?

Solution: **[2073 Chaitra]**



Bipolar DAC uses offset binary coding .It's is low the DAC will work a_1= usual it's output varies from 0 V to above 2 V voltage. When S is high the output will vary from – VR to + VR and hence acts as bipolar DAC.

Using KCL, we get

$$I_0 + I_n = I_1 + I_2 + I_3 + \dots\dots + I_n$$

$$\frac{V_0}{R} + \frac{V_R}{R} = \frac{V_R}{R} d_1 + \frac{V_R}{2R} d_2 + \frac{V_R}{2^2 R} d_3 + \dots\dots + \frac{V_R}{2^{n-1} R} d_n$$

$$V_0 = V_R \left(d_1 + \frac{d_2}{2} + \frac{d_3}{2^2} + \dots\dots + \frac{d_n}{2^{n-1}}\right) - V_R$$

$$V_0 = \frac{V_R}{2^{n-1}} (2^{n-1} d_1 + 2^{n-2} d_2 + 2^{n-3} d_3 + \dots\dots d_n) - V_R$$

$$V_0 = \frac{V_R}{2^{n-1}} (D) - V_R$$

Then for input word 0000 0

$$V_0 = -V_R$$

For input word 10000 0

$$V_0 = V_R - V_R = 0$$

For input word, 111 1

$$V_0 = \frac{V_R}{2^{n-1}} (2^n - 1) - V_R$$

$$= \frac{V_R 2^n}{2^{n-1}} - \frac{V_R}{2^{n-1}} - V_R$$

$$= 2V_R - V_R - \frac{V_R}{2^{n-1}}$$

$$= V_R - \frac{V_R}{2^{n-1}} \qquad \left(\because \frac{V_R}{2^{n-1}} \approx 0\right)$$

$\therefore$ $V_0 \approx +V_R$ (Approximate)

10. Draw and explain the circuit diagram of flash type ADC. What are the demerits of flash type ADC over other ADC'S?

[2071 Sharwan, 2069 Ashad]

Solution: Refer to theory.

and, $V^{+} = \frac{I}{4} \times 2R = \frac{V_{ref}}{4.3R} \times 2R$

$$V_0 = \left(1 + \frac{R}{2R}\right) \times \frac{V_{ref}}{4.3R} \cdot 2R = \frac{V_{ref}}{4}$$

Similarly for LSB,

$$V_0 = \frac{V_{ref}}{2^n}$$

So, the output of DAC is,

$$V_0 = \frac{V_{ref}}{2} B_{n-1} + \frac{V_{ref}}{2^2} B_{n-2} + \dots\dots + \frac{V_{ref}}{2^n} B_0$$

$$= \frac{V_{ref}}{2^n} [B_{n-1} 2^{n-1} + B_{n-2} 2^{n-2} + \dots\dots + B_0 2^0]$$

$$= \frac{V_{ref}}{2^n} D$$

8. Draw circuit for 4 bits inverted R – 2R ladder network ty DAC. Find the expression for output voltage and explain wh inverted R – 2R ladder DAC is better than R – 2R ladder DAC

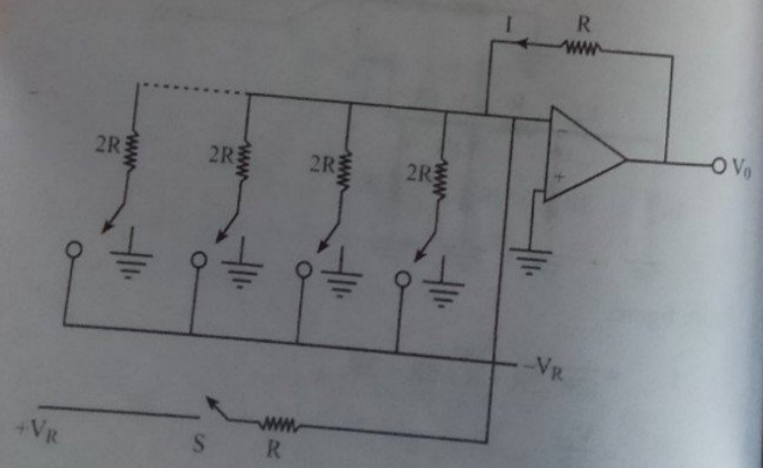
Solution:

Part I: Similar to 2071 Chaitra

Part II: Refer to theory

9. List out the advantages of bipolar D/A converter over binar weighted register. express output voltage of bipolar D/ converter. What happens when input is 0000,1000 and 1111?

Solution: [2073 Chaitra



Bipolar DAC uses offset binary coding .It's is low the DAC will work a_1= usual it's output varies from 0 V to above 2 V voltage. When S is high the output will vary from – VR to + VR and hence acts as bipolar DAC.

Using KCL, we get

$$I_0 + I_n = I_1 + I_2 + I_3 + \dots\dots + I_n$$

$$\frac{V_0}{R} + \frac{V_R}{R} = \frac{V_R}{R} d_1 + \frac{V_R}{2R} d_2 + \frac{V_R}{2^2R} d_3 + \dots\dots + \frac{V_R}{2^{n-1}R} d_n$$

$$V_0 = V_R \left(d_1 + \frac{d_2}{2} + \frac{d_3}{2^2} + \dots\dots + \frac{d_n}{2^{n-1}}\right) - V_R$$

$$V_0 = \frac{V_R}{2^{n-1}} (2^{n-1} d_1 + 2^{n-2} d_2 + 2^{n-3} d_3 + \dots\dots d_n) - V_R$$

$$V_0 = \frac{V_R}{2^{n-1}} (D) - V_R$$

Then for input word 0000 0

$$V_0 = -V_R$$

For input word 10000 0

$$V_0 = V_R - V_R = 0$$

For input word, 111 1

$$V_0 = \frac{V_R}{2^{n-1}} (2^n - 1) - V_R$$

$$= \frac{V_R 2^n}{2^{n-1}} - \frac{V_R}{2^{n-1}} - V_R$$

$$= 2V_R - V_R - \frac{V_R}{2^{n-1}}$$

$$= V_R - \frac{V_R}{2^{n-1}} \qquad \left(\because \frac{V_R}{2^{n-1}} \approx 0\right)$$

$\therefore$ $V_0 \approx +V_R$ (Approximate)

10. Draw and explain the circuit diagram of flash type ADC. What are the demerits of flash type ADC over other ADC'S?

[2071 Sharwan, 2069 Ashad]

Solution: Refer to theory.

11. Derive the expression for output voltage of R–2R ladder DA (voltage mode). List out demerits of Binary weighted resis DAC. [2077 Chaitr

Solution: Refer to theory (3.1)

12. For a 5-bit DAC with the reference voltage V_r being 10V, there is the is the fluctuation in the reference voltage of abo 10% what will be the deviation in the output for MSB and LS due to this fluctuation? [2077 Chaitr

Solution: Refer to theory

13. How does sigma delta ADC work? Justify with suitabl example. Write demerit of count up type ADC. [2075 Chaitr

Solution: Refer to theory (3.6)

❖❖❖

Chapter 4

Instrumentation and Isolation Amplifier

IA is dedicated differential amplifier with extremely high input impedance (to avoid loading effect) to recover small signal buried in large common mode noise and precise gain settling.

In general required in any measured system that uses electrical transducer to enhance the signal level which is often of low strength.

Characteristic of instrumentation amplifier

Practical characteristics of IA.

- High input impedance
- Low output impedance
- High CMRR
- High gain accuracy
- High gain stability with low temperature coefficient
- Low dc offset

Ideal characteristics of IA.

- Infinite input impedance
- Zero output impedance
- Infinite CMRR
- A constant gain factor with no gain error
- Zero amplifier noise
- Zero dc offset

4.1 Types of I.A.

(a) Single op-amp IA

(i) Single op-amp I.A with matched resistor

(ii) Single op-amp I.A with mismatched resistor

(b) Two op-amp IA.

(c) Three op-amp IA.

4.1.1 Single op-amp IA

(a) Single op-amp with matched resistor

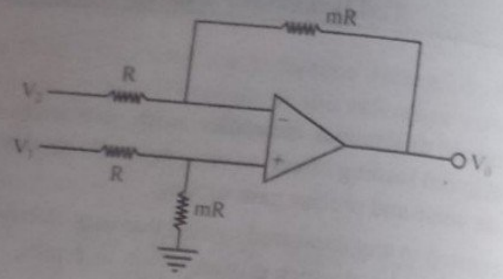


Fig: single op-amp I.A.

Above figure describes the configuration of single op-amp instrumentation amplifier with matched resistor 'm'

On applying superposition theorem,

$$V^{+} = \frac{mR}{mR + R} \cdot V_1 = \left(\frac{m}{m+1}\right) \times V$$

$$V_0^{+} = \left(1 + \frac{mR}{R}\right) \times v^{+}$$

$$= (1 + m)\frac{m}{(m+1)} V_1$$

$$= mV_1$$

Set $V_1 = 0$

$$V_0^{-} = \frac{-mR}{R} \times V_2$$

The resultant o/p is,

$$V_0 = V_0^{+} + V_0^{-}$$

$$= m(V_1 - V_2)$$

So single op-amp I.A is differential amplifier.

Single op-amp I.A with mismatched resistor

- In this type of I.A mismatched resistor is used and common mode signal along with differential signal is considered because, a common mode signal is also present in almost transducer.

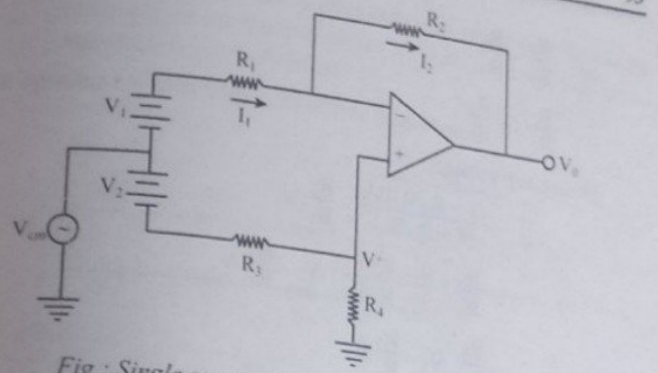


Fig : Single op-amp I.A with mismatched resistor

$$V^{+} = \frac{R}{R_3 + R_4}(V_{cm} + V_2) \quad \text{..... (i)}$$

Ideal op-amp draws no current so,

$$I_1 = I_2$$

$$\frac{V_{cm} + V_1 - V^{+}}{R_1} = \frac{V^{+} - V_0}{r_2} \quad \text{..... (ii)}$$

or, $V^{+} - V_0 = \frac{R_2}{R_1}(V_{cm} + V_1 - V^{+})$

$$V_0 = V^{+} - \frac{R_2}{R_1}(V_{cm} + V_1 - V^{+})$$

$$= \frac{R_4}{R_3 + R_4}(V_{cm} + V_2) - \frac{R_2}{R_1}\left(V_{cm} + V_1 - \frac{R_4}{R_3 + R_4}V_{cm} + V_2\right)$$

From equation (i)

$$= (V_{cm} + V_2)\frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1}(V_{cm} + V_1)$$

$$= \left(\frac{R_1R_4 + R_2R_4}{R_1(R_3 + R_4)} - \frac{R_2}{R_1}\right)V_{cm} + \frac{R_1R_4 + R_2R_4}{R_1(R_3 + R_4)} - \frac{R_2}{R_1}V_1$$

$$= \left[\frac{R_1R_4 + R_2R_4 - R_2R_3 - R_2R_4}{R_1(R_3 + R_4)}\right]V_{cm} + \frac{R_1R_4(1 + R_2/R_1)}{R_1R_4(1 + R_3/R_4)} - \frac{R_2}{R_1}V_1$$

For instrumentation amplifier to reject common mode signal V_{cm},

$$R_1R_4 - R_2R_3 = 0$$

or, $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$\therefore \frac{R_2}{R_1} = \frac{R_4}{R_3}$

Hence, o/p voltage,

$$V_0 = \frac{(1 + R_2/R_1)V_2}{(1 + R_3/R_4)} - \frac{R_2}{R_1} V_1$$

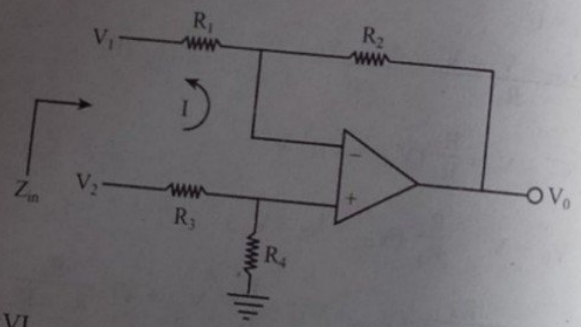
$$= \frac{R_4}{R_3}\left(\frac{1 + R_2/R_1}{1 + R_4/R_3}\right) V_2 - \frac{R_2}{R_1} V_1$$

$$= \frac{R_2}{R_1} V_2 - \frac{R_2}{R_1} V_1$$

$$= \frac{R_2}{R_1} (V_2 - V_1)$$

For i/p impedance,

$$Z_{in} = \frac{V_2 - V_1}{I}$$



Applying kVL,

$$V_2 - V_1 - IR_1 - IR_3 = 0$$

$$V_2 - V_1 - I\ (R_1 + R_3) = 0$$

$$\frac{V_2 - V_1}{I} = Z_{in} = R_1 + R_3$$

If $R_1 = R_3$ $\quad (\because Z_{in} = R_1 + R_3 = 2R)$

Limitation of resistor mismatched single op-amp I.A.

(a) It is difficult to change the gain because it should maintain the ratio $\frac{R_2}{R_1} = \frac{R_4}{R_3}$ at the same

- When I/A is required to have large difference gain R_1 should relatively be small which means it's input impedance decrease and result is source loading.

Single op-amp IA with non- zero source impedance:

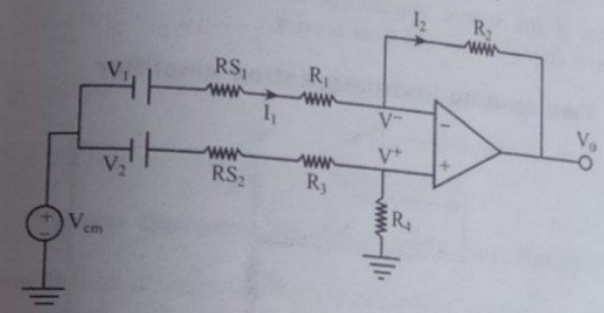


Fig: Single OP-Amp IA with non-zero source impedance

R_{S1} and R_{S2} are internal resistance of source V_1 and V_2 respectively.

If $R_{S1} = R_{S2}$; balance

$R_{S1} \neq R_{S2}$; unbalance

From the voltage divider rule;

$$V^+ = \frac{V_{cm} + V_2}{R_3 + R_4 + RS_2} R_4$$

For ideal op-amp Rin is infinite and

Due to virtual short circuit, $V^+ = V^-$ iii

$$I_1 = I_2$$

$$\frac{V_{cm} + V_1 - V^-}{R_1 + RS_1} = \frac{V^- - V_0}{R_2}$$

Solving equations

$$V_0 = \frac{V_{cm}(R_1R_4 + RS_1 R_4 - R_2 R_3 - R_2 RS_2)}{(R_1 + RS_1)(R_3 + RS_2 + R_4)}$$

$$+ \frac{R_2}{R_1 + RS_1}\left\{\frac{\left(1 + \frac{R_1 + RS_1}{R_2}\right)}{\left(1 + \frac{R_3 + RS_2}{R_4}\right)} V_2 - V_1\right\}$$

If the source impedance are not zero but equal i.e. $R_{S1} = R_{S2}$, the only effect is gain error because the ratio remains still the same.

$$\frac{R_2}{R_1 + RS_1} = \frac{R_4}{R_3 + RS_2}$$

$$\therefore \quad V_0 = \frac{R_2}{R_1 + RS_1}(V_2 - V_1)$$

However, if the source impedances are unequal the common mode rejection is degraded and also there is error.

4.1.2 Two op-amp instrumentation amplifier

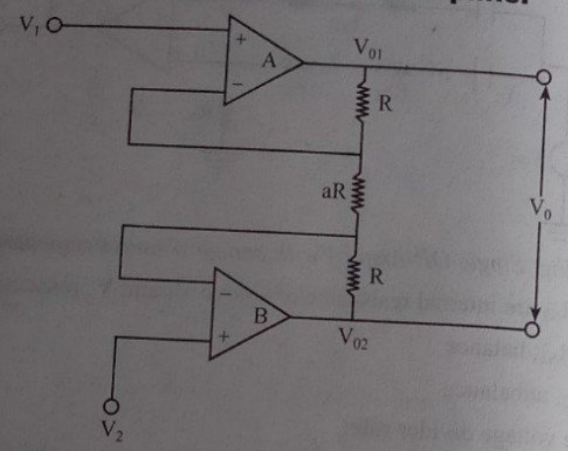


Fig: Two op-amp instrumentation amplifier

If the op-amp are ideal due to virtual short circuit of the input terminal, the i/p voltage, V_1 and V_2 appears at the two terminal of 'aR'.

Thus, the differential i/p voltage $(V_1 - V_2)$ appears across 'aR' resistor.

So, $I = \dfrac{V_1 - V_2}{aR}$ ... ... (i)

From figure, o/p of an op-amp A is given by

$$V_{01} - V_1 = IR$$

or, $V_{01} = V_1 + IR$

$$V_{01} = V_1 + \left(\frac{V_1 - V_2}{aR}\right) R \quad \text{... ... (ii)}$$

Similarly, o/p of op-amp B is given by

$$V_2 - V_{02} = IR$$

$$V_{02} = V_2 - IR$$

or, $V_{02} = V_2 - \dfrac{(V_1 - V_2)}{aR} . R$

The o/p of V_0 is given by,

$$V_0 = V_{01} - V_{02}$$

$$= V_1 - V_2 + \frac{(V_1 - V_2)}{aR} . R + \frac{(V_1 - V_2)}{aR} . R$$

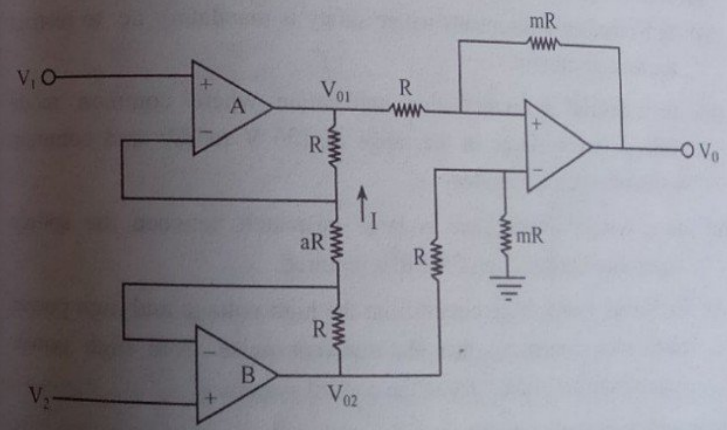
$$= V_1 - V_2 + 2\frac{(V_1 - V_2)}{a}$$

$$V_0 = (V_1 - V_2)\left(1 + \frac{2}{a}\right)$$

Which is the required expression for output voltage.

4.2 There Op-amp Instrumentation Amplifier

The combination of single op-amp and two amp instrumentation amplifier is known as three op-amp instrumentation amplifier. In first stage op-amp are configured as voltage follower so they offer very high impedance to the both inputs. Second stage is differential amplifier two resistor R_1 of first stage are internal to IC while R_2 being gain setting resistor can be internally or externally connected.



The o/p of two op-amp I.A is,

$$V_0 = V_{01} - V_{02} = (V_1 - V_2)(1 + 2/a)$$

And the o/p of single op-amp I.A is,

$$V_0 = m(V_{01} - V_{02})$$

$$= m(V_1 - V_2)(1 + 2/a)$$

4.3 Consideration of Non-ideal Prosperities

Following consideration are considered in 3 – op-amp.

- Very high impedance
- Gain depends on only one resistor
- I_{rad} is grounded
- Second stage completely remove any common signal appearing in first stage.

4.4 Isolation Amplifier Principles and Realization

It is similar to instrumentation amplifier having fixed differential gain over wide frequency range, high input impedance and low output impedance.

Isolation amplifier are used when two stages are to be separated in such a way that output depend on input however any variations in the output has no effect on the input.

Application of isolation amplifier

(a) In biomedical instruments where safety is mandatory i.e. to restrict the leakage current.

(b) In industrial instrumentation application where common mode voltage is very large in the range of 100 V to KV and common mode rejection is required.

(c) In a system where there is large mismatch between the source impedance but still high CMRR is required.

(d) To isolate low voltage circuit from the high voltage and high power electronics system so that the transient noise from high power system may not come back to the control system.

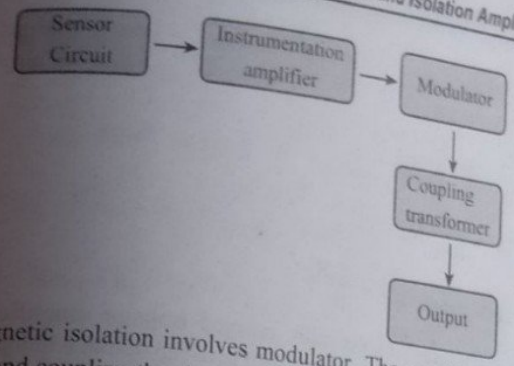
Types of I.A (Isolation Amp)

- **There are two types of isolation amplifier they are:**

(a) Electromagnetically coupled isolation amplifier

(b) Optical coupled amplifier

(a) Electromagnetically coupled isolation amplifier



Electromagnetic isolation involves modulator. The amplified signal with frequency and coupling the signal to output circuit using transformer. The transformer provides efficient coupling at the carrier frequency but has high impedance path at frequency when dangerous current mi9ght occurs such as (220 V/50 H_z).

(b) Optically coupled isolation amplifier

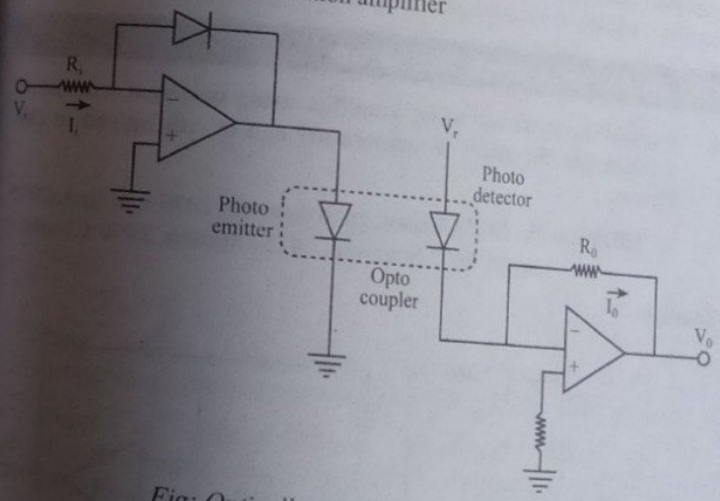


Fig: Optically coupled isolation amplifier

In optically coupled isolation amplifier. The i/p current I_1 due to the i/p signal excites the photo emitter to produce the light the intensity of the light depends on the i/p current the photo detector of o/p circuit detects. The light emitted by the photo emitter and cause (I_0) output current to flow through Ro. This o/p current provides the o/p signal.

Here, $I_0 \alpha I_i$

or, $I_0 = K_0 I_i$

and, $V_0 = -I_0R_0$

$$= -k_0I_1R_0$$

$$= -K_0\frac{V_i}{R_i}R_0$$

$$= \frac{-K_0R_0}{R_i}V_i$$

$$V_0 = k'V_i \text{ where } k' = \frac{-K_0R_0}{R_i}$$

The main advantages of optically coupled isolation amplifier is that completely eliminate the electrical path between output and input section

Advantages of 3 op-amp

An instrumentation amplifier has lower noise and common mod rejection ratio than standard operational amplifier. The CMRR important because we usually need to measure a small amount that ca oscillate violently around the ground.

Old Questions with Solution

1. Explain the operation of log amplifier using matched transistor. Explain how the effect of temperature can be minimized in this circuit.

[2078 Kartik, 2077 Chaitra, 2076 Ashwin, 2075 Chaitra, 2075 Ashwin, 2073 Sharwan, 2072 Chaitra, 2070 Chaitra]

Solution:

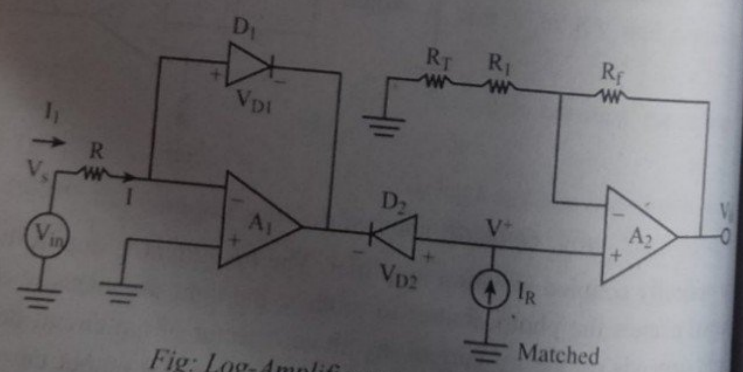


Fig: Log-Amplifier using two diode

Instead of two matched diodes it is possible to use a matched pair of transistor connected as in the figure to remove from the expression V_0 the factor η whose value normally depends upon the current flowing through diodes.

From figure,

$$V_{cc} = I_{c_2}R_5 + V_{BE_2} - V_{BE_1}$$

$\therefore \quad I_{c_2} = \frac{V_{cc}}{R_5}$ Again we have,

$$V_{BE_1} - V_{BE_2} = V_T\, l_n\left(\frac{I_{c1}}{I_s}\right) - V_T\, l_n\left(\frac{I_{c2}}{I_s}\right)$$

or, $0 - V_{E_1} - V_{B_2} + V_{E_2} = V_T\, l_n\left(\frac{I_{c_1}}{I_{c_2}}\right)$

or, $V_{B_2} = -V_T\, l_n\left(\frac{I_{c_1}}{I_{c_2}}\right) \qquad (\because V_{E_1} = V_{E_2})$

$$\therefore \quad V_0 = \left(1 + \frac{R_3}{R_4}\right)^{V_{B2}}$$

$$= \left(1 + \frac{R_3}{R_4}\right)\left[-V_T\, l_n\left(\frac{I_{c_1}}{I_{c_2}}\right)\right]$$

$$= -V_T\left(1 + \frac{R_3}{R_4}\right) l_n\left(\frac{I_{c_1}}{I_{c_2}}\right)$$

$$= -V_T\left(1 + \frac{R_3}{R_4}\right) l_n\left(\frac{V_{in}/R_1}{V_{cc}/R_5}\right)$$

Let $K_1 = -V_T(1 + R_3/R_4)$ and $K_2 = \left(\frac{R_1}{R_5V_{cc}}\right)$

Then,

$$V_0 = K_1\, l_n(k_2 V_{in})$$

Part II: The effect of temperature can be minimized by using temperature dependent resistor Rc which nully the effect of V_T.

2. What is instrumentation amplifier? What are it's characteristics? Derive necessary relation to find the input impedance and output voltage in case of single op-amp instrumentation amplifier with mismatched resistance.

[2077 Chaitra, 2075 Ashwin, 2074 Chaitra, 2074 Ashwin, 2073 Shrawan, 2073 Kartik, 2072 Kartik, 2072 Chaitra, 2071 Shrawan, 2069 Ashad, 2069 Chaitra]

Solution:

IA is dedicated differential amplifier with extremely high input impedance (to avoid loading effect) to recover small signal buried in large common mode noise and precise gain settling.

In general required in any measured system that uses electric transducer to enhance the signal level which is often of low strength.

Characteristic of instrumentation amplifier.

Practical characteristics of IA.

- High input impedance
- Low output impedance
- High CMRR
- High gain accuracy
- High gain stability with low temperature coefficient
- Low dc offset

Ideal characteristics of IA.

- Infinite input impedance
- Zero output impedance
- Infinite CMRR
- A constant gain factor with no gain error
- Zero amplifier noise
- Zero dc offset

Single op-amp I.A with mismatched resistor

- In this type of I.A mismatched resistor is used and common mode signal along with differential signal is considered because a common mode signal is also present in almost transducer.

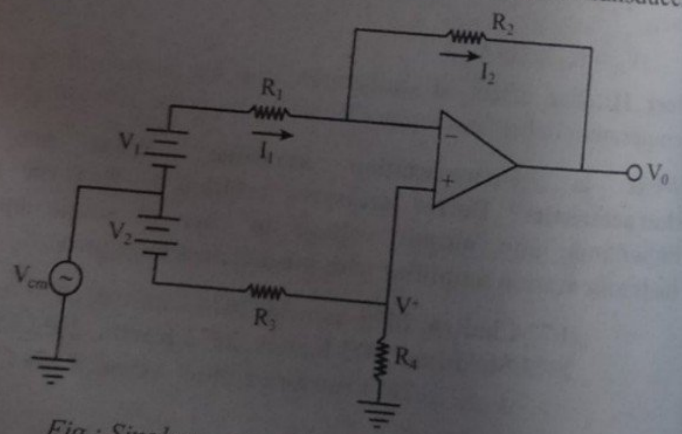


Fig : Single op-amp I.A with mismatched resistor

$$V^+ = \frac{R}{R_3 + R_4}(V_{cm} + V_2) \quad \text{..... (i)}$$

Ideal op-amp draws no current so,

$$I_1 = I_2$$

$$\frac{V_{cm} + V_1 - V^+}{R_1} = \frac{V^+ - V_0}{r_2} \quad \text{..... (ii)}$$

or, $$V^+ - V_0 = \frac{R_2}{R_1}(V_{cm} + V_1 - V^+)$$

$$V_0 = V^+ - \frac{R_2}{R_1}(V_{cm} + V_1 - V^+)$$

$$= \frac{R_4}{R_3 + R_4}(V_{cm} + V_2) - \frac{R_2}{R_1}\left(V_{cm} + V_1 - \frac{R_4}{R_3 + R_4}V_{cm} + V_2\right)$$

From equation (i)

$$= (V_{cm} + V_2)\frac{R_4}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right) - \frac{R_2}{R_1}(V_{cm} + V_1)$$

$$= \left(\frac{R_1R_4 + R_2R_4}{R_1(R_3 + R_4)} - \frac{R_2}{R_1}\right)V_{cm} + \frac{R_1R_4 + R_2R_4}{R_1(R_3 + R_4)} - \frac{R_2}{R_1}V_1$$

$$= \left[\frac{R_1R_4 + R_2R_4 - R_2R_3 - R_2R_4}{R_1(R_3 + R_4)}\right]V_{cm} + \frac{R_1R_4(1 + R_2/R_1)}{R_1R_4(1 + R_3/R_4)} - \frac{R_2}{R_1}V_1$$

For instrumentation amplifier to reject common mode signal V_{cm}.

$$R_1R_4 - R_2R_3 = 0$$

or, $$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

$$\therefore \frac{R_2}{R_1} = \frac{R_4}{R_3}$$

Hence, o/p voltage,

$$V_0 = \frac{(1 + R_2/R_1)V_2}{(1 + R_3/R_4)} - \frac{R_2}{R_1}V_1$$

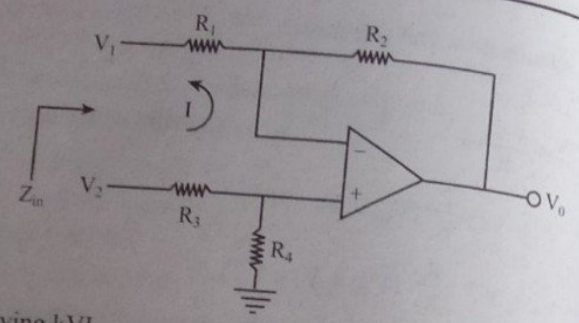
$$= \frac{R_4}{R_3}\left(\frac{1 + R_2/R_1}{1 + R_4/R_3}\right)V_2 - \frac{R_2}{R_1}V_1$$

$$= \frac{R_2}{R_1}V_2 - \frac{R_2}{R_1}V_1$$

$$= \frac{R_2}{R_1}(V_2 - V_1)$$

For i/p impedance,

$$Z_{in} = \frac{V_2 - V_1}{I}$$



Applying kVL,

$$V_2 - V_1 - IR_1 - IR_3 = 0$$

$$V_2 - V_1 - I\ (R_1 + R_3) = 0$$

$$\frac{V_2 - V_1}{I} = Z_{in} = R_1 + R_3$$

If $R_1 = R_3$ $\quad (\because Z_{in} = R_1 + R_3 = 2R)$

Limitation of resistor mismatched single op-amp I.A.

It is difficult to change the gain because it should maintain the ra

$\frac{R_2}{R_1} = \frac{R_4}{R_3}$ at the same

When I/A is required to have large difference gain R_1 shou relatively be small which means it's input impedance decrease a result is source loading.

3. Determine the condition required to reject common mode signa in a single op-amp instrumentation amplifier with mismatche resistor, list out the application of isolation amplifiers.

[2076 Ashwin, 2076 Chaitra, 2071 Shrawa

Solution: Refer to theory

Derive up to; for instrumentation amplifier to reject common mod signal V_{cm}

$$\frac{R_2}{R_1} = \frac{R_4}{R_3}$$

Application of isolation amplifier

(a) In biomedical instruments where safety is mandatory i.e. t restrict the leakage current.

(b) In industrial instrumentation application where common mod voltage is very large in the range of 100 V to KV and commo mode rejection is required.

(c) In a system where there is large mismatch between the source impedance but still high CMRR is required.

(d) To isolate low voltage circuit from the high voltage and high power electronics system so that the transient noise from high power system may not come back to the control system.

4. What are the advantages of 3 op-amp. IA over 1 – op-amp and 2 op-amp. List out the application of isolation amplifier. Explain the block diagram of electromagnetically coupled isolation amplifier?

[2071 Chaitra]

Solution: The advantages of 3 op-amp IA over 1 – op-amp and 2 op-amp IA are given below:

(a) Input impedance is very high.

(b) Gain depends only on one resistor.

(c) Any common mode signal appearing in first stage is completely removed by second stage.

Part II:

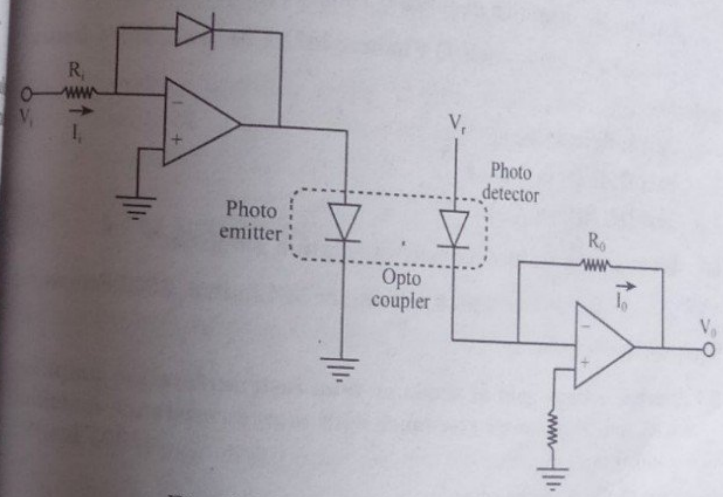


Fig: Optically coupled isolation amplifier

In optically coupled isolation amplifier. The i/p current I_i due to the i/p signal excites the photo emitter to produce the light the intensity of the light depends on the i/p current the photo detector of o/p circuit detects. The light emitted by the photo emitter and cause (I_0) output current to flow through Ro. This o/p current provides the o/p signal.

Here, $I_0 \alpha I_i$

or, $I_0 = K_0 I_i$

and, $V_0 = -I_0 R_0$

$$= -k_0 I_i R_0$$

$$= -K_0 \frac{V_i}{R_i} R_0$$

$$= \frac{-K_0 R_0}{R_i} V_i$$

$V_0 = k' V_i$ where $k' = \frac{-K_0 R_0}{R_i}$

The main advantages of optically coupled isolation amplifier is t it completely eliminate the electrical path between output and inp section.

5. **List out the practical characteristics of instrumentation amplifie What are the advantages of 3 op-amp instrumentation amplifi over one op-amp and two op-amp instrumentation amplifier Explain the operation of optically coupled isolation amplifier.**

[2073 Chaitra, 2072 Chaitra, 2069 Chaitra

Solution:

Part I: Refer to theory

Part II: Refer to Q no. 4

Part III: Refer to Q. No. 4

6. **What are the features of instrumentation amplifier?**

[2074 Ashwin, 2074 Chaitra, 2073 Sharwan

Solution: Refer to theory.

8. **Derive voltage gain of single op-amp instrumentation amplifier with non zero source resistance with source resistance matching condition.**

[2073 Kartik

Solution: Refer to theory (4.1)

6. **What are the features of Instrumentation Amplifier? Hence design a three op amp Instrumentation Amplifier having gain 50.**

[2075 Ashwin]

Solution: Refer to theory

❖❖❖

Chapter 5 Operational Amplifier-Bipolar Transistor Logarithmic Amplifier

Log and antilog amplifier are non-linear circuits in which the output voltage is proportional to the log or exponent of the input voltage respectively. Simple log and antilog amplifier are designed using the combination of op-amp and diode or transistor.

Application of log and antilog amplifier.

(a) Compression and Decompression of data

(b) To calculate the dB value of a given quantity

(c) Process control

(d) As a True RMS converter

(e) To perform mathematical operation like multiplication division, and exponentiation. (Multiplication is also sometime called mixing)

(f) Extending dynamic range of other circuit, like automatic gain control of transmit power in RF circuit or analog-to-digital converters.

5.1 Log amplifier

A log amplifier is an amplifier for which the output voltage V_{out} is k times the natural log of the input voltage V_{in}. This can be expressed as,

$$V_{out} = k\, ln\left(\frac{V_{in}}{V_{ref}}\right)$$

Where V_{ref} is the normalization constant k is the scale factor.

The logarithm amplifier gives an output voltage which is proportional to the logarithm of applied input voltage. To design a logarithm amplifier circuit, high performance of op-amps like LM1458, LM771, LM714 are commonly used and a compensated logarithm amplifier may include more than one in some situations, especially in RF domain, monolithic logarithmic amplifiers are also used to reduce number of components and space used, as well improve land width and noise performance.

Characteristics and features of log amplifier

(a) It has o/p voltage which is proportional to the logarithm of i/p voltage.

(b) Certain amplification of logarithmic amplifier is same as that of inverting configuration.

(c) The feedback element may be diode or BJT.

(d) Logarithmic amplifier offers significant dynamic range compression.

(e) The output signal gets distorted once the dynamic range of the signal has been compressed by the amplifier.

(f) The characteristics of LA are dependent on reverse saturation current I_s which is extremely temperature dependent and hence difficult of to control.

5.1.1 Log amplifier using simple op-amp and diode

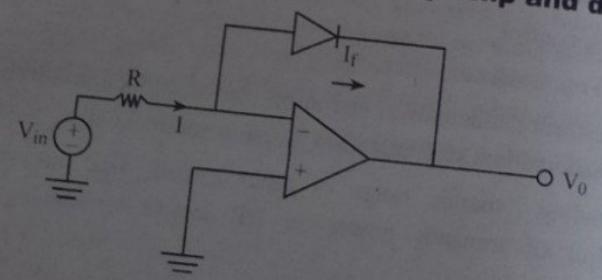


Fig: Opamp-diode log amplifier.

The scamatic of a simple Opamp-diode log amplifier is shown above. This is nothing but an opamp wired in closed loop inverting configuration with a diode in the feedback path. The voltage across the diode will be always proportional to the log of the current through it and when a diode is placed in the feedback path of an opamp in inverting mode, the output voltage will be proportional to the negative log of the input current. Since the input current is proportional to the input voltage, we can say that the output voltage will be proportional to the negative log of the input voltage.

According to the PN junction diode equation, the relationship between current and voltage for a diode is,

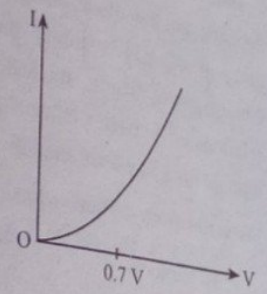
$$I_f = I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

Where,

I_s = Reverse saturation current

V_T = Thermal voltage

∴ for forward region



$$I_f \simeq I_s\, e^{\frac{V_D}{\eta V_T}}$$

or, $$\frac{V_D}{\eta v_T} = ln\left(\frac{I_f}{I_s}\right)$$

∴ $$V_D = \eta v_T . ln\left(\frac{I_f}{I_s}\right)$$

Since $V_o = -V_D$

∴ $$V_0 = -\eta v_T\, ln\left(\frac{I_f}{I_s}\right)$$

Also, $I_f = I = \frac{V_{in}}{R}$

∴ $$V_0 = -\eta v_T\, ln\left(\frac{V_{in}}{I_s R}\right)$$

∴ $$V_0 = k_1\, ln\,(k_2\, V_{in})$$

Here,

$$k_1 = -\eta v_T \text{ and } k_2 = \frac{1}{RIs}$$

Thus from above expression it is clear that output is proportional to logarithm of the input voltage.

5.1.2 Log amplifier using single op-amp and BJT

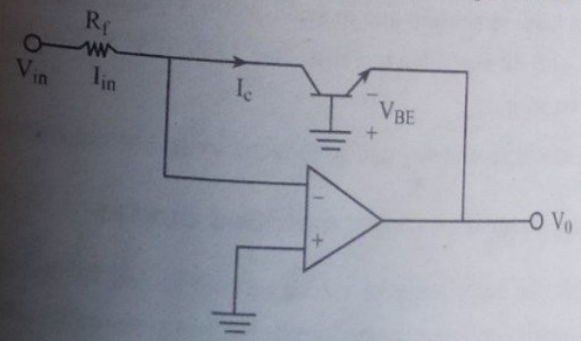


Fig: Basic log amplifier using BJT

The schematic of a op-amp transistor log amplifier is shown above. When a diode is replaced by a transistor the factor whose value normally depends on the diode current can be eliminated and the base emitter junction of BJT exhibits the logarithmic characteristics. The main advantage of using transistor over diode is that the exponential relationship between current and voltage expands over a much wider voltage for a transistor then diode.

We know from current voltage relationship of a transistor.

$$I_c = I_{EBO}\, e^{V_{BE}/V_T} = I_s\, e^{V_{BE}/V_T}$$

Where,

I_{EBO} = Emitter base leakage current

I_s = Reverse saturation current

Output voltage $V_0 = -V_{BE}$

or, $V_0 = V_T\, ln\left(\frac{I_c}{I_s}\right)$

$\therefore \quad V_0 = -V_T\, ln\left(\frac{V_{in}}{I_s R_i}\right)$

Hence the output is proportional to logarithm of the input voltage.

5.2 Non-ideal Effects

The output of single diode log amplifier is,

$$V_0 = -\eta v_T\, ln\left(\frac{V_s}{I_s R}\right)$$

V_0 is temperature dependent due to scale factor V_T and due to saturation current I_s. Also the o/p voltage is restricted to |0.7| V and to have an o/p v_{in} should be positive.

This temperature dependency can be reduced by following methods.

5.2.1 Log amplifier using matched diodes

The temperature dependency of v_0 can be minimized by using matched diodes D_1 and D_2, and the temperature dependent resistor R_T and constant current source which is independent of temperature.

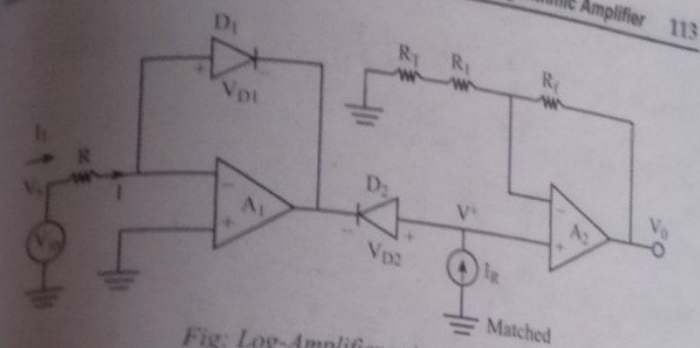


Fig: Log-Amplifier using two diode

For diode:

$$I_f = I_s \times \left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

$$I_f = I_s\, e^{\frac{V_D}{\eta V_T}} \qquad \left[\because e^{\frac{V_D}{\eta V_T}} \gg 1\right]$$

Thus, we can write

$$I_f = I_s \,.\, e^{\frac{V_D}{\eta V_T}}$$

Output diode voltage,

$$V_D = \eta \times V_T\, ln\left(\frac{I_f}{I_s}\right) \qquad \text{... ... ... (i)}$$

From above figure

$$D_{D1} + V^{+} = D_{D2}$$

$$\therefore \quad V^{+} = V_{D2} - D_{V1} \qquad \text{... ... ... (ii)}$$

Since, $V_{D2} = \eta_2 \times V_{T2}\, ln\left(\frac{I_R}{I_{S2}}\right)$

$$V_{D1} = \eta_1 \times V_{T1}\, ln\left(\frac{I}{I_{S1}}\right)$$

Also, $I = \frac{V_s}{R}$ ... ... (iii)

Eq^n (i) becomes,

$$V^{+} = \eta_2\, V_{T2}\, ln\left(\frac{I_R}{I_{S2}}\right) - \eta_1\, V_T\, ln\left(\frac{I}{I_{S1}}\right)$$

Assuming diodes are matched

i.e., $\eta_1 = \eta_2 = \eta$

$V_{T1} = V_{T2} = V_T$

Thus, $V^{+} = \eta V_T \ln\left(\frac{I_R}{I_S}\right) - \eta V_T \ln\left(\frac{V_s}{R I_s}\right)$ [∵ from eq^n (iii)]

or, $V^{+} = \eta V_T \left[\ln\left(\frac{I_R}{I_S}\right) - \ln\left(\frac{V_S}{R I_S}\right)\right]$

or, $V^{+} = \eta V_T \ln\left(\frac{I_R}{I_s} \times \frac{R I_s}{V_s}\right)$

Since, $V_0 = \left(1 + \frac{R_f}{R_1 + R_T}\right) \times V^{+}$

Then, $V_0 = \left(1 + \frac{R_f}{R_1 + R_T}\right) \eta V_T \ln\left(\frac{I_R R}{V_s}\right)$

$\therefore \quad V_0 = -\eta V_T \left(1 + \frac{R_f}{R_1 + R_T}\right) \ln\left(\frac{V_s}{I_R R}\right)$

Let $k_1 = -\eta V_T \left(1 + \frac{R_f}{R_1 + R_T}\right)$

$k_2 = \frac{1}{R I_R}$

$\therefore \quad V_0 = k_1 \ln (k_2 V_R)$ [∵ this form will be used in next chapter]

Note:

- Temperature sensitive scale factor $\eta \times V_T$ can be compensated by making the gain of Op-Amp (A_2) temperature sensitive.
- Using temperature dependent resistor R_T in such a way that $\eta \times V_T$ and R_T has a opposite effect and the circuit is independent of temperature.

Alternative

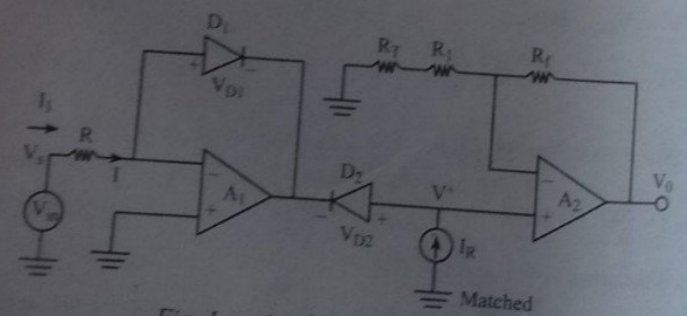


Fig: Log-Amplifier using two diode

Instead of two matched diodes it is possible to use a matched pour of transistor connected as in the figure to remove from the expression V_0 the factor η whose value normally depends upon the current flowing through diodes.

From figure,

$V_{cc} = I_{c2} R_5 + V_{BE_2} - V_{BE_1}$

$\therefore \quad I_{c2} = \frac{V_{cc}}{R_5}$ Again we have,

$V_{BE_1} - V_{BE_2} = V_T \ln\left(\frac{I_{c1}}{I_s}\right) - V_T \ln\left(\frac{I_{c2}}{I_s}\right)$

or, $0 - V_{E_1} - V_{B_2} + V_{E_2} = V_T \ln\left(\frac{I_{c1}}{I_{c2}}\right)$

or, $V_{B_2} = -V_T \ln\left(\frac{I_{c1}}{I_{c2}}\right)$ $(\because V_{E_1} = V_{E_2})$

$\therefore \quad V_0 = \left(1 + \frac{R_3}{R_4}\right) V_{B2} = \left(1 + \frac{R_3}{R_4}\right)\left[-V_T \ln\left(\frac{I_{c1}}{I_{c2}}\right)\right]$

$= -V_T \left(1 + \frac{R_3}{R_4}\right) \ln\left(\frac{I_{c1}}{I_{c2}}\right)$

$= -V_T \left(1 + \frac{R_3}{R_4}\right) \ln\left(\frac{V_{in}/R_1}{V_{cc}/R_5}\right)$

Let $K_1 = -V_T (1 + R_3/R_4)$ and $K_2 = \left(\frac{R_1}{R_5 V_{cc}}\right)$

Then, $V_0 = K_1 \ln (k_2 V_{in})$

5.2.2 Log amplifier using two matched transistors and two op-amps.

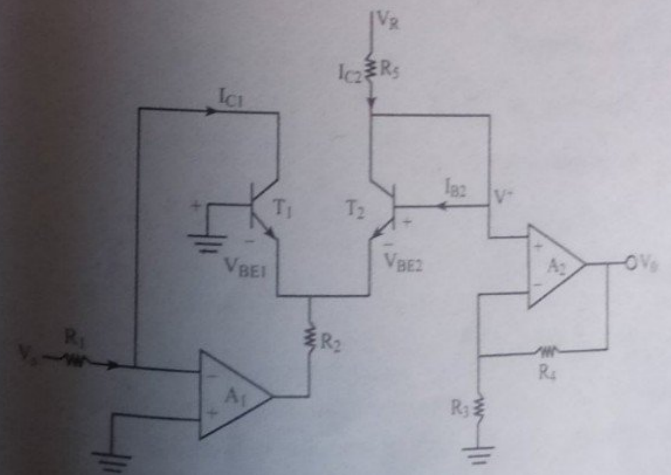


Fig: Logarithmic amplifier using two transistors

Transistor provides wide dynamic range amplification for input voltage then diode, so we use two matched transistor insted of two matched diode also the transistor is used to remove the factor n whose value normally depends upon the current flowing through diodes.

From figure we can write

$$V^+ - V_{BE2} + V_{BE1} = 0$$

$$V^+ = V_{BE2} - V_{BE1} \ldots\ldots (i)$$

For transistor,

$$I_c = I_s \times (e^{\frac{V_{BE}}{V_T}} - 1)$$

or, $$I_c = I_s \times e^{\frac{V_{BE}}{V_T}} \quad [\because e^{\frac{V_{BE}}{V_T}} \gg 1]$$

$$\therefore \quad V_{BE} = V_c = ln\left(\frac{I_c}{I_s}\right)$$

Assuming two transistor are matched

$$I_{s1} = I_{s2} = I_s$$

$$V_{T1} = V_{T2} = V_T$$

So,

For transistor T_1

$$V_{BE1} = V_{T1} \times ln\left(\frac{I_{c1}}{I_{s1}}\right)$$

For transistor T_2

$$V_{BE2} = V_{T2} \times ln\left(\frac{I_{c2}}{I_{s2}}\right)$$

From equation (i)

$$V^+ = V_{T2} \times ln\left(\frac{I_{c2}}{I_{s2}}\right) - V_{T1} \times ln\left(\frac{I_{c1}}{I_{s1}}\right)$$

Here,

$$I_{c1} = \frac{V_s}{R_1} \text{ and } I_{c2} = \frac{V_R}{R_2}$$

So,

$$V^+ = -V_T \times ln\left(\frac{V_s}{R_1} \times \frac{R_2}{V_R}\right)$$

From figure,

$$V_0 = \left(1 + \frac{R_4}{R_3}\right) \times V^+$$

Thus,

$$V_0 = -V_T\left(1 + \frac{R_4}{R_3}\right) \times ln\left(\frac{V_s}{V_R} \times \frac{R_2}{R_1}\right) = k_1\, ln(k_2\, V_{in})$$

Note: Temperature sensitive factor can be compensated by making the gain of amp A_2 also temperature sensitive by introducing of temperature dependent resistor so as to make the circuit in-dependent of temperature.

5.3 Stability Consideration

All the circuits described above have a tendency to oscillate due to the presence of an active element in the feedback that can provide gain rather than loss.

Ignoring op-amp input errors, for log amplifier using BJT, we have.

$$V_c = V_i - I_C R \text{ and } V_0 = -V_{BE}$$

For given value of V_i

Feedback factor $$\beta = \frac{dV_c}{dV_0}$$

$$= R\frac{dI_c}{dV_{BE}}$$

$$= R\frac{d}{dV_{BE}} \quad [\because I_s e^{V_{BE}/V_T}]$$

$$= R\frac{I_s e^{V_{BE}/V_T}}{V_T}$$

$$= \frac{R.I_c}{V_T}$$

$$\therefore \quad \beta = \frac{V_i}{V_T} \; (\because RI_c = V_i)$$

For higher value of β, higher order poles causes phase shift which makes the circuit unstable. An additional source of instability is the i/p stray capacitance 'C'. And for β to be greater than unity i/p voltage should be in the range of millivolt.

5.4 Anti-logarithmic operations

An anti-logarithmic amplifier, or an anti-log amplifier is an electric circuit that produces an output that is proportional to the anti-logarithm of the applied input. This section discuss about the op-amp based anti-logarithmic amplifies in detail. An op-amp based anti-logarithmic amplifier produces a voltage at the output, which is proportional to the anti-log of the voltage that is applied to the diode conned to its inverting terminal.

Note: Antilog amplifier is used in analog multiplier circuit

5.4.1 Anti-log amplifier using diode

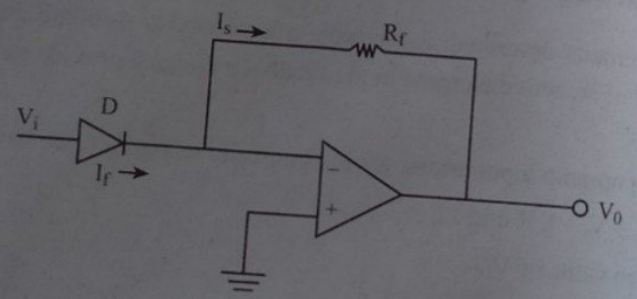


Fig: Antilog amplifier using a diode

In this circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. It means zero volts is applied to its non-inverting input terminal.

According to the virtual short circuit concept the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal so, the voltage at its inverting input terminal will be zero volts.

The node equation at the inverting input terminal's node is,

$$-I_f + \frac{0 - V_0}{R_f} = 0$$

$$\because \quad V_0 = -R_f I_f \ldots\ldots \text{(i)}$$

We know that the equation for the current flowing through a diode, when it is forward bias, is as given below,

$$I_f = I_s e^{\frac{V_f}{\eta V_T}}$$

From equation (i)

$$V_0 = -R_f I_s e^{\frac{V_f}{\eta V_T}} \ldots\ldots \text{(ii)}$$

Again, Applying KVL,

$$V_i - V_f = 0$$

$$\therefore \quad V_i = V_f$$

From equation (ii)

$$\therefore \quad V_0 = -R_f I_s e^{\frac{V_i}{\eta V_T}}$$

Note that, in the above equation the parameters n, V_T and I_s are constant. So the output voltage V_0 will be proportional to the anti-natural logarithm (exponential) of the input voltage v_i, for a fixed value of feedback resistance R_f.

Therefore the op-amp based anti-log amplifier circuit discussed above all produce an output which is proportional to the exponent of the input voltage V_i, when $R_f I_s = 1V$. Observe the output V_0 is having a negative sign, which indicates that there exists a 180 phase difference between input and the output.

5.4.2 Anti-logarithmic amplifier using single transistor

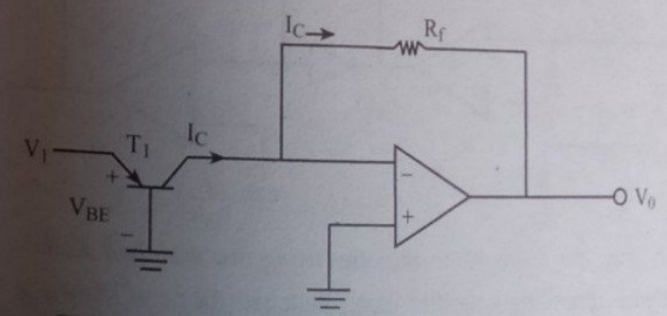


Fig: Anti-logarithmic amplifier using single transistor

The circuit arrangement for Anti-logarithmic amplifier is illustrated in figure. Here a general purpose NPN transistor is connected to inverting input of op-amp. A resistor is connected in feedback path. The output is dependent upon output current of transistor and feedback resistor.

Now, for diagram, output voltage can be written as,

$$V_0 = -R_f \times I_c \qquad \ldots\ldots \text{(i)}$$

Where,

I_s = Saturation current

V_T = Thermal voltage

$I_c = I_s \times (e^{V_{BE}/V_T} - 1)$

As we know,

$e^{V_{BE}/V_T} \gg 1$

Thus, we can write

$I_c = I_s \times e^{V_{BE}/V_T}$

Now putting the value of collector current of transistor I_c in equation (i) The output voltage expression becomes,

$V_0 = -R_f \times I_s \times e^{V_{BE}/V_T}$

From the figure we can also conclude that transistor base emitter voltage (V_{BE}) is equivalent input voltage V_i i.e. $V_{BE} = V_i$

Thus we can also write output voltage in contest of input voltage V_i.

$\therefore \quad V_0 = -R_f \times I_s \times e^{V_i/V_T}$

5.4.3 Antilogarithmic amplifier using matched diode

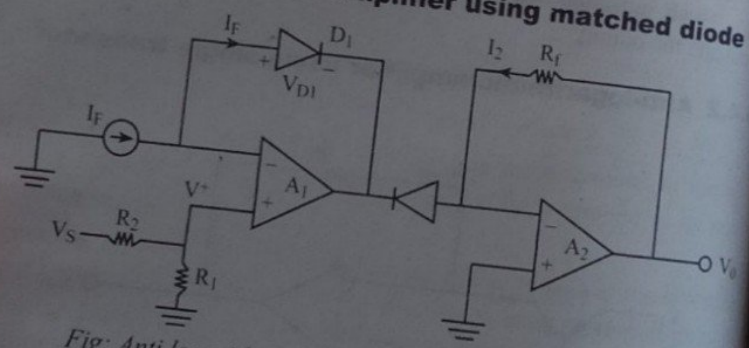


Fig: Anti logarithmic amplifier using two matched diode

The figure of anti-log amplifier using matched diode is shown in figure below. Two matched diodes are used here, where one diode (D_1) is connected in feedback path and second diode (D_2) is connected to inverting input of op-amp (A_2) in reverse bias mode as shown in figure. Voltage at inverting pin of op-amp (A_1) is potentially equal to voltage at non-inverting input of op-amp i.e. inverting input voltage = non-inverting input voltage = V^+ say. Thus, we can write.

$$V^+ = \frac{R_1}{R_1 + R_2} \times V_s \qquad \text{..... (i)}$$

Now we can use KVL in order to solve for V^+ voltage.

$V^+ - V_{D1} + V_{D2} = 0$

$V^+ = V_{D1} - V_{D2} \qquad \text{..... (ii)}$

Now, solving for diode

$I_D = I_s \times e^{V_D/\eta V_T}$

Output voltage of diode V_D can be written as

$$V_D = \eta V_T \, ln\left(\frac{I_D}{I_s}\right)$$

Now, we can calculate individual diode voltage i.e. V_{D1} and V_{D2}

$$V_{D1} = \eta_1 \times V_{T1} \times ln\left(\frac{I_f}{I_{s1}}\right)$$

$$V_{D2} = \eta_2 \times V_{T2} \times ln\left(\frac{I_2}{I_{s2}}\right)$$

Assuming both diode are matched thus material constant, thermal voltage of diode and saturation current of diode is also same. Thus, we can write

$\eta_1 = \eta_2 = \eta$

$V_{T1} = V_{T2} = V_T$

$I_{s1} = I_{s2} = I_s$,

From equation (ii) we can write

$$V^+ = \eta \times V_T \times ln\left(\frac{I_f}{I_2}\right)$$

or, $$V^+ = -\eta v_T \, ln\left(\frac{I_2}{I_f}\right)$$

$$\therefore \quad V^+ = -\eta V_T \, ln\left(\frac{V_0}{R_f . I_f}\right) \qquad \text{..... (iii)} \; [\because I_2 = \frac{V_0}{R_f}]$$

Now,

From equation (i) and (iii) we can write

$$\left(\frac{R_1}{R_1 + R_2}\right) \eta v_s = -\eta \times V_T \, ln\left(\frac{V_0}{R_f \times I_f}\right)$$

$$\therefore \quad V_0 = I_f \times R_f \times e^{\frac{-V_s}{\eta V_T} \times \frac{R_1}{R_1 + R_2}}$$

Temperature sensitive factor $\eta \times V_T$ can be eliminated by adjusting voltage divider also temperature sensitive in such a way that their effect get cancelled.

Alternative

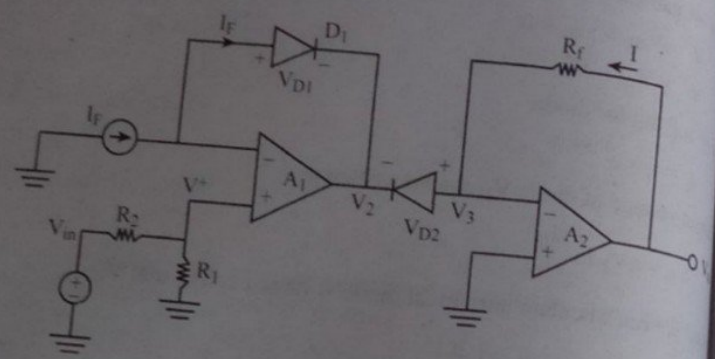


Fig: Anti logarithmic amplifier using two matched diode

From figure,

$$V^+ = \frac{R_1}{R_2 + R_1} V_{in}$$

Also, $V^+ = V_{D_1} + V_2$

or, $V^+ - V_2 = V_{D_1} = nV_T \, l_n \left(\frac{I_f}{I_s}\right)$

$\therefore \quad V_2 = V^+ - nV_T \, l_n \left(\frac{I_f}{I_s}\right) \quad \ldots\ldots (i)$

Also, we have

$$V_{D_2} = V_3 - V_2$$

But $V_3 = 0$

$\therefore \quad V_2 = -V_{D_2}$

$$V_2 = -nV_T \, l_n \left(\frac{I}{I_s}\right) \quad \ldots\ldots (ii)$$

So, from (i) and (ii)

$$V^+ - nV_T \, l_n \frac{I_f}{I_s} = -nV_T \, l_n \frac{I}{I_s}$$

or, $V^+ = -nV_T \, l_n \left(\frac{I}{I_f}\right)$

Here, $I = \frac{V_0}{R_3}$

or, $\frac{R_1}{R_1 + R_2} V_{in} = -nV_T \, l_n \left(\frac{V_0}{I_f R_3}\right)$

or, $l_n \left(\frac{V_0}{I_f R_3}\right) = -\frac{1}{nV_T} \times \frac{R_1}{R_1 + R_2} \times V_{in}$

or, $V_0 = I_f R_3 \exp\left[-\frac{1}{nV_T} \cdot \frac{R_1}{R_1 + R_2} \cdot V_{in}\right]$

Let $K_3 = I_f R_3$ and $K_4 = \frac{-1}{nV_T} \frac{R_1}{R_1 + R_2}$

$\therefore \quad V_0 = K_3 e^{k_4 V_{in}}$

Here we can compensate the effect of V_T by making R_2 temp dependent.

5.4.4 Antilogarithmic amplifier using two matched transistor

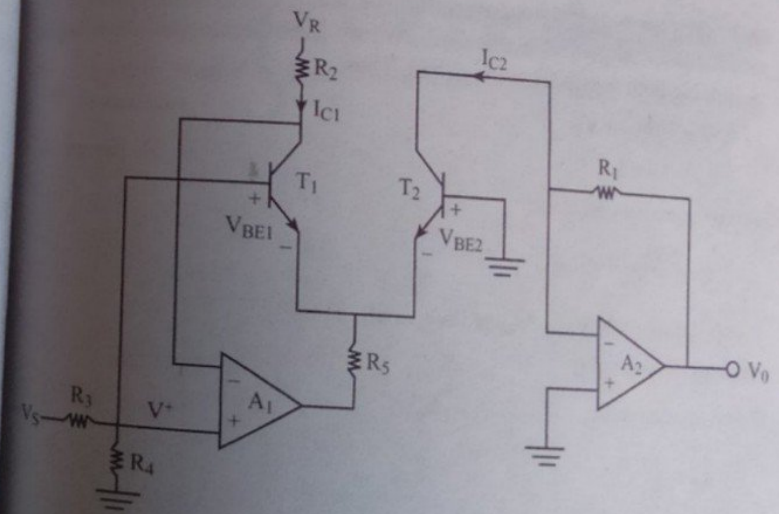


Fig: Antilog amplifier using matched transistor

The figure of anti-logarithm amplifier is shown in figure. Two matched transistor is used here as shown in figure, where input is given to the non-inverting amplifier op-amplifier. A_1.

From figure,

$$V^+ = \frac{R_4}{R_3 + R_4} \times V_S \quad \ldots\ldots (i)$$

Also,

$$V^{+} = V_{BE1} - V_{BE2} \qquad \ldots\ldots (ii)$$

From transistor,

$$I_c = I_s \times e^{\frac{V_{BE}}{V_T}}$$

$$\therefore \quad V_{BE} = V_T \, ln\left(\frac{I_c}{I_s}\right)$$

Now we can drive base emitter voltage of each transistor. Base emitter voltage of 1st transistor V_{BE1} can be written as,

$$V_{BE1} = V_{T1} \, ln\left(\frac{I_{c1}}{I_{s1}}\right)$$

Similarly for 2nd transistor

$$V_{BE2} = V_{T2} \, ln\left(\frac{I_{c2}}{I_{s2}}\right)$$

Assuming both transistor are matched. Thus

$$V_{T1} = V_{T2} = V_T$$

$$I_{s1} = I_{s2} = I_s$$

From figure we can write

$$I_{c1} = \frac{V_R - v^{+}}{R_2}$$

As we know $v^{+} = V_{B1} - V_{B2}$ is very small. Thus

We can write $v^{+} = 0$

Now, are can write,

$$I_{c1} = \frac{V_R}{R_2}$$

$$I_{c2} = \frac{V_0}{R_1}$$

Form equation (ii)

$$V_{BE1} - V_{BE2} = V_T \times ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

$$= V_T \, ln\left(\frac{V_R}{R_2} \times \frac{R_1}{V_0}\right)$$

$$= -V_T \, ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

Thus,

$$\frac{R_4}{R_3 + R_4} \times V_s = -V_T \, ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

$$\therefore \quad V_0 = \frac{V_R \times R_1}{R_2} \times e^{\left[\frac{-V_S \times R_4}{V_T (R_3 + R_4)}\right]}$$

This anti-logarithmic is temperature sensitive

Note: Final expression can be written as,

$$V_0 = k_3 \, e^{(k_4 V_R)}$$

Where, $k_3 = \frac{R_4}{R_3} \times VR$

Also, $k_4 = \frac{-R_4}{V_T(R_3 + R_4)}$

Old Questions with Solution

1. **Derive transfer function of antilog amplifier using match transistor.** **[2073 Chaitra]**

Solution:

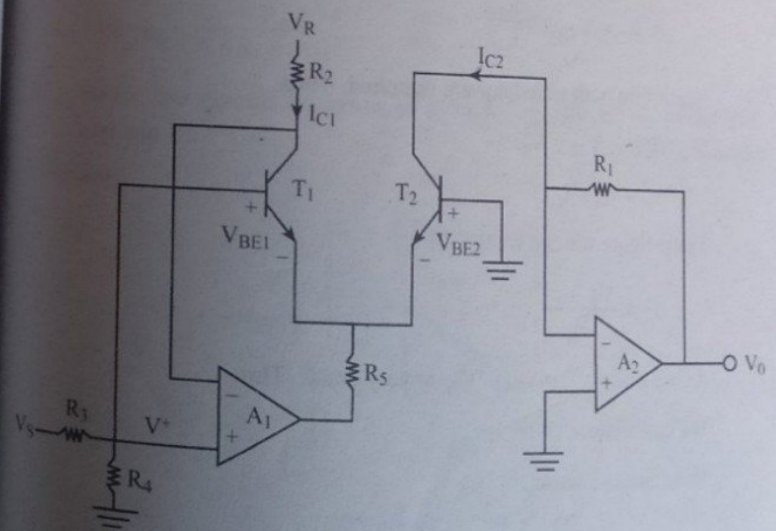


Fig: Antilog amplifier using matched transistor

The figure of anti-logarithm amplifier is shown in figure. Two matched transistor is used here as shown in figure, where input is given to the non-inverting amplifier op-amplifier. A_1.

From figure,

$$V^{+} = \frac{R_4}{R_3 + R_4} \times V_S \quad \text{..... (i)}$$

Also,

$$V^{+} = V_{BE1} - V_{BE2} \quad \text{..... (ii)}$$

From transistor,

$$I_c = I_s \times e^{\frac{V_{BE}}{V_T}}$$

$$\therefore \quad V_{BE} = V_T \ln\left(\frac{I_c}{I_s}\right)$$

Now we can drive base emitter voltage of each transistor. Base emitter voltage of 1st transistor V_{BE1} can be written as,

$$V_{BE1} = V_{T1} \ln\left(\frac{I_{c1}}{I_{s1}}\right)$$

Similarly for 2nd transistor

$$V_{BE2} = V_{T2} \ln\left(\frac{I_{c2}}{I_{s2}}\right)$$

Assuming both transistor are matched. Thus

$$V_{T1} = V_{T2} = V_T$$

$$I_{s1} = I_{s2} = I_s$$

From figure we can write

$$I_{c1} = \frac{V_R - v^{+}}{R_2}$$

As we know $v^{+} = V_{B1} - V_{B2}$ is very small. Thus

We can write $v^{+} = 0$

Now, are can write,

$$I_{c1} = \frac{V_R}{R_2}$$

$$I_{c2} = \frac{V_0}{R_1}$$

Form equation (ii)

$$V_{BE1} - V_{BE2} = V_T \times \ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

$$= V_T \ln\left(\frac{V_R}{R_2} \times \frac{R_1}{V_0}\right)$$

$$= -V_T \ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

Thus,

$$\frac{R_4}{R_3 + R_4} \times V_s = -V_T \ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

$$\therefore \quad V_0 = \frac{V_R \times R_1}{R_2} \times e^{\left[\frac{-V_s \times R_4}{V_T (R_3 + R_4)}\right]}$$

This anti-logarithmic is temperature sensitive

Note: Final expression can be written as,

$$V_0 = k_3 e^{(k_4 V_R)}$$

Where, $k_3 = \frac{R_4}{R_3} \times VR$

Also, $k_4 = \frac{-R_4}{V_T(R_3 + R_4)}$

2. **Draw the circuit diagram of a basic logarithmic amplifier and explain it.** **[2072 Kartik]**

Solution:

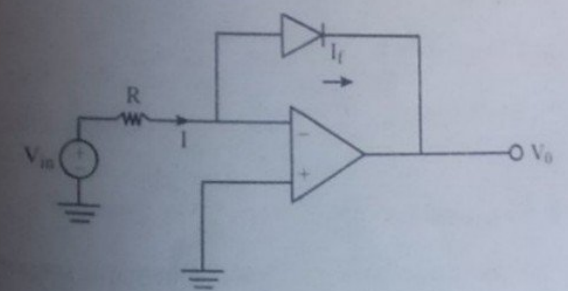


Fig: Opamp-diode log amplifier.

The scamatic of a simple Opamp-diode log amplifier is shown above. This is nothing but an opamp wired in closed loop inverting configuration with a diode in the feedback path. The voltage across the diode will be always proportional to the log of the current

through it and when a diode is placed in the feedback path of an opamp in inverting mode, the output voltage will be proportional to the negative log of the input current. Since the input current is proportional to the input voltage, we can say that the output voltage will be proportional to the negative log of the input voltage.

According to the PN junction diode equation, the relationship between current and voltage for a diode is,

$$I_f = I_s\,(e^{\frac{V_D}{\eta V_T}} - 1)$$

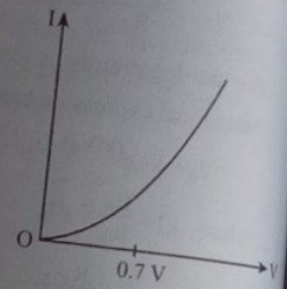
Where,

I_s = Reverse saturation current

V_T = Thermal voltage

∴ For forward region

$$I_f \simeq I_s\, e^{\frac{V_D}{\eta V_T}}$$



or, $\dfrac{V_D}{\eta v_T} = ln\left(\dfrac{I_f}{I_s}\right)$

∴ $V_D = \eta v_T \cdot ln\left(\dfrac{I_f}{I_s}\right)$

Since $V_o = -V_D$

∴ $V_0 = -\eta v_T\, ln\left(\dfrac{I_f}{I_s}\right)$

Also, $I_f = I = \dfrac{V_{in}}{R}$

∴ $V_0 = -\eta v_T\, ln\left(\dfrac{V_{in}}{I_s R}\right)$

∴ $V_0 = k_1\, ln\,(k_2\, V_{in})$

Here,

$k_1 = -\eta v_T$ and $k_2 = \dfrac{1}{RIs}$

Thus from above expression it is clear that output is proportional to logarithm of the input voltage.

3. Draw the circuit diagram for matched transistor antilog amplifier and hence derive the input and output voltage relationship. Explain how the effect of temperature can be minimized.

[2072 Chitra]

Solution:

Part I:

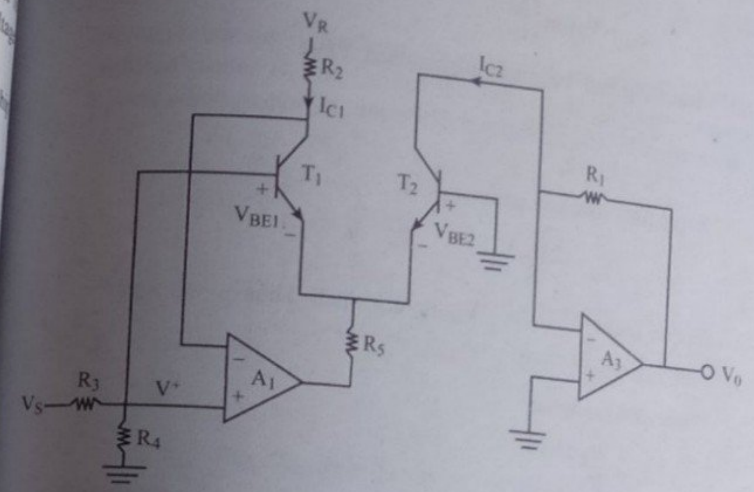


Fig: Antilog amplifier using matched transistor

The figure of anti-logarithm amplifier is shown in figure. Two matched transistor is used here as shown in figure, where input is given to the non-inverting amplifier op-amplifier. A_1.

From figure,

$$V^+ = \frac{R_4}{R_3 + R_4} \times V_S \qquad \text{..... (i)}$$

Also,

$$V^+ = V_{BE1} - V_{BE2} \qquad \text{..... (ii)}$$

From transistor,

$$I_c = I_s \times e^{\frac{V_{BE}}{V_T}}$$

∴ $V_{BE} = V_T\, ln\left(\dfrac{I_c}{I_s}\right)$

Now we can drive base emitter voltage of each transistor. Base emitter voltage of 1st transistor V_{BE1} can be written as,

$$V_{BE1} = V_{T1}\, ln\left(\frac{I_{c1}}{I_{s1}}\right)$$

Similarly for 2nd transistor

$$V_{BE2} = V_{T2}\, ln\left(\frac{I_{c2}}{I_{s2}}\right)$$

Assuming both transistor are matched. Thus

$$V_{T1} = V_{T2} = V_T$$

$$I_{s1} = I_{s2} = I_s$$

From figure we can write

$$I_{c1} = \frac{V_R - v^+}{R_2}$$

As we know $v^+ = V_{B1} - V_{B2}$ is very small. Thus

We can write $v^+ = 0$

Now, are can write,

$$I_{c1} = \frac{V_R}{R_2}$$

$$I_{c2} = \frac{V_0}{R_1}$$

Form equation (ii)

$$V_{BE1} - V_{BE2} = V_T \times ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

$$= V_T\, ln\left(\frac{V_R}{R_2} \times \frac{R_1}{V_0}\right)$$

$$= -V_T\, ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

Thus,

$$\frac{R_4}{R_3 + R_4} \times V_s = -V_T\, ln\left(\frac{V_0}{V_R} \times \frac{R_2}{R_1}\right)$$

$$\therefore \quad V_0 = \frac{V_R \times R_1}{R_2} \times e\left[\frac{-V_S \times R_4}{V_T(R_3 + R_4)}\right].$$

This anti-logarithmic is temperature sensitive

Part II: Temperature sensitive factor can be compensated by making the gain of op-amp A2 also temperature sensitive by introducing of temperature dependent resistor so as to make the circuit in-dependent of temperature.

4. Draw the circuit for the logarithmic amplifier using matched transistor and find its transfer function. [2071 Shrawan]

Solution:

The temperature dependency of v_0 can be minimized by using matched diodes D_1 and D_2, and the temperature dependent resistor R_T and constant current source which is independent of temperature.

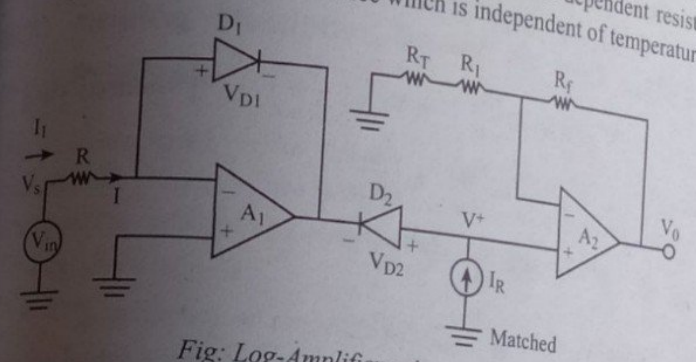


Fig: Log-Amplifier using two diode

For diode:

$$I_f = I_S \times (e^{\frac{V_D}{\eta V_T}} - 1)$$

$$I_f = I_S\, e^{\frac{V_D}{\eta V_T}} \qquad [\because e^{\frac{V_D}{\eta V_T}} \gg 1]$$

Thus, we can write

$$I_f = I_S \,.\, e^{\frac{V_D}{\eta V_T}}$$

Output diode voltage,

$$V_D = \eta \times V_T\, ln\left(\frac{I_f}{I_s}\right) \qquad \text{..... (i)}$$

From above figure

$$D_{D1} + V^+ = D_{D2}$$

$$\therefore \quad V^+ = V_{D2} - D_{V1} \qquad \text{..... (ii)}$$

Since, $V_{D2} = \eta_2 \times V_{T2}\, ln\left(\frac{I_R}{I_{S2}}\right)$

$$V_{D1} = \eta_1 \times V_{T1} ln\left(\frac{I}{I_{S1}}\right)$$

Also, $I = \frac{V_s}{R}$ ..... (iii)

Eq^n (i) becomes,

$$V^+ = \eta_2 V_{T2} \ln\left(\frac{I_R}{I_{S2}}\right) - \eta_1 V_T \ln\left(\frac{I}{I_{S1}}\right)$$

Assuming diodes are matched

i.e., $\eta_1 = \eta_2 = \eta$

$V_{T1} = V_{T2} = V_T$

Thus,

$$V^+ = \eta V_1 \ln\left(\frac{I_R}{I_S}\right) - \eta V_T \ln\left(\frac{V_s}{R I_s}\right) \qquad [\because \text{ from eq}^n \text{ (iii)}]$$

or, $V^+ = \eta V_T\left[\ln\left(\frac{I_R}{I_S}\right) - \ln\left(\frac{V_S}{R I_S}\right)\right]$

or, $V^+ = \eta V_T \ln\left(\frac{I_R}{I_s} \times \frac{R I_s}{V_s}\right)$

Since, $V_0 = \left(1 + \frac{R_f}{R_1 + R_T}\right) \times V^+$

Then, $V_0 = \left(1 + \frac{R_f}{R_1 + R_T}\right) \eta V_T \ln\left(\frac{I_R R}{V_s}\right)$

$\therefore \quad V_0 = -\eta V_1 \left(1 + \frac{R_f}{R_1 + R_T}\right) \ln\left(\frac{V_s}{I_R R}\right)$

Let $k_1 = -\eta V_T \left(1 + \frac{R_f}{R_1 + R_T}\right)$

$k_2 = \frac{1}{R I_R}$

$\therefore \quad V_0 = k_1 \ln (k_2 V_R)$

Note:

- Temperature sensitive scale factor $\eta \times V_T$ can be compensated by making the gain of Op-Amp (A_2) temperature sensitive.
- Using temperature dependent resistor R_T in such a way that $\eta \times V_T$ and R_T has a opposite effect and the circuit is independent of temperature.

5. Draw the circuit diagram for matched transistor antilog amplifier and hence derive the input and output voltage relationship. Explain how the effect of temperature can be minimized. **(Chaitra 2072)**

Solution: Refer to theory

❖❖❖

Chapter 6 Log-Antilog Circuit Application

6.1 Analog Multiplier Based on Log Antilog Principle

Multiplier are based on the fundamental logarithmic relationship that states that the product of two terms equals the sum of the logarithms of each term. This relationship is shown in the following formula.

$\ln(a \times b) = \ln a + \ln b$

➢ The multiplication procedure take three stops:

(a) To get the logarithm of a signal voltage use a log amplifies.

$V_1^* = \ln(V_1)$ and $V_2^* = \ln(V_2)$

(b) By summing the outputs of two log amplifiers, you get the logarithm of the product of the two original input voltages.

$V_0^* = V_2^* + V_1^*$

$= \ln(V_1) + \ln (V_2)$

$= \ln (V_1 \times V_2)$

(c) Then by taking the antilog, you get the product of the two input voltages as indicated in the following equation.

$V_0 = \exp (V_0^*) = \exp [\ln (V_1 V_2)]$

$= V_1 . V_2$

➢ The block diagram shows how the functions are connected to multiply two input voltages.

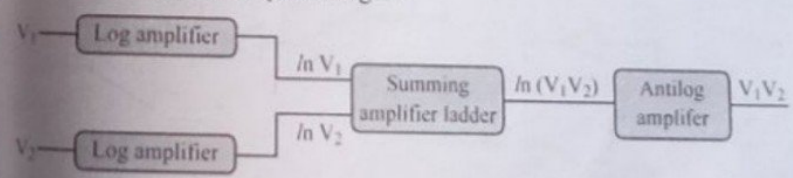


Fig: Multiplier

Alternative

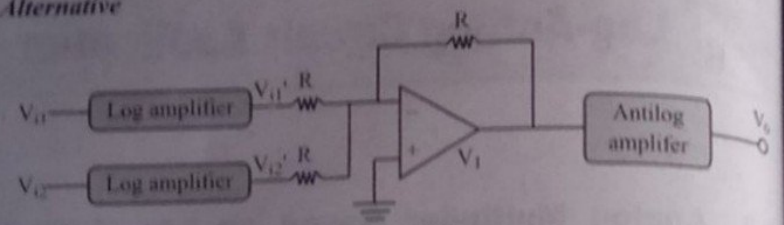


Fig: Multiplier

Multiplication of the numbers is the addition of their logs. So, if the logs of number are added using summing amplifier and its antilog is taken, the multiplication result is achieved.

From figure,

$$V_{i_1}^1 = K_1 l_n (K_2 V_{i_1})$$

$$V_{i_2}^1 = K_1 l_n (K_2 V_{i_2})$$

$$\therefore \quad V_1 = \frac{-R}{R} [V_{i_1}^1 + V_{i_2}^1] = -(V_{i_1}^1 + V_{i_2}^1) = -K_1 l_n (K_2^2 V_{i_1} V_{i_2})$$

For antilog amplifier,

$$V_0 = K_3 e K_4 V_1$$

$$= K_3 e K_4 (-K_1 l_n (K_2^2 V_{i_1} V_{i_2}))$$

$$= K_3 e x_p [-K_1 K_4 l_n (K_2^2 V_{i_1} V_{i_2})]$$

If $K_2 = K_3 = 1$ and $K_1 K_4 = -1$

$$V_0 = e x_p [l_n (V_{i_1} V_{i_2})]$$

$$\therefore \quad V_0 = V_{i_1} V_{i_2}$$

6.1.1 Multiplier using log and anti-log amplifier

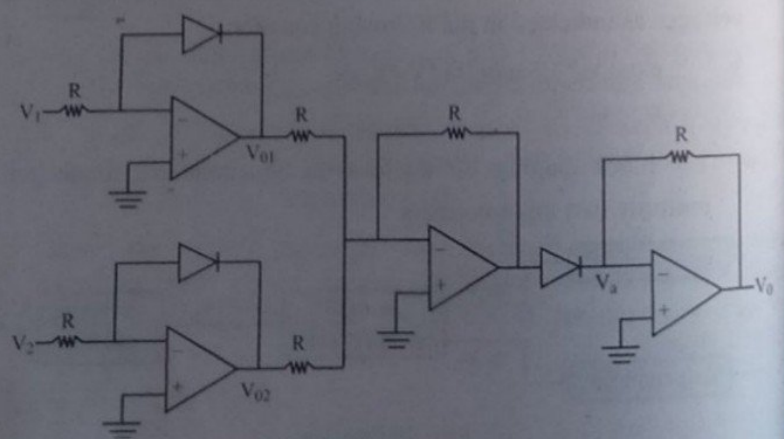


Fig: Multiplier circuit

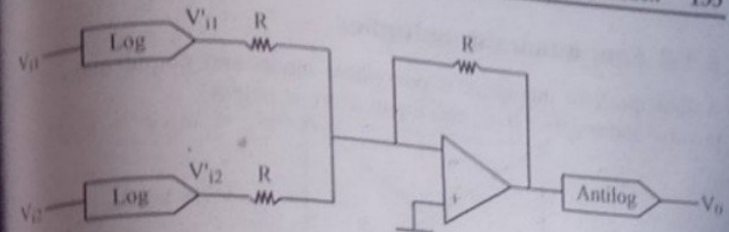


Fig: Block diagram of multiplyeer

From figure,

The output of log amplifier are

$$V_{01} = -\eta V_T \, ln \left(\frac{V_1}{I_s R}\right)$$

Also, $V_{02} = -\eta V_T \, ln \left(\frac{V_2}{I_s R}\right)$

Then, The output of adder circuit is,

$$V_a = -[V_{01} + V_{02}]$$

$$= -\left[-\eta V_T \, ln \left(\frac{V_1}{I_s R}\right) - \eta V_T \, ln \left(\frac{V_2}{I_s R}\right)\right]$$

$$= \eta V_T \, ln \left(\frac{V_1 V_2}{I_s^2 R^2}\right)$$

Thus, The output of antilog amplifier is,

$$V_0 = -R I_s e^{\left(\frac{V_a}{\eta V_T}\right)}$$

$$= -R I_s e^{\left[\frac{\eta V_T \, ln \left(\frac{V_1 V_2}{I_s^2 R^2}\right)}{\eta V_T}\right]}$$

$$= -R I_s e^{\left[ln \left(\frac{V_1 V_2}{I_s^2 R^2}\right)\right]}$$

$$= -R I_s \frac{V_1 V_2}{I_s^2 R^2}$$

$$= -\frac{V_1 V_2}{I_s R}$$

$$= k V_1 V_2$$

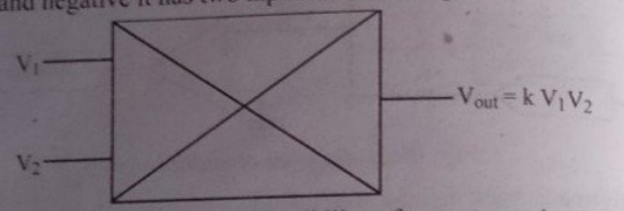
Hence,

$$V_0 \propto V_1 V_2$$

Where $k = \frac{-1}{I_s R}$

6.1.2 Four quadrant multiplier

A four quadrant multiplier is one where inputs and output may swing positive and negative it has two inputs and one output.



Typically k = 0.1 to reduce the possibility of output overload and has a dimension of $(\text{voltage})^{-1}$. It is called four quadrant because inputs and outputs can be positive and negative.

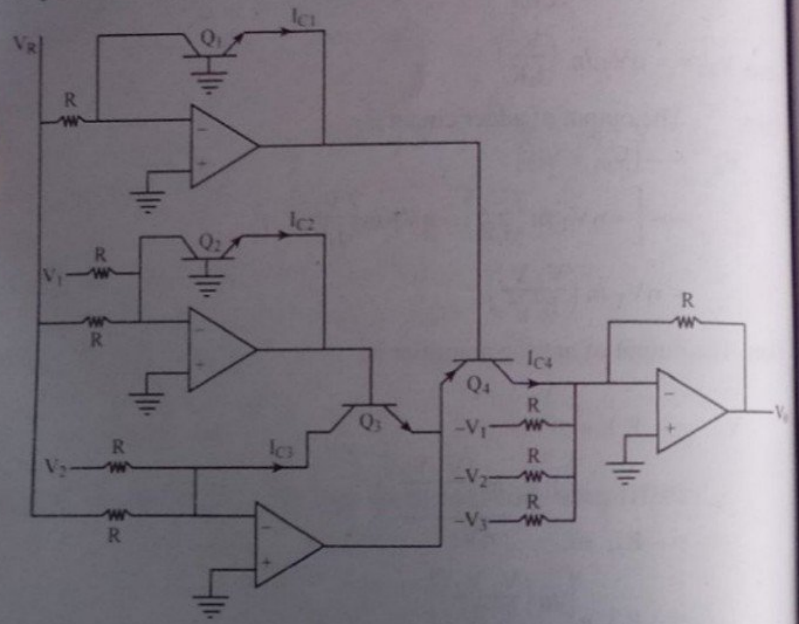


Fig: 4 Quadrant multiplier

From figure,

$$V_0 = V_1 + V_2 + V_R - I_{c4} R \quad \ldots\ldots (i)$$

Also, $V_{B4} = V_{E2} = -V_{BE2} + V_{B2}$

$$= -V_{BE2}$$

$$= -V_T \ln\left(\frac{I_{s1}}{I_s}\right)$$

$$= -V_T \ln\left(\frac{V_R}{RI_s}\right)$$

Again,

$$V_{E4} - 0 = -V_{BE3} - V_{BE2}$$

or, $$V_{E4} = -V_T \ln\left(\frac{I_{c3} \cdot I_{c2}}{I_s^2}\right)$$

or, $$V_{E4} = -V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2}\right)$$

Now,

$$V_{BE4} = V_{B4} - V_{E4}$$

$$= -V_T \ln\left(\frac{V_R}{RI_s}\right) + V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2}\right)$$

$$= V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2} \cdot \frac{RI_s}{V_R}\right)$$

$$= V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R} \cdot \frac{1}{I_s}\right)$$

So,

$$I_{C4} = I_s e^{\frac{V_{BE4}}{V_T}}$$

$$= I_s e^{\left[V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R}\right) \cdot \frac{1}{I_s} \cdot \frac{1}{V_T}\right]}$$

$$= I_s \left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R}\right) \cdot \frac{1}{I_s}$$

$$= \frac{1}{R}\left\{V_1 + V_2 + \frac{V_1 V_2}{V_R} + V_R\right\}$$

From (a),

$$V_0 = V_1 + V_2 + V_R - \frac{1}{R}\left\{V_1 + V_2 + \frac{V_1 V_2}{V_R} + V_R\right\} \times R$$

$$= \frac{1}{-V_R} \cdot V_1 V_2 = k V_1 V_2$$

$$\therefore \quad V_0 = k V_1 V_2$$

Where,

$$k = \frac{-1}{V_R}$$

6.1.3 Divider using log and antilog amplifier

Analog divider is a circuit in which the output is proportional to division of input voltages.

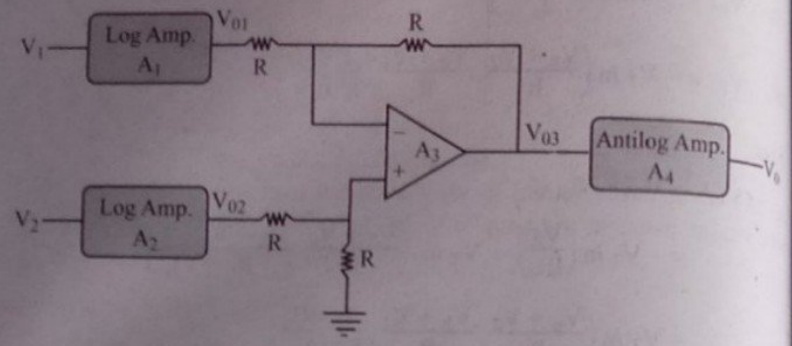


Fig: Divider using log and anti-log amplifier

Here,

For log amplifier : $V_0 = -\eta V_T \log \frac{V_{in}}{I_s . R}$

So,

$$V_{01} = -\eta V_T \log \frac{V_1}{I_s R}$$

Also

$$V_{02} = -\eta V_T \log \frac{V_2}{I_s R}$$

Then,

$$V_{03} = (V_{02} - V_{01})$$

$$= \left(-\eta V_T \log \frac{V_2}{I_0 R} + \eta V_T \log \frac{V_1}{I_s R}\right)$$

$$= \eta V_T \left(\log \frac{V_1}{I_s R} - \log \frac{V_2}{I_s R}\right)$$

$$= \eta V_T \log \left(\frac{V_1}{V_2}\right)$$

Thus,

$$V_0 = -I_0 R . e^{\frac{\eta V_T \log \left(\frac{V_1}{V_2}\right)}{\nu V_T}}$$

or, $V_0 = -I_0 R \frac{V_1}{V_2}$

$\therefore \quad V_0 \propto \frac{V_1}{V_2}$

Alternative

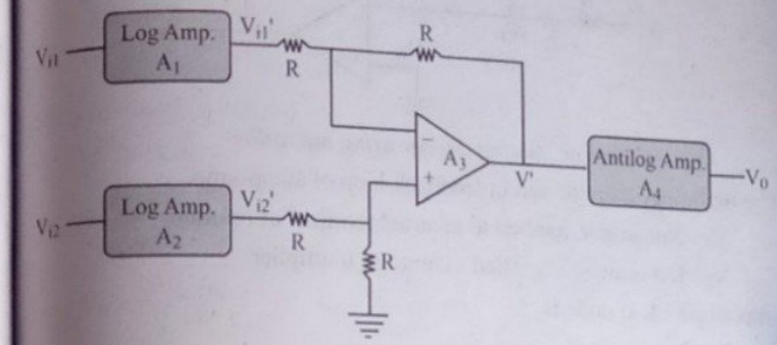


Fig: Divider using log and anti-log amplifier

Here, $V_{i_1}^1 = K_1 l_n (K_2 V_{i_1})$

$V_{i_2}^1 = K_1 l_n (K_2 V_{i_2})$

So, $V^1 = \left(1 + \frac{R}{R}\right) V_{i_2}^1 \left(\frac{R}{R+R}\right) + \left(\frac{-R}{R}\right) V_{i_1}^1$

$= V_{i_2}^1 - V_{i_1}^1$

$= K_1 l_n (K_2 V_{i_2}) - K_1 l_n (K_2 V_{i_1})$

$= K_1 l_n \left[\frac{K_2 V_{i_2}}{K_2 V_{i_1}}\right]$

$= K_1 l_n \left(\frac{V_{i_2}}{V_{i_1}}\right)$

$\therefore \quad V_0 = K_3 \exp (K_4 V^1)$

$= K_3 \exp \left[K_4 K_1 l_n \left(\frac{V_{i_2}}{V_{i_1}}\right)\right]$

If $K_1 = 1$ and $K_1 K_4 = 1$

$V_0 = \exp [l_n (V_{i_2} / V_{i_1})]$

$\therefore \quad V_0 = \frac{V_{i_2}}{V_{i_1}}$

6.1.4 Analog divider using multiplier

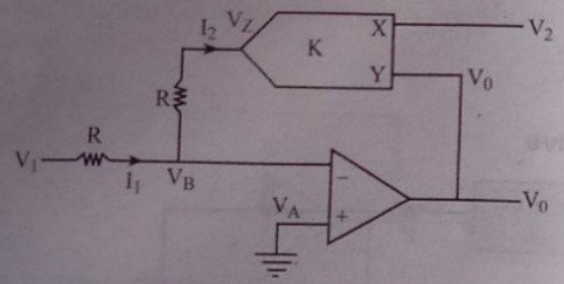


Fig: Analog divider using multiplier

The multiplier is connected in feedback loop of an op-amp.

V_1 : Numerator, applied to inverted terminal of op-amp.

V_2 : Denominator, applied to input of multiplier.

Applying kCL at node B,

$$I_1 = I_2$$

or, $$\frac{V_1 - V_B}{R} = \frac{V_B - V_z}{R} \quad \text{..... (i)}$$

By virtual ground concept $V_A = V_B = 0$

equation (i) becomes,

$$V_1 = -V_z$$

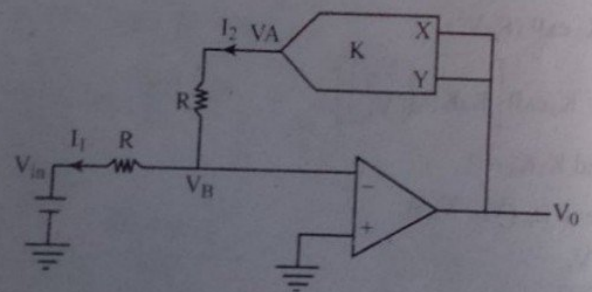
But, $V_z = kV_0V_2$

So, $V_1 = -kV_2 . V_0$

$$\therefore \quad V_0 = \frac{V_1}{-kV_2}$$

$$\therefore \quad V_0 \propto \frac{V_1}{V_2}$$

6.1.5 Analog square rooter using multiplier



The multiplier is connected in feedback path.

Both input's of multiplier is connected to the output of op. Amp (i.e.) "V_0"

The output of multiplier is,

$$V_A = k\,V_0^2 \quad \text{..... (i)}$$

Also, $I_1 = I_2$

or, $$\frac{V_A}{R} = \frac{-V_{in}}{R}$$

$$\therefore \quad V_A = -V_{in} \quad \text{..... (ii)}$$

From equation (i) and (ii)

$$-V_{in} = k\,V_0^2$$

or, $$V_0^2 = \frac{-V_{in}}{k}$$

$$\therefore \quad V_0 = \sqrt{\frac{|V_{in}|}{k}}$$

6.1.6 Power using log and antilog

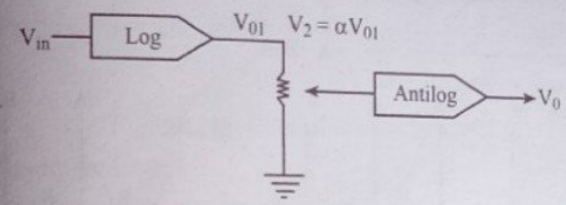


Fig: Log and anti-log amplifier to calculate power

From figure

$$V_{01} = k_1\, ln\,(k_2 V_{in})$$

And, $V_2 = \alpha V_{01}$ (Where $0 < \alpha \le 1$)

Also, $V_0 = k_3 \exp\,[k_4 V_2]$

$$= k_3 \exp\,[k_4\, \alpha\, V_{01}]$$

$$= k_3 \exp\,[k_4\, \alpha\, k_1\, ln\,(k_2 V_{in})]$$

$$= k_3 \exp\,[ln\,(k_2 V_{in})^{k_4 \alpha k_1}]$$

If $k_1 = k_2 = k_3 = k_4 = 1$,

$$v_0 = \exp\,[ln\,(V_{in})^{\alpha}]$$

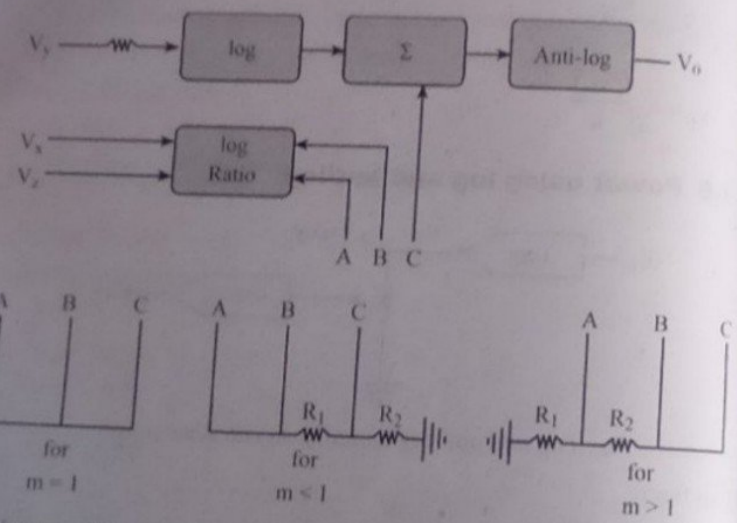
$$\therefore \quad V_0 = V_{in}^{\ \alpha}$$

6.2 The Multifunction Converter Circuit

A multifunction converter circuit is a circuit that accepts three inputs V_x, V_y and V_z and yields an output V_0 of the type.

$$V_0 = kV_y\left(\frac{V_z}{V_x}\right)^m$$

Where k is a suitable scale factor (typically k = 1) and m is a user programmable exponent in the range $0.2 < m < 5$. By proper selection of input configuration and exponent the circuit can be programmed for a variety of operations.



The input voltages can range from 0 to 10 v.

The multifunction converter is a useful I_c that can be used as a one-quadrant multiplier, squares, square rooter or exponent, depending on the voltage of m and accessory circuit used.

It is also can be used to produce an output voltage proportional to the sine, cosine or arctangent of an input voltage using additional circuit. The output may be,

$$V_0 = V_z V_y,\ V_0 = \frac{V_z}{V_x},\ V_0 = Z_z^{\ m},\ V_0 = V_z^{\ 1/m},\ V_0 = \frac{1}{V_x}$$

Operation of multifunction converter

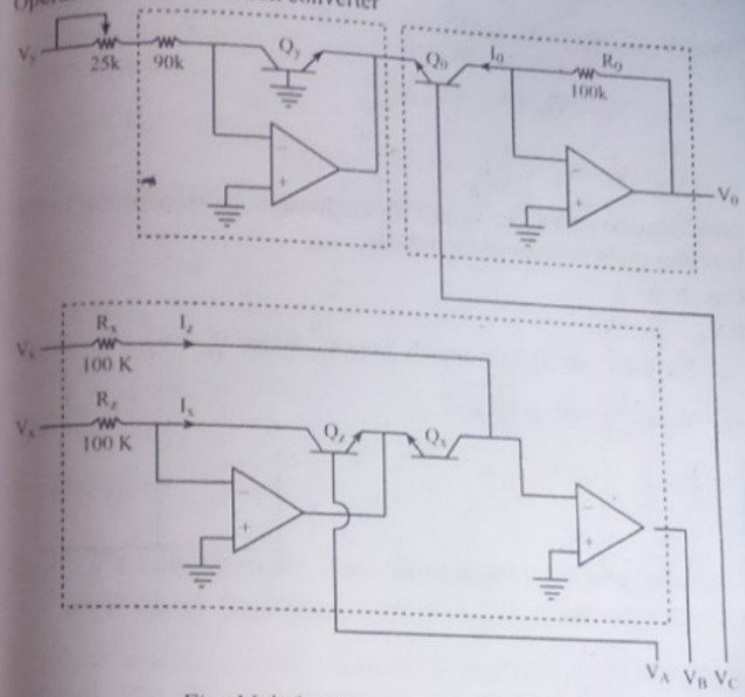


Fig: Multifunction converter in 43002 IC

From figure, we have,

$$I_x = \frac{V_x}{R_x};\ I_y = \frac{V_y}{R_y};\ I_z = \frac{V_z}{R_z};\ I_0 = \frac{V_0}{R_0}$$

Also, $V_{BEx} = V_T\, ln\left(\frac{I_x}{I_s}\right)$ and $V_{BEz} = V_T\, ln\left(\frac{I_z}{I_s}\right)$

So,

$$V_{BEz} - V_{BEx} = V_T\, ln\left(\frac{I_z}{I_x}\right)$$

or, $V_{Bz} - V_{Ez} - V_{Bx} + V_{Ex} = V_T\, ln\left(\frac{I_z}{I_x}\right)$

$\therefore$ $V_{Bz} = V_A = V_T\, ln\left(\frac{I_z}{I_x}\right)$ ..... (i)

Similarly,

$$V_{BEy} = V_T\, ln\left(\frac{I_y}{I_s}\right) \text{ and } V_{BE0} = V_T\, ln\left(\frac{I_0}{I_s}\right)$$

Then, $V_{BE0} - V_{BEy} = V_T \ln\left(\frac{I_0}{I_y}\right)$

or, $V_{B0} - V_{E0} - V_{By} + V_{Ey} = V_T \ln\left(\frac{I_0}{I_y}\right)$

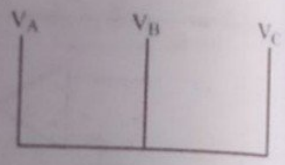
$\therefore \quad V_{B0} - V_C = V_T \ln\left(\frac{I_0}{I_y}\right) \quad \ldots\ldots (ii)$

From equation (i) and (ii) V_A and V_C are found to be proportional to the log ratios of the corresponding currents.

Case I: m = 1

If $V_A = V_B = V_C$

V_A and V_C are derived directly from V_B so that $V_A = V_C$



or, $V_T \ln\left(\frac{I_x}{I_x}\right) = V_T \ln\left(\frac{I_0}{I_y}\right)$

$\therefore \quad \frac{I_x}{I_x} = \frac{I_0}{I_y}$

or, $\frac{V_x/R_x}{V_x/R_x} = \frac{V_0/R_0}{V_y/R_y}$

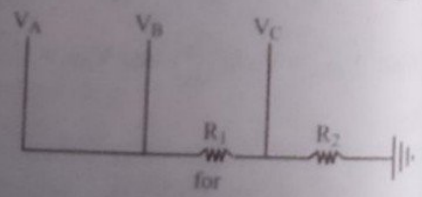
If $R_x = R_y = R_x = R_0$

$\therefore \quad V_0 = V_y\left(\frac{V_x}{V_x}\right)$

This shows that value of exponent m is 1

Case II: m < 1

V_A is directly derived from V_B which V_C is derived from V_B via a voltage divider circuit.



Here, $V_A = V_B = V_T \ln\left(\frac{I_x}{I_x}\right)$

And, $V_C = \frac{R_2}{R_1 + R_2} V_B$

or, $V_C = mV_B \qquad \left[\because \text{here } m = \frac{R_2}{R_1 + R_2} < 1\right]$

or, $V_T \ln\left(\frac{I_0}{I_y}\right) = m\, V_T \ln\left[\frac{I_x}{I_x}\right]$

or, $\frac{I_0}{I_y} = \left(\frac{I_x}{I_x}\right)^m$

Which implies, $V_0 = V_y\left(\frac{V_x}{V_x}\right)^m$ for equal value of resistors

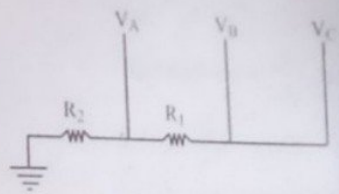
Case III: m > 1

V_C is derived directly from V_B which V_A is derived from V_B via a voltage divider circuit.

So, $V_C = V_B = V_T \ln\left(\frac{I_0}{I_y}\right)$

And, $V_A = \frac{R_2}{R_1 + R_2} V_B = \frac{1}{m} V_B \left[\text{Where } m = \frac{R_1 + R_2}{R_2} > 1\right]$

or, $V_A = \frac{1}{m} V_B$



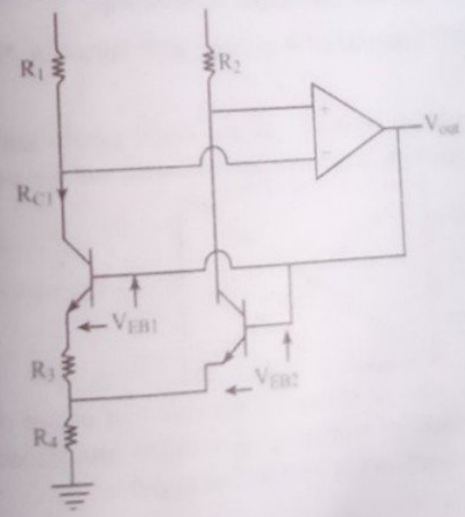
or, $V_T \ln\left(\frac{I_x}{I_x}\right) = \frac{1}{m} V_T \ln\left(\frac{I_0}{I_y}\right)$

or, $\frac{I_x}{I_x} = \left(\frac{I_0}{I_y}\right)^{1/m}$

Implies, $V_0 = V_y\left(\frac{I_x}{I_x}\right)^m$

6.3 Proportional to Absolute Temperature (PTAT) Devices

A voltage which is proportional to absolute temperature (PTAT) may be obtained from the base-emitter voltage difference of two bipolar transistors operating at different collector current densities. A corresponding PTAT current can be generated by reflecting the base-emitter voltage difference across a resistor.



$$V_{BE1} = \eta V_T \ln\left(\frac{I_{c1}}{I_s}\right)$$

And, $V_{BE2} = \eta V_T \ln\left(\frac{I_{c2}}{I_s}\right)$

Also, $\Delta V_{BE} = V_{BE1} - V_{BE2}$

$$= \eta V_T \ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

$$= \eta \frac{kT}{q} \ln\left(\frac{I_{c1}}{I_{c2}}\right)$$

Let, $\frac{I_{c1}}{I_{c2}}$ = constant then

$$\Delta V_{BE} = \eta \frac{kT}{q} \ln (N)$$

PTAT principle:

If two identical transistors are operated at a constant ratio of collector currents, the difference in their base emitter voltage will be directly proportional to absolute temperature i.e. $V_{BE} \propto T$. Hence, PTAT devices can be used as temperature sensor. e.g.: AD590 is an I_o temperature transducer that produces an output current proportional to absolute temperature.

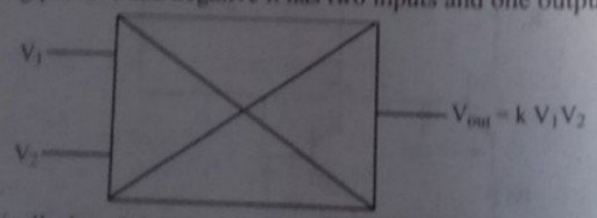
Old Questions with Solution

1. Draw the detailed circuit diagram for four quadrant multiplier and derive its input and output relationship.

[2077 Chaitra, 2075 Ashwin, 2073 Shrawan, 2070 Chaitra]

Solution:

A four quadrant multiplier is one where inputs and output may swing positive and negative it has two inputs and one output.



Typically k = 0.1 to reduce the possibility of output overload and has a dimension of $(\text{voltage})^{-1}$. It is called four quadrant because inputs and outputs can be positive and negative.

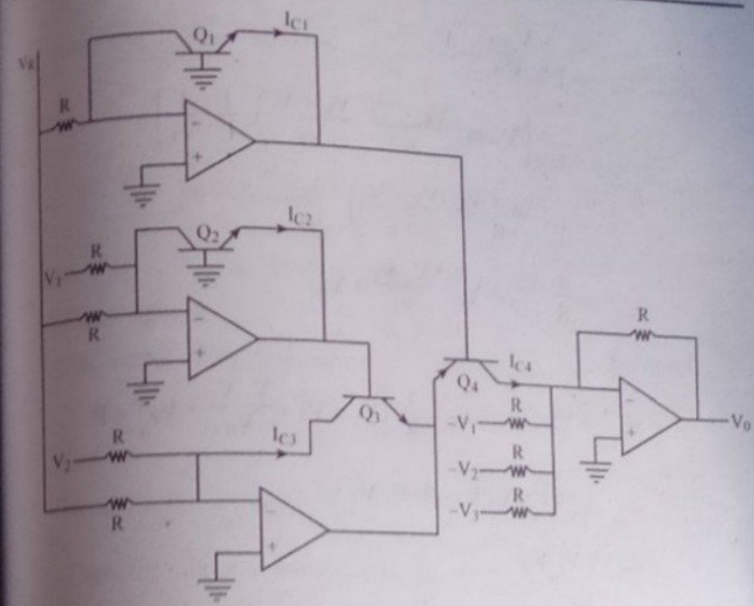


Fig: 4 Quadrant multiplier

From figure,

$$V_0 = V_1 + V_2 + V_R - I_{c4} R \quad \ldots\ldots (i)$$

Also, $V_{B4} = V_{E2} = -V_{BE2} + V_{B2}$

$$= -V_{BE2} = -V_T \ln\left(\frac{I_{c1}}{I_s}\right) = -V_T \ln\left(\frac{V_R}{RI_s}\right)$$

Again, $V_{E4} - 0 = -V_{BE3} - V_{BE2}$

or, $V_{E4} = -V_T \ln\left(\frac{I_{c3} \cdot I_{c2}}{I_s^2}\right)$

or, $V_{E4} = -V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2}\right)$

Now,

$$V_{BE4} = V_{B4} - V_{E4}$$

$$= -V_T \ln\left(\frac{V_R}{RI_s}\right) + V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2}\right)$$

$$= V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{R} \cdot \frac{1}{I_s^2} \cdot \frac{RI_s}{V_R}\right)$$

$$= V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R} \cdot \frac{1}{I_s}\right)$$

$$\text{So, } I_{C4} = I_s e^{\frac{V_{BE4}}{V_T}}$$

$$= I_s e^{\left[V_T \ln\left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R}\right) \cdot \frac{1}{I_s} \cdot \frac{1}{V_T}\right]}$$

$$= I_s \left(\frac{V_R + V_2}{R} \cdot \frac{V_R + V_1}{V_R}\right) \cdot \frac{1}{I_s}$$

$$= \frac{1}{R}\left\{V_1 + V_2 + \frac{V_1 V_2}{V_R} + V_R\right\}$$

From (a),

$$V_0 = V_1 + V_2 + V_R - \frac{1}{R}\left\{V_1 + V_2 + \frac{V_1 V_2}{V_R} + V_R\right\} \times R$$

$$= \frac{1}{-V_R} \cdot V_1 V_2 = k V_1 V_2$$

$$\therefore \quad V_0 = k V_1 V_2$$

where, $k = \frac{-1}{V_R}$

2. Why log antilog amplifier circuits are required? Draw the circuit diagram of antilog multiplier and explain it.

[2073 Chaitra, 2072 Kartik]

Solution:

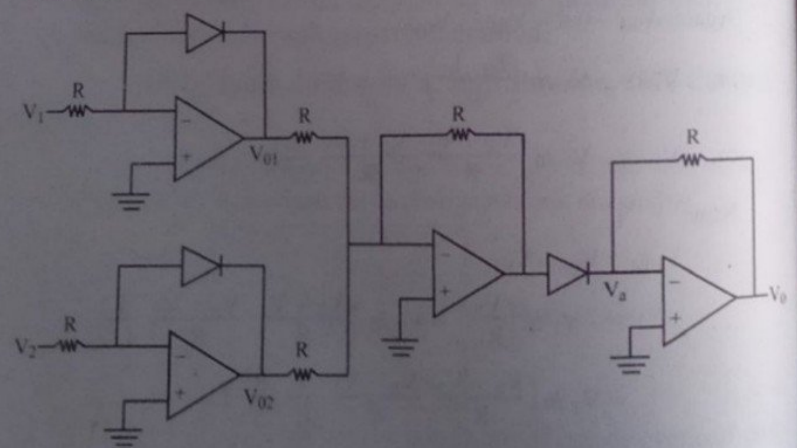


Fig: Multiplier circuit

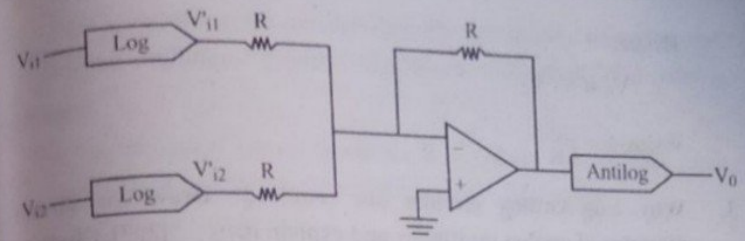


Fig: Block diagram of multiplyeer

From figure,

The output of log amplifier are

$$V_{01} = -\eta V_T \ln\left(\frac{V_1}{I_s R}\right)$$

Also, $V_{02} = -\eta V_T \ln\left(\frac{V_2}{I_s R}\right)$

Then, the output of adder circuit is,

$$V_a = -[V_{01} + V_{02}]$$

$$= -\left[-\eta V_T \ln\left(\frac{V_1}{I_s R}\right) - \eta V_T \ln\left(\frac{V_2}{I_s R}\right)\right]$$

$$= \eta V_T \ln\left(\frac{V_1 V_2}{I_s^2 R^2}\right)$$

Thus, the output of antilog amplifier is,

$$V_0 = -R I_s e^{\left(\frac{V_a}{\eta V_T}\right)}$$

$$= -R I_s e^{\left[\frac{\eta V_T \ln\left(\frac{V_1 V_2}{I_s^2 R^2}\right)}{\eta V_T}\right]}$$

$$= -R I_s e^{\left[\ln\left(\frac{V_1 V_2}{I_s^2 R^2}\right)\right]}$$

$$= -R I_s \frac{V_1 V_2}{I_s^2 R^2}$$

$$= -\frac{V_1 V_2}{I_s R}$$

$$= k V_1 V_2$$

Hence,

$$V_0 \propto V_1 V_2$$

Where $k = \frac{-1}{I_s R}$

3. **Why Log-Antilog circuits are required? Draw the circuit diagram of analog multiplier and explain it.** **[2071 Chaitra]**

Solution:

Part I: Refer to theory

Part II:

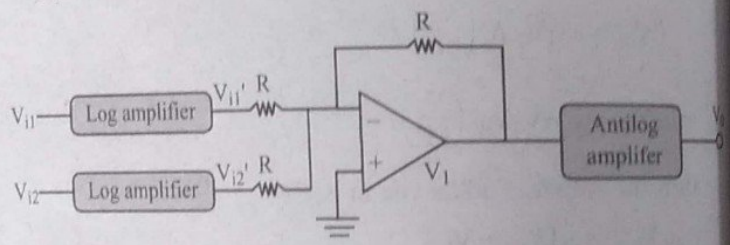


Fig: Multiplier

Multiplication of the numbers is the addition of their logs. So, if the logs of number are added using summing amplifier and its antilog is taken, the multiplication result is achieved.

From figure,

$$V_{i_1}^1 = K_1 l_n (K_2 V_{i_1})$$

$$V_{i_2}^1 = K_1 l_n (K_2 V_{i_2})$$

$$\therefore \quad V_1 = \frac{-R}{R}[V_{i_1}^1 + V_{i_2}^1] = -(V_{i_1}^1 + V_{i_2}^1) = -K_1 l_n (K_2^2 V_{i_1} V_{i_2})$$

For antilog amplifier,

$$V_0 = K_3 e K_4 V_1$$

$$= K_3 e K_4 (-K_1 l_n (K_2^2 V_{i_1} V_{i_2}))$$

$$= K_3 e x_p [-K_1 K_4 l_n (K_2^2 V_{i_1} V_{i_2})]$$

If $K_2 = K_3 = 1$ and $K_1 K_4 = -1$

$$V_0 = e x_p [l_n (V_{i_1} V_{i_2})]$$

$$\therefore \quad V_0 = V_{i_1} V_{i_2}$$

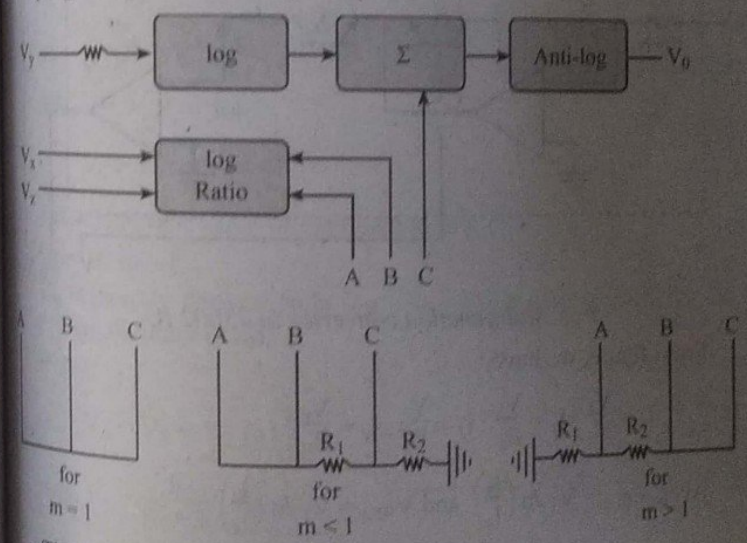
4. **How a multifunction converter can be constructed using log and antilog amplifiers? Explain with circuit realization.** **[2070 Ashad]**

Solution:

A multifunction converter circuit is a circuit that accepts three inputs V_x, V_y and V_z and yields an output V_0 of the type.

$$V_0 = kV_y \left(\frac{V_z}{V_x}\right)^m$$

Where k is a suitable scale factor (typically k = 1) and m is a user-programmable exponent in the range $0.2 < m < 5$. By proper selection of input configuration and exponent the circuit can be programmed for a variety of operations.



The input voltages can range from 0 to 10 v.

The multifunction converter is a useful I_c that can be used as a one-quadrant multiplier, squares, square rooter or exponent, depending on the voltage of m and accessory circuit used.

It is also can be used to produce an output voltage proportional to the sine, cosine or arctangent of an input voltage using additional circuit. The output may be,

$$V_0 = V_z V_y, \; V_0 = \frac{V_z}{V_x}, \; V_0 = Z_z^m, \; V_0 = V_z^{1/m}, \; V_0 = \frac{1}{V_x}$$

Operation of multifunction converter

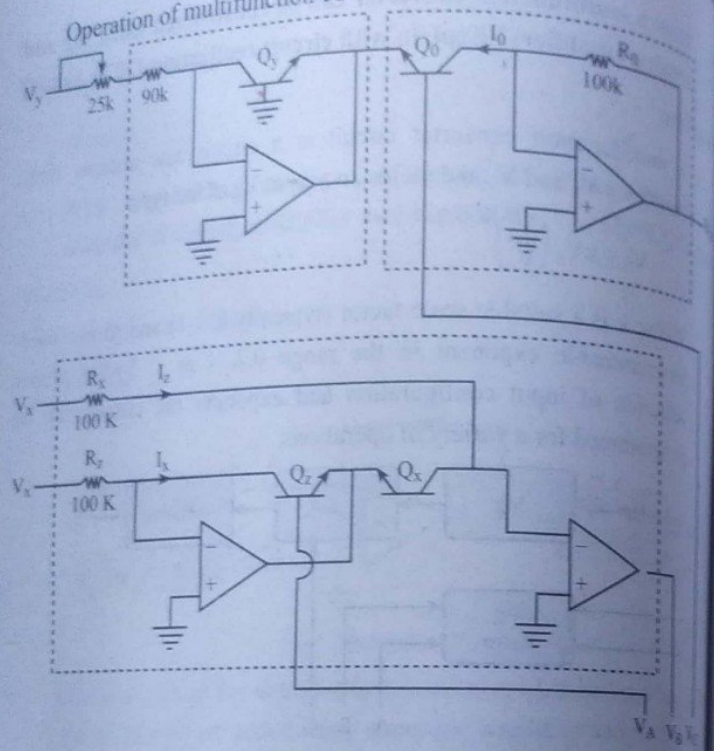


Fig: Multifunction converter in 43002 IC

From figure, we have,

$$I_x = \frac{V_x}{R_x};\ I_y = \frac{V_y}{R_y};\ I_z = \frac{V_z}{R_z};\ I_0 = \frac{V_0}{R_0}$$

Also, $V_{BEx} = V_T\, ln\left(\frac{I_x}{I_s}\right)$ and $V_{BEz} = V_T\, ln\left(\frac{I_z}{I_s}\right)$

So, $V_{BEz} - V_{BEx} = V_T\, ln\left(\frac{I_z}{I_x}\right)$

or, $V_{Bz} - V_{Ez} - V_{Bx} + V_{Ex} = V_T\, ln\left(\frac{I_z}{I_x}\right)$

$\therefore$ $V_{Bz} = V_A = V_T\, ln\left(\frac{I_z}{I_x}\right)$ ..... (i)

Similarly, $V_{BEy} = V_T\, ln\left(\frac{I_y}{I_s}\right)$ and $V_{BE0} = V_T\, ln\left(\frac{I_0}{I_s}\right)$

Then, $V_{BE0} - V_{BEy} = V_T\, ln\left(\frac{I_0}{I_y}\right)$

or, $V_{B0} - V_{E0} - V_{By} + V_{Ey} = V_T\, ln\left(\frac{I_0}{I_y}\right)$

$\therefore$ $V_{B0} = V_c = V_T\, ln\left(\frac{I_0}{I_y}\right)$ ..... (ii)

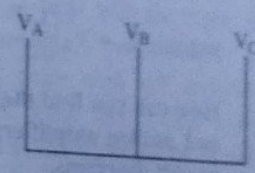
From equation (i) and (ii) V_A and V_C are found to be proportional to the log ratios of the corresponding currents.

Case I: m = 1

If $V_A = V_B = V_C$

V_A and V_C are derived directly from V_B so that $V_A = V_C$

or, $V_T\, ln\left(\frac{I_z}{I_x}\right) = V_T\, ln\left(\frac{I_0}{I_y}\right)$



$\therefore$ $\frac{I_z}{I_x} = \frac{I_0}{I_y}$

or, $\frac{V_z/R_z}{V_x/R_x} = \frac{V_0/R_0}{V_y/R_y}$

If $R_x = R_y = R_z = R_0$

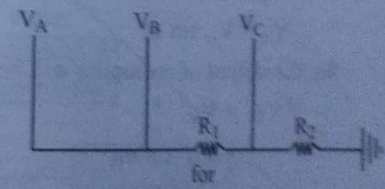
$\therefore$ $V_0 = V_y\left(\frac{V_z}{V_x}\right)$

This shows that value of exponent m is 1

Case II: m < 1

V_A is directly derived from V_B which V_C is derived from V_B via a voltage divider circuit.

Here,



$V_A = V_B = V_T\, ln\left(\frac{I_z}{I_x}\right)$

And, $V_C = \frac{R_2}{R_1 + R_2} V_B$

or, $V_C = mV_B$ $\left[\because \text{here } m = \frac{R_2}{R_1 + R_2} < 1\right]$

or, $V_T\, ln\left(\frac{I_0}{I_y}\right) = m\, V_T\, ln\left[\frac{I_z}{I_x}\right]$

or, $\frac{I_0}{I_y} = \left(\frac{I_z}{I_x}\right)^m$

Which implies, $V_0 = V_y\left(\frac{V_z}{V_x}\right)^m$ for equal value of resistors

Case III: m > 1

V_C is derived directly from V_B which V_A is derived from V_B via a voltage divider circuit.

So, $V_C = V_B = V_T \ln\left(\frac{I_0}{I_y}\right)$

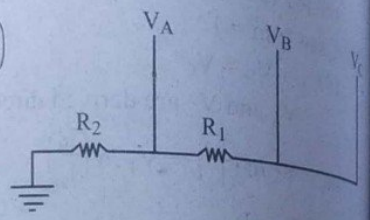
And, $V_A = \frac{R_2}{R_1 + R_2} V_B = \frac{1}{m} V_B \left[\text{Where } m = \frac{R_1 + R_2}{R_2} > 1\right]$

or, $V_A = \frac{1}{m} V_B$

or, $V_T \ln\left(\frac{I_z}{I_x}\right) = \frac{1}{m} V_T \ln\left(\frac{I_0}{I_y}\right)$

or, $\frac{I_z}{I_x} = \left(\frac{I_0}{I_y}\right)^{1/m}$

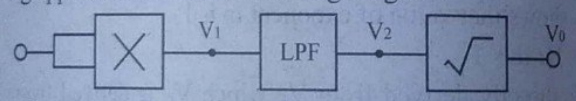
Implies, $V_0 = V_y \left(\frac{I_z}{I_x}\right)^m$



5. How can you find the RMS value of a sinusoidal signal using log and antilog amplifiers? Explain with necessary derivations and circuit diagrams. **[2069 Chaitra]**

Solution:

To find the RMS value of sinusoidal wave from a function of log antilog application we have following diagram



From figure, we have,

$V_{in} = V_m \sin \omega t$

So, the output of multiplier will be

$$V_1 = V_{in}^2$$
$$= V_m^2 \sin^2 \omega t$$
$$= \frac{V_m^2}{2}[1 - \cos 2\omega t]$$
$$= \frac{V_m^2}{2} - \frac{V_m^2}{2} \cos 2\omega t$$

The high pass frequency component $\cos_2\omega t$ is removed by low pass filter. So, output of LPF is

$$V_2 = \frac{V_m^2}{2}$$

So, the output of square route is,

$$V_0 = \sqrt{V_2} = \sqrt{\frac{V_m^2}{2}} = \frac{V_m}{\sqrt{2}}$$

❖❖❖

Chapter 7 Introduction to Power Electronics

7.1 Introduction

Power electronics involves the study of electronic circuits intended to control the flow of electrical energy. Power electronics combine power, electronics, and control. Control deals with the steady-state and dynamic characteristics of closed loop systems. Power deals with the static and rotating power equipment for the generation, transmission, and distribution of electric power. Electronics deals with the solid-state devices and circuit for signal processing to meet the desired control objective. Power electronics may be defined as the applications of solid-state electronics for the control and conversion of electric power. The interrelationship of power electronics with power, electronics, and control is shown in figure.

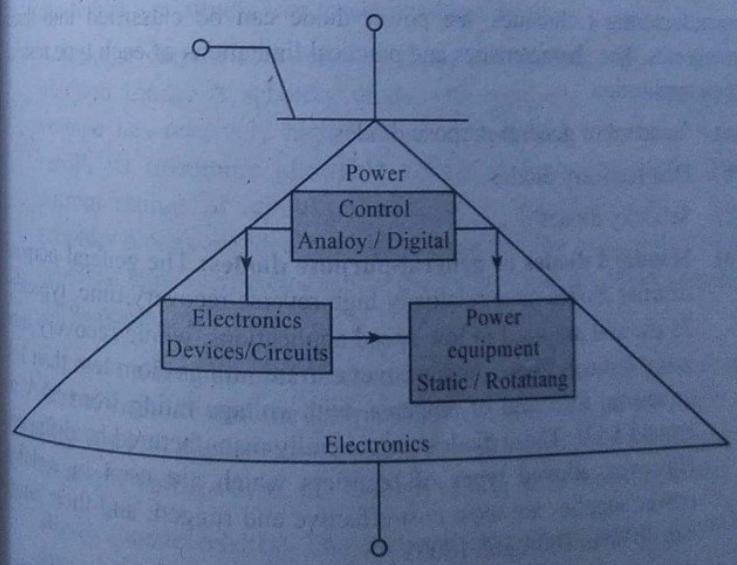


Fig: Relationship of power electrons to power, electronics and control

Power electronics is based primarily on the switching of the power semiconductor devices. With the development of power semiconductor technology, the power-handling capacities and the switching speed of the

power devices have improved tremendously. The development of microprocessors/microcomputer technology has a great impact on the control and synthesizing the control strategy for the power semiconductor devices. These circuits handle power flow at levels much higher than the individual device rating. Power semiconductor devices can be broadly divided into 5 types.

(a) Power diodes

(b) Thyristors

(c) Power BJTS

(d) Power MOSFETs

(e) Insulated-gate bipolar transistors (IGBTs) and static induction transistors (SI Ts)

7.1.1 Power diodes

Ideally, a diode should have no reverse recovery time. However, manufacturing cost of such a diode would increase. In many applications, the effect of reverse recovery time would not be significant and inexpensive diodes can be used. Depending on the recovery characteristics and manufacturing techniques, the power diode can be classified into three categories. The characteristics and practical limitations of each type restrict their application.

(a) Standard or general-purpose diodes

(b) Fast-recovery diodes

(c) Schottky diodes

(a) Standard diodes or general-purpose diodes: The general-purpose rectifier diodes have relatively high reverse recovery time, typically 25 μs, and are used in low-speed applications, whole recovery time is not critical. These diodes cover current ratings from less than 1 A to several thousand of amperes, with voltage rating from 50 V to around 5 kV. These diodes are generally manufactured by diffusion. However, alloyed types of rectifiers which are used in welding power supplies are most cost-effective and rugged; and their rating can go up to 300A and 1000V.

(b) Fast-Recovery diodes: The fast-recovery diodes have low recovery time, normally less than 5 μs. They are used in chopper and inverter circuits, where the speed of recovery is often of critical importance. These diodes cover current ratings from less than 1 A to hundreds of amperes, with voltage rating from 50V to around 3kV.

For voltage rating above 400V, fast-recovery diodes are generally made by diffusion and the recovery time is controlled by platinum or gold diffusion for voltage ratings below 400V, epitaxial diodes provide faster switching speeds than that of the diffused diodes. The epitaxial diodes have a narrow base width resulting in a fast recovery time of as low as 50ns.

(c) **Schottky diodes:** The charge storage problem of a pn-junction can be eliminated or minimized in a schottky diode. It is accomplished by setting up a "barrier potential" with a contact between a metal and a semi-conductor, A layer of metal is deposited on a thin exit axial layer of n-type silicon. The potential barriers simulates the behavior of a pn-junction. However, the rectifying action depends on the majority carriers only, and as a result there is no excess minority carriers to recombine. The recovery effect is due solely to the self-capacitance of the semiconductor junction.

The recovered charge of a schottky diode is much less than that of an equivalent pn-junction diode. Since it is due only to the junction capacitance, it is largely independent of the reverse di/dt. A schottky diode has a relatively low forward voltage drop.

A leakage current of a schottky diode is higher than that of a pn-junction diode. A schottky diode with relatively low conduction voltage has relatively high leakage current, and vice versa. As a result, its maximum allowable voltage is limited to 100V. The current ratings of schottky diodes varies from 1 to 300 A. The schottky diodes are ideal for high-current and low-voltage do power supplies. However, they are also used in low-current power supplies for increased efficiency.

- **A power diode conducts when its anode voltage is higher than that of cathode and the forward voltage drop of a power diode is very low. Typically 0.5 V. If the cathode voltage is higher than its anode voltage then, the diode is said to be in blocking mode.**

- **Diode characteristics: The forward current of power diode is given by**

$$I_0 = I_s\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

Where,

I_D is current through the diode

V_D is diode voltage

I_s is reverse saturation current

η is emission coefficient $(\because n \to 1, 2)$

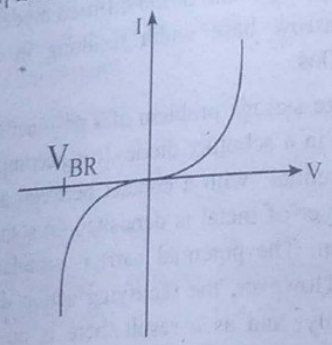


Fig: Practical

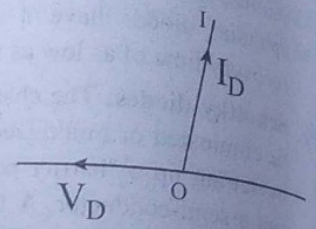


Fig: Ideal

Also, $V_T = \frac{kT}{q}$ = thermal voltage

T = Absolute temp

q = Charge of electron

k = Boltzmann constant

The reverse breakdown voltage V_{BR} is of the range 1 kV.

7.1.2 Thyristors

A Thyristor is the most important type of power semiconductor devices. Thyristors are extensively used in power electronic circuits. They are operated as bitable switches from no conducting state to conducting state. Although for the development of power conversion techniques in earlier chapters, thyristors are assumed as ideal switches, the practical thyristors exhibit certain characteristics and limitations.

Thyristors are usually three-terminal devices with four layers of alternating p and n-type material (i.e. three p – n junctions). The three terminals are anode(A), cathode (K) and gate (g) . Generally, anode is connected to positive with respect to cathode and control signal is given to the gate. It is widely used as switching devices in high power (> 1 kV, 100 A) control applications. It can control loads by switching current off and on up to many thousand times in a second. It allows the current to flow only in one direction so also be used as rectifier.

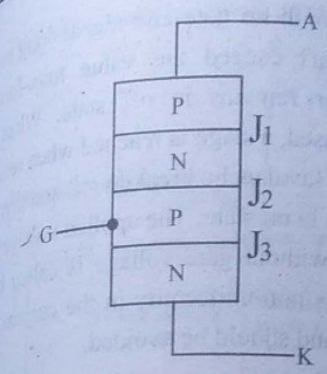


Fig: Thyristors

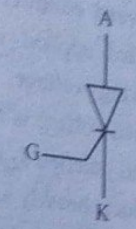
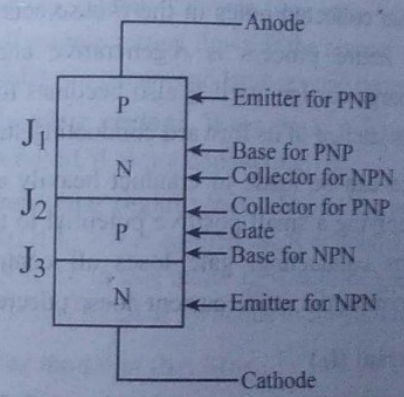


Fig: Symbol

The thyristor is sometimes also known as silicon controlled rectifier.

Basic operation of thyristors



There are generally three modes of operation.

(a) **Reverse blocking mode:** When the higher potential is applied to cathode than anode the device is in reverse blocking mode4.

(b) **Forward blocking mode:** When a positive voltage is applied to the anode with respect to cathode and the gate is open circuited, the thyristor is in forward blocking state. In practice, the gate is biased to a small negative voltage with respect to cathode to reverse base J_3 junction and hence to prevent charge carriers from being injured into the p-base.

(c) **Forward conducting mode:** With no gate current, as long as the forward applied voltage doesn't exceed the value max-forward blocking voltage, the thyristor remains in off state. When the applied voltage is further increased, a stage is reached when reverse-biased junction J_2 breaks down (avalanche breakdown) and thyristor conducts heavily and said to be in on state. The applied voltage with which SCR conducts heavily without gate voltage is called break over voltage. This mode causes non-uniformity in the current flow which is generally destructive and should be avoided.

When a gate is positive with respect to cathode, J_3 is forward biased and the electrons are emitted from the n-base. This collected charge causes a change in the bias current of J_1. The change in bias of J_1 causes holes to be injected from the p-emitter into the n-base. Those holes diffuse across the n-base and are collected in p-base. The addition of this collected holes in the p-base acts the same as gate current. The entire process is regenerative and will cause the increase in charge carriers until J_2 also becomes forward biased and the thyristor is latched in its forward conducting state.

So, the device can be made to conduct heavily at smaller applied voltage by applying a small positive potential to the gate. Once the thyristor starts conducting, gate loses all control. Even if gate voltage is removed, the anode current doesn't decrease at all.

- **Latching current (I_L)**

It is the minimum anode current required to maintain the thyristor in the ON-state immediately after a thyristor has been turned ON, and gate signal has been removed. So to turn the SCR ON, the forward current must be more than latching current.

- **Holding current (I_H)**

It is the minimum anode current required to maintain the thyristor ON-state. If the forward current is reduced below holding current the depletion layer again appears around junction J_2 and SCR will go to in blocking mode. The holding current is always less than latching current.

IV Characteristics curve of thyristor

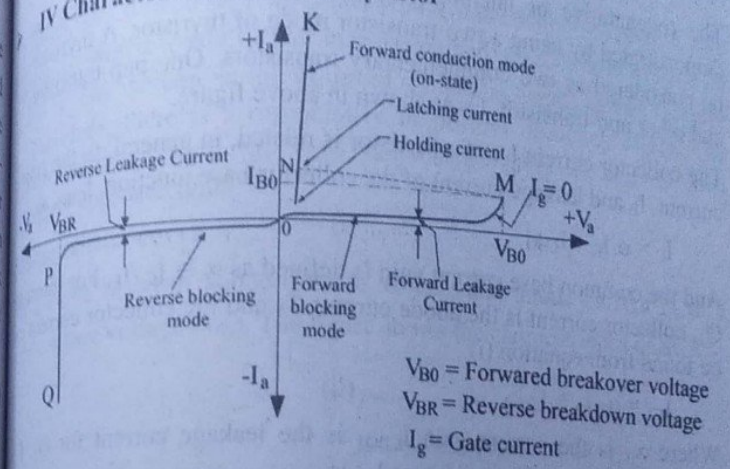


Fig: VI characteristic of thyristor

There are three regions

(a) **Reverse blocking region:** Cathode is positive with respect to anode and very small reverse current flows. If the reverse voltage is increased, avalanche breakdown occurs and large reverse current flows.

(b) **Forward blocking region:** When $V_Ak < V_{B0}$, forward leakage current flows but SCR is not conducting.

(c) **Forward conducting region:** When $V_{AE} > V_{B0}$ and $I_G = 0$, the SCR is in ON-state. If $I_G > 0$ is applied, SCR is conducting even if $V_{Ak} < V_{B0}$. for SCR to be in this mode I_A should be greater than I_C and if I_A is reduced below I_H, SCR switches to forward blocking region.

Two transistor model of thyristor.

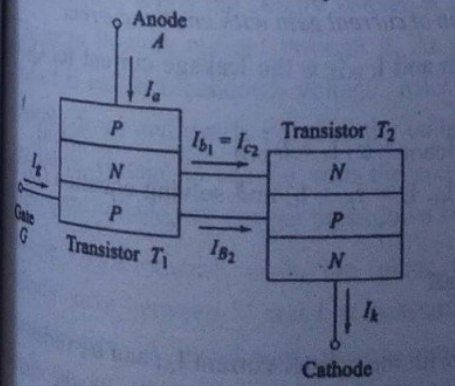


Fig: Basic structure

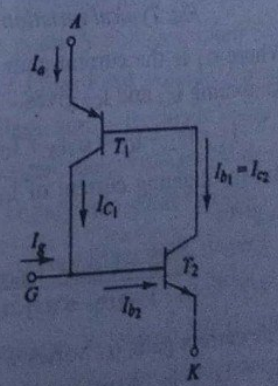


Fig: Equivalent circuit

The regenerative or latching action due to positive feedback can be demonstrated by using a two-transistor mode of thyristor. A thyristor can be considered as two complementary transistors. One pnp-transistor, Q_1 and other npn-transistor, Q_2 as shown in above figure.

The collector current I_C, of a thyristor is related, in general, to the emitter current. I_E and leakage current of the collector-base junction, I_{CBO}, as .

$$I_C = \alpha I_E + I_{CBO} \quad \text{... ... (i)}$$

And the common base current gain is defined as $\propto \cong I_C / I_E$. For transistor Q_1, collector current is the anode current, I_A and the collector current can be found from equation (i)

$$I_{C1} = \alpha_1 I_A + I_{CBo1} \quad \text{... ... (ii)}$$

Where $\propto_1$ is the current gain I_{CBO1} is the leakage current for Q_1. For transistor Q_2, the collector current I_{C2} is

$$I_{C2} = \alpha_2 I_k + I_{CBO2}$$

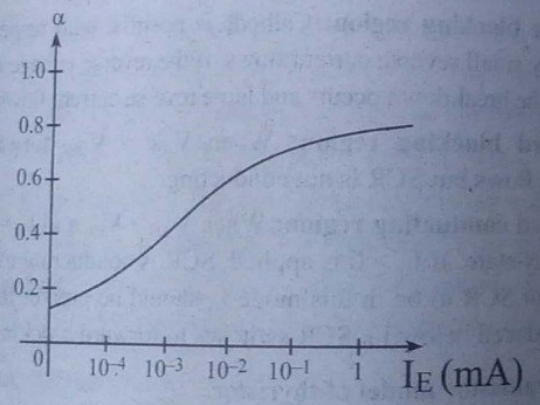


Fig: Typical variation of current gain with emitter current

Where α_2 is the current gain and I_{CBO2} is the leakage current for Q_2. By combining I_{C1} and I_{C2} gives.

$$I_A = I_{C1} + I_{C2} = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_1 + I_{CBO2} \quad \text{... ... (iii)}$$

But for a gating current of I_G, $I_k = I_A + I_G$ and solving equation (iii) for I_A gives

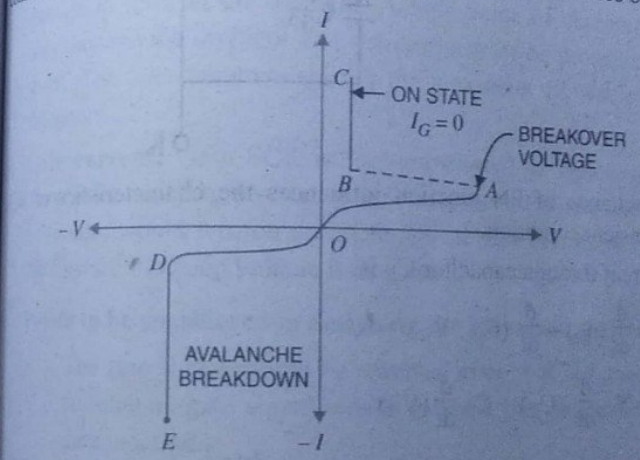
$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

The current gain, α_1 varies with the emitter current I_A; and α_2 varies with $I_k = I_A + I_G$, A typical variation of current gain, $\propto$, with the emitter current, I_E, is shown in above figure. If the gate current, I_G is suddenly

increased, say from 0 to 1 mA, this would immediately increase anode current, I_A, which would further increase α_1 and α_2. α_2 would depend on I_A and I_G. The increase in the values of α_1 and α_2 would further increase I_A. Therefore, there is a regenerative or positive feedback effect. The process continues until $(\alpha_1 + \alpha_2)$ approaches unity α_1 and α_2 can't separately approach unity.

Characteristics curve

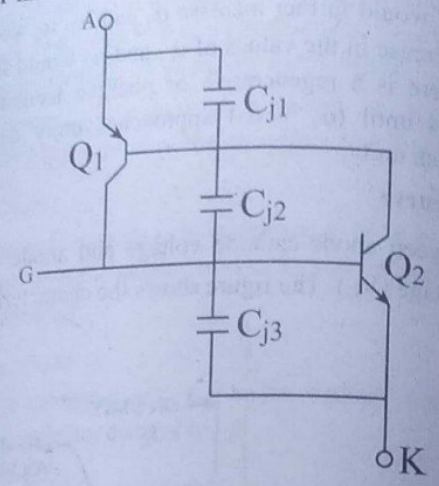
It is a curve between anode-cathode voltage and anode current I_A at a constant gate voltage (V_G). The figure shows the characteristics of SCR.



Forward characteristics: When a node is positive with respect to cathode curve between V and I at constant gate voltage called forward characteristics. When the supply voltage is increased from 0, at point A, SCR starts flowing current through it. At point A voltages when SCR conduct is called breakdown voltage. After breakdown voltage, voltage suddenly drops and nearly equal to the voltage across the load. Value of breakdown voltage is change with the constant gate voltage. With the proper gate voltage, we can get breakdown voltage at a small voltage.

Reverse characteristics: when the anode is negative with respect to cathode curve between V and I at constant gate voltage called reverse characteristics. A maximum reverse voltage at which SCR start conducting is called reverse breakdown voltage. You can see the reverse characteristics of SCR in the figure.

Two transistor model showing junction capacitances



The capacitance of PN junction influences the characteristics of SCR under transient condition.

Current through capacitor C_{j2} is

$$I_{j2} = \frac{d}{dt}(q_{j2}) = \frac{d}{dt}(C_{j2} \cdot V_{j2})$$

$$\therefore \quad I_{j2} = V_{j2}\frac{d}{dt}(C_{j2}) + C_{j2}\frac{d}{dt}(V_{j2})$$

This shows that if the rate of rise of voltage $\frac{dv}{dt}$ is large then I_{j2} would be large and this would result in increased leakage current I_{CBO1} and I_{CBO2}. It results in undesirable turn-ON of SCR.

➢ **Thyristor turn-OA**

A thyristor can be turned on by increasing the anode current. This can be accomplished in one of the following ways.

(a) **Thermals:** If the temperature of a thyristor is high, there will be an increase in the number of electron-hole pairs, which would increase the leakage currents. This increase in current would cause α_1 and α_2 to increase. Due to the regenerative action, $(\alpha_1 + \alpha_2)$ may tend to be unity and the thyristor may be turned on. This type of turn-on may cause thermal runaway and is normally avoided.

(b) **Light :** If light is allowed to strike the junctions of a thyristor, the electron-hole pair will increase; and the thyristor may be turned on. The light-activated thyristors are turned on by allowing light to strike the silicon water.

(c) **High voltage:** If the forward anode-to-cathode voltage is greater than the forward breakdown voltage V_{BO}, a sufficient leakage current will flow to initiate regenerative turn-on. This type of turn-on may be destructive and should be avoided.

(d) **dv/dt:** It can be noticed from

$$I_{j2} = \frac{d(q_{j2})}{dt} = \frac{d}{dt}(C_{j2}\,V_{j2}) = V_{j2}\frac{d\,C_{j2}}{dt} + C_{j2}\frac{d\,V_{j2}}{dt}$$

That if the rate of rise of the anode-cathode voltage is high, the charging current of the capacitive junctions may be sufficient enough to turn on the thyristor. A high value of charging current may damage the thyristor and the device must be protected against dv/dt. The manufacturers specify the maximum allowable dv/dt of thyristors.

(e) **Gate current:** If a SCR is forward biased, he injection of gate current (by applying positive gate voltage between gate and cathode terminals) would turn on the SCR. As the gate current is increased the forward blocking voltage is decreased.

➢ **Points to be considered in designing the gate control circuit.**

- The gate signal should be removed after SCR is turned ON. A continuous gate signal would increase the power loss in the gate junction.
- While SCR is reverse biased; there should be no gate signal other vise SCR may fail due to an increased leakage current.
- The width of gate pulse must be larger than time required for the anode current to rise to the holding current I_H.

➢ **di/dt protection of SCR**

The anode current starts flowing through the SCR when it is turned ON by the application of gate signal. This anode current takes some finite time to spread across the junctions of an SCR. For a good working of SCR, this current must spread uniformly over the surface of junction.

If the rate of rise of anode current (di/dt) is high results a non-uniform spreading of current over the junction. Due to the high current density, this further leads to form local hot spots near the gate-cathode junction. This effect may damage the SCr due to overheating. Hence, during turn ON process of SCR, the di/dt must be kept below the specified limits.

To prevent the high rate of change of an inductor is connected in series with thyristor. Typical SCR di/dt ratings are in range between 20 – 500 ampere per microseconds.

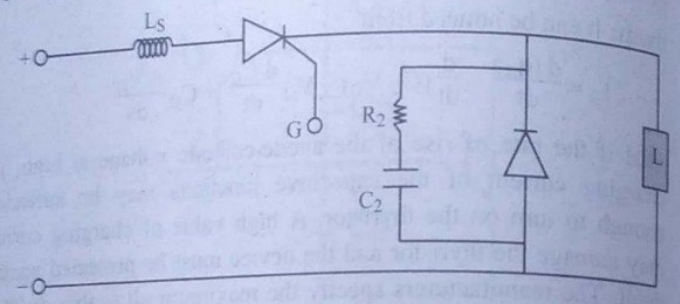


Fig: Dildt protection circuit

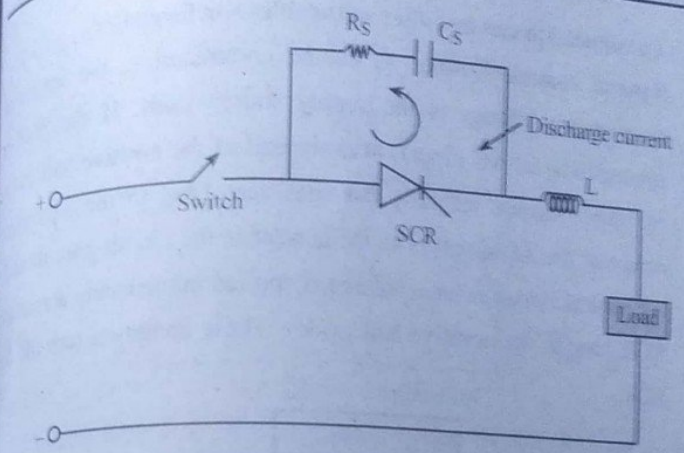
➢ **dv/dt protection of SCR**

When the SCR is forward biased, junctions J_1 and J_3 forward biased and junction J_2 is reverse biased. This reverse biased junction J_2 exhibits the characteristics of a capacitor. Therefore, if the rate of forward voltage applied is very high across the SCR, charging current flows through the junction J_2 is high enough to turn ON the SCR even without any gate signal.

This is called as dv/dt triggering of the SCR which is generally not employed as it is false triggering process. Hence, the rate of rise of anode to cathode voltage, dv/dt must be in specified limit to protect the SCR against false triggering. This can be achieved by using RC snubber network across the SCR.

➢ **Working of snubber circuit**

As we discussed above, the protection against high voltage reverse transients and dv/dt is achieved by using an RC snubber circuit. This snubber circuit consists of a series combination of capacitor and resistor which is connected across the SCR. This also consist an inductance in series with the SCR to prevent the high di/dt. The resistance value is of few hundred ohms. The snubber network used for the protection of SCR is shown below.



When the switch closed, a sudden voltage appears across the SCR which is bypassed to the RC network. This is because the capacitor acts as a short circuit which reduces the voltage across the SCR to zero. As the time increases, voltage across the capacitor builds up at slow rate such that dv/dt across the capacitor is too small to turn on the SCR. Therefore, the dv/dt across the SCR and the capacitor is less than the maximum dv/dt rating of the SCR.

Normally, the capacitor is charged to a voltage equal the maximum supply voltage which is the forward blocking voltage of the SCR. If the SCR is turned ON, the capacitor starts discharging which causes a high current to flow through the SCR.

This produces a high di/dt that leads to damage the SCR. And hence, to limit the high di/dt and peak discharge current a small resistance is placed in series with the capacitor as shown in above. These snubber circuits can also be connected to any switching circuit to limit the high surge or transient voltages.

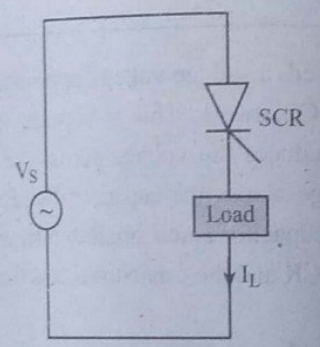
➢ **Turning off the SCR**

SCR after turning ON is not affected by gate voltage. It can only be turned off by reducing forward current to a level below the holding current I_H.

In all commutation techniques, the anode current is maintained below the holding current for a sufficiently long time so that all the excess carriers in the four layers are swept out or recombined.

- **Commutation can be either natural/line or forced.**

(a) **Natural communication:** In natural commutation, the source of commutation voltage is the supply source itself. If the SCR is connected to an AC supply, at every end of the positive half cycle, the anode current naturally becomes zero (due to the alternating nature of the AC supply). As the current in the circuit goes through the natural zero, a reverse voltage is applied immediately across the SCR (due to the negative half cycle). These condition turn off the SCR.



This method of commutation is also called as source commutation or AC line commutation or class F commutation. This commutation is possible with line commutated inverters, controlled rectifiers, cycle converters, and AC voltage regulators because the supply is the AC source in all these converters.

During the positive half cycle of the AC supply, the load current flows normally. But during the negative cycle, the SCR will turn off. For successful natural commutation, the turn off time off must be less than the duration of half cycle of the supply.

(b) **Forced communication:** To turn off a thyristor, the forward anode current should be brought to zero for sufficient time to allow the removal of charged curriers. In case of DC circuit, the forward current should be forced to zero by means of external circuits. This process is called forced commutation.

One of the method of forced commutation is shown below.

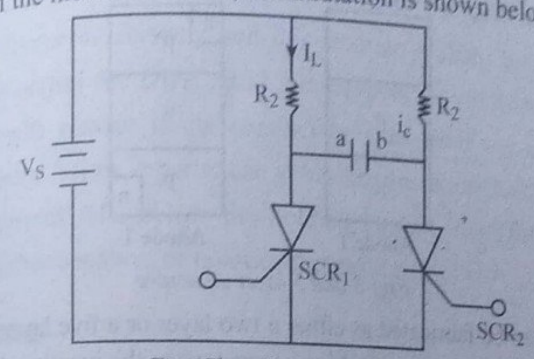


Fig: Class C commutation

Initially both SCR_1 and SCR_2 are off. Now SCR_1 is fired load current I_l flows through R_1. At the same time the capacitor C gets charged to V volts through R_2 and SCR_1 ('b' becomes + Ve w. r.t. 'a'). When capacitor gets fully charged, the capacitor current I_C becomes zero.

To turn off SCR_1, SCR_2 is fired, the voltage across C comes across SCR_1 and reverse biases it, hence SCR_1 turn off. At the same time the load current flows through R_1 and SCR_2. The capacitor 'C' charges towards V through and is finally charged to V volts with 'a' plate positive. When the capacitor is fully charged the capacitor current becomes zero. To turn off SCR_2, SCR_1 is triggered, the capacitor voltage (with 'a' positive) comes across SCR_2 and SCR_2 turns off.

7.1.3 DIAC

A DIAC is a full-wave or bidirectional semiconductor switch that can be turned on in both forward and reverse polarities. DIACs may also be called symmetrical trigger diodes-a term resulting from the symmetry of their characteristic curve.

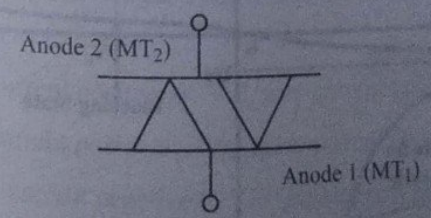


Fig: DIAC circuit symbol

DIACs are bi-direction devices in which the terminals cannot be labeled as anode and cathode as they are for a diode. Instead they may be labeled as A_1 and A_2 or MT_1 and MT_2, where MT stands for "Main terminal".

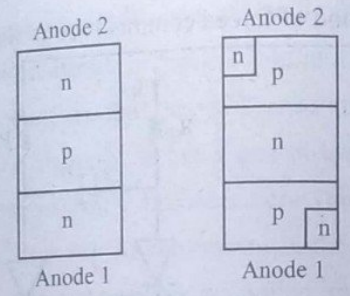


Fig: 3 and 5 layer structure

The DIAC can be fabricated as either a two layer or a five layer structure. In the tree layer structure the switching accurse when the junction that is reverse biased experiences reverse breakdown. The three layer version of the device is the more common and can have a break-over voltage of around 30V. Operation is almost symmetric wing to the symmetry of the device.

A five layer DIAC structure is also available. This doesn't act in quits the same manner, although it produces an I–V curve that is very similar to the three layer version. It can be considered as two break-over diodes connected back to back.

DIAC circuits use the fact that a DIAC only conduct current only after a certain breakdown voltage has been exceeded. The actual breakdown voltage will depend upon the specification for the particular component type.

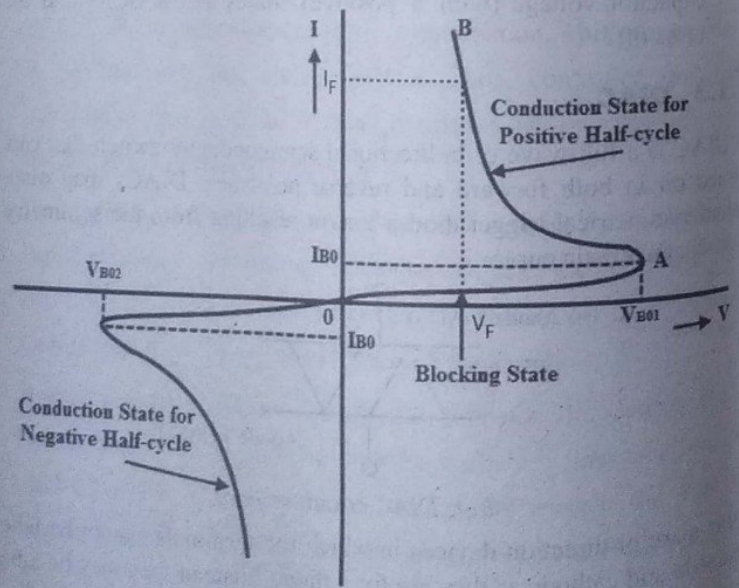


Fig: DIAC I-V characteristic

When the DIAC breakdown voltage occurs, the resistance of the component decreases abruptly and this leads to a sharp decrease in the voltage drop across the DIAC, and a corresponding increase in current. The DIAC will remain in its conducting state until the current flew through it drops below a particular value known as the holding current. When the current falls below the holding current, the DIAC switches back to its high resistance, or non-conducting state.

7.1.4 TRIAC

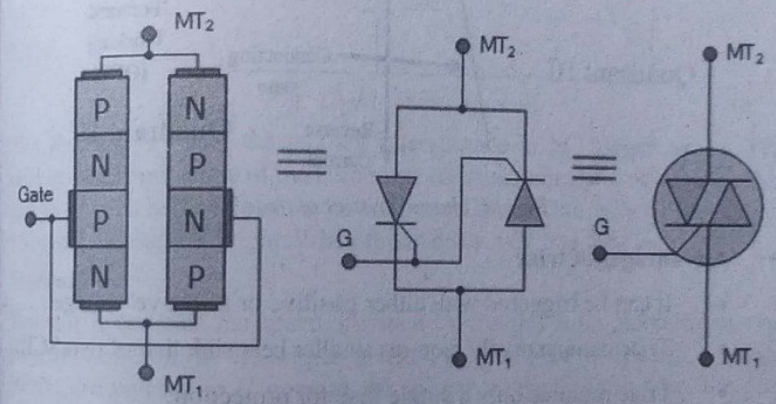


Fig: Physical construction ≡ Two-thyristor analogy ≡ circuit symbol

A triac is three terminal device that conducts current in either direction when triggered. A Triac can be triggered into conduction by both positive and negative voltages applied to its anode and with positive and negative trigger pulses applied to its gate terminal making it a two-quadrant switching gate controlled device. Then a triac has four possible triggering mode of operation as follows.

I + mode = MT_2 current positive (+ Ve), gate current positive (+ Ve)

I – mode = MT_2 current positive (+ Ve), gate current negative (– Ve)

III + mode = MT_2 current negative (– Ve), gate current positive (+ Ve)

III – mode = MT_2 current negative (– Ve), gate current negative (– Ve)

And these four modes in which a triac can be operated are shown using the triac I – V characteristic curves.

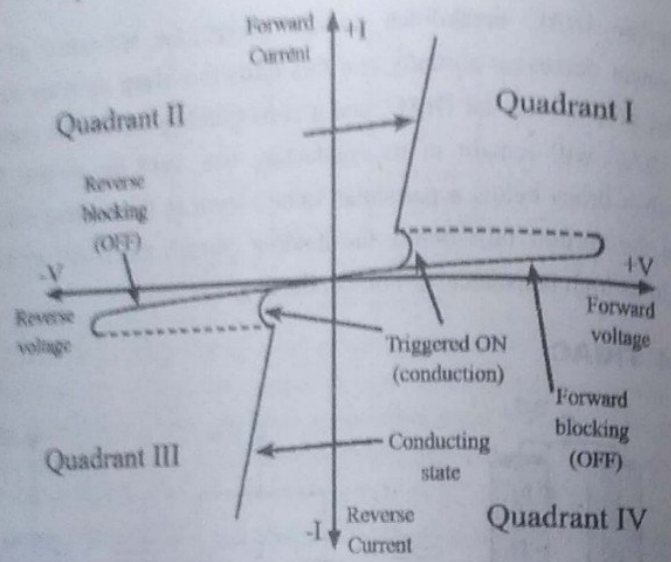


Fig: I-V characteristics of traic

- **Advantages of triac**
  - It can be triggered with either positive or negative voltage.
  - Triac comparatively requires smaller heat sink that of two SCR.
  - Triac requires only a single fuse for protection.
- **Disadvantages**
  - Triac are less reliable than SCR
  - Triac has less ratings than that of SCR
  - Triac has lower dv/dt rating
  - Triac trigger circuit needs careful consideration
- **Application of triac**
  - In many control application it has replaced SCR, due to its bidirectional conductivity.
  - Used in motor speed regulator, temperature control, illumination control, liquid level control, phase control circuits, power switches etc.
- **Light dimmer circuit :** Using thyristor, TRIACs, light dimmer can be made with small size and inexpensive with good efficiency to use in movie theatres, stages etc.

- **Working principle:** Solid-state light dimmers work by varying the duty cycle of the full AC voltage that is applied to the lights being controlled for eg. if only positive half cycle of applied voltage is used, the brightness of light will be low.

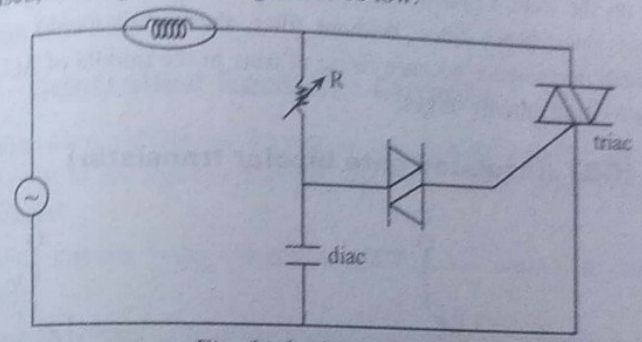


Fig: Light dimmer circuit

The rheostat R varies the amount of resistance in RC trigger circuit. This enables the firing angle of the triac to be adjusted throughout nearly the entire length of each half cycle of the power line AC waveform. When fired early in the cycle, the light is bright. When fired late in cycle, the light is dimmed.

Operation:

Resistor R controls the speed at which C, charges from incoming power. Higher the value of R, longer it takes C to charge to specific voltage. When the voltage at C goes to the trigger voltage of the diac, the diac starts to conduct, which discharge the charge from C through the diac to the triac gate causing it to trigger. Triac conducting causes power to flow through the circuit to the load. The voltage across triac is also zero. So, the capacitor doesn't charge as long as the triac conducts. At the next cycle, zero crossing voltage, charging of capacitor occurs. triac conducts as long as there is enough current flowing through it.

- **AC dimmer circuit**

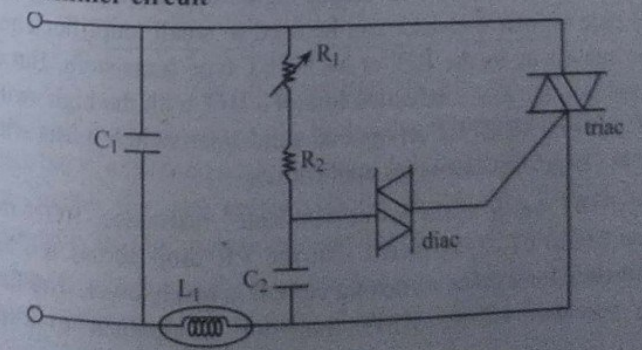


Fig: Dimmer circuit with filter

R_1 and C_2 in a diac-triac combination is just to delay the firing angle of diac from zero crossing. Larger the value of $(R_1 + R_2)$, longer it takes for the voltage across capacitor to rise to the point where the diac fires turning on the triac. Capacitor C_1 and inductor L_1 makes a simple radio frequency interference filter. Without filter, the circuit would generate quite much interference because firing of triac in the middle of AC phase cause fast rising current surges.

7.1.5 IGBT (Insulated gate bipolar transistor)

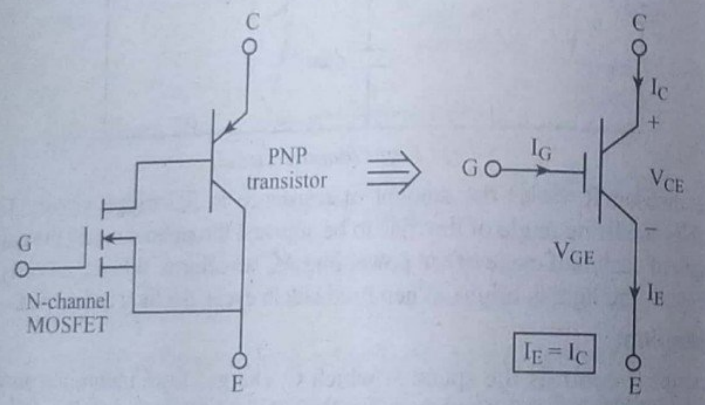


Fig: Simplified equivalent circuit and circuit symbol

Insulated gate bipolar transistor is a three terminal transconductanc device that combines an insulated gate N-channel MOSFET input with a PNP bipolar transistor output connected in a type of Darlington configuration. Two of its terminals (C – E) are associated with the conductance path which passes current, while its third terminal (G) controls the device.

The amount of amplification achieved by the insulated gate bipolar transistor is a ratio between its output signal and its input signal. The insulated gate bipolar transistor can be used in small amplifier circuit in much the same way as the BJT or MOSFET type transistors. But as the IGBT combines the low conduction loss of a BJT with the high switching speed of a power MOSFET an optimal solid state switch exists which is ideal for use in power electronics applications.

Also, the IGBT has a much lower "On-state" resistance, RON that an equivalent MOSFET. This means that the I^2R drop across the bipolar output structure for a given switching current is much lower. The forward blocking operation of the IGBT transistor is identical to a power MOSFET.

They are mostly used in

- Inverters
- Converters
- Power supplies

7.2 Controlled Rectifier Circuits

Rectifier using diodes are known as uncontrolled rectifier because for fixed value of AC input voltage the output DC voltage is fixed and cannot be changed.

Rectifier circuits using thyristors (SCRs) are known as controlled rectifier.

The output voltage of thyristor rectifiers is varied by controlling the delay or firing angle of thyristors. A phase-controlled thyristor is turned on by applying a short pulse to its gate and turned off due to natural or line commutations; and in case of a highly inductive load, it is turned off by firing another thyristor of the rectifier during the negative half-cycle of input voltage. These rectifier are simple and less expensive, the efficiency of these rectifier is above 95%.

➢ **SCR half wave rectifier circuit**

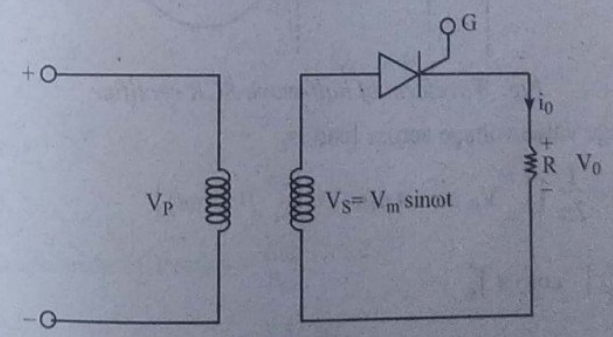


Fig: Half rectifier using SCR

For $-V_e$ half cycle, anode is $-V_e$ with respect to cathode so SCR will not conduct. SCR will conduct for positive half cycles if proper gate current flows. Greater the gate current smaller is the V_{B0}, SCR is turned off automatically due to line/nature commutation.

Firing angle is phase angle at which conduction begins. Conduction angle is angle of phase over which SCR conducts.

$$\phi = \pi - \alpha$$

ϕ – Conduction angle

$\propto$ – Firing angle

$\propto$ can be changed by changing gate current.

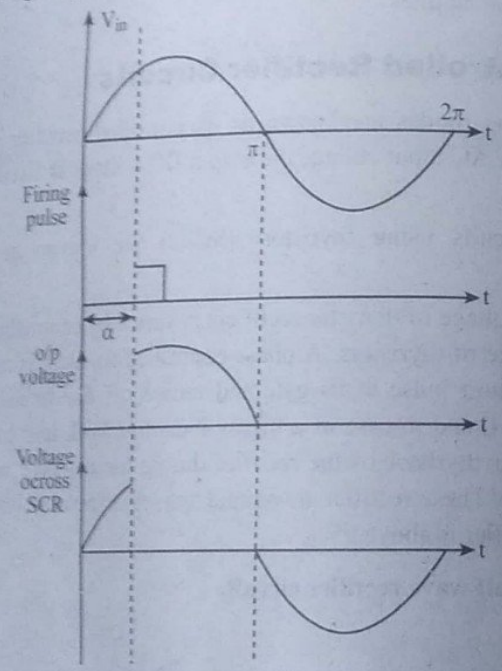


Fig: Waveform of half-wave SCR rectifier

The average value voltage across load is,

$$V_{DC} = \frac{1}{2\pi}\left[\int_{\propto}^{\pi} V_m \sin\omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0.\, d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}\left[-\cos\omega t\right]_{\pi}^{\propto}$$

$$= \frac{V_m}{2\pi}\left[1 + \cos\propto\right] \quad \text{..... (i)}$$

And, $I_{DC} = \frac{V_{dc}}{R} = \frac{V_m}{2\pi R}\left[1 + \cos\propto\right]$ ..... (ii) [∵ from equation (i)]

Also, $P_{DC} = \frac{V_{dc}}{t} \times I_{DC}$

$$= \frac{V_m}{2\pi}(1 + \cos\propto).\frac{V_{dc}}{t}$$ [∵ from equation (i) and (ii)]

Then,

RMS voltage across load is,

$$V_{RMS} = \left[\frac{1}{2\pi}\int_{\propto}^{\pi} V_m^2 \sin^2(\omega t)\, d(\omega t)\right]^{1/2}$$

$$= V_m\left[\frac{1}{2\pi}\int_{\propto}^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right).\, d(\omega t)\right]^{1/2}$$

$$= V_m\left[\frac{1}{4\pi}\left[\omega t - \frac{\sin 2\omega t}{2}\right]_{\propto}^{\pi}\right]^{1/2}$$

$$= V_m\sqrt{\frac{\pi-\propto}{4\pi} + \frac{\sin 2\propto}{8\pi}} \quad \text{..... (iii)}$$

Thus,

$$I_{RMS} = \frac{V_{RMS}}{R}$$

$$= \frac{V_m}{R}\sqrt{\frac{\pi-\propto}{4\pi} + \frac{\sin 2\propto}{8\pi}}$$ [∵ from equation (iii)]

Then,

$$P_{ac} = V_{RMS} \times I_{RMS}$$

Case I	**Case II**
If $\propto = 0$	If $\propto = \pi$
$V_{DC} = \frac{V_m}{\pi}$	$V_{DC} = 0$
$\therefore\ V_{RMS} = \frac{V_m}{2}$	$\therefore\ V_{RMS} = 0$

Thus,

$$\text{Rectification efficiency} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{V_{dc}.I_{dc}}{V_{RMS}.I_{RMS}}$$

Then,

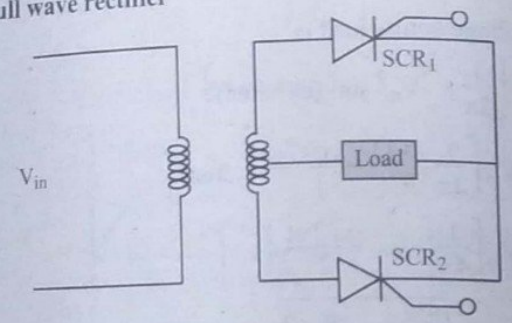
$$\text{Form factor} = \frac{V_{RMS}}{V_{dc}}$$

Also,

$$\text{Ripple factor} = \sqrt{(\text{form factor})^2 - 1}$$

$$\text{Trans formation utilization factor} = \frac{P_{dc}}{V_s.\ I_s\ (\text{in RMS})}$$

➢ **SCR full wave rectifier**



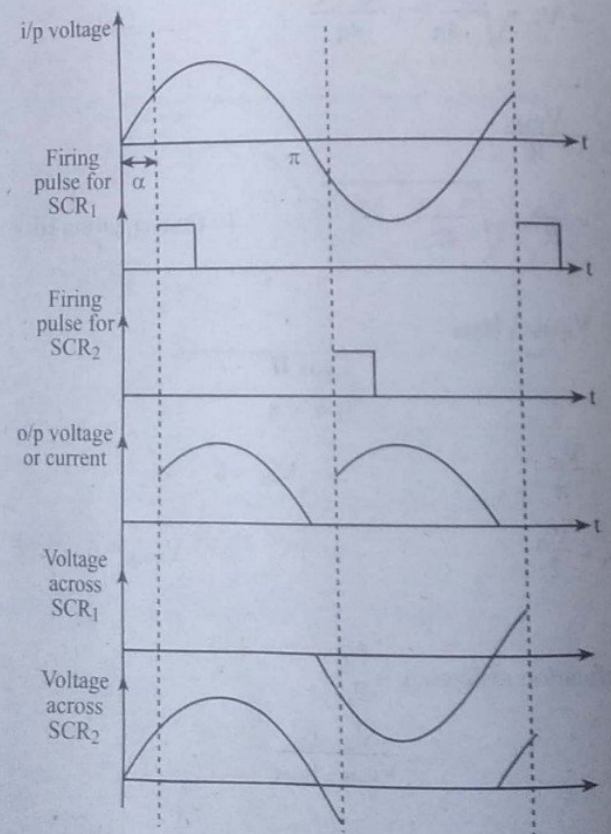


Fig: Waveform of SCR full wave rectifier

Average value of voltage across load is

$$\therefore \quad V_{DC} = \frac{2}{2\pi}\int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi}(1 + \cos \alpha)$$

Also,

$$I_{DC} = \frac{V_{dc}}{R} = \frac{V_m}{R\pi}(1 + \cos \alpha)$$

Thus,

$$P_{DC} = V_{DC} \times I_{DC}$$

$$= \frac{V_m^2}{R\pi^2}(1 + \cos \alpha)^2$$

Then,

$$V_{RMS} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= V_m = \left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{1/2}$$

Again,

$$I_{RMS} = \frac{V_{RMS}}{R}$$

$$= \frac{V_m}{R}\left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{1/2}$$

And, $P_{RMS} = V_{RMS} \times I_{RMS}$.

➢ **Resistance triggering circuit**

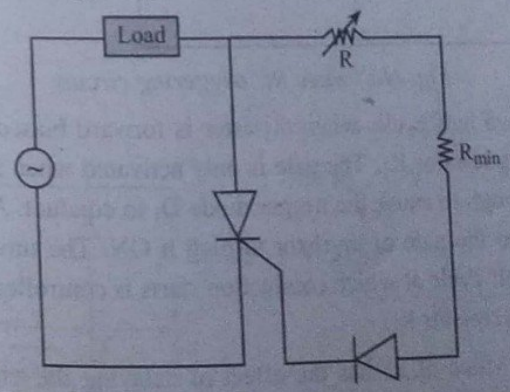


Fig: Resistance triggering circuit

The firing angle α can be controlled by varying resistance R. If R is more, the gate current will attain the value of I_{gmin} at a higher value of α and the conduction period of SCR would be lowered. When R = 0, the firing angle α is also minimum. Under this condition, only R_{min} is in the

circuit. The resistance R_{min} should be such that when R = 0, the gate current doesn't exceed the max allowable value,

$$\therefore \quad R_{min} \geq \frac{V_{max}}{I_{gmax}}$$

➢ **Drawbacks**

(a) The firing angle ∝ depends on I_{gmin} since the value of I_{gmin} is not absolute constant and is also temperature dependent, the value of ∝ can not be determined precisely.

(b) ∝ can vary only from 0° to 30°. This is because gate current must exceed I_{gmin}, when $V_s = V_{smax}$. In case of gate current is less than I_{gmin} at peak of supply voltage, SCR will not triggered at all.

➢ **Rc Triggering circuit**

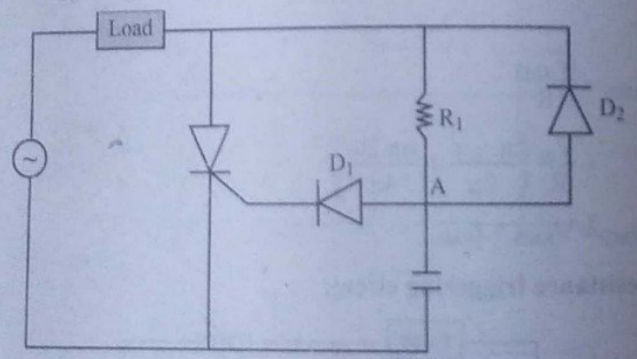


Fig: Half wave RC triggering circuit

During positive half cycle, when thyristor is forward biased, capacitor C charges up via resistor R_1. The gate is only activated when the voltage at point A is enough to cause the trigger diode D_1 to conduct. And capacitor discharges into the gate of thyristor turning it ON. The time duration in the positive half cycle at which conduction starts is controlled by RC time constant set by resistor R_1.

Increasing the value of R_1 has the effect of delaying the trigger voltage supplied to the thyristor gate which in turn causes a lag in the devices conduction time. As a result, a fraction of the cycle over which the device conducts can be controlled between 0° and 180°. However, the thyristor is a unidirectional device, so only a minimum of 50% power can be supplied.

7.3 Inverters

DC to AC converters are known as inverters. The function of an inverter is to change a DC input voltage to a symmetrical AC output voltage of desired magnitude and frequency. The output voltage could be fixed or variable at a fixed or variable frequency. A variable output voltage can be obtained by varying the input DC voltage and maintaining the gain of the inverter constant. On the other hand, if the DC input voltage is fixed and it is not controllable, a variable output voltage can be obtained by varying the gain of the inverter, which is normally accomplished by pulse- width-modulation (PWM) control within the inverter. The ratio of the AC output voltage to DC input voltage.

The output voltage waveforms of ideal inverters should be sinusoidal. However, the waveforms of practical inverters are non sinusoidal and contain certain harmonics. Inverters can be broadly classified into two types.

(a) Single-phase inverters

(b) Three-phase inverters

➢ **Half-wave single phase inverter**

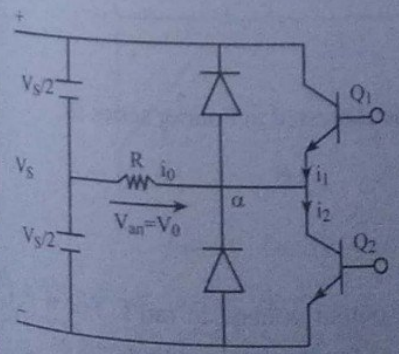


Fig (a): Circuit

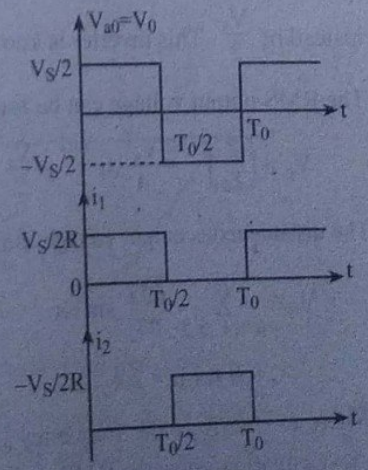


Fig (b): Wave form with resistive load

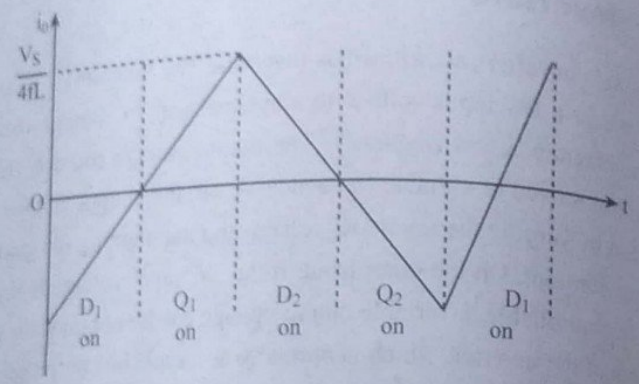


Fig (c): Single phase half-bridge inverter

The principle of single phase inverters can be explained with fig a. The inverter circuit consist of two choppers. When only transistor Q is turned on for a time $\frac{T_0}{2}$, the instantaneous voltage across the load V_0 is $\frac{V_s}{2}$. If transistor Q_2 only is turned on for a time $\frac{T_0}{2}$, $\frac{-V_s}{2}$ appears across the load. The logic circuit should be designed such that Q_1 and Q_2 are not turned on at the same time. Fig b shows the waveforms for the output voltage and transistor currents with a resistive load. This inverter requires a three-wired DC source, and when a transistor is off its reverse. Voltage is V_s, instead of $\frac{V_s}{2}$. This inverter is known as a half-bridge inverter.

The RMS output voltage can be found from

$$V_0 = \left(\frac{2}{T_0}\int_0^{T_0/2} \frac{V_s^2}{4}\,dt\right)^{1/2} = \frac{V_s}{2}$$

The instantaneous output voltage can be expressed in Fourier series as,

$$V_0 = \sum_{n=1,3,5}^{\infty} \frac{2V_s}{n\pi} \sin \omega t$$

$$= \theta \text{ for } n = 2,4 \ldots \ldots$$

Where $\omega = 2\pi f_0$ is the frequency of output voltage in rad/s. For n = 1, above equation gives the RMS value of fundamental components as.

$$V_1 = \frac{2V_s}{\sqrt{2}.\pi} = 0.45\ V_s$$

For an inductive load, the load current cannot change immediately with the output voltage. If Q_1 is turned off at $t = T_0/2$ the load current would continue to flow through D_2, load, and the lower half of the DC source until the current falls to zero. Similarly, when Q_2 is turned off at $t = T_0$, the load current flows through D_1, load, and the upper half of the DC source.

Single-phase bridge inverters

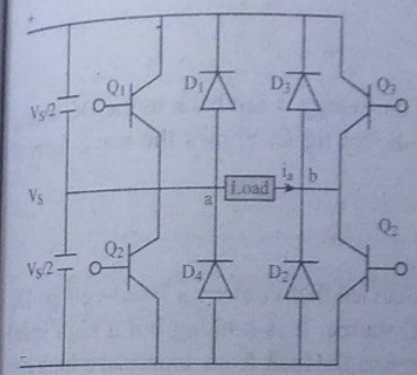


Fig (a): Circuit

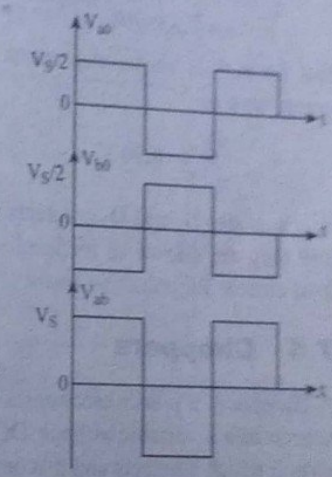


Fig (b): Wave forms

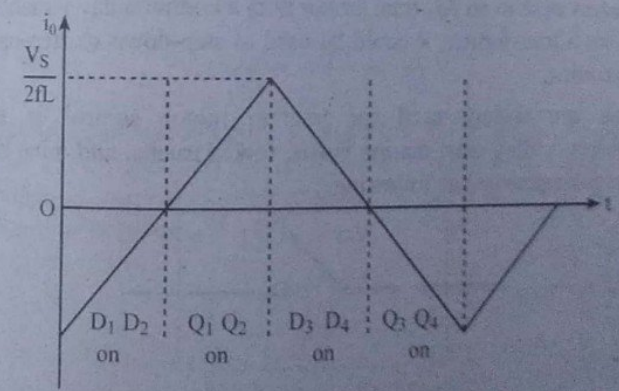


Fig (c): Load current with inductive load

A single-phase bridge inverter is shown in fig a. It consists of four choppers. When transistor Q_1 and Q_2 are turned on simultaneously, the input voltage V_s appears across the load. If transistors Q_3 and Q_4 are turned on at the same time the voltage across the load is reversed and is $-V_s$. The waveform for the output voltage is shown in fig b.

The RMS output voltage can be found from

$$V_0 = \left(\frac{2}{T_0}\int_0^{T_0/2} . V_s^2\, dt\right)^{1/2} = V_s$$

Above expression can be extended to express the instantaneous output voltage in a Fourier series as,

$$V_0 = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi} \sin n\omega t$$

and for n = 1, above expression gives the RMS value of fundamental component as,

$$V_1 = \frac{4V_s}{\sqrt{2}\pi} = 0.90\, V_s$$

When diodes D_1 and D_2 conducts the energy is fed back to the DC source and they are known as feedback diodes fig C. Shows the wave form of load current for inductive loads.

7.4 Choppers

A chopper is a power electronics device that convert a fixed-voltage DC source into a variable-voltage DC source. It is nothing but a high speed switch which connects and disconnects the load from source at a high rate to get variable or chopped voltage at output. A chopper can be considered as DC equivalent to an AC transformer with a continuously variable turns ratio. Like a transformer, it could be used to step-down or step-up a DC voltage source.

Choppers are widely used for traction motor control in electric automobiles, trolley cars, marine hoists, forklit trucks, and mine haulers. Chopper is represented as following.

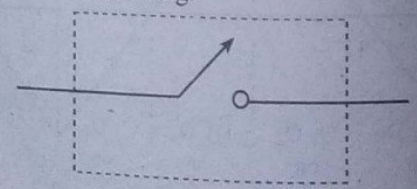


Fig: Chopper symbol

➢ **Chopper classification**

According to the direction of output voltage and current, chopper can be categorized as follows.

(a) First quadrant converter (Class A)

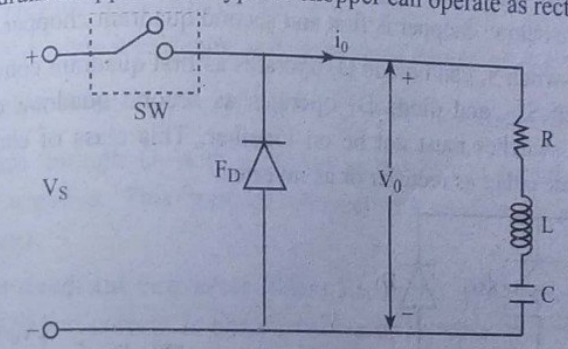
(b) Second quadrant converter (Class B)

(c) First and second quadrant converter (Class C)

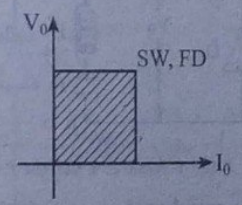
(d) Third and fourth quadrant converter (Class D)

(e) Four quadrant converter (Class E)

(a) **First quadrant chopper/converter (Class A):** If both o/p voltage and load current is positive i.e. if load current flows into the load with positive o/p voltage as shown in figure, the chopper is 1st quadrant chopper. This type of chopper can operate as rectifier.



For both case of switch (i.e. ON and OFF) current flows into load and V_0 is positive.



(b) **Second quadrant chopper (Class B):** If the current flows out of the load and output voltage is positive as shown in figure below, chopper is second quadrant chopper. In figure battery 'E' is the part of load or in DC motor it is back emf.

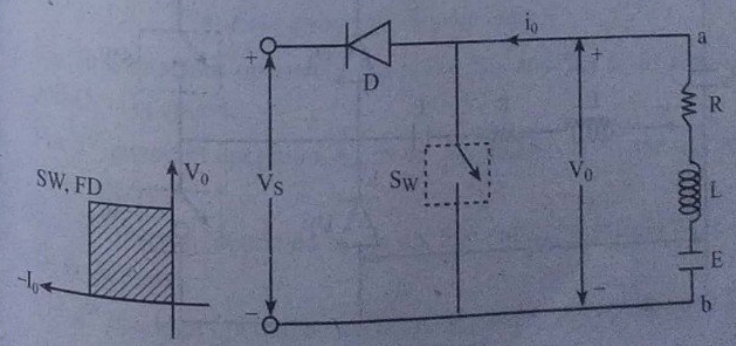


Fig: Close B chopper

When the S_w is on, E drives current through inductor and $V_0 = 0$ when the S_w is off, the energized inductor causes the load current to flow $\left[E + L\frac{di}{dt} > V_s\right]$ through diode towards i/p voltage. This type of chopper can operate as inverter.

(c) **First and second quadrant chopper (Class C):** If the load current is either positive or negative and o/p voltage is positive as shown in figure below, chopper is first and second quadrant chopper.

The switch S_{w1} and diode D_2 operates as first quadrant converter and switch S_{w2}, and diode D_1 operates as second quadrant converter. Two switches must not be on together. This class of chopper can operate either as rectifier or as inverter.

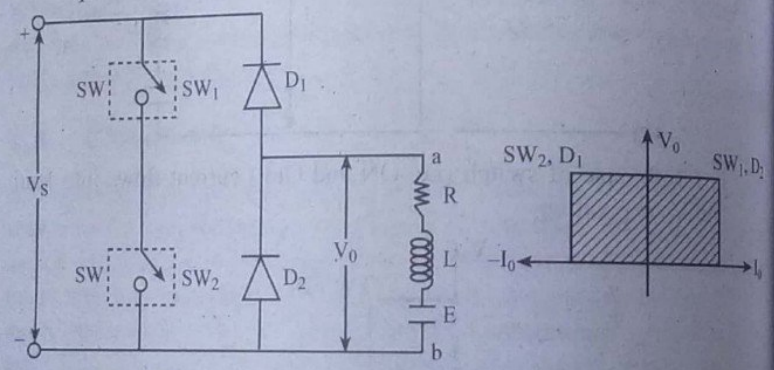


Fig: Class C chopper

(d) **Third and fourth quadrant converter (Class D):** If the o/p voltage is negative and load current is either positive or negative, the chopper is called third and fourth quadrant converter.

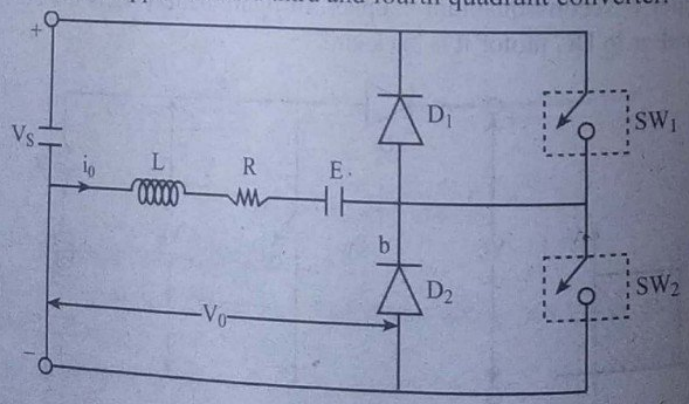


Fig: Class D chapper

When S_{w2} is off, S_{w1} and D_2 operates to yield negative output voltages and negative load current. When S_{w1} is closed and S_{w2} is open, $V_0 = V_{ab}$ is negative i.e. $V_{ab} = V_0 = -V_s$. So positive current flows from 'b' to 'a' but if load current is taken as shown, L_0 will be negative.

When S_{w1} is off S_{w2} and D_1 operates to yield negative o/p voltage and positive load current. So, if S_{w2} is on and S_{w1} is off, current flows as shown in figure and inductor is energized, but V_{ab} is still negative. When S_{w2} is off, $\left(E + L\frac{d_1}{dt}\right)$ will be sufficient to flow the current through D_1 with direction as shown and output voltage is still negative. This type of chopper can operate as rectifier or inverter.

(e) **Four quadrant converter (Class E):** In this type of chopper, load voltage and current is either positive or negative. It is the parallel combination of class C and class D chopper.

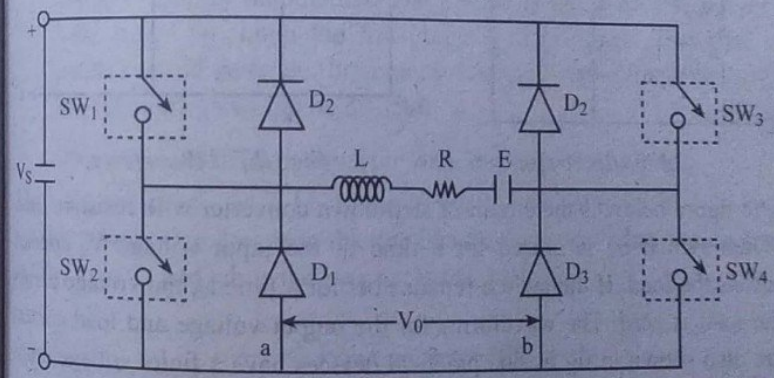


Fig: Four quadrant chopper class E

For first quadrant operation, S_{w4} is on, S_{w2} and S_{w3} is off and S_{w1} and D_1 is operated.

For 2nd quadrant operation, S_{w4} is on, S_{w1} and S_{w3} is off and S_{w2} and D_2 is operated.

For 3rd quadrant operation S_{w2} is on, S_{w1} and S_{wa} is off and S_{w3} and D_3 is operated.

For 4th quadrant operation, S_{w2} is on, S_{w1} and S_{w3} is off and S_{w4} and D_4 is operated.

7.5 DC-DC Conversion

The circuit which converts constant DC voltage/power to variable DC voltage/power is called DC-DC converter.

Basically there are two types of DC-DC conversion step down (Buck) converter and step-up (Boost) converter.

These step down and step up converter with different loads (resistive, inductive) are described below.

➢ **Step-Down (Buck) converter with resistive load**

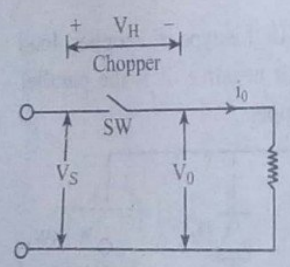


Fig: (a) circuit

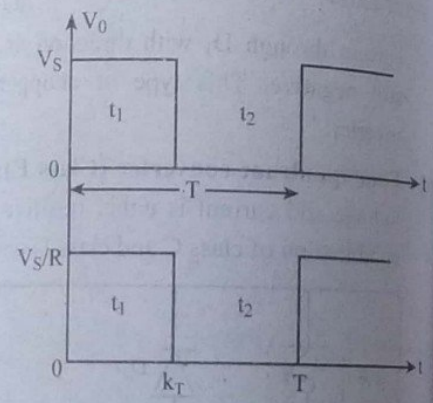


Fig: (b) Waveform

The figure below is the circuit of step-down converter with resistive load. When switch S_w is closed for a time t_1, the input voltage V_s appears across the load. If the switch remains off for a time t_2, the voltage across the load is zero. The waveforms for the output voltage and load current are also shown in fig b. The practical devices have a finite voltage drops ranging from 0.5 to 2V and for the sake of simplicity the voltage drops of these power semiconductor devices are neglected.

The average output voltage is given by.

$$V_0 = \frac{1}{T}\int_0^{t_1} V_0\, dt = \frac{t_1}{T} V_s = f\, t_1\, V_s = kV_s$$

and the average load current, $I_a = V_a/R = kV_s/R$, where T is the chopping period, $k = t_1/T$ is the duty cycle of a chopper, and f is the chopping frequency. The RMS value of output voltage is found from.

$$V_0 = \left(\frac{1}{T}\int_0^{kT} V_0^2\, dt\right)^{1/2} = \sqrt{K}\, V_s$$

Assuming a loss less chopper, the input power to the chopper is the same as the output power and is given by.

$$P_i = \frac{1}{T}\int_0^{kT} V_0\, i\, dt = \frac{I}{T}\int_0^{kT} \frac{V_0^2}{R}\, dt = k\frac{V_s^2}{R}$$

The effective input resistance seen by the source is,

$$R_i = \frac{V_s}{I_a} = \frac{V_s}{kV_2/R} = \frac{R}{k}$$

The duty cycle, k, can be varied from 0 to 1 by varying t_1, T or f. Therefore, the output voltage V_0 can be varied from 0 to V_s by controlling k and the power flow can be controlled.

(a) **Constant-frequency operation:** The chopping frequency, and (or chopping period T), is kept constant and the on-time, t_1, is varied. The width of the pulse is varied and this type of control is known as pulse-width-modulation (PWM) control.

(b) **Variable-frequency operation:** The chopping frequency, f, is varied either on-time, t_1, or off-time, t_2, is kept constant. This is called frequency modulation. The frequency has to be varied over a wide range to obtain the full output voltage range. This type of control would generate harmonics at unpredictable frequencies and the fitter design would be difficult.

➢ **Step down (BUCK) converter with inductive (RL) load**

This is also known as a buck converter. In this chopper, the average voltage output V_0 is less than that the input voltage V_s. When the chopper is ON, $V_0 = V_s$ and when the chopper is off, $V_0 = 0$

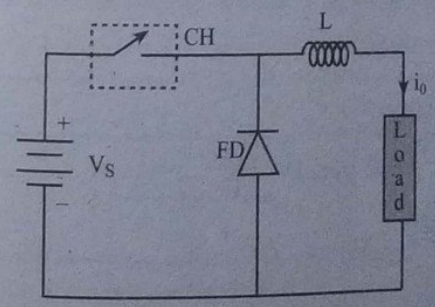


Fig: Free-wheel diode

When the chopper is ON

$$V_s = (V_1 + V_0)$$

or, $V_1 = V_s - V_0$

or, $L\frac{di}{dt} = V_s - V_0$

$\therefore \quad L\frac{\Delta i}{I_{ON}} = V_s + V_0$

Thus peak-to-peak current load is given by,

$$\Delta i = \frac{k_s - V_0}{L} T_{ON}$$

When the chopper is off, polarity reversal and discharging occurs at the inductor. The current passes through the free-wheel diode and the inductor to the load. This gives,

$$L\frac{di}{dt} = V_0 \quad \ldots\ldots (i)$$

Rewritten as : $L\frac{\Delta i}{T_{Off}} = V_0$

$$\therefore \Delta i = V_0 \frac{T_{off}}{L} \quad \ldots\ldots (ii)$$

Equation (i) and (ii) given;

$$\frac{V_s - V_0}{L} T_{ON} = \frac{V_0}{L} T_{off}$$

or, $\frac{V_s - V_0}{V_0} = \frac{T_{off}}{T_{ON}}$

or, $\frac{V_s}{V_0} = \frac{T_{ON} - T_{off}}{T_{ON}}$

The above equation gives,

$$V_0 = \frac{T_{ON}}{T} V_s = DV_s$$

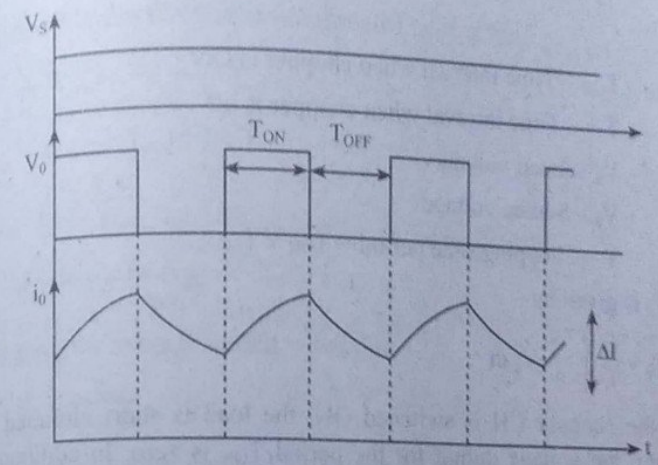
equation (i) gives –

$$\Delta i = \frac{V_s - DV_s}{L} DT; \text{ from } D = \frac{T_{ON}}{T}$$

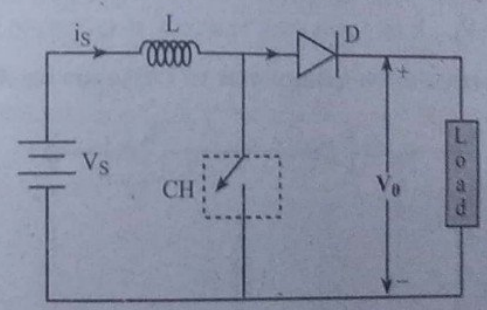
$$= \frac{V_s (I - D)D}{L.f}$$

$\therefore \quad f = \frac{I}{T}$ = chopping frequency

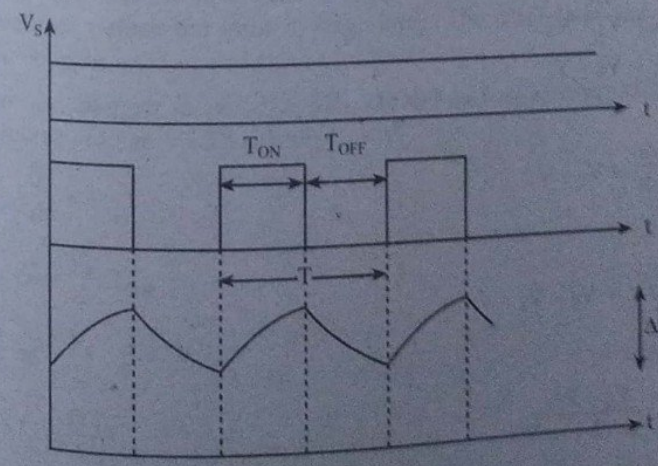
The current and voltage waveforms are given below for a step down chopper the voltage output is always less than the voltage input. This is shown by the waveform below.



- **Step up chopper (Boost converter with resistive load)**



The average voltage output (V_0) in a step up chopper is greater that the voltage input (V_s). The figure above shows a con figuration of a step up chopper. V_0 (average output voltage) is positive when chopper is switched ON and negative when the chopper is off as shown in the waveform below.



Where,

T_{ON} – Time interval when chopper is ON

T_{off} – Time interval when chopper is off

V_L – Load voltage

V_s – Source voltage

T – Chopping time period = $T_{ON} + T_{off}$

V_0 is given by –

$$V_0 = \frac{1}{T}\int_0^{T_{ON}} V_s\, dt$$

When the chopper CH is switched ON, the load is short circuited and therefore, the voltage output for the period T_{ON} is zero. In addition the inductor is charged during this time.

This gives $V_s = V_L$

$$L\frac{di}{dt} = V_s$$

$$\therefore \quad \frac{\Delta i}{T_{ON}} = \frac{V_s}{L}$$

Hence,

$$\Delta i = \frac{V_s}{L} \cdot T_{ON}$$

Δi = is the inductor peak to peak current. When the chopper CH is off, discharge occurs through the inductor L. Therefore, the summation of the V_s and V_L is given as follows,

$$V_0 = V_s + V_L$$

$$\therefore \quad V_L = V_0 - V_s$$

But,

$$L\frac{di}{dt} = V_0 - V_s$$

Thus,

$$L\frac{\Delta i}{T_{off}} = V_0 - V_s$$

This gives,

$$\Delta i = \frac{V_0 - V_s}{L} T_{off}$$

Equation Δi from ON state to Δi from off state gives,

$$\frac{V_s}{L} T_{ON} = \frac{V_0 - V_s}{L} T_{off}$$

or, $V_s (T_{ON} + T_{off}) = V_0 T_{off}$

$$\therefore V_0 = \frac{T V_s}{T_{off}}$$

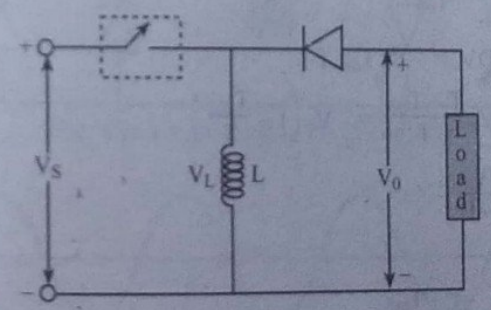
$$\therefore \quad V_0 = \frac{V_s}{(T + T_{ON})/T}$$

This gives the average output voltage as,

$$V_0 = \frac{V_s}{1 - D}$$

The above equation shows that V_0 can be varied from V_s to infinity. It proves that the output voltage will always be more than the voltage input and hence, it boosts up or increases the voltage level.

- **Buck Boost converter or step-up step-down converter**



This is also known as a buck-boost converter. It makes it possible to increase or reduce the input voltage level. The diagram shows a buck-boost chopper.

When the chopper is switched ON, the inductor L becomes charged by the source voltage V_s. Therefore, $V_s = V_L$.

$$L\frac{di}{dt} = V_s$$

or, $\Delta i = \frac{V_s}{L} T_{ON}$

or, $\Delta i = \frac{V_s}{L} \cdot T \cdot \frac{T_{ON}}{T}$

$$\therefore \quad \Delta i = \frac{DV_s}{L.f}$$

Where,

$$D = \frac{T_{ON}}{T} \text{ and } f = \frac{1}{T} \quad \text{..... (iii)}$$

When the chopper is switched off, the inductor's polarity reverses and this causes it to discharge through diode and the load.

Hence,

$$V_0 = -V_L$$

$$\therefore \quad L\frac{di}{dt} = -V_0$$

$$\text{or,} \quad L\frac{\Delta i}{T_{off}} = -V_0$$

$$\therefore \quad \Delta i = \frac{-V_0}{L} \cdot T_{off} \quad \text{..... (iv)}$$

Evaluating equation (iii) and (iv) gives

$$\frac{DV_s}{Lf} = \frac{-V_0}{L} T_{off}$$

$$\therefore \quad DV_s = -DV_s = -V_0 T_{off} \cdot f$$

$$\text{or,} \quad DV_s = -V_0 \frac{T - T_{ON}}{T} = -V_0\left(1 - \frac{T_{ON}}{T}\right)$$

$$\therefore \quad V_0 = -\frac{DV_s}{1-D}$$

Because,

$$D = \frac{T_{ON}}{T} = \frac{T - T_{off}}{1-D}$$

This gives,

$$V_0 = \frac{DV_s}{1-D}$$

D can be varied from 0 to 1. When,

$D = 0;\ V_0 = 0$

When $D = 0.5,\ V_0 = V_s$

When $D = 1,\ V_0 = \infty$

Hence in the interval $0 \le D \le 0.5$, Output voltage varies in the range $0 \le V_0 \le V_s$ and we get step down or buck operation. Whereas, in the interval $0.5 \le D \le 1$, output voltage varies in the range $V_s \le V_0 \le \infty$ and we get step up or boost operation.

7.6 AC to AC Conversion

The power electronics converter which is used to convert the AC waveforms of specific magnitude and specific frequency into AC current waveforms with different magnitude and different frequency, is called AC-AC converter.

There are many types of AC to AC converters like step up step down, single phase to single phase, three phases to single phase, 3 phase to 3 phase etc.

- **Single phase to single phase cyclo-converter**

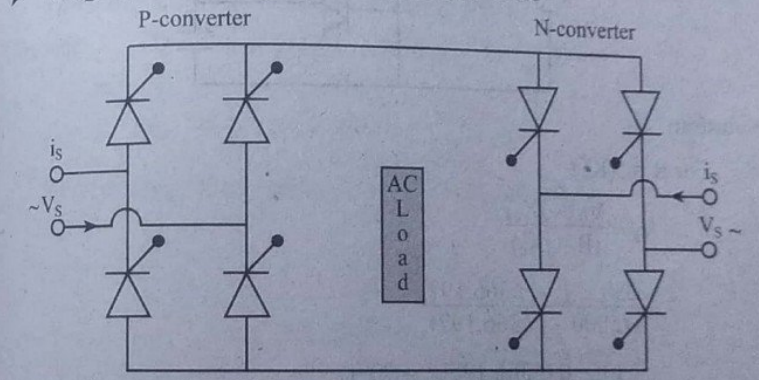


Fig: Circuit diagram of cyclo-converter

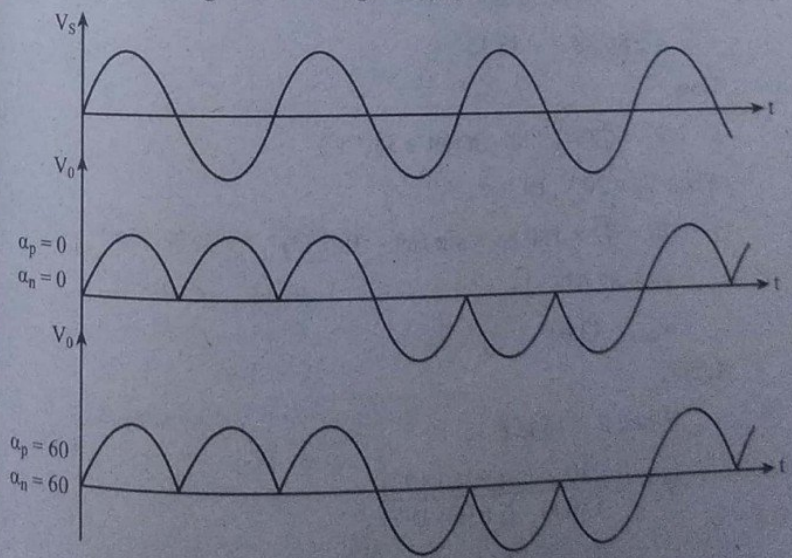
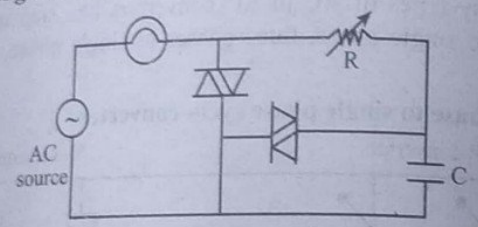


Fig: i/p and o/p waveforms of cycle converter

Simple cyclo-converter consists of two limbs, one for p-half cycle and other for n-half cycle of power supply. Each limb consists of 4 thyristors.

Numerical Problems

1 **In the TRIAC firing circuit, input voltage is 130 V, 50 Hz, DIAC breakdown voltage is 20 V, capacitance C = 0.5 μF, R can be varied from 5 KΩ to 15 KΩ. Find minimum and maximum firing angle of TRIAC.**



Solution:

For R = 5 KΩ

$$\therefore \quad V_c = \frac{V_0(-jX_c)}{(R - jX_c)}$$

$$= \frac{230 \angle (-j\,6366.197)}{(5000 - j\,6366.197)}$$

$$= \frac{230 \angle 0\,(6366.197 \angle -90°)}{8094.96 \angle -51.85}$$

$$= \angle 80.88 \angle -38.15$$

Thus,

$$\therefore \quad V_c = \sqrt{2} \times 18.88 \sin(\omega t - 38.15°)$$

When $V_c = 20$ V, $\omega t = \alpha_1 = ?$

$$\therefore \quad 20 = \sqrt{2} \times 180.88 \times \sin(\omega t - 38.15°)$$

$$\therefore \quad \alpha_1 = 42.63°$$

$$\therefore \quad \alpha_{min} = 42.63°$$

Again,

When R = 15 kΩ

$$V_c = \frac{230 \angle (-j\,6366.197)}{15000 - (j\,6366.197)}$$

$$= \frac{230 \angle (6366.197 \angle -90)}{1695.04 \angle -22.97}$$

$$= 89.85 \angle -67.03$$

So, $V_c = \sqrt{2} \times 89.85 \sin(\omega t - 68°)$

When $V_c = 20$ V, $\omega t = \alpha_2$

$$20 = \sqrt{2} \times 89.85 \sin(\alpha_2 - 68°)$$

$$\alpha_2 = 77.05°$$

$$\therefore \quad \alpha_{max} = 77.05°$$

2. **A SCR used in half-wave controlled rectifier is fired at angle of 30°. Input voltage for rectifier is 50 sin (200 t) and load resistance is 100Ω. Find average load voltage, RMS load voltage, efficiency and ripple factor for the rectifier.**

Solution:

$\alpha = 30°$ $\quad V_m = 50$ V

$f = 50$ $\quad R = 100\ \Omega$

Here, average load voltage $= \frac{V_m}{2\pi}[1 + \cos\alpha]$

$$= \frac{50}{2\pi}[1 + \cos 30]$$

$$= 14.84 \text{ V}$$

Also, RMS load voltage $= V_m\sqrt{\frac{(\pi - \alpha)}{4\pi} + \frac{\sin 2\alpha}{8\pi}}$

$$= 50\sqrt{\frac{(180 - 30)\pi}{4\pi \times 180} + \frac{\sin(2 \times 30°)}{8\pi}}$$

$$= 50\sqrt{0.2084 + 6.0345}$$

$$= 24.64 \text{ V}$$

$$\therefore \quad \text{Form factor} = \frac{V_{RMS}}{V_{dc}}$$

$$= \frac{24.64}{14.84}$$

$$= 1.660$$

$$\therefore \quad \text{Ripple factor} = \sqrt{(\text{form factor})^2 - 1}$$

$$= \sqrt{(1.66)^2 - 1}$$

$$= 1.325$$

$$P_{dc} = V_{dc} \cdot I_{dc} = V_{dc} \cdot \frac{V_{dc}}{R}$$

$$= 14.84 \times \frac{14.84}{100} = 2.202$$

$$P_{AC} = V_{RMS} \cdot I_{RMS}$$

$$= V_{RMS} \cdot \frac{V_{RMS}}{R}$$

$$= 24.64 \times \frac{24.64}{100}$$

$$= 6.071$$

$$\text{Rectifier efficiency} = \frac{P_{dc}}{P_{ac}}$$

$$= \frac{2.202}{6.071} \times 100\% = 36.26\%$$

3. The circuit below is adjusted so that the conductor angle commences 90° degree after the start of each + Ve cycle of applied voltage. The SCR voltage drop is negligible. The applied voltage 306 V RMS sinusoidal and the load is 50Ω resistor calculate.

(a) Average voltage

(b) The DC load current

(c) The power dissipated by the load

(d) RMS load current

Solution:

We have,

RMS voltage $V_{RMS} = 306$ V

$\therefore$ Peak voltage $V_{pp}(V_m) = \sqrt{2}\ V_{RMS}$

$= 432.74$ V

(a) Average voltage $= V_a = \frac{1}{2\pi}\int_{\pi}^{180} V_m \sin\theta\, d\theta$

$= V_a = 68.87$ V $\quad [\because \alpha = 90°]$

(b) DC load current $= \frac{V_a}{R_L} = \frac{68.87\text{ V}}{90\ \Omega} = 1.37$ A$_{mp}$

(c) Power dissipated by the load,

$P = I_\omega^2 R_L = (1.37)^2 \times 50$

$= 94.8\ \omega$

(d) Ram load current $(I_{rms}) = 1.1 \times I_{av}$

$= 1.1 \times 1.377$

$= 1.5147$ Amp.

$\left[\because \text{form factor} = 1.1 = \frac{I_{rms}}{I_{av}}\right]$

4. An AC voltage V = 240 sin 314 t is applied to an SCR. If the SCK has a forward breakdown voltage of 180 V. Find the time during which SCR remains off. Also find average current.

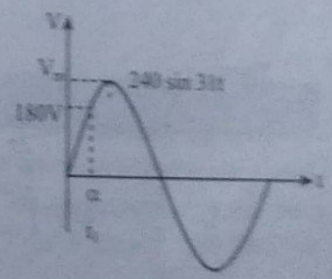
Solution:

We have,

$V = 240 \sin 314\, t$

Forward breakdown $V_0 = 180$ V

Consider the figure shown up to time t_1, the SCR remains off



Thus,

At time $t = t_1$

$V = 180$ V

$\therefore$ $180\text{ V} = 240 \sin 314\, t_1$

$\therefore$ $t_1 = \frac{1}{314}\sin^{-1}\left(\frac{180}{240}\right)$

$\therefore$ $t_1 = 2.7$ m sec

Then,

For $I_H = 200$ mA

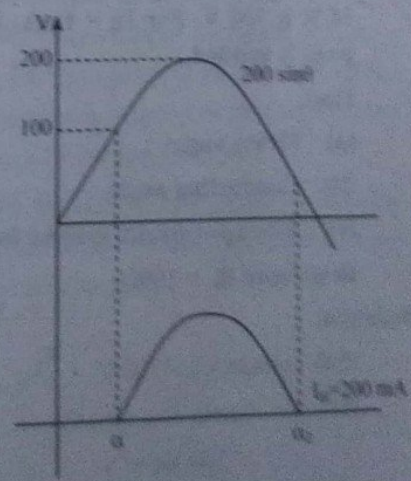
So, firing angle at

$\theta = \alpha$, $V = 200$ V

$100 = 200 \sin \alpha$

$\alpha = \sin^{-1}\left(\frac{100}{200}\right)$

$\therefore$ $\alpha = 30°$



5. To find the angle at which SCR will turn off. The angle now will be less than 180°. At $\theta = \alpha_2$ the SCR will be turn off.

Solution:

$$I_H = \frac{V}{R_L} \sin\theta$$

$$\therefore \quad 200 \text{ mA} = \frac{200}{100} \sin \alpha_2$$

$$\therefore \quad \alpha_2 = \sin^{-1}(100 \text{ m})$$

$$= \sin^{-1}(0.1)$$

$$= 5.74 \approx 6$$

So, turn off point will be $(180\times - \alpha_2) = 180 - 6° = 174°$

$\therefore$ Conduction angle $= 174° - 30°$

$= 144°$

Then,

$$\text{Average current } I_{av} = \frac{1}{2\pi}\int_{30°}^{144°} \frac{200}{100} \sin\theta \, d\theta$$

$$I_{av} = \frac{1}{\pi}(-\cos\theta)\int_{30°}^{144°} \frac{1}{\pi}(\cos 30° - \cos 144°)$$

$$\therefore \quad I_{av} = \frac{1}{\pi}(0.866 + 0.809) = 0.533 \text{ Amp.}$$

6. A half wave rectifier circuit employing an SCR is adjusted to have a gate current of 1 mA. The forward breakdown voltage of SCR is 100 V. For 1g = 1mA. If the sinusoidal voltage is 2004 peak is applied.

Find,

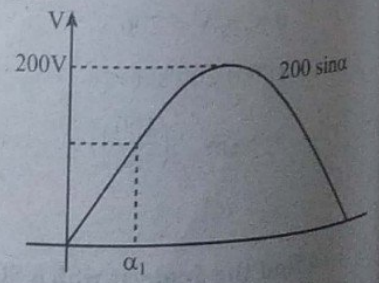
(a) Firing angle

(b) Conducting angle

(c) Average current, assume load

Resistance $R_L = 100\Omega$

Solution:



Peak voltage $V_m = 200$ V

(a) $V = V_m \sin \alpha$

$= 200 \sin \alpha$

at $\alpha = \alpha_1$

$V = 100$ V

$\therefore \quad 100 = 200 \sin \alpha_1$

$$\therefore \quad \text{Firing angle } \alpha_1 = \sin^{-1}\left(\frac{100 \text{ V}}{200 \text{ V}}\right) = 30°$$

(b) Conduction angle $= \phi = 180° - \alpha_1 = 150°$

$$\text{(c) Average current} = \frac{\text{Average voltage}}{R_L}$$

$$\text{or,} \quad I_a = \frac{V_m(1 + \cos\alpha_1)}{2\pi R_L}$$

$$= \frac{200\,(1 + \cos 30°)}{2 \times \pi \times 100}$$

$$= 0.5925 \text{ Amp.}$$

Old Questions with Solution

1. Define chopper circuit. Explain the working principle of signal phase half bridge inverter, with the necessary circuits and waveforms. **[2075 Ashwin, 2075 Chaitra]**

Solution:

A chopper is a power electronics device that convert a fixed-voltage DC source into a variable-voltage DC source. It is nothing but a high speed switch which connects and disconnects the load from source at a high rate to get variable or chopped voltage at output. A chopper can be considered as DC equivalent to an AC transformer with a continuously variable turns ratio. Like a transformer, it could be used to step-down or step-up a DC voltage source.

Choppers are widely used for traction motor control in electric automobiles, trolley cars, marine hoists, forklit trucks, and mine haulers. Chopper is represented as following.

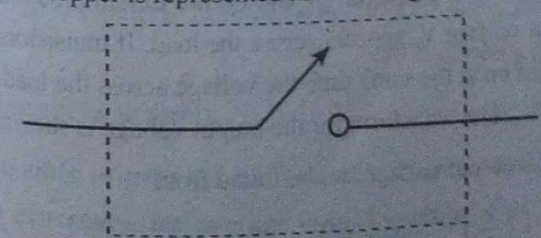


Fig: Chopper symbol

Single-phase bridge inverters

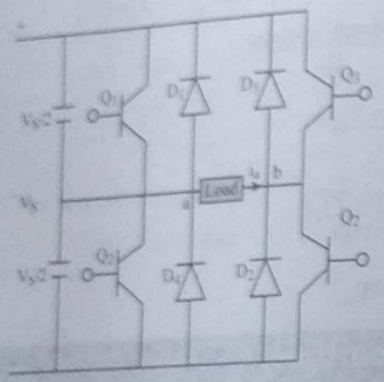


Fig (a): Circuit

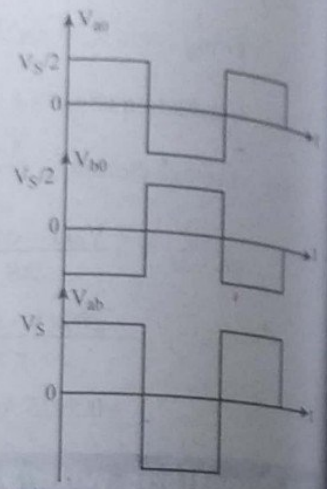


Fig (b): Wave forms

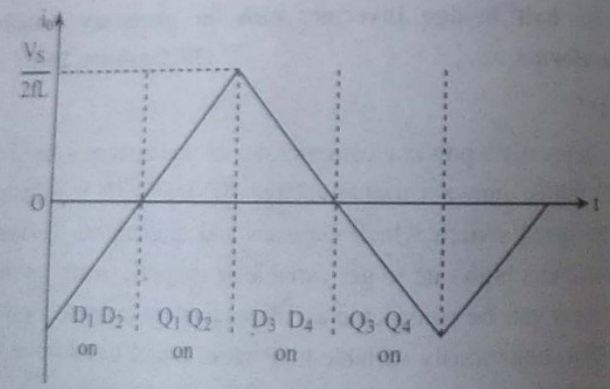


Fig (c): Load current with inductive load

A single-phase bridge inverter is shown in fig a. It consists of four choppers. When transistor Q_1 and Q_2 are turned on simultaneously the input voltage V_s appears across the load. If transistors Q_3 and Q_4 are turned on at the same time the voltage across the load is reversed and is $-V_s$. The waveform for the output voltage is shown in fig b.

The RMS output voltage can be found from

$$V_0 = \left(\frac{2}{T_0}\int_0^{T_0/2} V_s^2\, dt\right)^{1/2} = V_s$$

Above expression can be extended to express the instantaneous output voltage in a Fourier series as,

$$V_0 = \sum_{n=1,3,5}^{\infty} \frac{4V_s}{n\pi} \sin n\omega t$$

and for n = 1, above expression gives the RMS value of fundamental component as,

$$V_1 = \frac{4V_s}{\sqrt{2}\pi} = 0.90\ V_s$$

When diodes D_1 and D_2 conducts the energy is fed back to the DC source and they are known as feedback diodes fig C. Shows the wave form of load current for inductive loads.

2. What is the importance of Freewheeling Diode? Explain the principle of step up operation in Chopper with necessary figures and expressions. **[2074 Chaitra]**

Solution:

First part: Freewheeling diode is used to protect the circuit from unusual damage caused due to abrupt reduction in the current flowing through the circuit. It is also known as Flyback diode and forms connection across the inductor to remove Flyback voltage generated across it.

Second part: Refer to theory.

3. Explain the working principle of Silicon Controlled Rectifier, utilizing two transistor model with its VI curve.

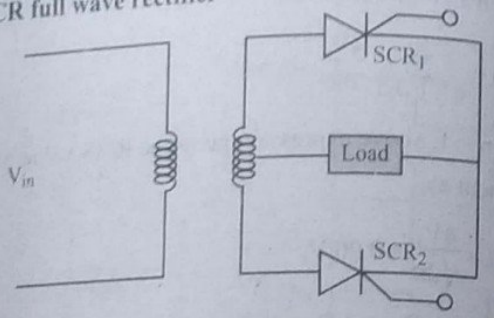
[2077 Chaitra, 2076 Ashwin, 2074 Chaitra, 2073 Shrawan, 2073 Chaitra, 2072 Kartik]

Solution: Please refer to theory

4. Is it possible to get variable output voltage in inverter? How? Derive expression for average output voltage of SCR full wave rectifier. **[2072 Chaitra]**

Solution:

➢ **SCR full wave rectifier**



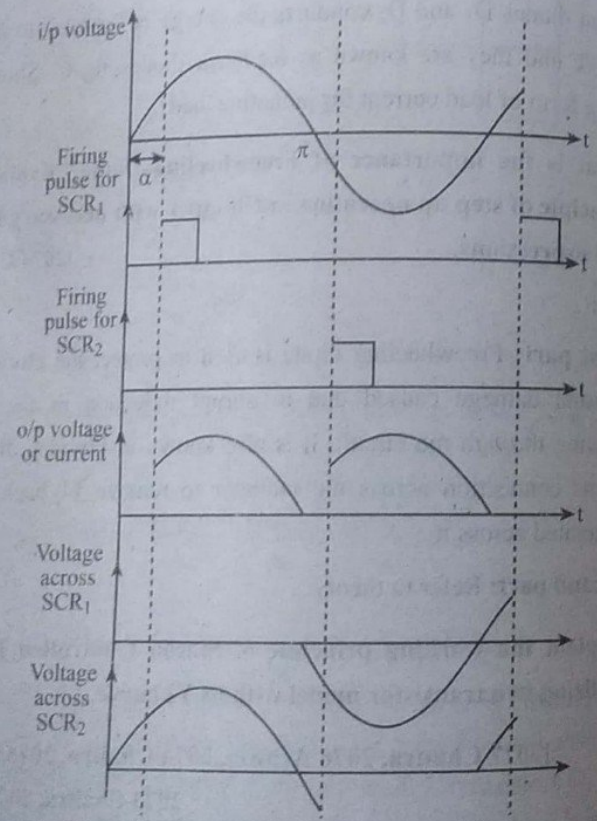


Fig: Waveform of SCR full wave rectifier

Average value of voltage across load is

$$\therefore \quad V_{DC} = \frac{2}{2\pi}\int_{\alpha}^{\pi} V_m \sin \omega t \, d(\omega t)$$

$$= \frac{V_m}{\pi}(1 + \cos \alpha)$$

Also,

$$I_{DC} = \frac{V_{dc}}{R} = \frac{V_m}{R\pi}(1 + \cos \alpha)$$

Thus,

$$P_{DC} = V_{DC} \times I_{DC}$$

$$= \frac{V_m^2}{R\pi^2}(1 + \cos \alpha)^2$$

Then,

$$V_{RMS} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 \sin^2 \omega t \, d(\omega t)\right]^{1/2}$$

$$= V_m = \left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{1/2}$$

Again,

$$I_{RMS} = \frac{V_{RMS}}{R}$$

$$= \frac{V_m}{R}\left[\frac{\pi - \alpha}{2\pi} + \frac{\sin 2\alpha}{4\pi}\right]^{1/2}$$

And, $P_{RMS} = V_{RMS} \times I_{RMS}$,

5. Explain the working of a step-down chopper with RL load with necessary derivations and Diagram. [2071 Shrawan]

Solution:

➢ **Step down (BUCK) converter with inductive (RL) load**

This is also known as a buck converter. In this chopper, the average voltage output V_0 is less than that the input voltage V_s. When the chopper is ON, $V_0 = V_s$ and when the chopper is off, $V_0 = 0$

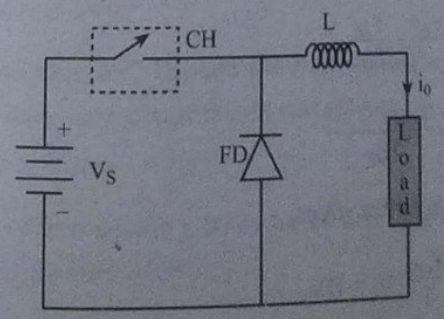


Fig: Free-wheel diode

When the chopper is ON

$$V_s = (V_l + V_0)$$

or, $V_l = V_s - V_0$

or, $L\frac{di}{dt} = V_s - V_0$

$\therefore$ $L\frac{\Delta i}{I_{ON}} = V_s + V_0$

Thus peak-to-peak current load is given by,

$$\Delta i = \frac{k_s - V_0}{L} T_{ON}$$

When the chopper is off, polarity reversal and discharging occurs at the inductor. The current passes through the free-wheel diode and the inductor to the load. This gives,

$$L\frac{di}{dt} = V_0 \qquad \text{..... (i)}$$

Rewritten as : $L\frac{\Delta i}{T_{Off}} = V_0$

$\therefore$ $\Delta i = V_0 \frac{T_{off}}{L}$ ..... (ii)

Equation (i) and (ii) given;

$$\frac{V_s - V_0}{L} T_{ON} = \frac{V_0}{L} T_{off}$$

or, $\frac{V_s - V_0}{V_0} = \frac{T_{off}}{T_{ON}}$

or, $\frac{V_s}{V_0} = \frac{T_{ON} - T_{off}}{T_{ON}}$

The above equation gives,

$$V_0 = \frac{T_{ON}}{T} V_s = DV_s$$

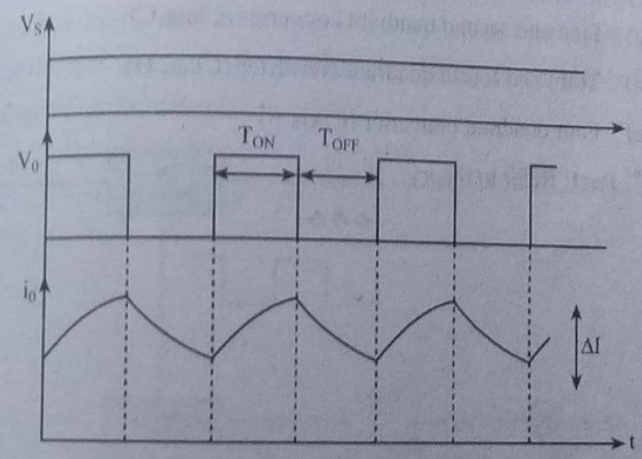
Equation (i) gives

$$\Delta i = \frac{V_s - DV_s}{L} DT; \text{ from } D = \frac{T_{ON}}{T}$$

$$= \frac{V_s (1 - D)D}{L.f}$$

$\therefore$ $f = \frac{1}{T}$ = chopping frequency

The current and voltage waveforms are given below for a step down chopper the voltage output is always less than the voltage input. This is shown by the waveform below.



6. **What are choppers? Explain the working principle of single phase, full bridge inverter with necessary diagrams and waveforms.** **[2071 Chaitra]**

Solution: Refer to theory

7. **What is an inverter? Explain the Buck switching regulator with required necessary diagram and waveforms.** **[2071 Chaitra]**

Solution: Refer to theory

8. **Can two complementary BJTs be used to make SCR? Explain about turning OFF of SCR.** **[2070 Chaitra]**

Solution: Refer to theory

9. **Classify chopper on the basis of power flow. Explain the principle of step-up converter with resistive load. [2070 Chaitra]**

Solution: Refer to theory

10. **Classify chopper. Explain principle of step-down chopper with RL load. [2078 Chaitra, 2076 Ashwin, 2068 Chaitra]**

Solution: According to the direction of output voltage and current, chopper can be categorized as follows.

(a) First quadrant converter (Class A)

(b) Second quadrant converter (Class B)

(c) First and second quadrant converter (Class C)

(d) Third and fourth quadrant converter (Class D)

(e) Four quadrant converter (Class E)

2nd Part: Refer to theory

❖❖❖

Chapter 8 Switched Power Supplies

The DC choppers can be used as switching mode regulators to convert a DC voltages, normally unregulated, to a regulated DC output voltage. The regulation is normally achieved by pulse-width modulation at fixed frequency and the switching device is normally a power BJT or MOSFET. The elements of switching mode regulators are shown in figure. We know that the output of DC choppers with resistive load is discontinuous and contains harmonics. The ripple content is normally reduced by an LC circuit.

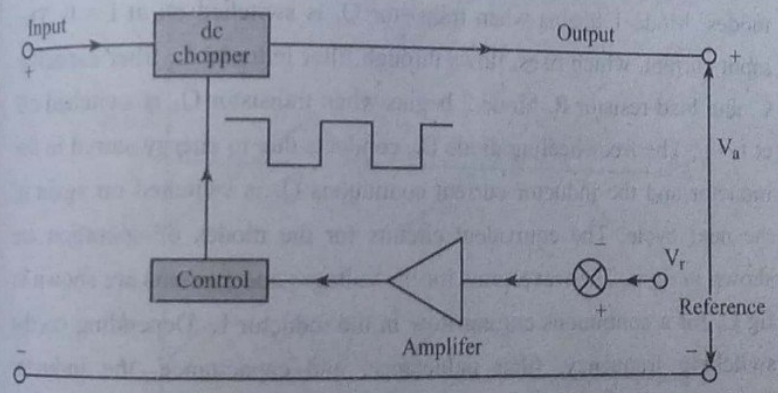


Fig: Elements of switching mode regulator

Switching regulators are commercially available as integrated circuits. The designer can select the switching frequency by choosing the values of R and C of frequency oscillator. As a rule of thumb to maximize efficiency, the minimum oscillator period should be about 100 times longer than the transistor switching time, for example, if a transistor has a switching time of 0.5μs, the oscillator period would be 50μs, which gives the maximum oscillator frequency of 20 kHz. This is due to the switching loss in the transistor. The transistor switching loss increases with the switching frequency and the efficiency decreases. In addition, the core

loss of inductors limits the high-frequency operation. There are four basic topologies of switching regulators.

(a) Buck regulators

(b) Boost regulators

(c) Buck-boost regulators

(d) Cut-regulators

8.1 Buck Regulators

In a buck regulator, the average output voltage V_a, is less than the input voltage, V_S hence the name "buck" a very popular regulator. The circuit diagram of a buck regulator using a power BJT is shown in fig a_c and this is like a step-down chopper. The circuit operation can be divided into two modes. Mode 1 begins when transistor Q, is switched on at t = 0. The input current, which rises, flows through filter inductor L, filter capacitor C, and load resistor R. Mode 2 begins when transistor Q_1 is switched off at $t = t_1$. The freewheeling diode D_m conducts due to energy stored in the inductor and the inductor current continuous Q_1 is switched on again in the next cycle. The equivalent circuits for the modes of operation are shown in fig b. The waveforms for the voltages and currents are shown in fig C, for a continuous current flow in the inductor L. Depending on the switching frequency, filter inductance, and capacitance, the inductor current could be discontinuous.

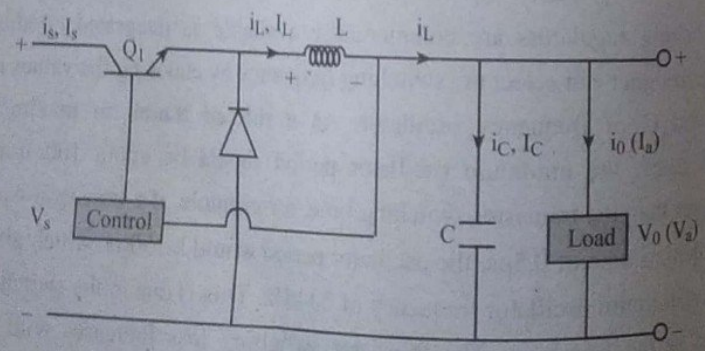


Fig: circuit diagram of Buck regulator

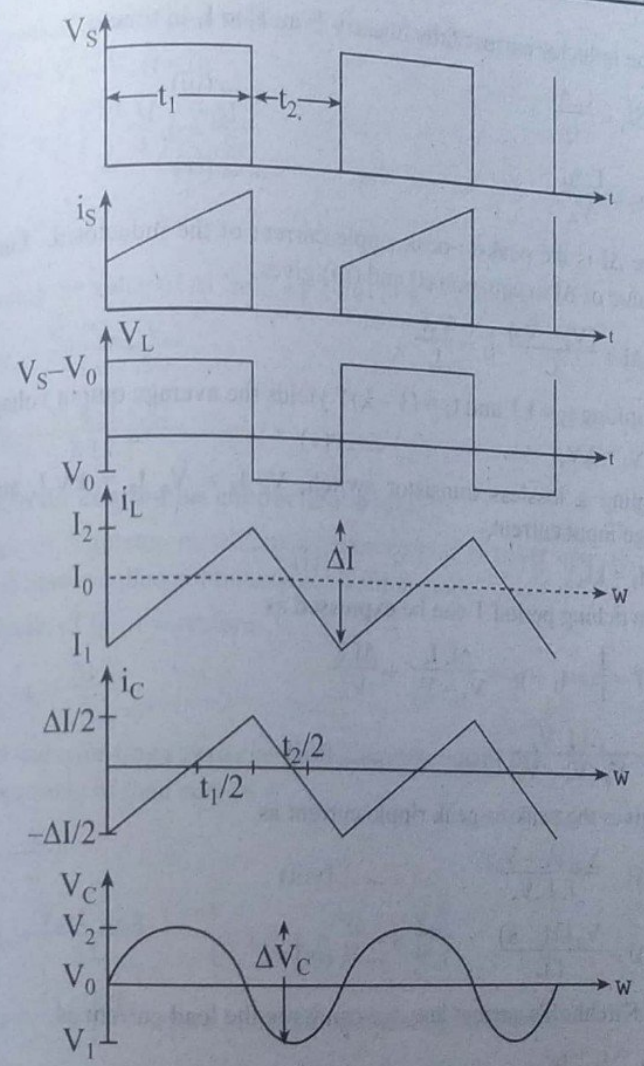


Fig: Waveforms of Buck Regulator

The voltage across the inductor, L is in general

$$V_L = L\frac{di}{dt}$$

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s - V_a = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1} \quad \text{..... (i)}$$

$$\therefore \quad t_1 = \frac{\Delta IL}{V_s - V_a} \quad \text{..... (ii)}$$

and the inductor current falls linearly from I_2 to I_1 in time t_2,

$$V_a = \frac{L.\Delta I}{t_2} \qquad \text{... ... (iii)}$$

$$\therefore \quad t_2 = \frac{L.\Delta I}{V_a} \qquad \text{... ... (iv)}$$

Where ΔI is the peak-to-peak ripple current of the inductor, L. Equating the value of ΔI in equation (i) and (iii) gives.

$$\Delta I = \frac{(V_s - V_a)}{L} t_1 = \frac{V_a t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1-k)T$ yields the average output voltage as,

$$V_a = kV_s \qquad \text{... ... (v)}$$

Assuming a lossless transistor switch, $V_s\ I_s = V_a\ I_a = kV_sI_a$ and the average input current,

$$I_s = kI_a \qquad \text{... ... (vi)}$$

The switching period T can be expressed as

$$T = \frac{I}{f} = t_1 + t_2 = \frac{\Delta I.\ L}{V_s - V_a} + \frac{\Delta I.L}{V_a}$$

$$= \frac{\Delta I.L\ V_s}{V_a(V_s - V_a)} \qquad \text{... ... (vii)}$$

And gives the peak-to-peak ripple current as,

$$\Delta I = \frac{V_a(V_s - V_a)}{f.\ L.V_s} \qquad \text{... ... (viii)}$$

$$\therefore \quad \Delta I = \frac{V_s\ k(I-k)}{f.L} \qquad \text{... ... (ix)}$$

Using Kirchhoff's current law, we can write the load current as,

$$i_L = i_c + i_a$$

If we assume that the load ripple current Δi_0, is very small and negligible, $\Delta i_L = \Delta i_c$. The average capacitor current, which flows for

$$\frac{t_1}{2} + \frac{t_2}{2} = \frac{T}{2} \text{ is}$$

$$I_c = \frac{\Delta I}{4}$$

The capacitor voltage is expressed as,

$$V_c = \frac{1}{C}\int i_c\, dt + V_c(t=0)$$

and the peak-to-peak ripple voltage of the capacitor is,

$$\Delta V_c = V_c - V_c(t=0)$$

$$= \frac{1}{C}\int_0^{T/2} \frac{\Delta I}{4}\, dt = \frac{\Delta I.T}{8c}$$

$$= \frac{\Delta I}{8fc} \qquad \text{... ... ... (x)}$$

Substituting the value of ΔI from eq^n (viii) in eq^n (x) yields,

$$\Delta V_c = \frac{V_a(V_s - V_a)}{8\ Lc\ f^2\ V_s}$$

$$\therefore \quad \Delta V_c = \frac{V_s\ k\ (I-k)}{8\ Lc\ f^2}$$

Condition for continuous conduction mode:

The state of regulator in which inductor current is never zero for any period of time is called continuous conduction mode.

From figure, of $I_L - t$ waveform

$$I_0 = I_L + \frac{\Delta I}{2}$$

If $I_L = 0$, inductor flows zero current for short period of time. So the minimum value of load current is

$$I_0 = \frac{\Delta I}{2}$$

$$\text{or,} \quad 2I_0 = \frac{V_s\ (I-k)t}{f.L} \qquad \left[\because I_0 = I_a = \frac{V_0}{R} = k\frac{V_s}{R}\right]$$

$$\therefore \quad L_c = \frac{(1-k)R}{2.f}$$ where L_C is critical value of inductance.

Similarly, for critical value of capacitance from figure,

$$V_0 = V_1 + \frac{\Delta V_C}{2}$$

If $V_1 = 0$, output voltage is zero so,

$$2.V_0 = \Delta V_C$$

$$\text{or,} \quad 2kV_s = V_s\frac{(1-k)k}{8LCf^2}$$

$$\therefore \quad C_c = \frac{(1-k)}{16Lf^2}$$

The buck regulator requires only transistor, is simple, and has high efficiency. The di/dt of the load current is limited by inductor L. However, the input current is discontinuous and a smoothing input filter is normally required. It provides one polarity of output voltage and unidirectional output current. It requires a protection circuit in case of possible short circuit of the diode path.

Alternative

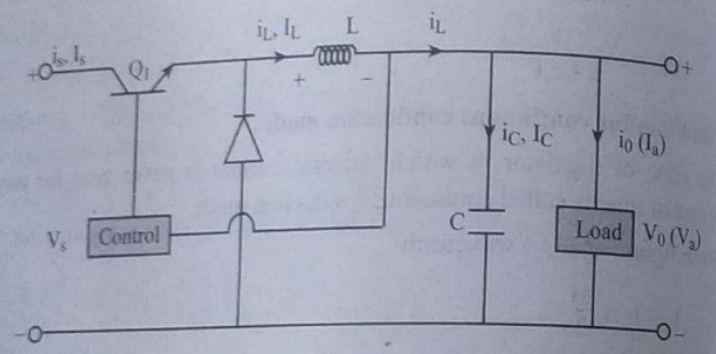


Fig: circuit diagram of Buck regulator

In this regulator, output average collage is less than i/p voltage V_s. When the transistor is on, value of is starts to increase from I_1 to maximum value I_2 and the applied voltage V_s is dropped across inductor and load.

If we suppose, if the current rises linearly and the voltage drop across transistor is negligible,

$$V_s = L\frac{di}{dt} + V_0$$

or, $V_s = L\frac{(I_2 - I_1)}{t_1} + V_0$ where t_1– on time of transistor

or, $V_s = L\frac{\Delta I}{t_1} + V_0$ where ΔI peak-to-peak inductor current or ripple current through inductor

$$\therefore \quad \Delta I = \frac{V_s - V_0}{L} \cdot t_1 \qquad \text{..... (i)}$$

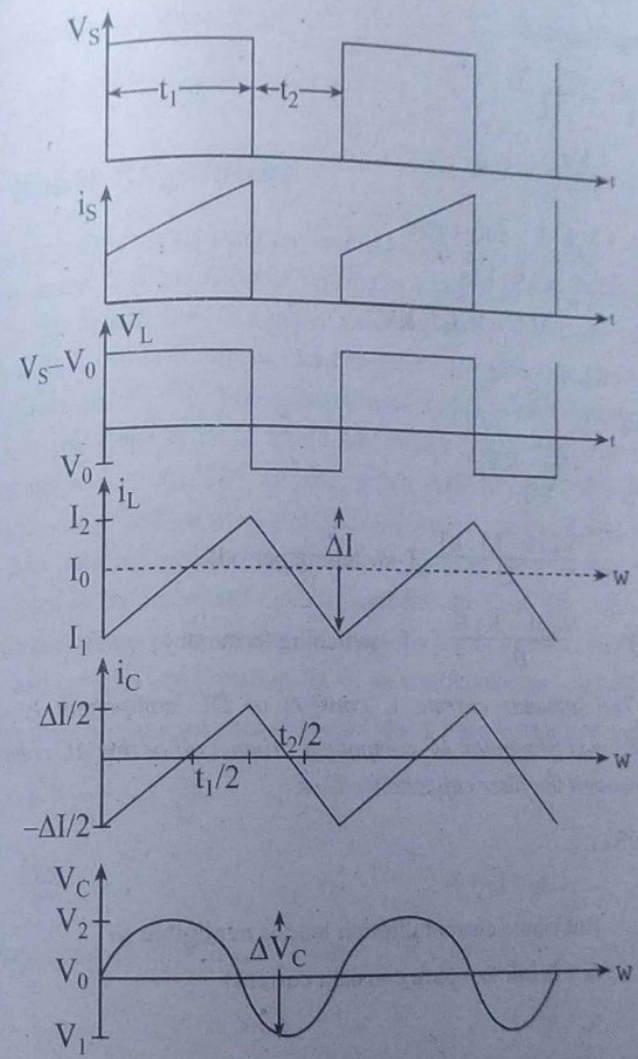


Fig: Waveforms of Buck Regulator

When the switch is off for t_2 time, $i_s = 0$ but inductor de-energized and current still flows through diode. If we suppose, inductor current falls linearly, up to I_1 as shown in figure, we

Have, $L\frac{di}{dt} = V_0$ (Voltage dropped across diode is negligible)

or, $L\frac{(I_2 - I_1)}{t_2} = V_0$

or, $\Delta I = \frac{V_0}{L} t_2 \qquad \text{..... (ii)}$

Equating (i) and (ii)

$$\frac{V_0 t_2}{L} = \frac{V_s - V_0}{L} t_1$$

or, $V_0 = \frac{V_s t_1}{t_1 + t_2} = V_s K$

$\therefore$ $V_0 = V_s K$ k – duty cycle

if circuit is loss less,

$P_i = P_0 \Rightarrow V_s I_s = V_0 I_0 = K V_s I_0$

$\therefore$ $I_s = K I_0$

From eq^n (i)

$$\Delta I = \frac{(V_S - KV_S)}{L} t_1$$

$$= \frac{V_S (1-k).kT}{L} \text{ (T-switching period)}$$

$$\therefore \Delta I = \frac{V_S (1-K) K}{fL} \quad [\because \text{f - switching frequency}]$$

Note: The inductor current i_L consists of DC component I_0 with a superimposed triangular AC component. Almost all of this AC component flows through the filter capacitance C as i_C.

We know,

$$i_L = i_C + i_0$$

But ripple current through load is negligible so

$i_0 = I_0$ (almost pure constant current)

$\therefore$ $i_L = i_C$

and $\Delta i_L = \Delta i_C$ (shown in figure i.e. wave form)

Now, Ripple voltage across capacitor is

$$\Delta V_C = \frac{\Delta Q}{C} = \frac{\text{Area of triangle in } i_C - t \text{ wave form}}{C}$$

$$= \frac{\frac{1}{2} \times \frac{\Delta I}{2} \times \frac{T}{2}}{C}$$

$$\therefore \Delta V_C = \frac{\Delta I T}{8C} = \frac{\Delta I}{8fC}$$

Substituting the value of ΔI,

$$\Delta V_C = \frac{V_S (1-K) K}{8LC f^2}$$

3.2 Boost Regulators

In a boost regulators, the output voltage is greater than the input voltage-hence the name "boost". A boost regulators using a power MOSFET is shown in fig a, and this is similar to a step-up chopper. The circuit operation can be divided into two modes. Mode 1 begins when transistor Q_1 is switched on at t = 0. The input current, which rises, flows through inductor L and transistor Q_1. Mode M_2 begins when transistor Q_1 is switched off at $t = t_1$. The current which was flowing through the transistor would now flow through L, C, load, and diode D_m. The inductor current falls until transistor Q_1 is turned on again in the next cycle. The energy stored in the inductor L is transferred to the load. The equivalent circuit for the modes of operation are shown in fig b. The waveforms for voltages and currents are shown in fig C, for continuous load current.

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1} \quad \text{... ... (i)}$$

$$\therefore t_1 = \frac{\Delta I . L}{V_s} \quad \text{... ... (ii)}$$

And inductor current falls linearly from I_2 to I_1 in time t_2.

$$V_a = V_s + L \frac{\Delta I}{t_2} \quad \text{... ... (iii)}$$

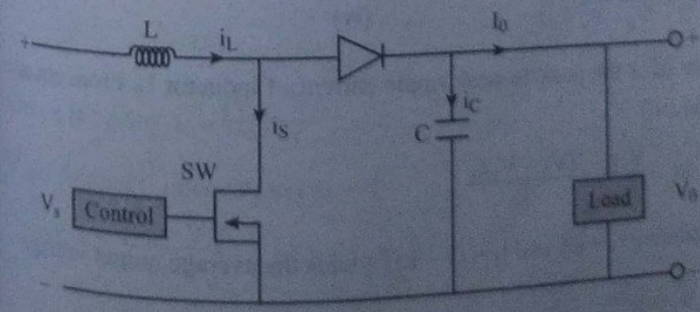


Fig: Boost regulator

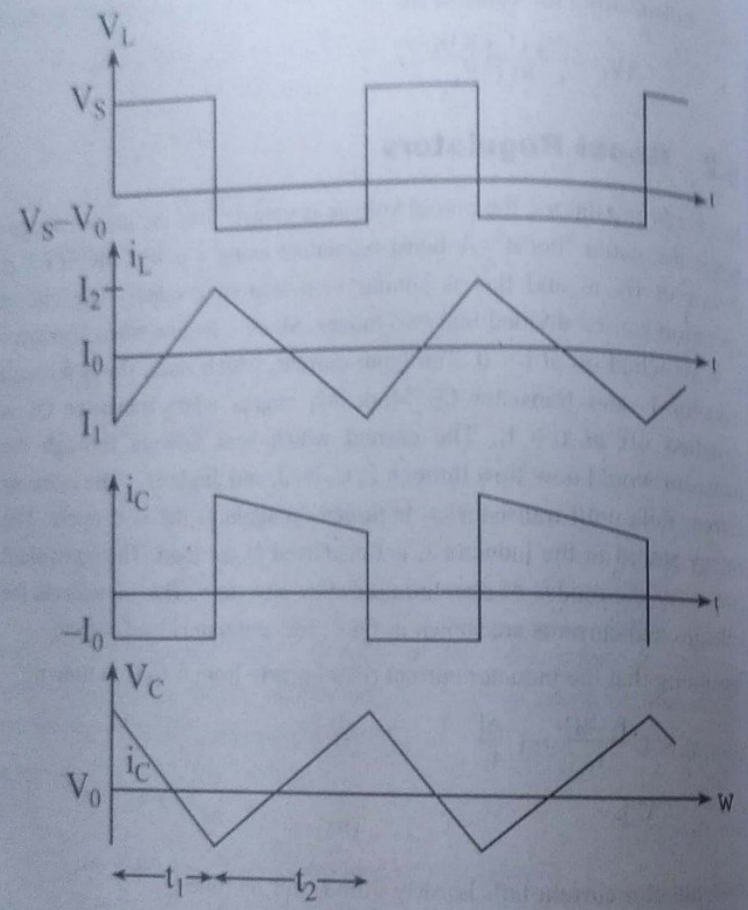


Fig: Waveform of boost regulation

$$\therefore \quad t_2 = \frac{\Delta I \cdot L}{V_a - V_s} \qquad \text{..... (iv)}$$

Where ΔI is the peak-to-peak ripple current of inductor L. From equation (i) and (iii)

$$\Delta I = \frac{V_s t_1}{L} = \frac{(V_a - V_s)t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)T$ yields the average output voltage

$$V_a = \frac{V_s}{1 - k} \qquad \text{..... (v)}$$

Assuming a lossless transistor,

$$I_s V_s = V_a I_a = \frac{V_s I}{(1 - k)}$$

And the average input current is,

$$I_s = \frac{I_a}{1 - k} \qquad \text{..... (vi)}$$

The switching period T can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta IL}{V_s} + \frac{\Delta IL}{V_a - V_s}$$

$$= \frac{\Delta I \cdot LV_a}{V_s (V_a - V_s)} \qquad \text{..... (vii)}$$

And this gives the peak to peak ripple current,

$$\Delta I = \frac{V_s (V_a - V_s)}{f LV_a} \qquad \text{..... (viii)}$$

$$\therefore \quad \Delta I = \frac{V_s \cdot k}{fL} \qquad \text{..... (ix)}$$

When the transistor is on the capacitor supplies the load current for $t = t_1$. The average capacitor current is $I_C = I_a$ and the peak-to-peak ripple voltage of the capacitor is.

$$\Delta V_C = V_C - V_C (t = 0)$$

$$= \frac{1}{C} \int_0^{t_1} Ic \, dt$$

$$= \frac{1}{C} \int_0^{t_1} Ia$$

$$= \frac{I_a t_1}{C} \qquad \text{..... (x)}$$

Equation (v) gives $t_1 = \frac{(V_a - V_s)}{V_a \cdot f}$

and substituting t_1 in equation (x)

$$\Delta V_C = I_a \frac{(V_a - V_s)}{V_a \cdot fc}$$

$$\therefore \quad \Delta V_C = \frac{I_a k}{f \cdot c}$$

For continuous conduction mode

$$I_0 = I_1 + \frac{\Delta I}{2}$$

When $I_1 = 0$

$$\therefore \quad I_0 = \frac{\Delta I}{2}$$

$$= \frac{V_s . k}{2fL}$$

$$\text{or,} \quad \frac{V_0}{R} = \frac{V_s . k}{2fL} \Rightarrow \frac{V_s}{(1-k)R} = \frac{V_s k}{2ft}$$

$$\therefore \quad L_C = \frac{K(1-k)R}{2f}$$

Where L_C = critical value of inductance.

For critical value of capacitor,

$$\frac{\Delta V_C}{2} = V_0$$

$$\text{or,} \quad \frac{I_0 k}{2fc} = \frac{V_s}{1-k}$$

$$\text{or,} \quad C_c = \frac{(1-k)k}{2f} \cdot \frac{I_0}{V_s}$$

$$= \frac{(1-k).k}{2f} \cdot \frac{I_0}{V_0(1-k)}$$

$$\therefore \quad C_c = \frac{k}{2fR}$$

The boost regulator can step up the output voltage without a transformer. Due to single transistor, it has high efficiency. The input current is continuous. However, a high peak current has to flow through the power transistor. The output voltage is very sensitive to changes in the duty cycle k and it might be difficult to stabilize the regulator. Since the transistor is in shunt with the load circuit, it might also be difficult to protect the output circuit in case of short circuit. The average output current is less than the average inductor current by a factor of (1 – k), and a much higher RMS current would flow through the filter capacitor, resulting in the use of a larger filter capacitor and a larger inductor than those of a buck regulator.

Alternative

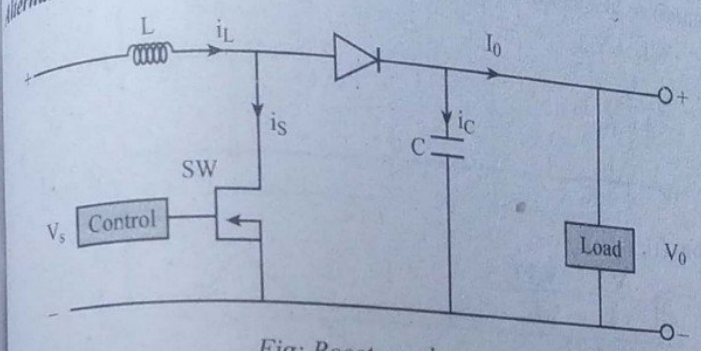


Fig: Boost regulator

In this type of regulation output voltage is greater than i/p voltage. When the control circuits on the switch, current starts to rise through inductor and transistor. If the current rises linearly, during time t_1 as shown in figure, the inductor is energized.

$$V_s = L\frac{di}{dt} = L\frac{I_2 - I_1}{t_1}$$

where I_1 – initial value and I_2 – final value of current

$$\therefore \quad \Delta I = \frac{V_s}{L} t_1 \qquad \text{..... (i)}$$

When the switch is off is will be zero and current starts to flow through diode and inductor is also de energized. So, the energy stored by inductor is transformed to load. Suppose inductor current falls linearly as shown in waveform.

$$V_s + L\frac{di}{dt} = V_0 \ (\because \text{ inductor reverses its polarity})$$

$$\text{or,} \quad \Delta I = \frac{V_0 - V_s}{L}, \quad t_2 - \text{off time}$$

From (i),

$$\frac{V_s}{L} t_1 = \frac{V_0 - V_s}{L} t_2$$

$$\text{or,} \quad V_0 = V_s \frac{(t_1 + t_2)}{t_2} = \frac{V_s}{(T - t_1)/T} = \frac{V_s}{1-K}$$

$$\therefore \quad V_0 = \frac{V_s}{1-K}$$

Assuming lossless circuit,

$$V_s I_s = V_0 I_0$$

$$= \frac{V_s}{1-K} I_0$$

$$\therefore \quad I_s = \frac{I_s}{1-K}$$

From (i),

$$\Delta I = \frac{V_s t_1}{L} = \frac{V_s kT}{L}$$

$$\therefore \quad VI = \frac{V_s K}{fL}$$

Ripple voltage of capacitor is $\Delta V_c = \frac{\text{Area of retangle}}{C}\left(\frac{\Delta Q}{C}\right) = \frac{I_0 \times t_1}{C}$

$$\therefore \quad \Delta V_c = \frac{I_0 kT}{C} = \frac{I_0 k}{fc} = \frac{I_s k}{fc}$$

For continuous conduction mode,

$$I_0 = I_1 + \frac{\Delta I}{2}$$

When $I_1 = 0$

$$I_0 = \frac{\Delta I}{2}$$

$$\text{or,} \quad I_0 = \frac{V_s K}{2fL} \Rightarrow \frac{V_0}{R} = \frac{V_s k}{2fL} \Rightarrow \frac{V_s}{(1-k)R} = \frac{V_s K}{2fL}$$

$$\therefore \quad L_c = \frac{k(1-k)R}{2f}$$, where hc-critical value of inductance.

Similarly, for critical value of capacitor,

$$\frac{\Delta V_c}{2} = V_0$$

$$\therefore \quad \frac{I_0 K}{2fc} = \frac{V_s}{1-k}$$

$$\therefore \quad C_c = \frac{(1-k)K}{2f} \cdot \frac{I_0}{V_s}$$

$$= \frac{(1-k)K}{2f} \cdot \frac{I_0}{V_0(1-k)}$$

$$\therefore \quad C_c = \frac{K}{2fR}$$

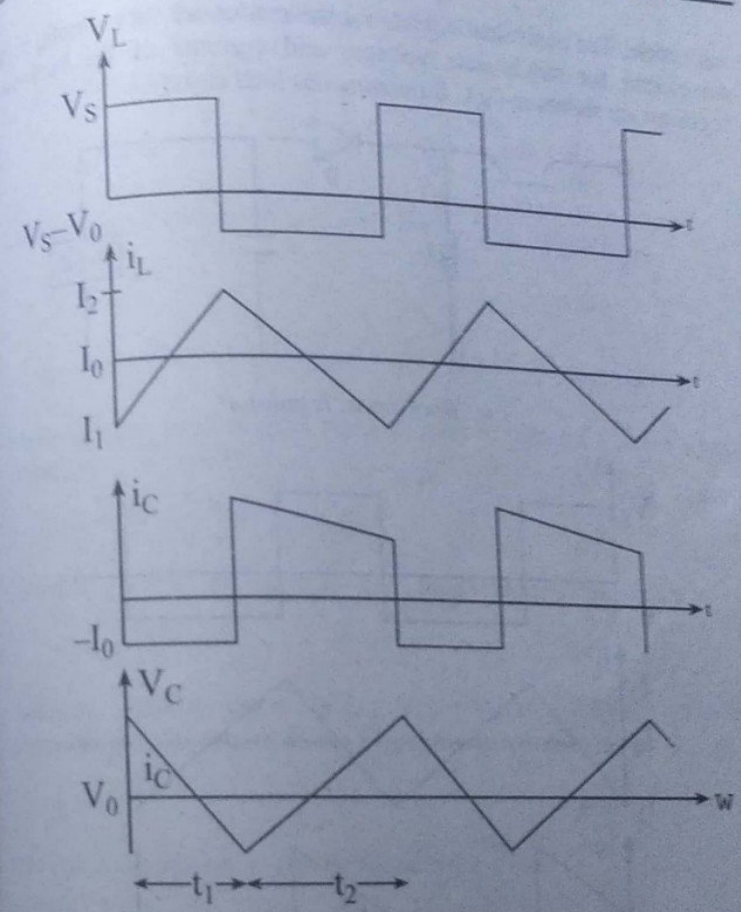


Fig: Waveform of boost regulation

8.3 Buck-Boost Regulators

A buck-boost regulator provides an output voltage which may be less than or greater than the input voltage-hence the name "buck-boost"; the output voltage polarity is opposite to that of the input voltage. This regulator is also known as an inverting or fly back regulator. The circuit arrangement of a buck-boost regulator is shown in fig a.

The circuit operation can be divided into two modes. During mode 1, transistor Q_1 is turned on and diode D_m is reversed biased. The input current, which rises, flows through inductor L and transistor Q_1. During mode 2, transistor Q_1 is switched off and the current which was flowing through inductor L_1 would now flow through L, C, D_m, and the load. The energy stored in inductor L would be transferred to the load and the inductor current would fall until transistor Q_1 is switched on again in the

next cycle. The equivalent circuits for the modes are shown in fig b. The waveforms for steady-state voltages and currents of the buck-boost regulator are shown in fig C for continuous load current.

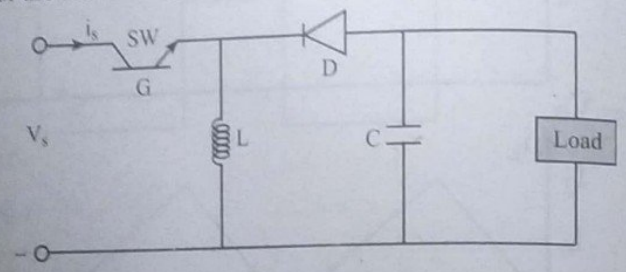


Fig: Buck-boost regulator

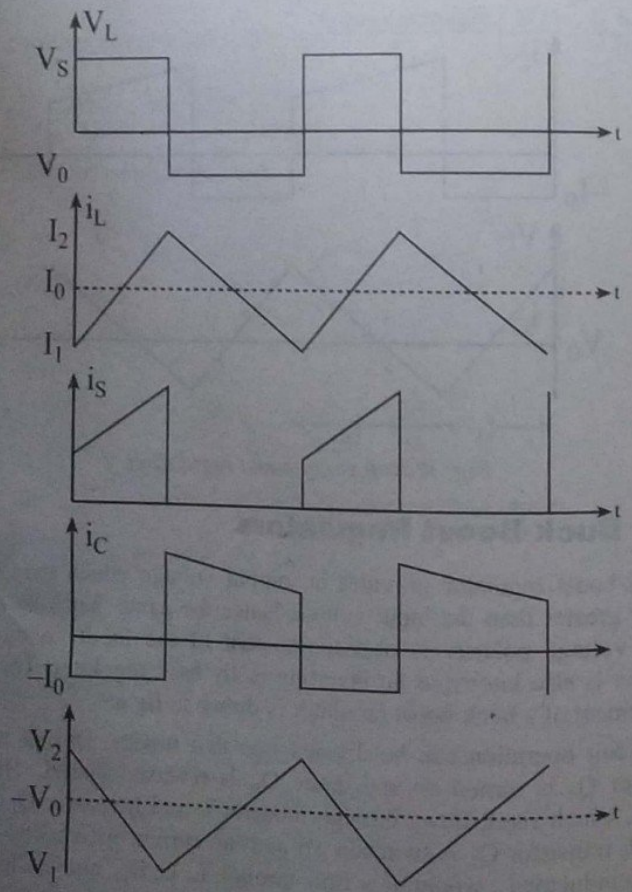


Fig: Waveforms of buck-boost regulator

Assuming that the inductor current rises linearly from I_1 to I_2 in time t_1,

$$V_s = L\frac{I_1 - I_1}{t_1} = L\frac{\Delta I}{t_1} \quad \text{..... (i)}$$

$$\therefore t_1 = \frac{\Delta I \,.\, L}{V_s} \quad \text{..... (ii)}$$

And the inductor current falls in early from I_2 to I_1 in time t_2,

$$V_a = -L\frac{\Delta I}{t_2} \quad \text{..... (iii)}$$

$$\therefore \quad t_2 = \frac{-\Delta I \,.\, L}{V_a} \quad \text{..... (iv)}$$

Where ΔI is the peak-to-peak ripple current of inductor L. from equation (i) and (iii)

$$\Delta I = \frac{V_s\, t_1}{L} = \frac{-V_a\, t_2}{L}$$

Substituting $t_1 = kT$ and $t_2 = (1 - k)\,T$, the average output voltage is

$$V_a = \frac{-V_s\, k}{1 - k} \quad \text{..... (v)}$$

Assuming a lossless circuit, $V_sI_s = V_aI_a = V_sI_ak/(1 - k)$ and the average input current, I_s, is related to the average output current, I_a, by

$$I_s = \frac{I_a \,.\, k}{1 - k} \quad \text{..... (vi)}$$

The switching period, T, can be found from

$$T = \frac{1}{f} = t_1 + t_2 = \frac{\Delta I.\, L}{V_s} - \frac{\Delta I.\, L}{V_a}$$

$$= \Delta IL\,\frac{(V_a - V_s)}{V_s \,.\, V_a} \quad \text{..... (vii)}$$

And this gives the peak-to peak ripple current,

$$\Delta I = \frac{V_s\, V_a}{fL\,(V_a - V_s)} \quad \text{..... (viii)}$$

$$\therefore \quad \Delta I = \frac{V_S\, k}{fL} \quad \text{..... (ix)}$$

When transistor Q_1 is on, the filter capacitor supplies the load current for $t = t_1$. The average discharging current of the capacitor is $I_c = I_a$ and the peak-to-peak ripple voltage of the capacitor is

$$\Delta V_c = \frac{1}{C}\int_0^{t_1} I_c\, dt = \frac{1}{C}\int_0^{t_1} I_a\, dt = \frac{I_a\, t_1}{C} \quad \text{..... (x)}$$

Equation (v) gives $t_1 = V_a I\,[(V_a - V_s)f]$ and equation (x) becomes

$$\Delta V_c = \frac{I_a V_a}{(V_a - V_s)fC}$$

$$\therefore \quad \Delta V_c = \frac{I_a k}{fC}$$

Condition for continuous inductor current and capacitor voltage.

from figure,

$$I_0 = I_1 + \frac{\Delta I}{2}$$

$$\therefore \quad I_0 = \frac{\Delta I}{2} \text{ for continuous conduction (i.e. } I_{min} = I_1 = 0)$$

$$\therefore \quad \frac{V_0}{R} = \frac{\Delta I}{2}$$

$$\text{or,} \quad \frac{k V_s}{(1-k)R} = \frac{V_s k}{2\,fL}$$

$$\therefore \quad L_c = \frac{(1-k)R}{2f} \text{ where } L_c = \text{critical value of inductance}$$

Similarly, for critical capacitance,

$$V_0 = V_1 + \frac{\Delta V_c}{2}$$

$$\therefore \quad V_0 = \frac{\Delta V_c}{2} \text{ for continuous capacitor voltage i.e. } V_1 = 0$$

$$\text{or,} \quad I_0 R = \frac{I_0 k}{2fc}$$

$$\therefore \quad C_c = \frac{k}{2fR}$$

A buck-boost regulator provides output voltage polarity reversal without a transformer. It has high efficiency. Under a fault condition of the transistor, the di/dt of the fault current would be V_s/L and is limited by the inductor L. Output short-circuit protection would be easy to implement. However, the input current is discontinuous and a high peak current flows through transistor Q_1.

Alternative

It gives output voltage that may be less than or greater than the i/p voltage. In this type of regulator, output voltage is opposite to that of input voltage so also known as inverting regulator.

When the switch is ON, the diode is reverse biased and the current flows through inductor L which starts rising from the value of I_1 and reaches its maximum value I_2. We consider the current rises linearly, and t_1 is period of switch on.

$$\text{So,} \quad V_s = L\frac{di}{dt} = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1}$$

ΔI-peak-to-peak inductor current or ripple current

$$\therefore \Delta I = \frac{V_s}{L} t_1 \quad \ldots\ldots \text{(i)}$$

Now, if switch is off for t_2 period of time, the diode is forward biased with reverse polarity of inductor and the energy stored by inductor is now transferred to the load. So the inductor current falls until the switch is ON again.

$$\therefore \quad V_0 = -L\frac{di}{dt} = -L\frac{(I_2 - I_1)}{t_2} = -L\frac{\Delta I}{t_2}$$

$$\therefore \quad \Delta I = \frac{-V_0}{L} t_2$$

From (i),

$$\frac{V_s}{L} t_1 = -\frac{V_0}{L} t_2$$

$$\text{or,} \quad V_0 = -V_s\frac{t_1}{t_2} = -V_s\frac{t_1}{T - t_1} = \frac{-V_s KT}{T - KT} = \frac{-V_s K}{1 - K}$$

$$\therefore \quad V_0 = \frac{-V_s K}{1 - K}$$

Output voltage is also the average voltage so,

$$V_a = \frac{-V_s K}{1 - K}$$

If the circuit is loss less, $V_s I_s = -V_0 I_0 = \frac{V_s K}{1 - K} I_0$

$$\therefore I_0 = \frac{I_s(1 - K)}{K}$$

From equation (i),

$$\Delta I = \frac{V_s}{L} KT = \frac{V_s K}{fL}$$

The inductor current i_c consists of de component I_0 (I_a) with super imposed triangular ac component almost all of component flows through

the filter capacitor cosi$_c$. Due to this ripple current, there will be ripple voltage across capacitor so, ripple voltage $\Delta V_c = \frac{\Delta Q}{C}$

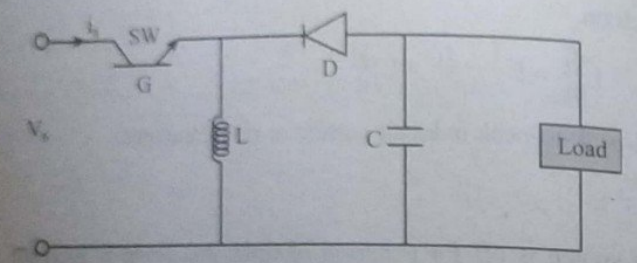


Fig: Buck-boost regulator

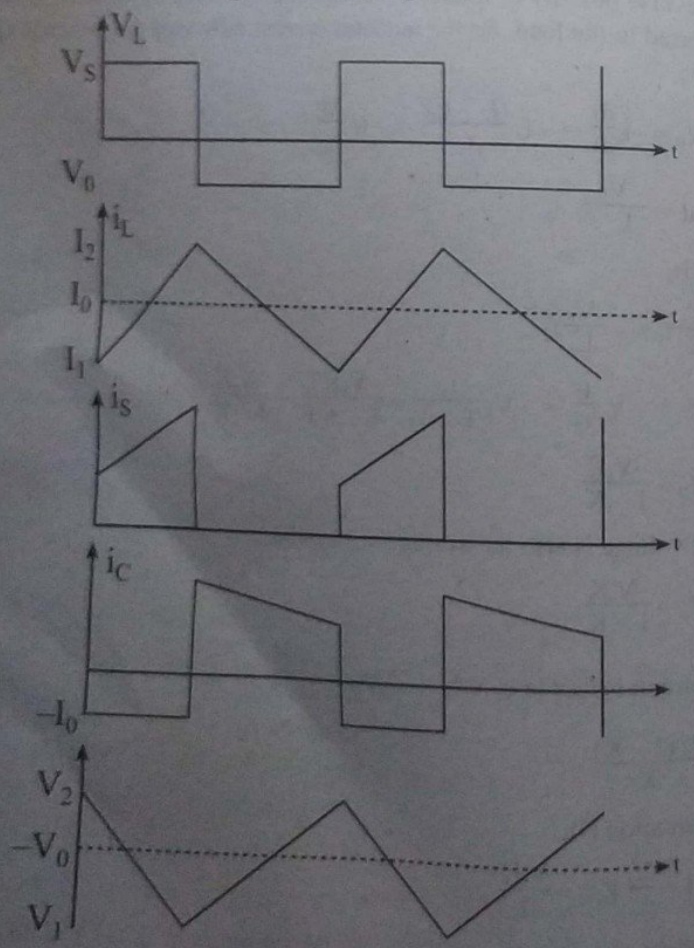


Fig: Waveforms of buck-boost regulator

$$= \frac{I_0 \times t_1}{C} \text{ (area of rectangle in waveform)}$$

$$= \frac{I_0 \times KT}{C}$$

$$\therefore \Delta V_c = \frac{I_0 K}{fc}$$

Since $I_0 = I_a$

$$\Delta V_c \frac{I_a K}{fc}$$

Condition for continuous inductor current and capacitor voltage (continuous conduction mode)

From figure,

$$\frac{\Delta I}{2} + I_1 = I_0$$

$$\therefore I_0 = \frac{\Delta I}{2} \text{ for continuous conduction (i .e. } I_{min} = I_1 = 0)$$

$$\therefore \frac{V_0}{R} = \frac{\Delta I}{2}$$

$$\text{or, } \frac{KV_s}{(1-K)R} = \frac{V_s K}{2fL}$$

$$\therefore L_c = \frac{(1-K)R}{2f} \quad L_c \text{ – critical value of inductance}$$

Similarly for critical capacitance,

$$V_0 = V_1 + \frac{\Delta V_c}{2}$$

$$\therefore V_0 = \frac{\Delta V_c}{2} \text{ for continuous capacitor ie. } V_1 = 0$$

$$\text{or, } I_0 R = \frac{I_0 K}{2fc}$$

$$\therefore C_c = \frac{K}{2fR}$$

8.4 Filtering Considerations

A filter is an AC circuit that separates some frequencies from others within mixed-frequency signals and Filtering is the act of supplying only desired amount of frequency within the circuit.

Filtering consideration on in a switching power supply should be done because of following:

- to prevent electromagnetic interference, generated by the switching source from reaching the power line and affecting other equipment.
- to prevent high frequency voltage on the power line from passing through the output of the power supply.

8.5 Control Circuits, IC Switched

(a) **Control circuit:** A control circuit is a special type of circuit used to control the operation of a completely separate power circuit. A common control circuit example is the thermostat to the air conditioner in a house. The thermostat is part of a low-voltage control circuit that controls a relay that actually energizes and de-energizes the power circuit to the air conditioning compressor. Control circuits can be divided into two major types:

- three-wire control circuits
- four-wire control circuits.

(b) **Switching IC:** One of the ways to reduce supply current of the running applications is to cut off the power supply for unnecessary circuits according to the operating state. By inserting a switch IC, it becomes able to easily turn ON/OFF and even protect the power supply line. Switch ICs do not have voltage control functions like LDO regulators or DC/DC converters, but when a large current flows, they are more efficient in the perspectives of voltage drop and power loss.

Also, they are equipped with protections against such as over-current and over-temperature, which discreet FETs cannot have. Therefore, multi-functional protection circuits featuring small mounting area can be constructed with switch ICs

We provide a line up of switch ICs featuring low ON resistance and various protection functions. Choose the best switch IC that matches the usage. Some of the switch IC are:

(i) USB switch IC
(ii) Rectifier switch IC
(iii) Load switch IC
(iv) Battery line switch IC
(v) Intelligent power switch IC
(vi) OVP which IC/external power switch IC.

Numerical Problems

For the Buck regulator if input voltage $V_s = 12$ V the required average output voltage is 6 V at R = 450Ω and peak to peak output ripple voltage is 20m V_1 switching frequency is 20 KH_z and peak to peak ripple current of inductor is 0.8A find.

(a) Duty cycle
(b) Filter capacitance C.
(c) Filter inductance L.

Solution:

(a) Duty cycle $k = \frac{V_0}{V_s} = \frac{6}{12} = 0.5$

(b) Filter inductance, $L = \frac{V_s(1-k)k}{\Delta I.f}$

$$= \frac{12(1-0.5)\ 0.5\text{mH}}{0.8 \times 20}$$

$$= 0.1875 \text{ mH}$$

(c) Filter capacitance, $C = \frac{\Delta I}{\Delta V_c \times 8 \times f}$

$$= \frac{0.8}{20 \times 10^{-3} \times 8 \times 20 \times 10^{-3}}$$

$$= 250\ \mu f$$

A boost regulator has input voltage of $V_s = 5V$. The average output voltage $V_a = 15$ V and average load current $I_a = 0.5\ A_1$ the switching frequency is 25 kH_z. If L = 150mH and c = 220 μf. Determine.

(a) Duty cycle
(b) The peak current of inductor I_2.
(c) Ripple voltage of filter capacitor
(e) Critical value of L and C

Solution:

(a) $V_a = \frac{V_s}{1-k}$

$$15 = \frac{5}{1-k}$$

$$\therefore \quad k = 0.66$$

(b) $\Delta I = \frac{V_s k}{fL} = \frac{5 \times 0.66}{25 \times 10^3 \times 150 \times 10^{-3}}$

$= 0.88$ mA

We know,

$I_0 = I_1 + \frac{\Delta I}{2}$

or, $0.5 = I_1 + \frac{0.88 \times 10^{-3}}{2}$

$\therefore I_1 = 0.49950$ A

Also,

$I_2 = I_1 + \Delta I = 0.49956 + 0.00088$

$= 0.50044$A

(c) $\Delta V_c = \frac{I_0 k}{fc} = \frac{0.5 \times 0.66}{25 \times 10^3 \times 220 \times 10^{-6}}$

$= 0.06$ V

(d) $L_c = \frac{k(1-k)R}{2f}$

$= \frac{0.66(1-2/3)}{2 \times 25 \times 10^3} \frac{15}{0.5}$

$= 0.133$ mH.

$C_c = \frac{k}{2fR} = \frac{2/3}{2 \times 25 \times 10^3} \times \frac{0.5}{15}$

$= 0.4444$ µf

3. A buck regulator has an input voltage of $V_s = 14V$ the required output voltage is $V_a = 8V$ at $R = 500\Omega$ and peak to peak output voltage ripple is 15mV the switching frequency 15 limited to 20 kHz. If peak to peak ripple current of the inductor is limited to 0.8 mA. Determine.

(a) Duty cycle

(b) Filter inductance

(c) Filter capacitance

(d) Critical value of L 86.

Solution:

(a) Duty cycle $k = \frac{V_0}{V_s}$

$= \frac{8}{14} = 0.571$

(b) Filter inductance, $L = \frac{V_s(1-k).k}{f.\Delta I}$

$= \frac{14 \times (1-0.57) \times 0.571}{20 \times 10^3 \times 0.8}$

$= 0.214 \times 10^{-3}$H

$= 0.214$ MH.

(c) Filter capacitance, $C = \frac{\Delta I}{8f \times \Delta V_c}$

$= \frac{0.8}{8 \times 20 \times 10^3 \times 15 \times 10^{-3}}$

$= 333.33$ µf.

(d) Critical inductance, $L_c = \frac{(1-k)R}{2f}$

$= \frac{(1-0.571)\,500}{2 \times 20 \times 10^3}$

$= 5.36$ MH.

Critical capacitance, $C_c = \frac{(1-k)}{16Lf^2}$

$= \frac{(1-0.571)}{16 \times 0.214 \times 10^{-3} \times (20 \times 10^3)^2}$

$= 0.3132$ µf.

4. The buck-boost regulator has input voltage $V_s = 15$ V, duty cycle $k = 40\%$ and switching frequency of 20 kHz. The inductance L = 120 µH, filter capacitance, C = 200 µf and average load current $I_a = 1.25$A. Determine.

(a) The average output voltage

(b) Peak to peak output ripple voltage

(c) Peak to peak output ripple current

Solution:

(a) $V_a = \frac{-V_s . k}{1-k}$

$= \frac{-15 \times 0.4}{1-0.4}$

$= -10$ V

(ii) $\Delta I = \frac{V_s . k}{f. L} = \frac{15 \times 0.4}{20 \times 10^3 \times 120 \times 10^{-6}}$

$= 2.5$ A

(c) $\Delta V = \frac{I_0 k}{fc} = \frac{1.25 \times 0.4}{20 \times 10^3 \times 200 \times 10^{-6}}$

$= 0.125$ V

5. **Given, Filter capacitance (C) = 470 μf**

To find,

Peak voltage ripple in the output of the (ΔV_c)

Solution:

We have,

$$\Delta V_c = \frac{\Delta I}{8\ fc} = \frac{2.304}{8 \times 20 \times 10^3 \times 470 \times 10^{-6}}$$

$= 30.63$ MV.

6. **Given, Buck converter**

Load voltage (V_0) = 5 V

Resistance (R_L) = 0.05Ω

Source voltage (V_s) = 24 V

Internal resistance of source voltage = 0.1Ω

To find,

(a) Inductor current

(b) Terminal voltage

(c) Duty cycle

Solution:

We have,

(a) Inductor current $i_L = \frac{vs}{R_L + R_i}$

$= \frac{24\ V}{(0.05+1)} = 160$ A.

(b) Terminal voltage $(V_T) = V_s - i_L \times R_i$

$= 24\ V - 160 \times 0.1 = 8$ V.

(c) Duty cycle (k) $= \frac{V_0}{V_T} = \frac{5}{8} = 0.625$

Given, Buck regulator,

Input voltage (V_s) = 12 V

Output voltage (V_0) = 5 V at R = 400Ω

Peak-peak output ripple voltage ΔV_c = 15 MV.

Switching frequency (f_c) = 30kHz

Peak-peak ripple current (ΔI) = 0.5 Amp

To find,

(a) Filter inductance

(b) Filter capacitance

(c) Critical value of L and C

Solution:

(a) Filter inductance,

$$L = \frac{V_a(V_s - V_a)}{\Delta I.\ fs - V_s}$$

$$= \frac{5(12-5)}{0.5 \times 30 \times 10^3 \times 12}$$

$= 0.1944$ MH.

(b) Filter capacitance,

We have,

$$\Delta V_c = \frac{\Delta I}{8fc}$$

$$\therefore \quad C = \frac{0.5}{8\ (30 \times 10^3)\ 15 \times 10^{-3}}$$

$= 138.88$ μf.

(c) Critical value of L and C.

$$L_c = \frac{(1-k)R}{2\,fs} = \frac{(1-0.416)\,400}{2 \times 10^3 \times 30}$$

$$= 3.893 \text{ MH.}$$

$$C_c = \frac{1-k}{16L\,fs^2} = 10.52\ \mu f.$$

8. Given,

$V_s = 5$ V	$L = 250\ \mu H$	$R_L = 20\Omega$
$C = 470\ \mu f$	$F_9 = 20$ kHz	$K = 0.4$

To find,

(a) ΔI, V_0

(b) Sketch the inductor current i_L

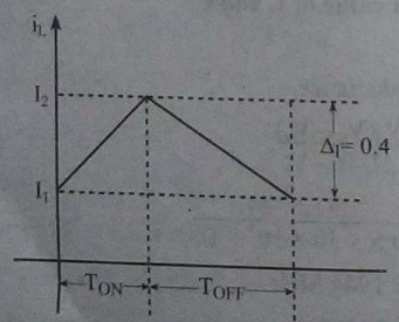
(c) Determine the peak-peak voltage ripple in the output

Solution:

(a) $$\Delta I = \frac{V_s.k}{f.L} = \frac{5\text{ V} \times 0.4}{20 \times 10^3 \times 250 \times 10^{-6}} = 0.4 \text{ Amp}$$

$$V_0 = \frac{V_s}{1-k} = \frac{5\text{ V}}{1-0.4} = 8.33 \text{ V}$$

(b) Sketch the inductor current i_L



(c) Peak-peak voltage ripple

$$\Delta V_c = \frac{I_a \cdot k}{fc}$$

$$= \frac{0.4165 \times 0.4}{20 \times 10^3 \times 470 \times 10^{-6}F}$$

$$= 0.0177 \text{ V}$$

$$I_a = \frac{V_\alpha}{R_c}$$

$$= \frac{8.33\text{ V}}{20\Omega}$$

$$= 0.4165$$

Given, Buck-boost regulator in CCM mode

$V_s = 12$ V

$L = 250\ \mu H$

$R_L = 20\Omega$

$C = 470\ \mu f$

$F_S = 20$ kHz

$k = 0.7$

To find,

(a) ΔI, V_0

(b) Sketch the inductor current i_L.

(c) Determine peak-peak voltage ripple in the o/p.

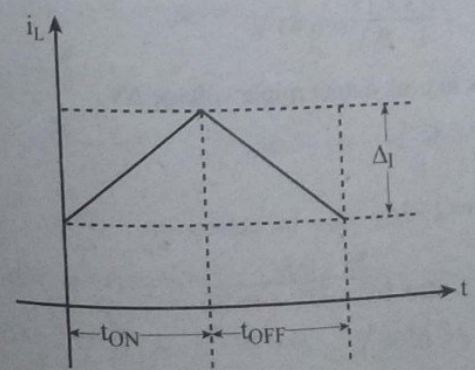
Solution:

(a) $$\Delta I = \frac{V_S\,k}{f\,L} = \frac{12 \times 0.7}{20 \times 10^3 \times 250 \times 10^{-6}}$$

$$= 1.68 \text{ Amp}$$

$$V_0 = \frac{V_S \cdot k}{1-k} = \frac{12 \times 0.7}{1-0.7} = 28 \text{ V so functioning boost.}$$

(b) Sketching inductor current,



(c) Peak-peak voltage ripple in the o/p.

$$\Delta V_C = \frac{I_a \times k}{f.c}$$

$$= \frac{1.4 \times 0.7}{20 \times 10^3 \times 470 \times 10^{-6}}$$

$$= 0.104 \text{ V}$$

$$I_a = \frac{V_0}{R_L} = \frac{28}{20} = 1.4 \text{ A}$$

10. Given, Buct-boost regulator,

Input voltage (V_S) = 15 V

Duty cycle (K) = 0.3

Switching frequency (f_s) = 30 kHz

Inductance (L) = 140 μH

Filter capacitance (C) = 220 μF

Average load current (I_a) = 1.25 Amp

To find,

(a) Average output voltage.

(b) Peak to peak output ripple voltage.

(c) Peak to peak output current of inductor.

Solution:

(a) Average output voltage V_a

$$V_a = V_0 = \frac{k V_S}{1-k}$$

$$= \frac{0.3 \times 15}{1-0.3} = 6.43 \text{ V}$$

(b) Peak to peak output ripple voltage ΔV_0

$$\Delta V_C = \frac{I_a . k}{fc}$$

$$I_a = 1.25$$

$$= \frac{1.25 \times 0.3}{30 \times 10^3 \times 220 \times 10^{-6}}$$

$$= 0.0568 \text{ V}$$

(c) Peak to peak output current of inductor

$$\Delta I = \frac{V_0 . k}{f . L}$$

$$= \frac{15 \times 0.3}{30 \times 10^3 \times 140 \times 10^{-6}}$$

$$= 0.1071 \text{ Amp.}$$

Old Questions with Solution

1. Explain the operation of Buck regulator with necessary diagram and derivation.

[2078 Kartik, 2073 Shrawan, 2071 Chaitra, 2069 Ashad]

Solution:

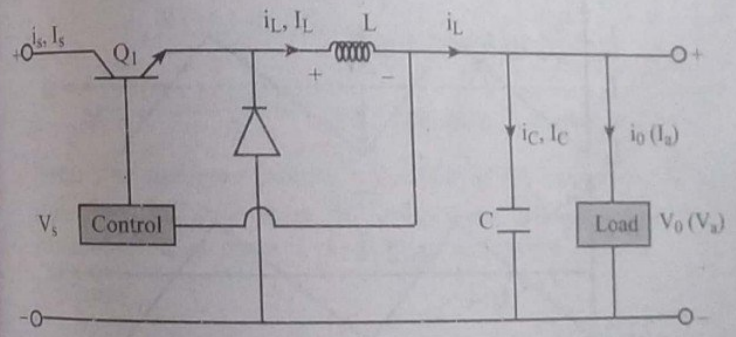


Fig: circuit diagram of Buck regulator

In this regulator, output average collage is less than i/p voltage V_s. When the transistor is on, value of is starts to increase from I_1 to maximum value I_2 and the applied voltage V_s is dropped across inductor and load.

If we suppose, if the current rises linearly and the voltage drop across transistor is negligible,

$$V_s = L\frac{di}{dt} + V_0$$

or, $V_s = L\frac{(I_2 - I_1)}{t_1} + V_0$ where t_1– on time of transistor

or, $V_s = L\frac{\Delta I}{t_1} + V_0$ where ΔI peak-to-peak inductor current or ripple current through inductor

$$\therefore \quad \Delta I = \frac{V_s - V_0}{L} . t_1 \quad \text{..... (i)}$$

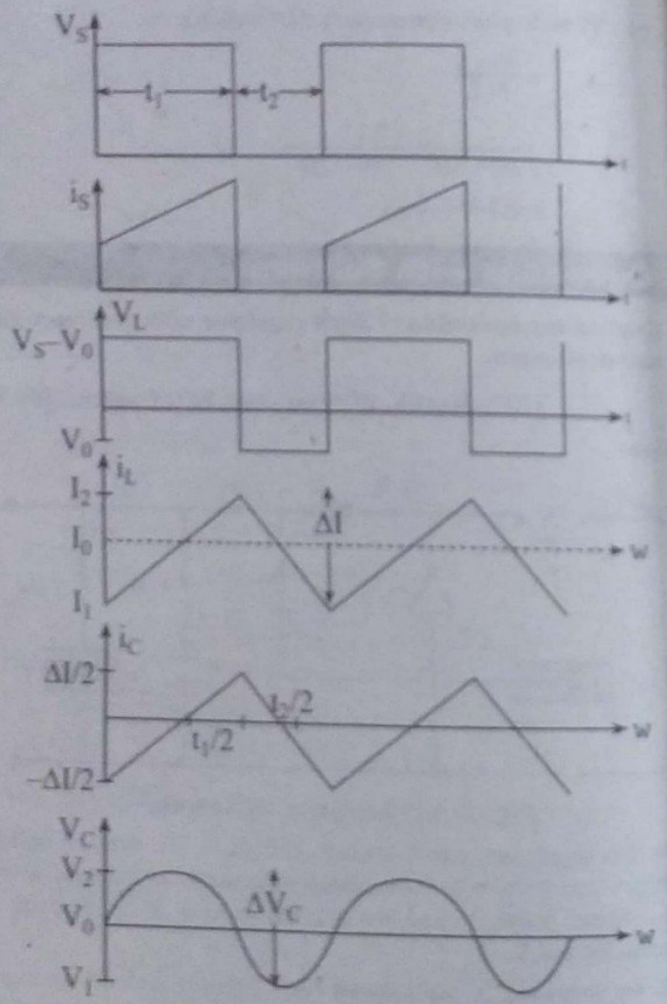


Fig: Waveforms of Buck Regulator

When the switch is off for t_2 time, $i_s = 0$ but inductor de-energized and current still flows through diode. If we suppose, inductor current falls linearly, up to I_1 as shown in figure, we

We have, $L\frac{di}{dt} = V_0$ (Voltage dropped across diode is negligible)

or, $L\frac{(I_2 - I_1)}{t_2} = V_0$

or, $\Delta I = \frac{V_0}{L} t_2$ ——— (ii)

Equating (i) and (ii)

$$\frac{V_0 t_2}{L} = \frac{V_s - V_0}{L} t_1$$

or, $V_0 = \frac{V_s t_1}{t_1 + t_2} = V_s K$

$\therefore$ $V_0 = V_s K$ k – duty cycle

If circuit is loss less,

$P_i = P_0 \Rightarrow V_s I_s = V_0 I_0 = K V_s I_0$

$\therefore$ $I_s = K I_0$

From eq^n (i)

$$\Delta I = \frac{(V_S - KV_S)}{L} t_1$$

$$= \frac{V_S (1 - k) . kT}{L} \text{ (T-switching period)}$$

$\therefore$ $\Delta I = \frac{V_S (1 - K) K}{fL}$ [$\because$ f - switching frequency]

Note: The inductor current i_L consists of DC component I_0 with a superimposed triangular AC component. Almost all of this AC component flows through the filter capacitance C as i_C

We know,

$$i_L = i_C + i_0$$

But ripple current through load is negligible so

$i_0 = I_0$ (almost pure constant current)

$\therefore$ $i_L = i_C$

and $\Delta I_L = \Delta I_C$ (shown in figure i.e. wave form)

Now, Ripple voltage across capacitor is

$$\Delta V_C = \frac{\Delta Q}{C} = \frac{\text{Area of triangle in } i_C - t \text{ wave form}}{C}$$

$$= \frac{\frac{1}{2} \times \frac{\Delta I}{2} \times \frac{T}{2}}{C}$$

$\therefore$ $\Delta V_C = \frac{\Delta I T}{8C} = \frac{\Delta I}{8fC}$

Substituting the value of ΔI,

$$\Delta V_C = \frac{V_S (1 - K) K}{8LC f^2}$$

2. Explain the working principle of Boost regular with necessary circuit, wave from is and expressions.

[2076 Ashwin, 2073 Chaitra, 2070 Ashad, 2068 Chaitra]

Solution:

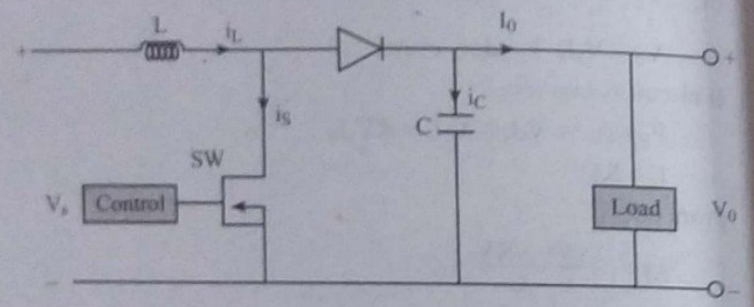


Fig: Boost regulator

In this type of regulation output voltage is greater than i/p voltage. When the control circuits on the switch, current starts to rise through inductor and transistor. If the current rises linearly, during time t_1 as shown in figure, the inductor is energized.

$$V_s = L\frac{di}{dt} = L\frac{I_2 - I_1}{t_1}$$

where I_1 – initial value and I_2 – final value of current

$$\therefore \quad \Delta I = \frac{V_s}{L} t_1 \qquad \ldots\ldots (i)$$

When the switch is off is will be zero and current starts to flow through diode and inductor is also de energized. So, the energy stored by inductor is transformed to load. Suppose inductor current falls linearly as shown in waveform.

$$V_s + L\frac{di}{dt} = V_0 \quad (\because \text{inductor reverses its polarity})$$

$$\text{or,} \quad \Delta I = \frac{V_0 - V_s}{L}, \quad t_2 - \text{off time}$$

From (i),

$$\frac{V_s}{L} t_1 = \frac{V_0 - V_s}{L} t_2$$

$$\text{or,} \quad V_0 = V_s \frac{(t_1 + t_2)}{t_2} = \frac{V_s}{(T - t_1)/T} = \frac{V_s}{1 - K}$$

$$\therefore \quad V_0 = \frac{V_s}{1 - K}$$

Assuming lossless circuit,

$$V_s I_s = V_0 I_0$$

$$= \frac{V_s}{1 - K} I_0$$

$$\therefore \quad I_s = \frac{I_s}{1 - K}$$

From (i),

$$\Delta I = \frac{V_s t_1}{L} = \frac{V_s kT}{L}$$

$$\therefore \quad VI = \frac{V_s K}{fL}$$

Ripple voltage of capacitor is $\Delta V_c = \frac{\text{Area of retangle}}{C}\left(\frac{\Delta Q}{C}\right)$

$$= \frac{I_0 \times t_1}{C}$$

$$\therefore \quad \Delta V_c = \frac{I_0 kT}{C} = \frac{I_0 k}{fc} = \frac{I_s k}{fc}$$

For continuous conduction mode,

$$I_0 = I_1 + \frac{\Delta I}{2}$$

When $I_1 = 0$

$$I_0 = \frac{\Delta I}{2}$$

$$\text{or,} \quad I_0 = \frac{V_s K}{2fL} \Rightarrow \frac{V_0}{R} = \frac{V_s k}{2fL} \Rightarrow \frac{V_s}{(1-k)R} = \frac{V_s K}{2fL}$$

$$\therefore \quad L_c = \frac{k(1-k)R}{2f}$$, where hc-critical value of inductance.

Similarly, for critical value of capacitor,

$$\frac{\Delta V_s}{2} = V_0$$

$$\therefore \quad \frac{I_s K}{2fc} = \frac{V_s}{1-k}$$

$$\therefore \quad C_c = \frac{(1-k)K}{2f} \cdot \frac{I_0}{V_s}$$

$$= \frac{(1-k)K}{2f} \cdot \frac{I_0}{V_0(1-k)}$$

$$\therefore \quad C_c = \frac{K}{2fR}$$

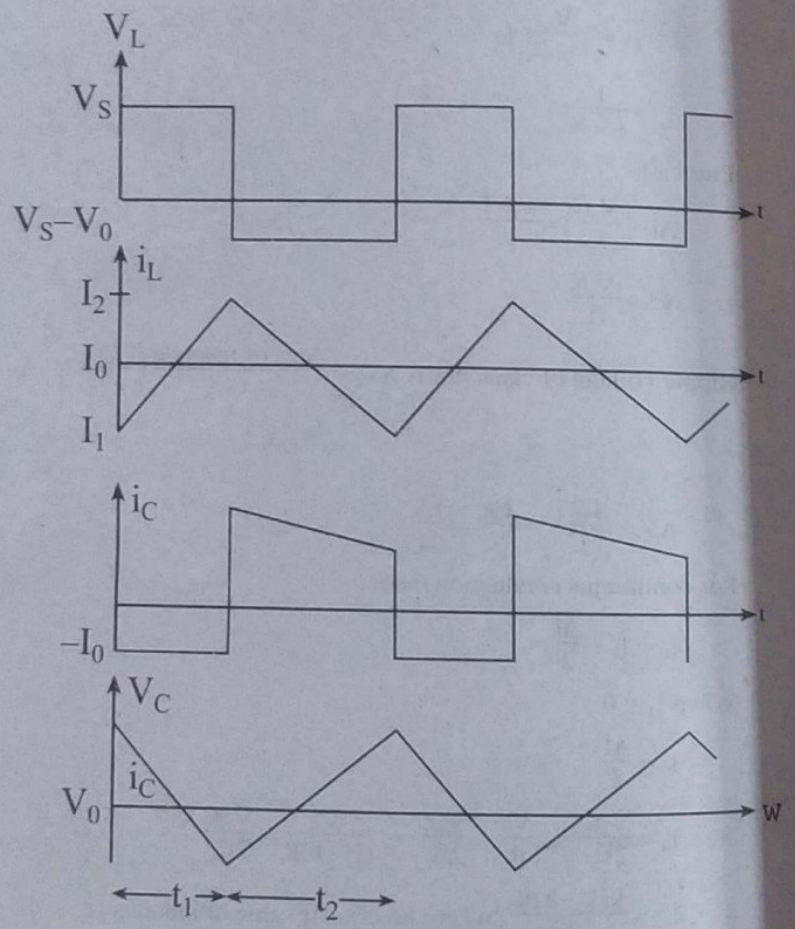


Fig: Waveform of boost regulation

3. Derive expression for average output voltage, peak to peak ripple current of inductor of Buck-Boost regulator with necessary figure and wave forms. [2072 Chaitra, 2068 Chaitr]

Solution:

It gives output voltage that may be less than or greater than the i/p voltage. In this type of regulator, output voltage is opposite to that of input voltage so also known as inverting regulator.

When the switch is ON, the diode is reverse biased and the current flows through inductor L which starts rising from the value of I_1 and reaches its maximum value I_2. We consider the current rises linearly, and t_1 is period of switch on.

$$\text{So, } V_s = L\frac{di}{dt} = L\frac{I_2 - I_1}{t_1} = L\frac{\Delta I}{t_1}$$

ΔI-peak-to-peak inductor current or ripple current

$$\therefore \quad \Delta I = \frac{V_s}{L} t_1 \qquad \text{... ... (i)}$$

Now, if switch is off for t_2 period of time, the diode is forward biased with reverse polarity of inductor and the energy stored by inductor is now transferred to the load. So the inductor current falls until the switch is ON again.

$$\therefore \quad V_0 = -L\frac{di}{dt} = -L\frac{(I_2 - I_1)}{t_2} = -L\frac{\Delta I}{t_2}$$

$$\therefore \quad \Delta I = \frac{-V_0}{L} t_2$$

From (i),

$$\frac{V_s}{L} t_1 = -\frac{V_0}{L} t_2$$

$$\text{or, } V_0 = -V_s\frac{t_1}{t_2} = -V_s\frac{t_1}{T - t_1} = \frac{-V_s KT}{T - KT} = \frac{-V_s K}{1 - K}$$

$$\therefore \quad V_0 = \frac{-V_s K}{1 - K}$$

Output voltage is also the average voltage so.

$$V_a = \frac{-V_s K}{1 - K}$$

If the circuit is loss less, $V_s I_s = -V_0 I_0 = \frac{V_s K}{1 - K} I_0$

$$\therefore \quad I_0 = \frac{I_s (1 - K)}{K}$$

From equation (i),

$$\Delta I = \frac{V_s}{L} KT = \frac{V_s K}{fL}$$

The inductor current i_c consists of de component I_0 (I_a) with super imposed triangular ac component almost all of component flows

through the filter capacitor $\cos i_c$. Due to this ripple current, there will be ripple voltage across capacitor so, ripple voltage $\Delta V_c = \frac{\Delta Q}{C}$

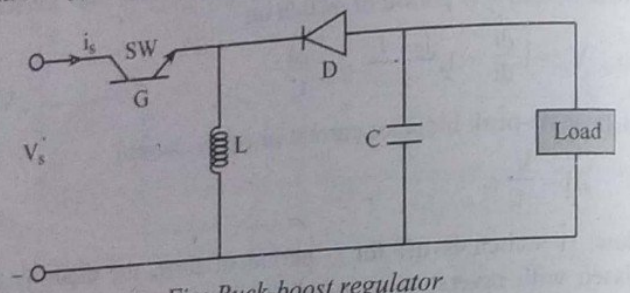


Fig: Buck-boost regulator

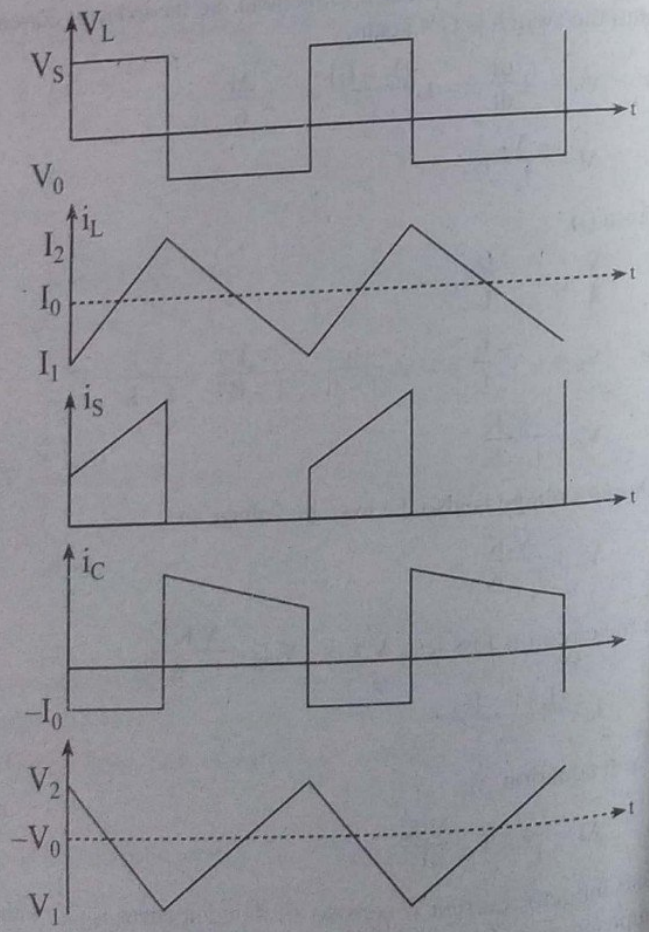


Fig: Waveforms of buck-boost regulator

$$= \frac{I_0 \times t_1}{C} \text{ (area of rectangle in waveform)}$$

$$= \frac{I_0 \times KT}{C}$$

$$\therefore \quad \Delta V_c = \frac{I_0 K}{fc}$$

Since $I_0 = I_a$

$$\Delta V_c = \frac{I_a K}{fc}$$

Condition for continuous inductor current and capacitor voltage (continuous conduction mode)

From figure,

$$\frac{\Delta I}{2} + I_1 = I_0$$

$$\therefore \quad I_0 = \frac{\Delta I}{2} \text{ for continuous conduction (i .e. } I_{min} = I_1 = 0)$$

$$\therefore \quad \frac{V_0}{R} = \frac{\Delta I}{2}$$

$$\text{or,} \quad \frac{KV_s}{(1-K)R} = \frac{V_s K}{2fL}$$

$$\therefore \quad L_c = \frac{(1-K)R}{2f} \quad L_c \text{ – critical value of inductance}$$

Similarly for critical capacitance,

$$V_0 = V_1 + \frac{\Delta V_c}{2}$$

$$\therefore \quad V_0 = \frac{\Delta V_c}{2} \text{ for continuous capacitor i.e. } V_1 = 0$$

$$\text{or,} \quad I_0 R = \frac{I_0 K}{2fc}$$

$$\therefore \quad C_c = \frac{K}{2fR}$$

❖❖❖

Short Notes

Some Important short notes from exam point of view.

(a) Differential Amplifier with active load.

(b) Generation of RMS output of Sinusoidal wave using log antilog application.

(c) Current sterring circuit.

(d) Switching regulator.

(e) Working principle of TRIAC.

(f) Define term CMRR, PMRR and slew rate.

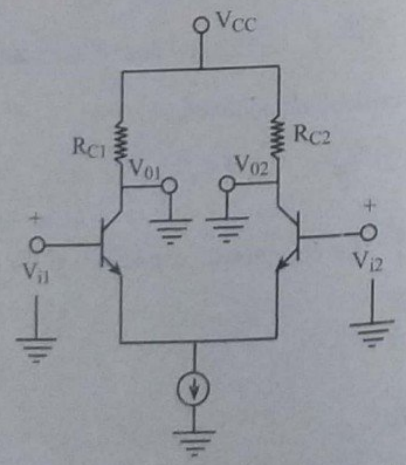
(g) Application of log and anti log Amplifier.

(h) SMPS.

(i) Instrumentation Amplifier.

(j) Noise in op-amp circuit.

(a) The Differential amplifier: The output of a different amplifier is proportional to the difference between the two input voltages.



- The basic differential amplifier has two transistors θ_1 and θ_2 having emitter configuration.
- θ_1 and θ_2 are perfectly matched CB are same.

- Base terminals are input S collector terminal are output.
- Differential input voltage is $V_{id} = (V_{i1} - V_{i2})$

  Differential output voltage is $V_{od} = (V_{01} - V_{02})$

  or, $(V_{02} - V_{01})$

Symbolically,

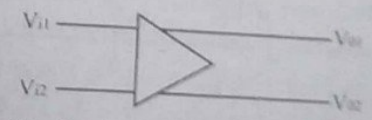
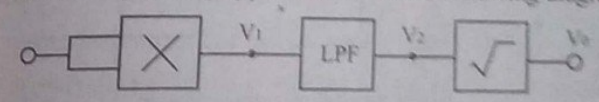


Fig: Symbol for differential amplifier.

(Double ended input and double ended output amplifier)

(b) Generation of RMS output of sinusoidal wave using log anti-log application: To find the RMS value of sinusoidal wave from a function of log antilog application we have following diagram



From figure, we have,

$$V_{in} = V_m \sin \omega t$$

So,

The output of multiplier will be

$$V_1 = V_{in}^2$$

$$= V_m^2 \sin^2 \omega t$$

$$= \frac{V_m^2}{2}[1 - \cos 2\omega t]$$

$$= \frac{V_m^2}{2} - \frac{V_m^2}{2}\cos 2\omega t$$

The high pass frequency component $\cos 2\omega t$ is removed by low pass filter. So, output of LPF is

$$V_2 = \frac{V_m^2}{2}$$

So, the output of square route is,

$$V_0 = \sqrt{V_2} = \sqrt{\frac{V_m^2}{2}} = \frac{V_m}{\sqrt{2}}$$

(c) **Current steering circuit:** Current mirror are used in IC fabrication to reproduce current for biasing various circuit.

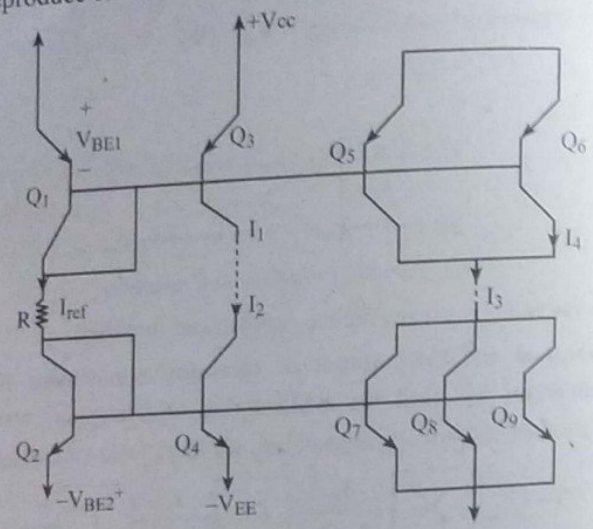


Fig: Current sterring circuit

Generalization of the no of constant current sources using KVL

$$I_{ref} = \frac{V_{CE} + V_{EE} - V_{BE1} - V_{BE2}}{R}$$

Assuming the transistor has high band neglecting early effect the A forms a current mirror with θ_3. Thus θ_3 will supply a constant current I equal to I_{ref} transistor θ_3 can supply this current to any load as long as the voltage that develops at the collector does not exceed (V_{CE} − 0.3 V) otherwise θ_3 would enter the saturation region to generate a DC current twice than the value of I_{ref} two transistor θ_5 and θ_6 are connected in parallel and combination forms a mirror with θ_1 thus.

$$I_3 = 2I_{ref}$$

Parallel combination of θ_5 and θ_6 is equivalent to the transistor whose EBJ area is double that θ_1. In IC fabrication the EBJ area is doubled if the current has to be doubled.

Current mirror are indeed used to provide multiple of the reference current provide multiple of the reference current by simply designing the transistor to have an area ratio equal to the desired multiple.

The effect of finite 'β' becomes more severe as the number of output the mirror is increased. This is because the addition of more transistor means that their base current have to be supplied by the reference source.

(d) **Switching regulator:** A switching regulator is a circuit that uses a power switch, an inductor and a diode to transfer energy from input to output. The power switch usually field effect transistor (FET) is turned on and off by a switching controller IC that monitors the output of the switching regulator in a feedback control loop. This ensures that it maintains a constant output under normal operating conditions. In some switching regulators, the FET is a discrete component, external to the switching controller. In other version the FET and controller are in the same IC.

The basic components of the switching circuit can be rearranged to form a step down (buck) converter a step-up (boost) convert or an inverter (fly back). These designs are shown in figure 1, 2, 3, and 4 respecting where figure 3 and 4 are the same except for the transformer and diode polarity.

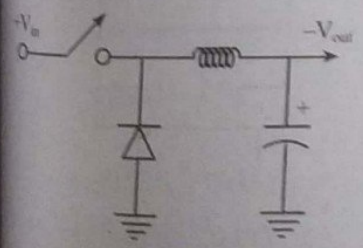


Fig: (a) Buck converter topology

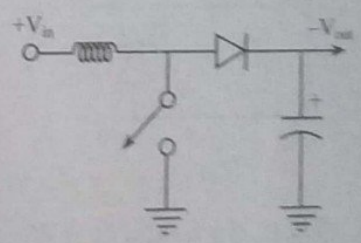


Fig: (b) Simple boost converter

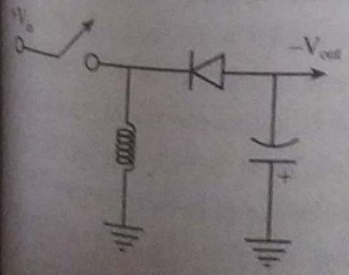


Fig: (c) Inverting topology

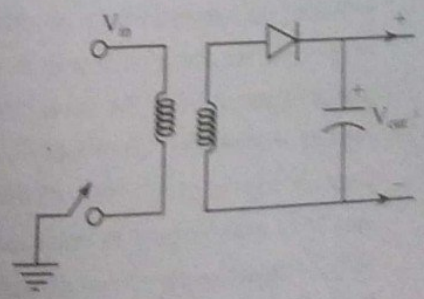


Fig: (d) Transform flyback topology

(e) **Working principle of TRIAC:** A TRIAC is three terminal device that conduct current in either direction when triggered the forward and reverse characteristics of TRIAC are identical to forward characteristics of SCR.

Generally a TRIAC can be said as gated DIAC. It can represented as two SCRs connected.

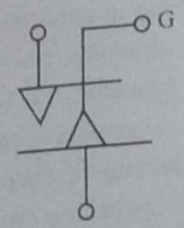


Fig: TRIAC symbol

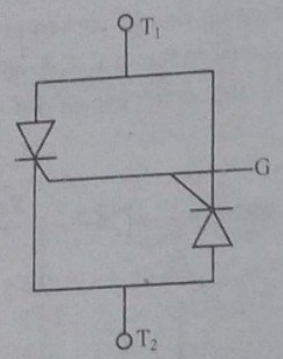


Fig: TRIAC represented by SCRS

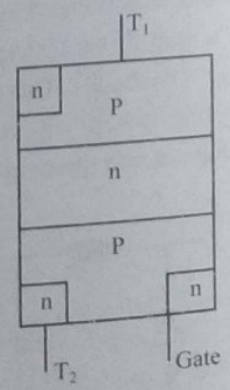


Fig: TRIAC physical layer

Though the TRIAC can be turned on without any gate current provided the supply voltage becomes equal to the break over voltage of the traic but the normal way to turn on the TRIAC is by applying a proper gate current. As in case of SCR here too the larger the gate current the smaller the supply voltage at which the TRIAC can conduct current irrespective of the voltage polarity of terminal MT_1 and MT_2 with respect to each other and that of gate and terminal MT_2. Consequently four different possibilities of operation of TRIAC exists they are.

(i) Terminal MT_2 and gate are positive with respect to terminal MT_1.

(ii) Terminal MT_2 is positive but gate is negative with respect to terminal MT_1.

(iii) Terminal MT_2 and gate are negative with respect to terminal MT_1.

(iv) Terminal MT_2 is negative but gate is positive with respect to terminal MT_1.

Define terms CMRR PMRR and slew rate:

CMRR: If there is perfect matching between two input terminals the value of A_{cm} will be zero so, to measure the degree of matching between two input terminal two input terminals the term CMRR is defined as,

$$CMRR = \frac{A_d}{-A_{cm}} = \frac{\text{differential mode gain}}{\text{common mode gain}}$$

$$\text{In dB, } CMRR = 20 \log \left(\frac{A_d}{A_{cm}}\right)$$

Also, CMRR is also expressed as the ratio of change in input offset voltage to total change in common mode voltage i.e.

$$CMRR = \frac{V_{i0}}{V_{cm}}$$

$$\text{In dB, } CMRR = 20 \log \left(\frac{V_{i0}}{V_{cm}}\right)$$

PSRR: It is the measure of the ability of op-amp to ignore change in power supply. PSRR is the ratio of change in output voltage to the change in power supply voltage. It is usually expressed in microvolt per volt or in decibel.

Stew rate: The maximum possible rate at which an amplifier output voltage can change is called slew rate. It is measured in volt per microseconds (V/μsec) used mathematically.

$$\text{Slew rate} = \left.\frac{dV_0}{dt}\right|_{max}$$

Also, $SR = AV_m 2\pi f$.

(g) **Application of log and antilog amplifier:** The electronic circuit which perform the mathematical operation such as logarithm and anti-logarithm (exponential) with an amplification are called as logarithmic and anti logarithmic amplifier respectively. Log and anti log amplifier are non-linear circuit in which the output voltage is proportional to the log or exponent of the input voltage.

It's application are:

(i) Multiplication, Division, Power, Roots

(ii) Compression and Decompression

(iii) True RMS Detection

(iv) To convert in dB

(v) Process control

(h) **SMPS:** SMPS stands for switched mode power supply. SMPS is an electronics power supply that incorporates a switching regulator to convert electrical power efficiently. Like other power supply SMPS transfer power from source to load. In linear power supply power is transferred to the load continuously. But in power is transferred to the load continually. But in the case of SMPS power is not transferred continuously but by switching the switches on and off, power is transferred. SMPS is mainly applicable in power connector, desktop power server control etc.

Types of SMPS are:

(i) DC-DC converter

(ii) Forward converter

(iii) Fly back converter

(iv) Self-oscillating fly back converter

It main's advantage is power supply encompasses in smaller size with light weight and wide yield range and its main drawback is it is complex in designing, higher yield swell and control is worse. Also causes harmonic distortion.

(i) **Instrumentation Amplifier:** It is a dedicated differential amplifier with extremely high input impedance (to avoid loading effect of transducers), high common mode rejection ratio (to recover small signal buried in large common mode noise) and precise gain setting.

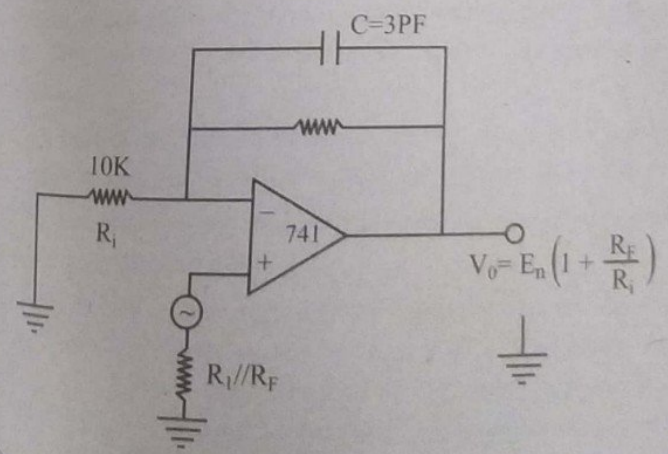
It is required in any measurement system to enhance signal level (in microvolt range) for further processing.

Characteristics of instrumentation Amplifier

- Extremely high input impedance
- Low output impedance
- High CMMR
- High gain accuracy
- High gain stability

(j) **Noise in op-amp circuit:** Electronic circuit is susceptible to noise and op-amp is not an exception. Apart from external noise, op-amp has internal noise sources like offset voltages, current, bias current and internal component. And noise is also amplified by op-amp just as signal voltage.

The internal op-amp noise is modeled simply by a noise voltage source E_n.



- Op-amp 741 has 24V total noise for ($10H_z$ $10\ KH_z$)

- Valid for $R_1 = 100\Omega - 20\ K\Omega$
- If $R_1 > 20\ K\Omega$, noise increase rapidly

Following measure can be taken to minimize the internal noise

- Keep series input resistor R_1 and R_f low value
- By pass R_f with small capacitor this reduce noise gain at higher frequencies
- Never connect a capacitor across input resistor or (– input) to ground.

❖❖❖