EXPERIMENT 06

STUDY OF CMOS PLL 4046

AIM

To familiarise with CMOS phase locked loop IC CD4046A and study it's functional characteristics.

COMPONENTS:

CD4046A, Resistors, Capacitors, DC power supply, Signal generator, bread board and CRO.

THEORY

PLL is a circuit designed to synchronize with an incoming signal and remain in synchronization despite the incoming signal variations. PLL mainly consists of a phase detector, a low pass filter and a voltage controlled oscillator. Phase detector provides a DC voltage proportional to the phase difference between inputs. Low pass filter removes high frequency noise. The DC Voltage Controls the VCO frequency. VCO frequency is fed back and compared with input frequency and automatically gets itself equal to the input frequency.

The 74c/HCT 4046-A is a silicon gate CMOS device. It has pins compatible with 4046-B. It mainly consists of a VCO and three phase gate. PC_2 is an edge triggered RS flip flop. PC_3 consists of two DFFs with associated components. Large signals can be connected directly to the signal inputs of PLL while series capacitor is used to couple the signal inputs to connect the small signals.

VCO required one external capacitor C_1 (between C_{1A} and C_{1B}) and one external resistor R_1, (between R_1 and ground). If frequency offset is not required for VCO, R_2 is omitted. Register R_1 and Capacitor C_1 determines the frequency range of VCO. A low level at the inhibit input enables the VCO and the demodulator. The difference between HC and HCT versions is in input level specifications.

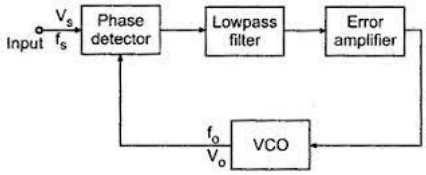


Fig. 2.123 Block diagram of PLL

DESIGN

Centre frequency is given by $f_0 = 1/2R_1 (C_1 + 32 \text{ PF})$ at V_{DD} 5V

Let the required to f_0 be 10kHz. Let R_1 = 100kHz

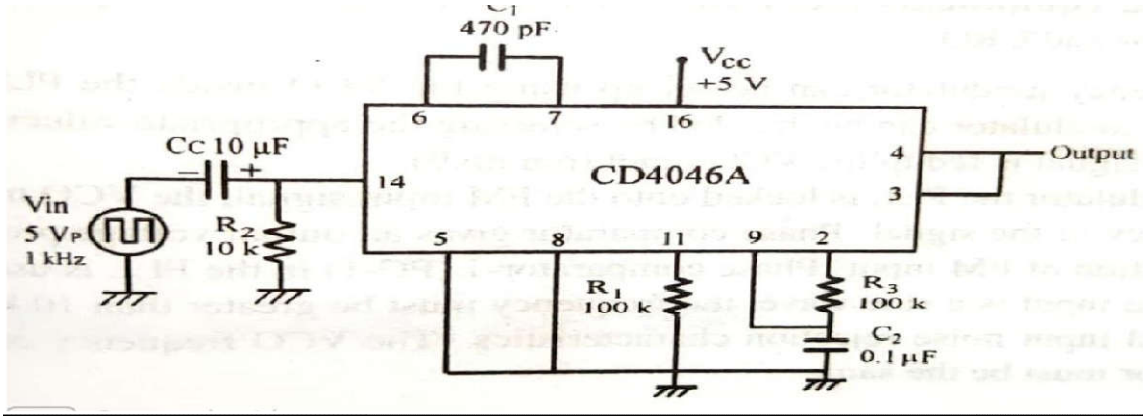
Then C_1 = 500 pF use 470 pf.

Capture range $2f_c = (1/\pi) (2\pi f_2 / R_3C_2)^{1/2}$

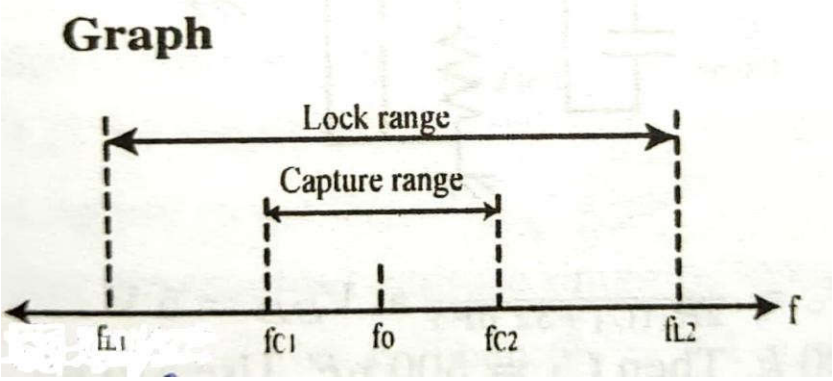
Let the required capture range be 800Hz. Take $R_3 = 100\ k\Omega$. Then $C_2 = 0.1\mu F$.

Use 10μF Capacitor and 10kΩ resistance for ac coupling of input signal.

CIRCUIT



WAVEFORM



PROCEDURE

1. Let the circuit and observe the free running frequency f_0
2. Feed a square pulse input signal and it's frequency from 100 Hz to 1 MHz and note down f_{c1} and f_{L2}.
3. Decrease the frequency from high value to low value and note down f_{c2} and f_{L1}.
4. Calculate Capture range $f_c = f_{c2} – f_{c1}$ and lock range $f_L = f_{L2} – f_{L1}$

RESULT

Familiarised with CMOS phase locked Loop IC 4046A and studied it's functional characteristics.

Free running frequency , f_0 =
Lock range =
Capture range =