

Ex-No: 1	ANALYSIS OF MOS DEVICE CHARACTERISTICS
DATE:	

To study the I-V characteristics of NMOS and PMOS.

SOFTWARE REQUIRED:

- Cadence Virtuoso Software

THEORY:

The MOSFET is a four-terminal device, whose substrate, or body terminal must be always held at one of the extreme voltages in the circuit, either the most positive for the PMOS or the most negative for the NMOS. One unique property of the MOSFET is that the gate draws no measurable current.

In Triode Region, Id current equation of the MOSFET (n-type) is given by,

$$I_d = k_n [(V_{gs} - V_{tn}) V_{ds} - \frac{1}{2} V_{ds}^2]$$

In Saturation region, Id current equation of the MOSFET (n-type) is given by,

$$I_d = \frac{1}{2} k_n (V_{gs} - V_{tn})^2$$

In Triode Region, Id current equation of the MOSFET (p-type) is given by,

$$I_d = k_p [(V_{sg} - |V_{tp}|) V_{sd} - \frac{1}{2} V_{sd}^2]$$

In Saturation region, Id current equation of the MOSFET (n-type) is given by,

$$I_d = \frac{1}{2} k_p (V_{sg} - V_{tp})^2$$

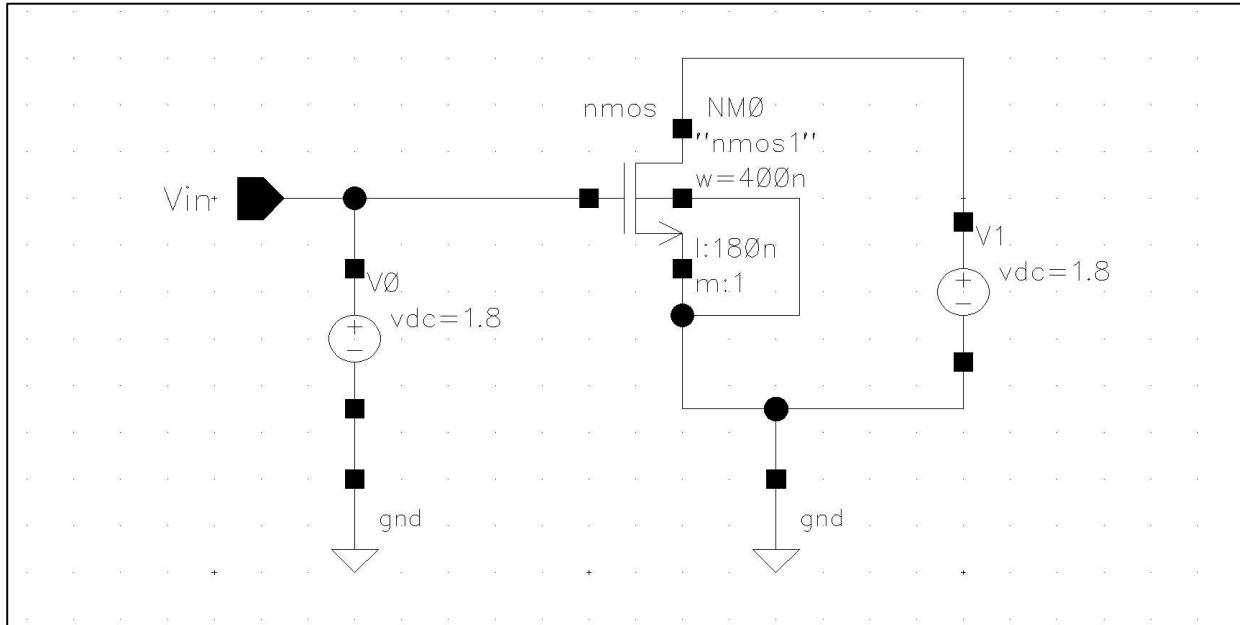
PROCEDURE:

Virtuoso:

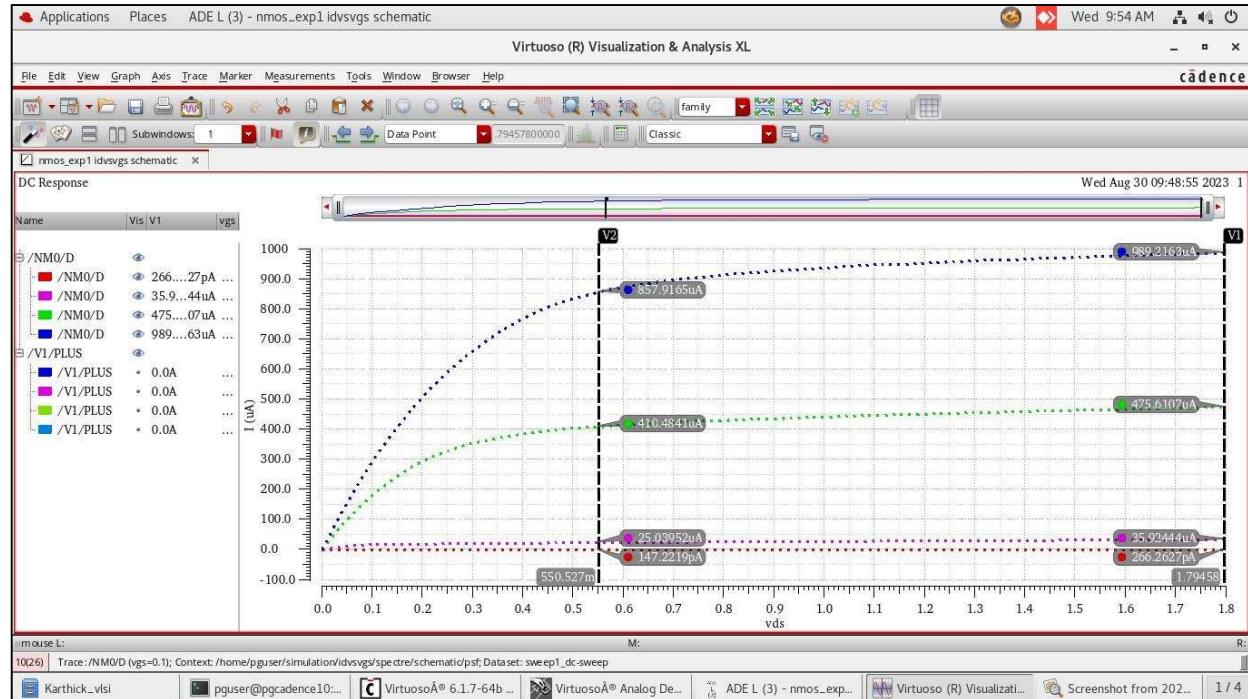
- Boot the system using Red-hat Linux and open the terminal.
- Using command “cd” (change directory) move into the created folder i.e., “cd ‘name of the directory’”.
- Type “csh” in terminal to invoke “cshell” in the terminal i.e., we are looking into the home directory to commands from the “.cshrc” file.

NMOS:

SCHEMATIC:



NMOS ID Vs VDS:



- Now type the command “source /home/install/cshrc “in terminal to setup the environment to launch virtuoso.
- Type “virtuoso” to launch the virtuoso suite of cadence software, virtuoso windowpops up.
- Click on the following to create a new library:
 - File -> New -> Library
 - Name is given to the library
 - In the technology file section “Attach to an existing technology library” is selected.
 - “gpdk180” is selected.
- Click on the following to create a cell view:
 - File -> New -> Cell view
 - Name is given to the cell view.
 - Library created in the previous step is selected.

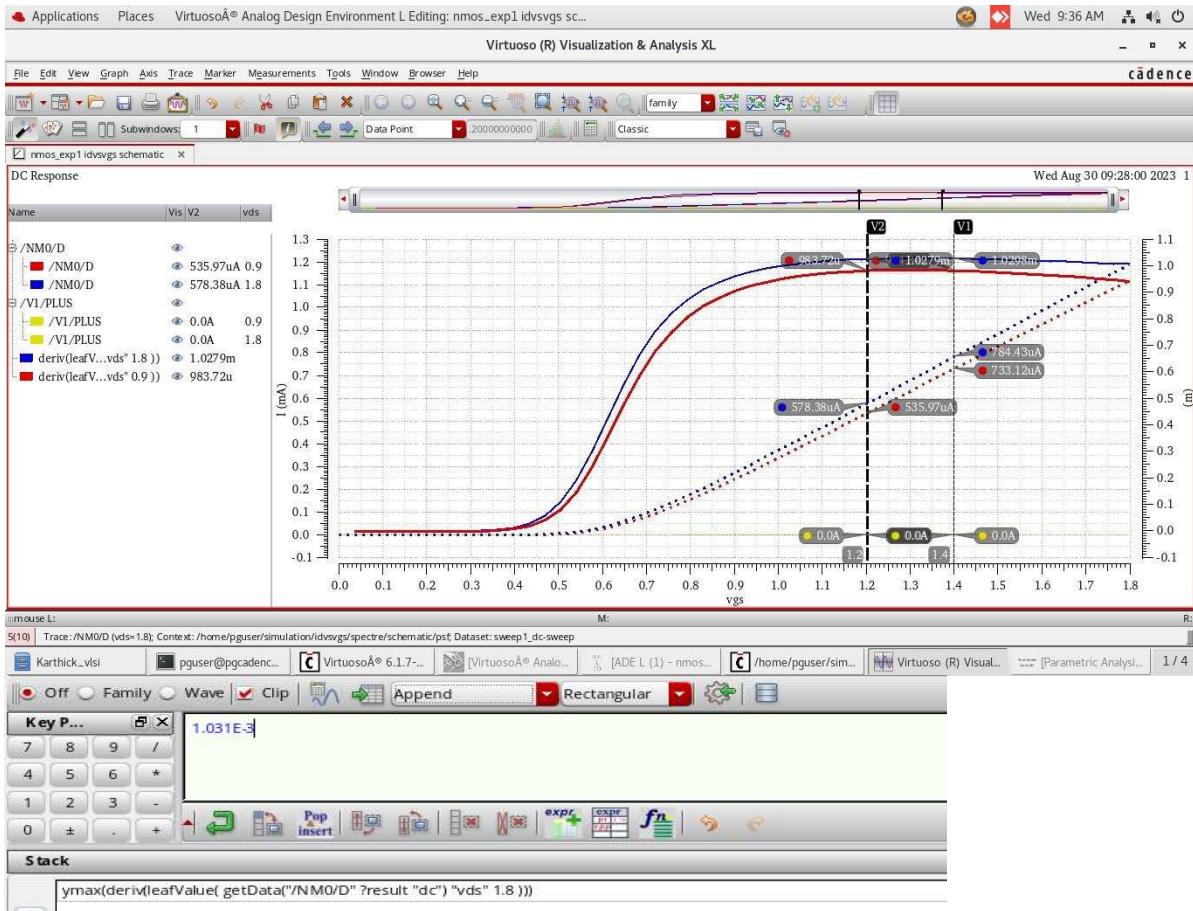
NMOS:

- Select the option “Create instance” to place the components to form a circuit.
 - NMOS is selected from “gpdk180” i.e., “nmos1v”.
 - Vdc, Iprob are selected from “analoglib” library.
 - The Circuit is created by connecting the components as shown in the circuitdiagram.
 - Two vdc present in the circuit is given Va, Vb voltage respectively.
- Click on the Launch option and select “ADE L” option, Analog Design Environment pops up.
- Select the “Variable” option and create two variables “V_a, V_b”.
- Set the start value as 0 v and end value as 1.8v for both variables in analyses optionand provide a standard 1v to both variables.

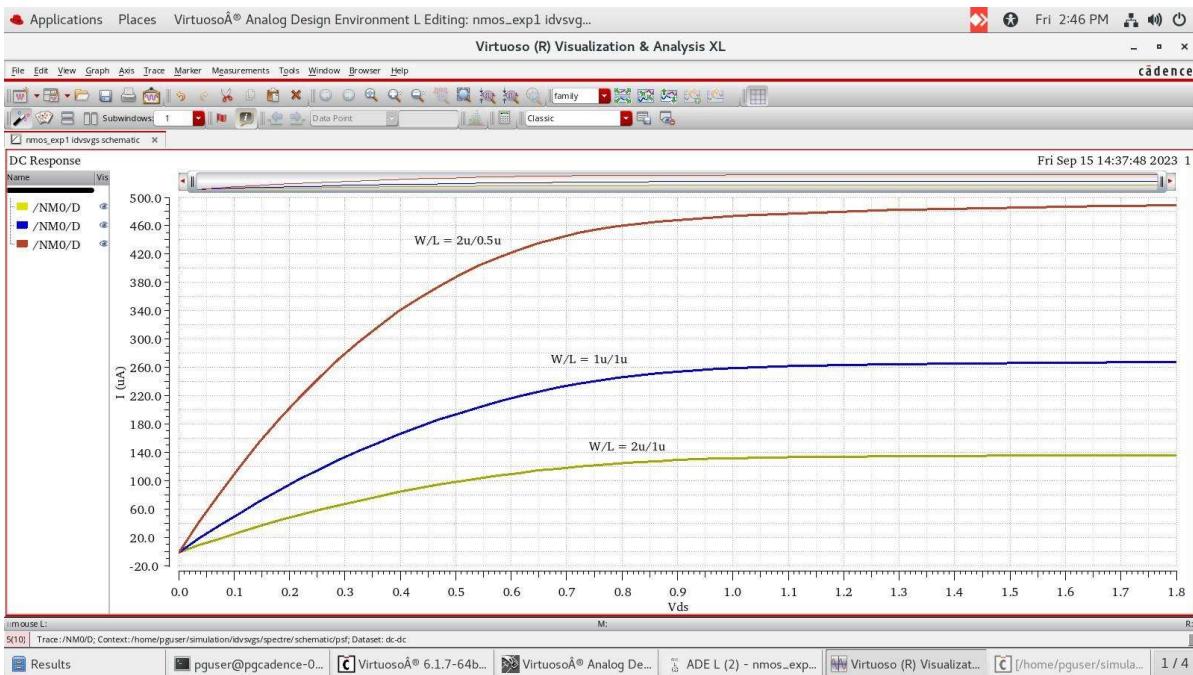
Click on the “Analyses” option to set the type of analyses.

- Select “dc” in analysis option.
- Tick the box “Save DC operating point”.
- Select “design variable” and set is as “V_b”
- Set start value as 0 v and stop value 1.8v

NMOS ID Vs VGS (Gm Deriv):



NMOS ID vs VDS (W/L Change):

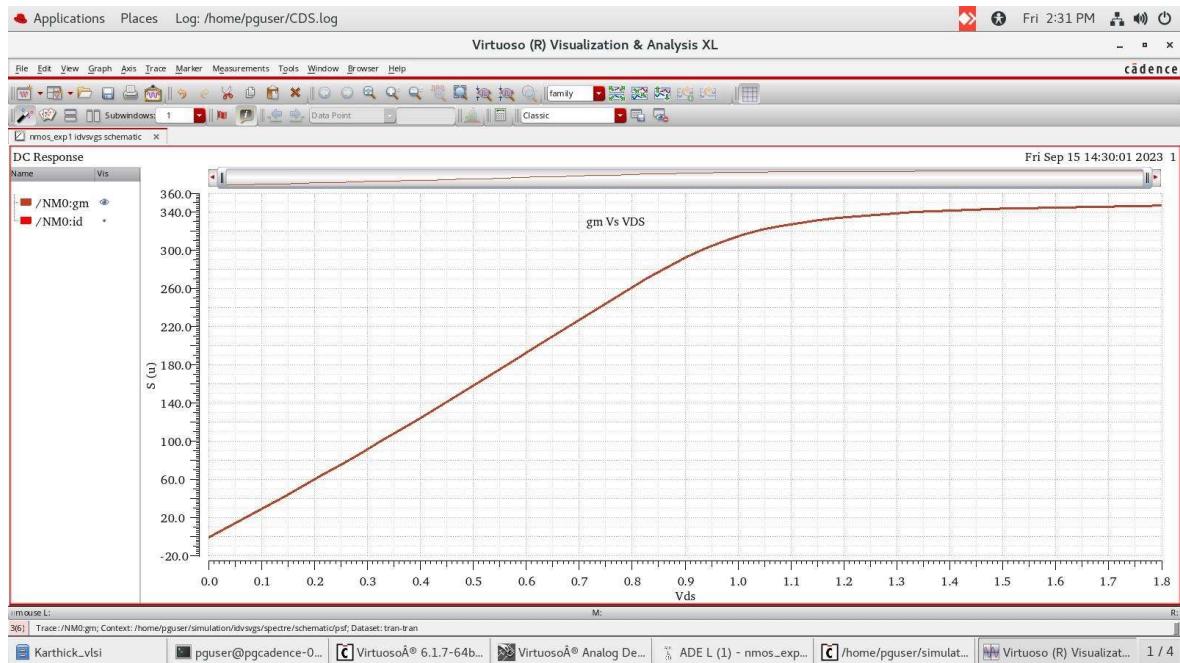


- Select the “Variable” option and create two variables “ V_a , V_b ”.
- Click on option “Outputs”:
 - Tick the box “to be plotted”
 - Select the parameters to be plotted from the schematic diagram i.e., I_d and V_{ds} .
- Click on the simulation option to plot the I_d vs V_{ds} graph.

PMOS:

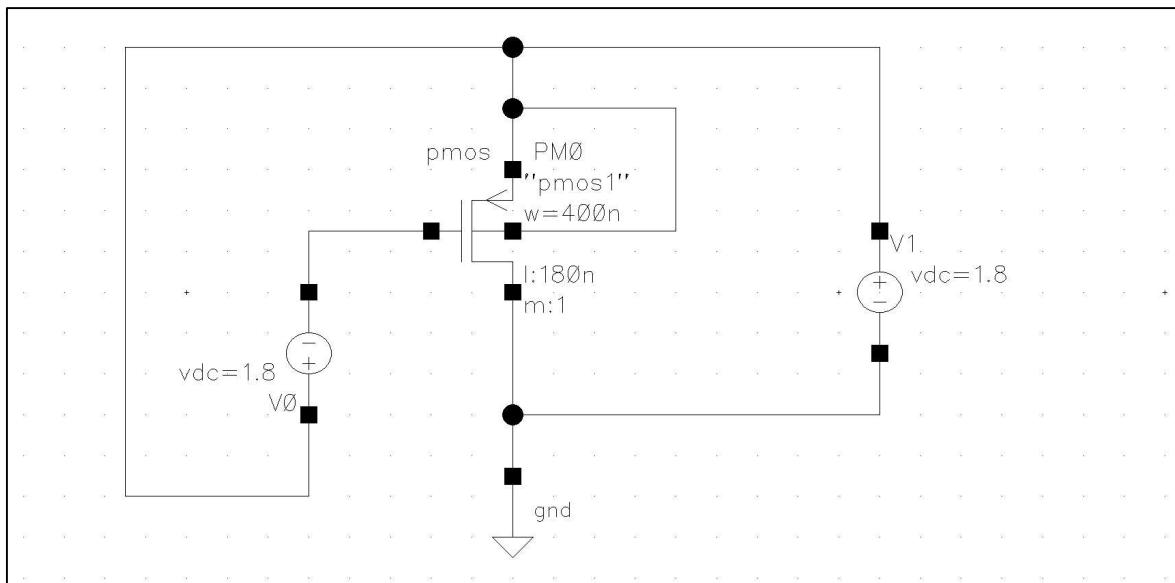
- A new cell view is created by following steps given above in virtuoso section.
- Select the option “Create instance” to place the components to form a circuit.
 - NMOS is selected from “gpdk180” i.e., “pmos1v”
 - Vdc, Iprob are selected from “analoglib” library.
 - The circuit is created by connecting the components as shown in the circuit diagram.
 - Two vdc present in the circuit is given V_a , V_b voltage respectively.
- Follow the same steps in NMOS and set the standard value as -1V to both variables.
- Click on the “Analyses” option to set the type of analyses
 - Select on “dc” in analysis option
 - Tick the box “Save DC operating point”.
 - Select “design variable” and set it as “ V_b ”.
 - Set the start value as 0 V and stop value as -1.8V.
- Click on option “Outputs”:
 - Tick the box “to be plotted”
 - Select the parameters to be plotted from the schematic diagram i.e., I_d and V_{sd}
 - Click on the simulation option to plot the I_d vs V_{ds} .

NMOS – gm vs VDS:



PMOS:

SCHEMATIC:



INFERENCE:

1. ID vs VDS:

From Id Vs Vds graph we will know and find MOSFET different regions of operation (cutoff, linear & Saturation).

- NMOS → As Vds increases Id increase linearly for $V_{gs} > V_t$ and upto $V_{gs}-V_{th}$. After ($V_{gs}-V_{th}$) VDS increases Id will saturate.
- PMOS → As $|V_{ds}|$ increases Id decreases linearly upto ($|V_{gs}| - V_{tp}$). After $V_{ds} < V_{gs} - V_{tp}$ Id will saturate.

For different vgs constant value higher Vgs Value Saturation current is high (Id) ($|Id|$ for pmos)

- $Id \propto V_{gs}^4$ (1.6v) $>$ V_{gs}^3 (1.1iv) $>$ V_{gs}^2 (0.6v) $>$ VE $>$ V_{gs} , (0.1V)

2. ID vs VGS:

- The transfer characteristics of the MOSFET shows the behavior, Starting from cutoff region, after VT (Threshold Voltage) transitioning through the linear region, and finally entering the saturation Region.
- As Vgs increases, device starts to conduct after Vgs in reaching VT and Id will start rising exponentially.

For higher Vds → Id will starts early to rise exponentially

(V_{ds} (1.8V) $>$ V_{ds} (0.9)) → NMOS.

($|V_{ds}|$ (1.8V) $>$ $|V_{ds}|$ (0.9)) → PMOS.

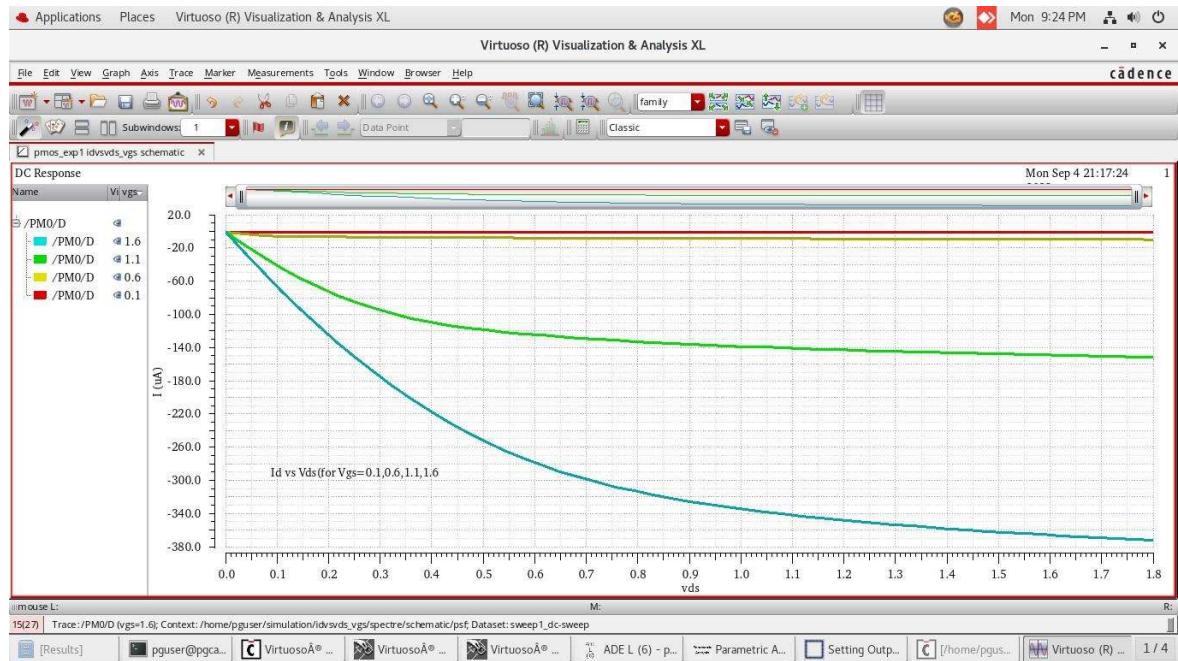
3. gm & gm Vs VDS:

- gm (Transconductance) → (Change in ID / Change in VGS)
- gm Vs Vds MOSFET in saturation $V_{ds} > V_{gs}-V_{th}$ and Linear (Triode region) $V_{ds} < V_{gs}-V_{th}$.

4. Change in W/L Ratio:

- If W/L increases ID will increase.

PMOS ID vs VDS:



PMOS ID vs VGS:



Calculation:

To find g_m

For NMOS:

Here, we know the gain of the transistor A_v and resistance load R_D value, so the formula to find g_m is

$$g_m = \frac{\Delta ID}{\Delta V_{GS}}$$

i) g_m for NMOS

$$V_d = 1.8V$$

$$\frac{Id}{V_{GS}} = \frac{784.43 - 578.38}{1.4 - 1.2} = 1.03 \text{ m}\Omega$$

ii) g_m for PMOS

$$\text{for } V_d = 1.8$$

$$\frac{Id}{V_{GS}} = \frac{0.00046 - 0.00002}{1.8 - 0.43} = \frac{0.00044}{1.37} = 0.00032 \Omega$$

For Pitch-off voltage:

i) NMOS

$$\text{NMOS} = 0.6V$$

ii) PMOS

$$\text{PMOS} = 0.4V$$

R_s value calculation: $r_o = \frac{V_{DS}}{I_d}$

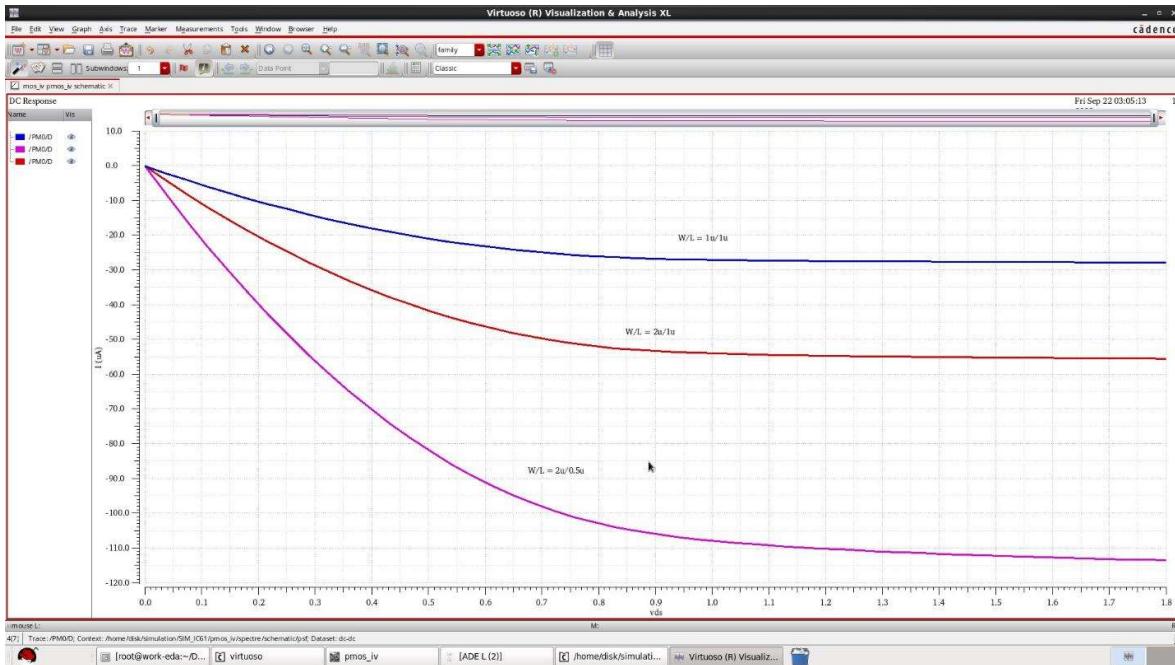
i) for NMOS

$$r_o = \frac{0.6 - 0.4}{(0.9 - 0.7)10^{-3}} = \frac{0.2}{0.2 * 10^{-3}} = 1 \text{ k}\Omega$$

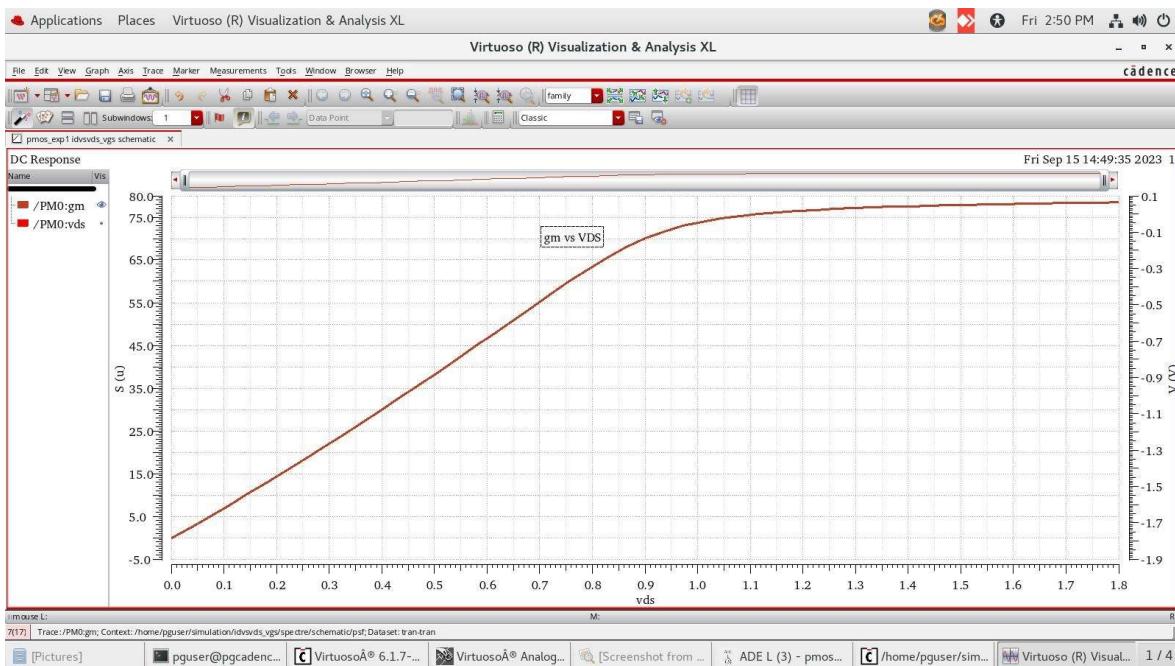
ii) for PMOS

$$r_o = \frac{0.3 - 0.2}{(175 - 110)10^{-6}} = \frac{0.1}{165 * 10^{-6}} = 1.53 \text{ k}\Omega$$

PMOS ID vs VDS (W/L Change):



PMOS gm vs VDS:



RESULT:

Thus, the I-V Characteristics of NMOS and PMOS 180nm Technology is simulated and analyzed using Cadence Virtuoso.

Ex-No: 2	DESIGN AND SIMULATION OF COMMON SOURCE AMPLIFIER WITH RESISTIVE LOAD AND ACTIVE LOAD
DATE:	

AIM:

- To Study the dc, transient and ac characteristics of a NMOS common source amplifier with resistive load and Active Load.
- To design a common source amplifier with resistive load and Active load having gain of 20 and to produce a current of $100\mu A$.

SOFTWARE REQUIRED :

- Cadence Virtuoso software

THEORY :

In NMOS with resistive load, an enhancement-type nMOS transistor acts as the driver device. RL acts as the load. VDD is the power supply voltage of the circuit. When the input of the driver transistor is less than the threshold voltage V_{th} i.e., $V_{in} < V_{th}$, the driver transistor is in the cut – off region and acts as a closed switch thus, does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the supply voltage VDD.

Now, when the input voltage is increased then the driver transistor will start conducting and it will provide some non-zero drain current and the driver transistor is in saturation region.

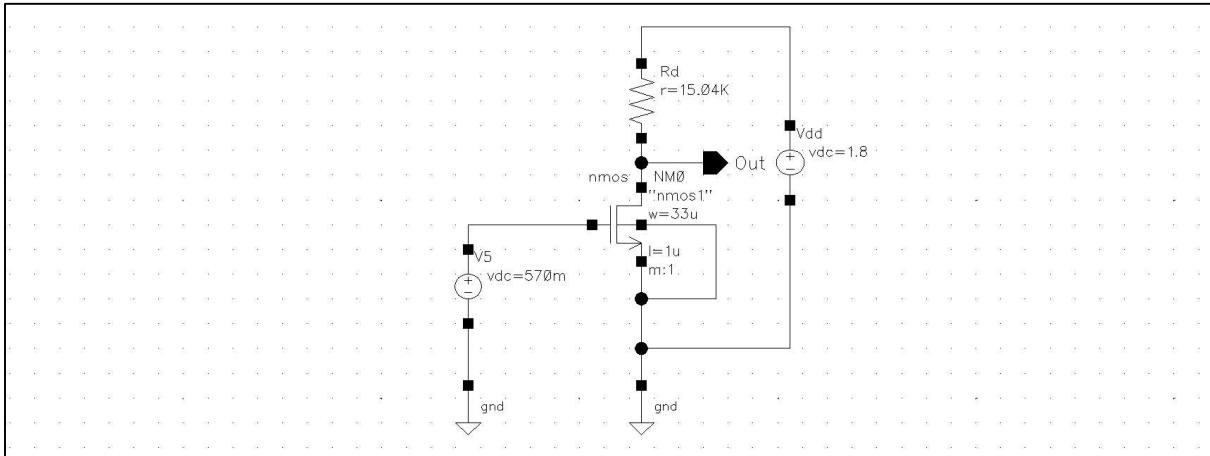
□ Saturation region:

- $V_{ds} > V_{gs} - V_{tn}$
- $I_d = \frac{1}{2} k_n (V_{gs} - V_{tn})^2$
- $g_m = 2I_d/V_{gs} - V_{tn}$
- $V_{ds} = V_{dd} - I_d R_d$

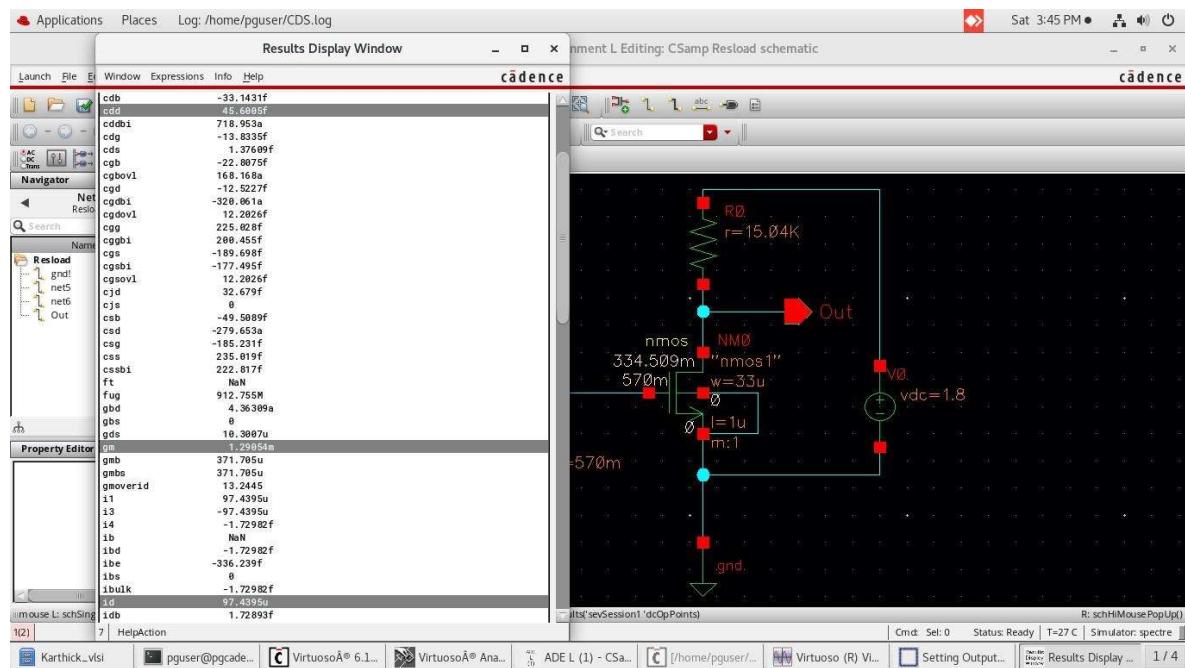
PROCEDURE:**Virtuoso:**

- Boot the system using Redhat linux and open the terminal

SCHEMATIC – RESISTIVE LOAD:



DC OPERATING POINTS:



- Type “csh” in the terminal to invoke “cshell” in the terminal i.e., we are looking into the homedirectory to commands from the “.cshrc” file.
- Now type the command “source /home/install/cshrc “in terminal to setup the environment to launch virtuoso.
- Type “virtuoso” to launch the virtuoso suite of cadence software, virtuoso window pops up.
- Click on the following to create a new library:-
 - File -> New -> Library
 - Name is given to the library
 - In the technology file section “ Attach to an existing technology library” is selected.
 - “gpdk180” is selected.
 - Click on the following to create a cellview:-
 - File -> New -> Cellview
 - Library created in the previous step is selected.

Designing the circuit:-

- Select the option “Create instance “ to place components to form a circuit:-
 - NMOS is selected from “gpdk180” i.e., “nmos1v”
 - “Vdc,gnd” is selected from “analoglib” library.
 - Circuit is created as per the circuit diagram.
 - For Active Load replace the Load Resistance with pmos device

Simulation Setup:-

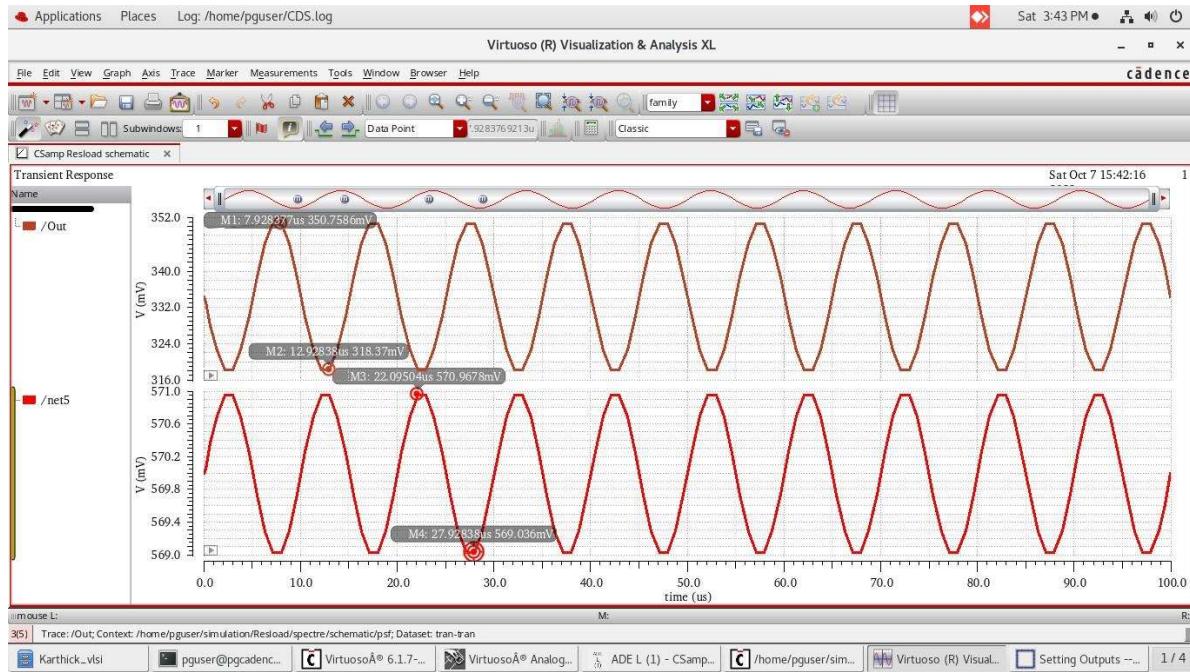
- Click on the following to do the simulation setup:-
 - Launch -> ADE L -> Setup -> Simulation directory -> clickok

Setup -> model libraries -> Select the corresponding gpdk file which is of start type (NN) and click ok

DC Analysis:

- Vdc at Vds is given a constant value of a variable Va
- Click on the following to do the DC analysis:-
 - Launch -> ADE L -> Analog Design Environment

TRANSIENT ANALYSIS:



- Variables -> copy from cellview -> Set Vg= 1V
- Outputs -> to be saved -> Select "OP parameters" -> Click on NMOS -> Click on the graph symbol on the launch menu to plot the graph.
- Before plotting the graph from ADE L menu OP parameters are selected clicking on the (...) button the ADE L menu.
- Select "gm over Id" and "Id" and click ok
- Parameters are selected.
- Analyses -> Analysis ="dc" -> tick save DC operating point.
- Sweep variable -> design variable -> vg is selected
- Sweep range -> Start value as 0 V and Stop value as 1.8V
- Sweep type -> Automatic-> click ok
- Simulate to obtain the graph by clicking on the play button present in ADE L
- After the plot is obtained -> click on the "Id" in the graph -> click on tools -> calculator.
- After opening the calculator, divide the current Id equation by the w given in the schematic diagram.
- Click on the graph symbol to obtain the "Id/w" as graph overlapping on the existing graph by changing the plot setting to "append" in ADE L.

Transient Analysis:

- From the DC analysis Vgs, W and R of the circuit is obtained and designed.
- Click on the following to do the transient analysis
 - Launch -> ADE L -> Analog design environment
 - Analyses -> Analysis="trans" -> set stop time = 8u (stop time = n x 1/f [n=8, 1/f = 1u])
 - Outputs -> to be plotted -> select from design -> select the output and input terminal from schematic -> click ok.
 - Simulation -> Netlist and run to plot output graph of transient analysis of the given transistor.

AC ANALYSIS:



AC Analysis:

- AC magnitude and offset voltage is set before the analysis is done
- Click on the following to do AC analysis:-
 - Launch -> ADE L -> Analog Design Environment
 - Analyses -> Analysis =”ac”
 - Sweep variable -> Frequency -> Sweep range -> start 10 and stop 100 GHZ
 - Sweep type -> Logarithmic -> set points per decade =10-> click ok
 - Outputs -> to be plotted -> Select on design -> Select the output terminal -> clickok
 - Simulation -> Netlist and Run -> output gets plotted i.e., a graph of AC analysisof the NMOS.
 - Results -> AC magnitude and Phase -> To obtain the graph of magnitude andphase plot of transistor.

DESIGN CALCULATION: (RESISTIVE LOAD):

To calculate width ‘W’ of the MOSFET

Given:

$$A_v = 20$$

(Take K_n as 580μ) $L = 1\text{um}$,

$$I = 100\mu\text{A}, R_D = 9\text{K}\Omega$$

To find: g_m

$$|A_v| = g_m * R_d$$

$$g_m = \frac{Av}{Rd} = \frac{20}{9*10^3} = 2.22 \text{ mS}$$

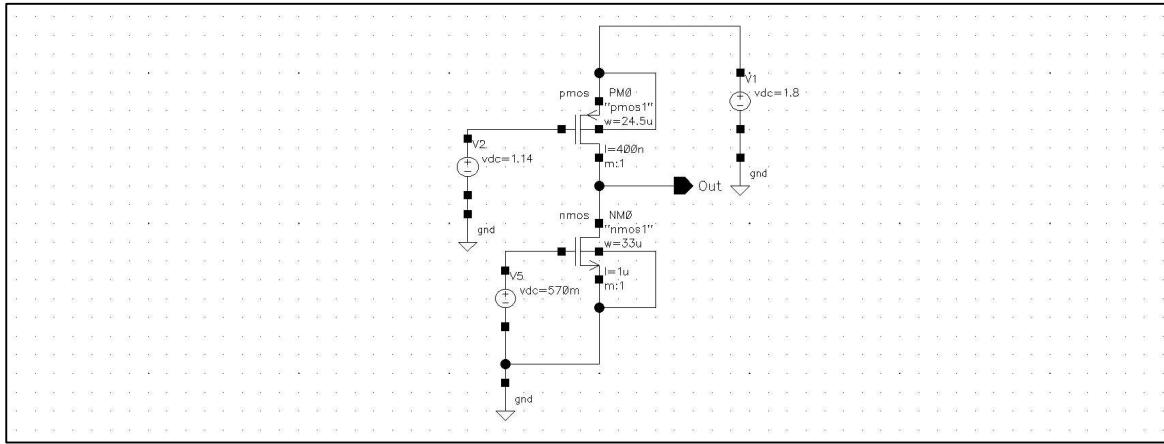
we know,

$$g_m = \sqrt{(2 * \mu n * Cox * \left(\frac{w}{l}\right) * Id)}$$

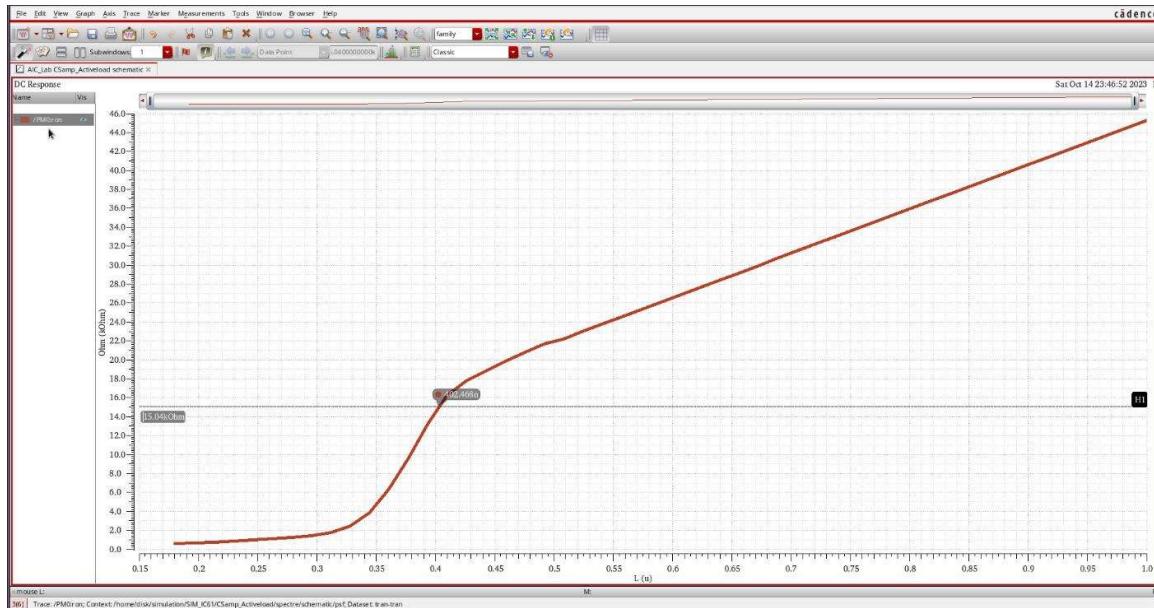
$$g_m = \sqrt{(2 * K_n' * \left(\frac{w}{l}\right) * Id)}$$

Squaring on both sides,

SCHEMATIC: (ACTIVE LOAD)



PMOS RON MATCH:



$$g_m^2 = 2 * Kn' * \left(\frac{w}{l}\right) * Id$$

$$\frac{w}{l} = \frac{gm^2}{2*Kn'*Id}$$

$$W = \frac{gm^2}{2*Kn'*Id} * L$$

$$W = \frac{2.22*10^{-6}}{2*100*10^{-6}*580*10^{-6}} = 42.5*10^{-6} \text{ m} \quad L = 1 \mu\text{m}$$

In DC Analysis:

NMOS parameters obtained as given below

$$I_d = 97.439 \text{ uA}$$

$$g_m = 1.29 \text{ mS} \quad (\text{For } R_d = 15.04 \text{ k}\Omega \rightarrow \text{To match } I_d = 100 \text{ uA})$$

Region = 2 (Saturation)

In transient analysis:

Gain calculation from transient analysis,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{(350.758 - 318.37)}{(570.96 - 569.036)} m = 16.83$$

In dB, take $20 * \log(A_v)$

$$\text{Gain in dB} = 20 * \log(16.83)$$

$$\text{Gain in dB} = 24.52 \text{ dB}$$

Active load:

NMOS transistor as driver and PMOS transistor as load.

Design calculation:

$$A_v = 20$$

$$I_d = 100 \mu\text{A}$$

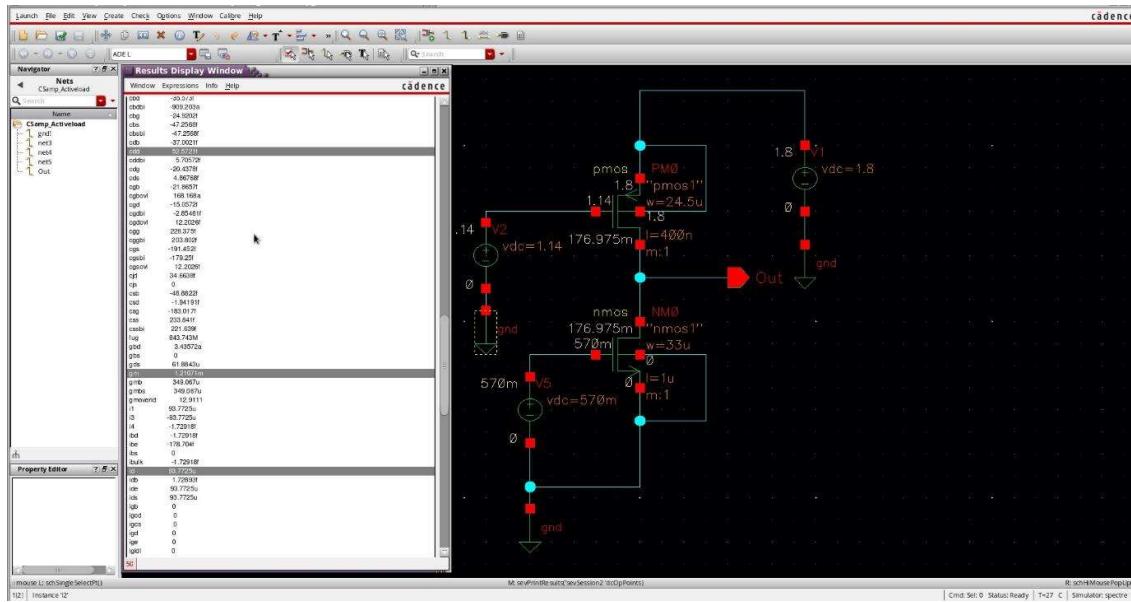
$$Kd' = \frac{Kn'}{3} = \frac{580}{3} = 193.3 \mu\text{A}/v^2$$

$$V_{GS} \geq 1.14 \text{ V} = V_b \text{ (Bias Voltage)}$$

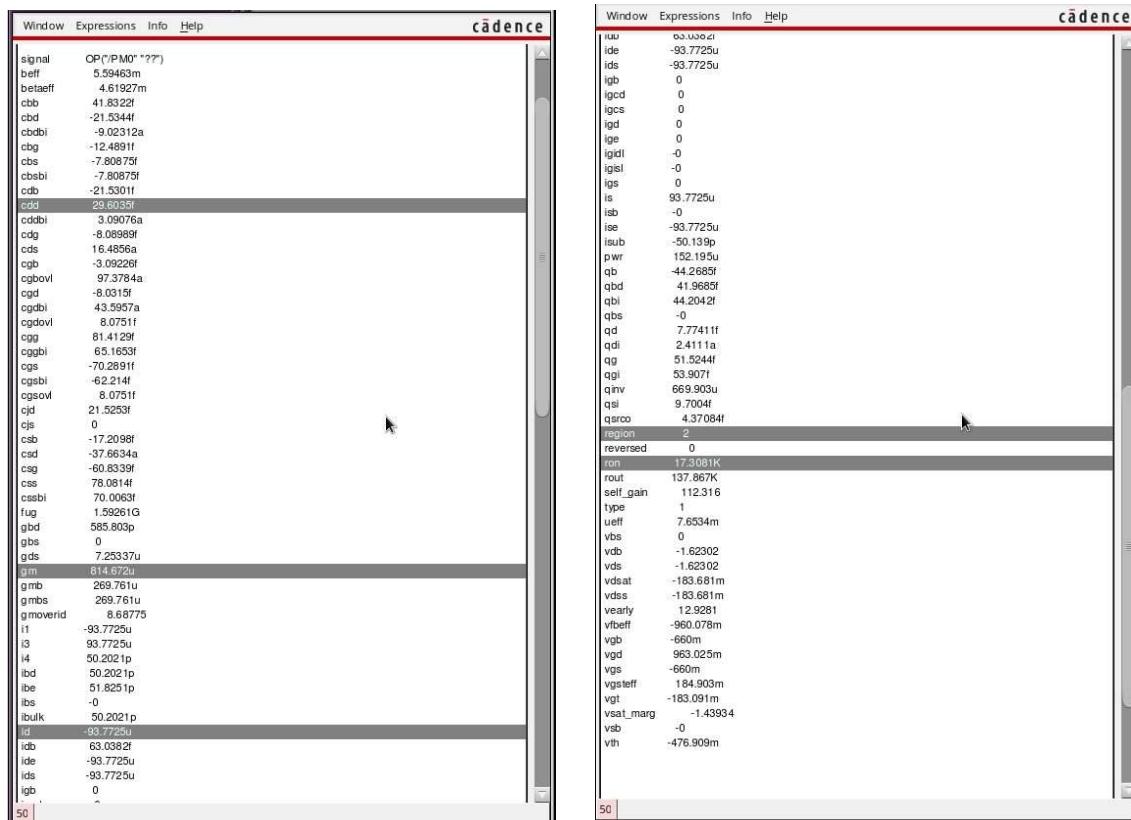
To operate PMOS in Saturation Region, here to match the PMOS

DC OPERATING POINTS:

NMOS:



PMOS:



$r_{on} \sim 15 \text{ k}\Omega$ (same as resistive load)

By sweeping L, we get required r_{on}

For $r_{on} = 15.04 \text{ k}\Omega$, $L = 403.468\text{n}$

(value are taken from graph r_{on} Vs L)

For DC analysis:

PMOS:

$$I_d = -93.7725\mu\text{A}$$

$$r_{on} = 17.3 \text{ k}\Omega$$

Region = 2 (Saturation)

$$V_{th} = -476 \text{ mV}$$

NMOS:

$$I_d = 93.772\mu\text{A}$$

$$g_m = 1.21\text{mV}$$

$$C_{dd} = 52.572 \text{ fF}$$

Region = 2 (saturation)

$$V_{th} = 485 \text{ mV}$$

$$f_3(\text{dB}) = \frac{1}{2\pi r_{on,p} C_{dd,n}} = \frac{1}{2 * 3.14 * 17.3 * 10^3 * 52.57 * 10^{-15}} = 175.08\text{MHz}$$

Transient Analysis:

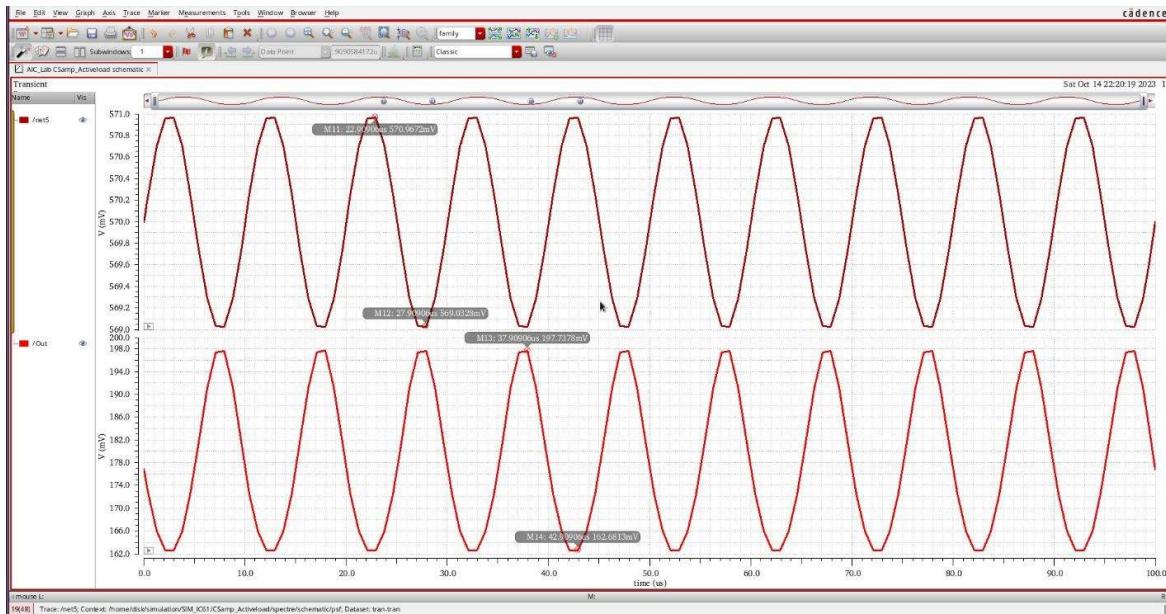
$$|A_v| = \frac{V_{out}}{V_{in}} = \frac{(197.737 - 162.681)\text{mV}}{(570.96 - 569.03)\text{mV}} = 18.16$$

The above A_v for input amplitude of 1mV & frequency 100KHz

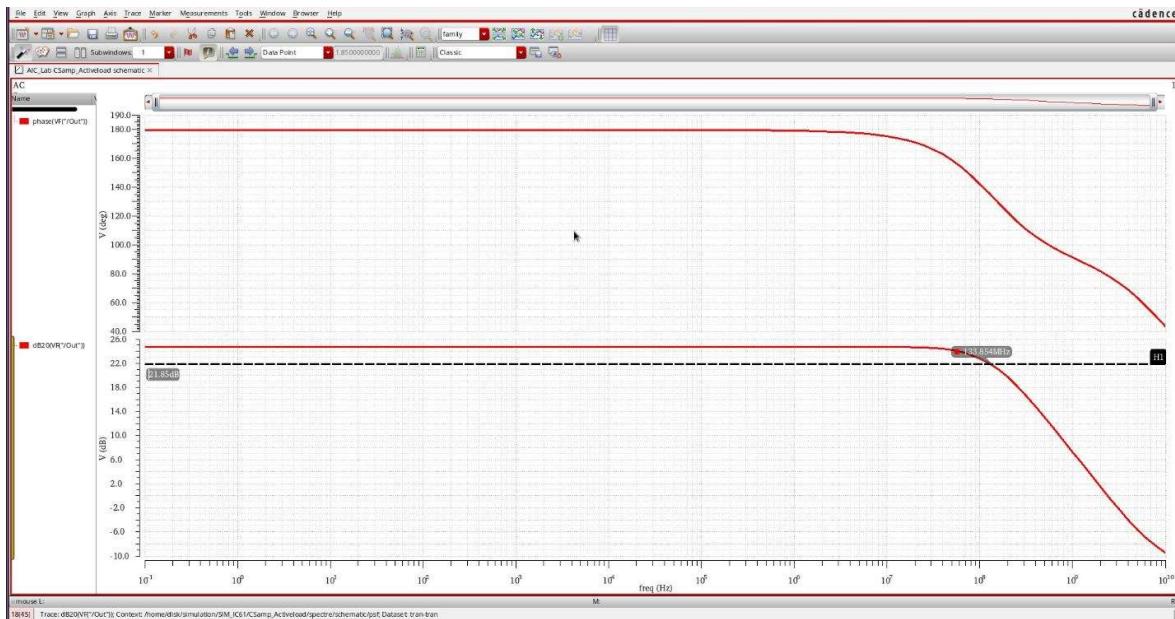
A_v in transient analysis

$$A_v(\text{dB}) = 20 * \log(18.16) = 25.18 \text{ dB}$$

TRANSIENT ANALYSIS:



AC ANALYSIS:



Design value: (Resistive Load)

Designed Value	Practical Value
$I_d = 100 \mu A$	$I_d = 97.439 \mu A$
$A_v = 20$	$A_v = 16.83$
$A_v = 26.02 \text{ dB}$	$A_v = 24.5 \text{ dB}$
$F_{3dB} = 232 \text{ MHz}$	$F_{3dB} = 267.5 \text{ MHz}$

Design value: (Active Load)

Designed Value	Practical Value
$I_d = 100 \mu A$	$I_d = 93.77 \mu A$
$A_v = 20$	$A_v = 18.16$
$A_v = 26.02 \text{ dB}$	$A_v = 24.85 \text{ dB}$
$F_{3dB} = 175 \text{ MHz}$	$F_{3dB} = 133.854 \text{ MHz}$

INFERENCE:

1. The common source amplifier exhibited noticeable gain, indicating ability to amplify the input signal.
2. The gain was influenced by the values of Resistor and transconductance of the MOSFET.
3. In active Load, MOSFET amplifier circuits, instead of a passive resistor, the active component- MOSFET (PMOS) is used to increase the gain of the amplifier.

RESULT:

The study of dc, transient and ac characteristics of a NMOS Common Source Amplifier with Resistive Load and Active Load with gain of 20 and I_d of $100 \mu A$ is simulated and observed.

Ex-No: 3	DESIGN AND SIMULATION OF CMOS INVERTER
DATE:	

AIM:

To simulate the CMOS inverter circuit using Cadence and plot its transient response to calculate the propagation delay.

SOFTWARE TOOLS REQUIRED:

- Cadence Virtuoso

THEORY:

Complementary MOS is a technology that uses both NMOS and PMOS in the same circuit. We know that NMOS gives strong 0 and weak 1 while PMOS gives weak 0 and strong 1. In order to get both strong 0 and 1 in same circuit, we go with CMOS technology. The pull-up network that provides strong 1 is realized using PMOS and the pull-down network that provides strong 0 is realized using NMOS.

PROCEDURE FOR CREATING SCHEMATIC:

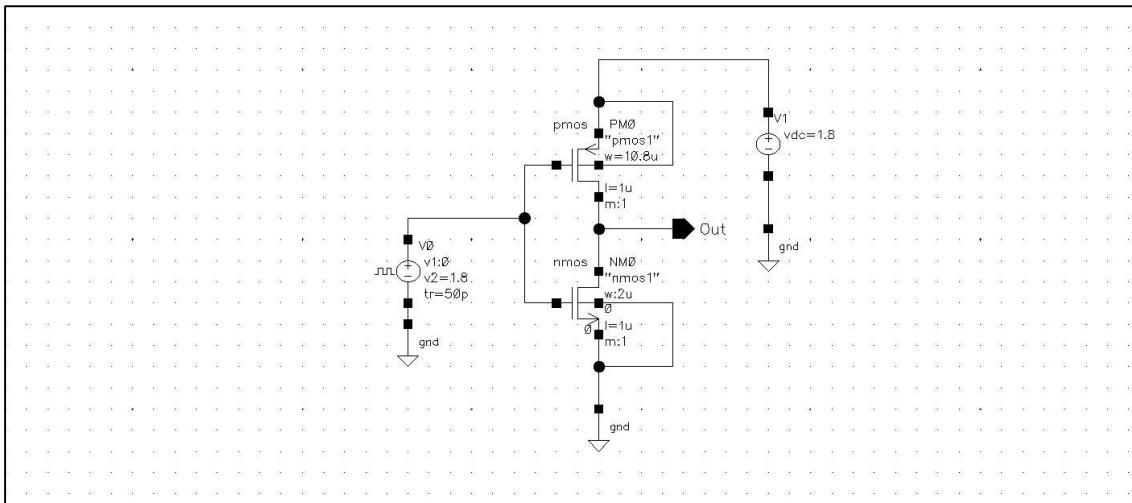
LAUNCHING CADENCE TOOL SUITE:

- Create a folder in desktop → Right click on the folder → Select open in terminal window.
- In the terminal window, enter the following commands to invoke C;
- \$ csh
- \$ source /home/install/cshrc Press Enter key
- Type, “Virtuoso” and press Enter to open the virtuoso window.

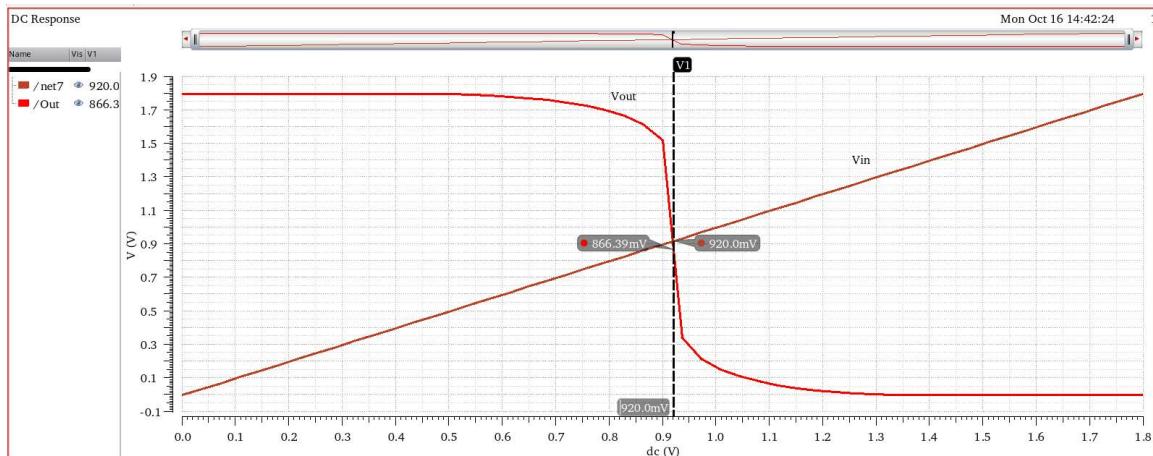
CREATING A NEW LIBRARY AND SCHEMATIC

- Go to File → New → Library and name the library → select “Attach to anexisting technology library” → OK → select “gdk180” → OK.
- Go to file → New→ cell view→ give cell name → enter OK.
- To access the components→ press “I” →component window open.

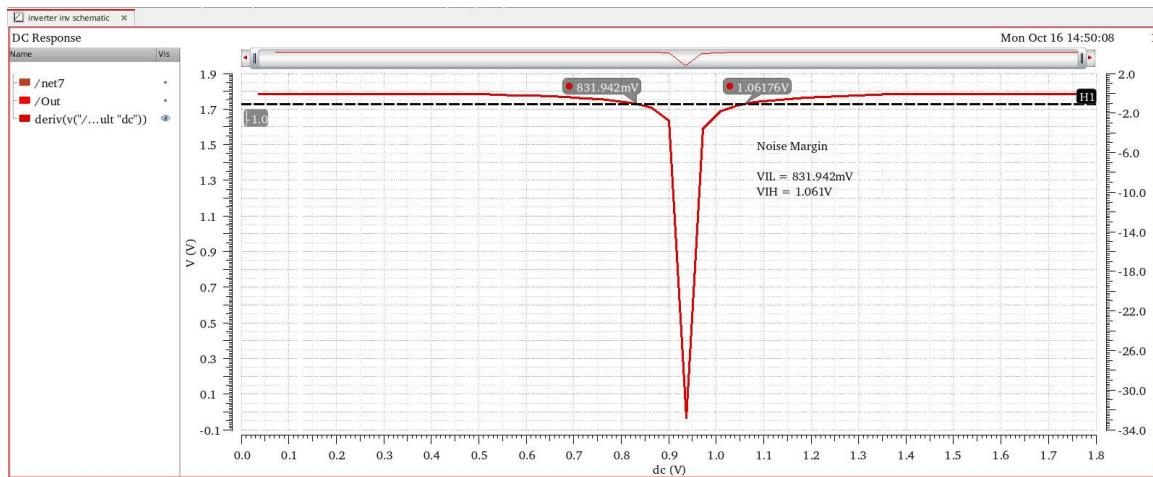
SYMMETRICAL INVERTER - SCHEMATIC:



VOLTAGE TRANSFER CHARACTERISTICS:



NOISE MARGIN:



- For NMOS AND PMOS → Select gpd़k180→ select nmos1v → press hide → place the component in virtuoso window → esc.
- For resistance → analog.lib → res→ press hide → place the component → esc.
- For supply voltages → analog.lib→ Vdc → press hide→ place component→ esc.
- Press “w” to connect the components using wires.
- Draw the schematic in virtuoso window and save the schematic.

PROCEDURE FOR SIMULATION :

Before beginning any simulation, setup The Simulation directory and modellibraries by following the steps;

- Launch → ADEL → Setup → Simulation directory → Click Ok.
- Go to Setup → Model libraries → Select the corresponding gpd़k180 file which is stat type and click Ok.

DC ANALYSIS :

- Launch → ADEL → Choose DC → Select, “Save DC operating point” → Component parameter → Select Component from schematic → Select input voltage source → Click Ok.
- Set start and stop values of voltage for analysis and click Ok.

Go to Output → To be plotted → Select from design → Select the output terminals → Go to Simulation → Netlist and Run.

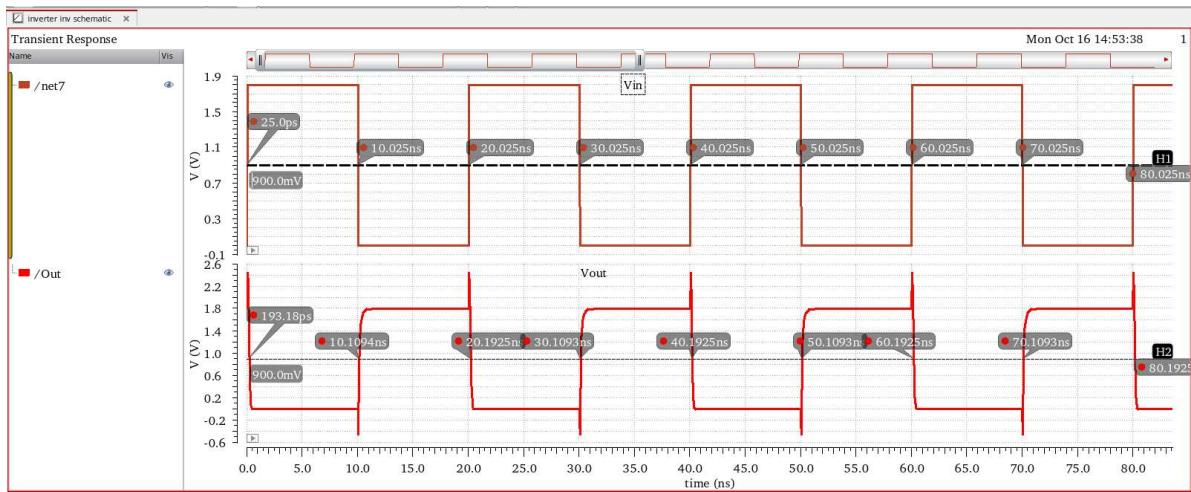
SYMMETRIC VTC (VOLTAGE TRANSFER CHARACTERISTICS):

The Switching threshold VM is defined as the point where Vin = Vout. Its value can be obtained graphically from the intersection of VTC with the line given by Vin=Vout.

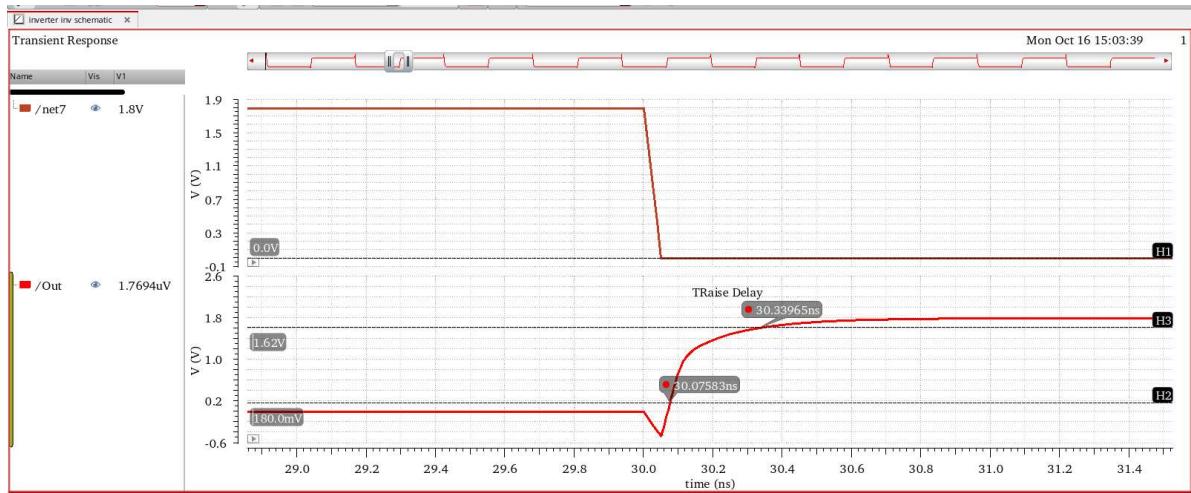
$$V_M = \frac{V_{th} + (V_{DD} + V_{tp})}{1 + r} \quad \text{with } r = \sqrt{Kp/Kn}$$

For symmetry VTC, VM is chosen as V_{DD}/2 |

PROPAGATION DELAY – SYMMETRICAL INVERTER:



RISE TIME:



NOISE MARGINS:

It is a measure of the sensitivity of a gate to noise is given by the noise margins NM_L (low) and NM_H (high) which quantize the size of the legal “0” and “1” and set a fixed maximum threshold on the noise value.

$$NML = VIL - VOL$$

$$NMH = VOH - VIH$$

PROPAGATION DELAY:

The propagation delay t_p of an inverter defines how quickly it response to a change at its inputs. It expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms

$$Tp = (t_{PHL} + t_{PLH}) / 2$$

DESIGN Calculation :

1. Symmetric VTC

$$\text{ii)} \quad V_m = \frac{V_{th} + r(V_{dd} + V_{tp})}{1+r}$$

$$\text{Here, } V_{th,n} = 485.208\text{m}$$

$$V_{th,p} = -456.952\text{m}$$

$$V_{DD} = 1.8\text{V}$$

$$V_m = \frac{V_{dd}}{2} = 0.9\text{V}$$

$$0.9 = \frac{485.208 + r(1.8 - 456.952)}{1+r}$$

$$r = 0.938$$

$$\text{iii)} \quad r = \sqrt{\frac{\mu p * Cox * \left(\frac{w}{l}\right)p}{\mu n * Cox * \left(\frac{w}{l}\right)n}}$$

$$r^2 = \frac{\mu p * Cox * \left(\frac{w}{l}\right)p}{\mu n * Cox * \left(\frac{w}{l}\right)n}$$

$$0.938^2 = \left(\frac{6.0028}{37.39}\right) \left(\frac{wp}{wn}\right)$$

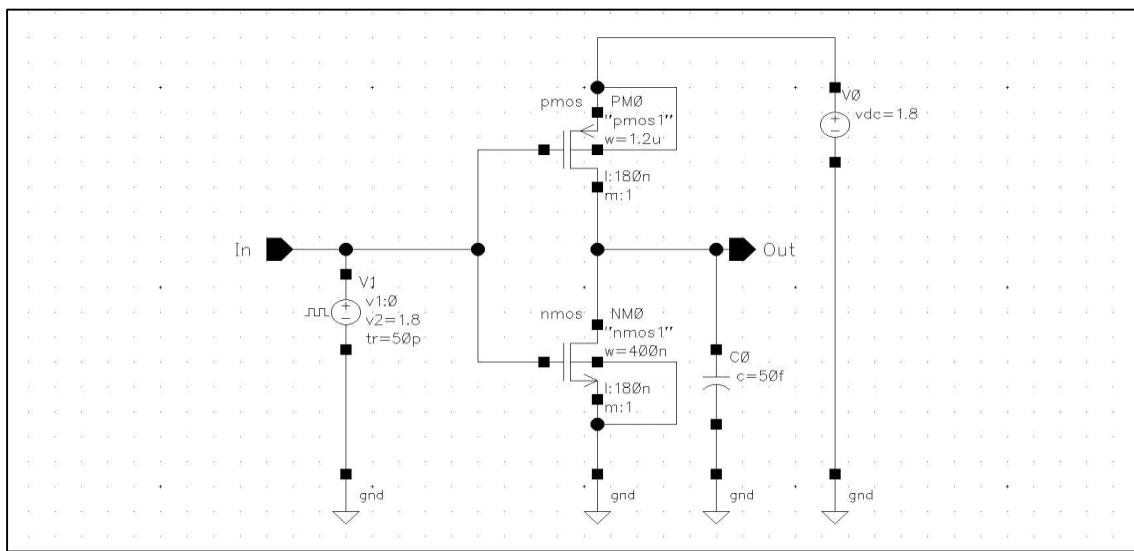
$$w_p = \frac{0.87}{10.83} * 2\text{um}$$

$$w_p = 10.83 \text{ um}$$

FALL TIME:



SCHEMATIC – SYMMETRICAL TRANSIENT RESPONSE:



Transient size

$$\left(\frac{w}{l}\right)_p = \left(\frac{10.8*10^{-6}}{1u}\right) \mu\text{m}$$

$$\left(\frac{w}{l}\right)_n = \left(\frac{2*10^{-6}}{1u}\right) \mu\text{m}$$

To calculate:

1) Noise margin:

$$N_{ML} = V_{IL} - V_{OL} = 0.831 - 0 = 0.831 \text{ V}$$

$$N_{MH} = V_{IH} - V_{OH} = 1.8 - 1.061 = 0.739 \text{ V}$$

2) Propagation delay:

$$t_{plh} = (30.109 - 30.025) \text{ ns} = 0.084 \text{ ns} = 84 \text{ ps}$$

$$t_{phl} = (20.192 - 20.025) \text{ ns} = 0.167 \text{ ns} = 167 \text{ ps}$$

$$t_p = \frac{tplh + tphl}{2} = \frac{(167+84)}{2} = 125.5$$

$$t_p = 125.5 \text{ ps}$$

3) Rise delay:

$$t_r = 30.339 \text{ ns} - 30.075 \text{ ns} = 0.264 \text{ ns}$$

$$t_r = 264 \text{ ps}$$

4) Fall delay

$$t_f = 20.291 \text{ ns} - 20.150 \text{ ns} = 0.141 \text{ ns}$$

$$t_f = 141 \text{ ps}$$

2. Symmetric transient response:

To find Req n,p from MOS 1V characteristics (from I_d and V_{ds} graph \ $V_{gs}=1.6 \text{ V}$)

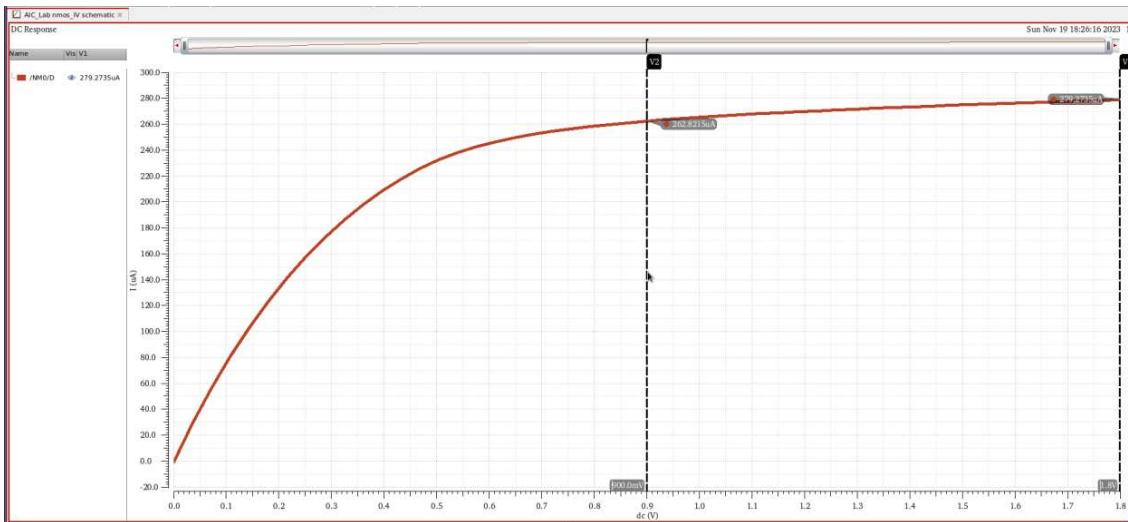
NMOS:

$$R_1 = \frac{Vdd}{\text{equivalent current}}$$

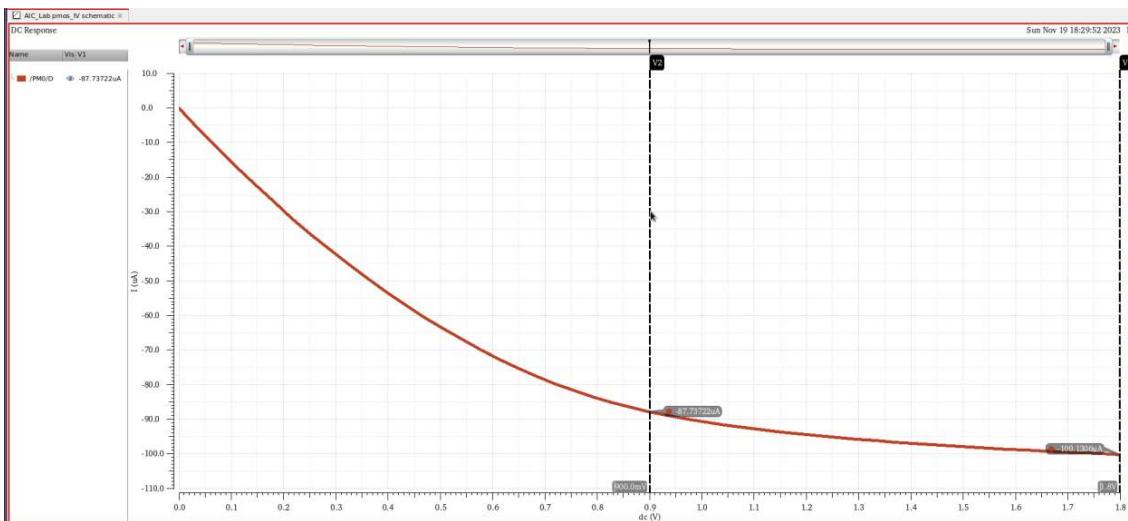
$$R_1 = \frac{1.8}{279.273*10^{-6}} = 6.44 \text{ k}\Omega$$

$$R_2 = \frac{0.9}{262.82*10^{-6}} = 3.42 \text{ k}\Omega$$

NMOS – Reqn:



PMOS – Reqn:



$$R_{eqn} = \frac{R1+R2}{2}$$

$$R_{eqn} = 4.93 \text{ k}\Omega$$

PMOS:

$$R_1 = \frac{Vdd}{\text{equivalent current}}$$

$$R_1 = \frac{1.8}{100.13 * 10^{-6}} = 17.9 \text{ k}\Omega$$

$$R_2 = \frac{0.9}{87.73 * 10^{-6}} = 10.2 \text{ k}\Omega$$

$$R_{eqp} = \frac{R1+R2}{2}$$

$$R_{eqp} = 14.05 \text{ k}\Omega$$

$$(w/l)_p = r (w/l)_n$$

$$w_p = \frac{14.05 k}{4.93 k} * 2u$$

$$w_p = 1.139 \mu\text{m}$$

With load capacitance ($C_L = 50\text{f}$)

1) Propagation delay:

$$t_{plh} = (30.219 - 30.025)\text{ns} = 0.194 \text{ ns} = 194 \text{ ps}$$

$$t_{phl} = (40.214 - 40.025)\text{ns} = 0.189 \text{ ns} = 189 \text{ ps}$$

$$t_p = \frac{tplh + tphl}{2} = \frac{194 + 189}{2} = 191.5 \text{ ps}$$

$$t_p = 191.5 \text{ ps}$$

2) Rise & Fall Delay:

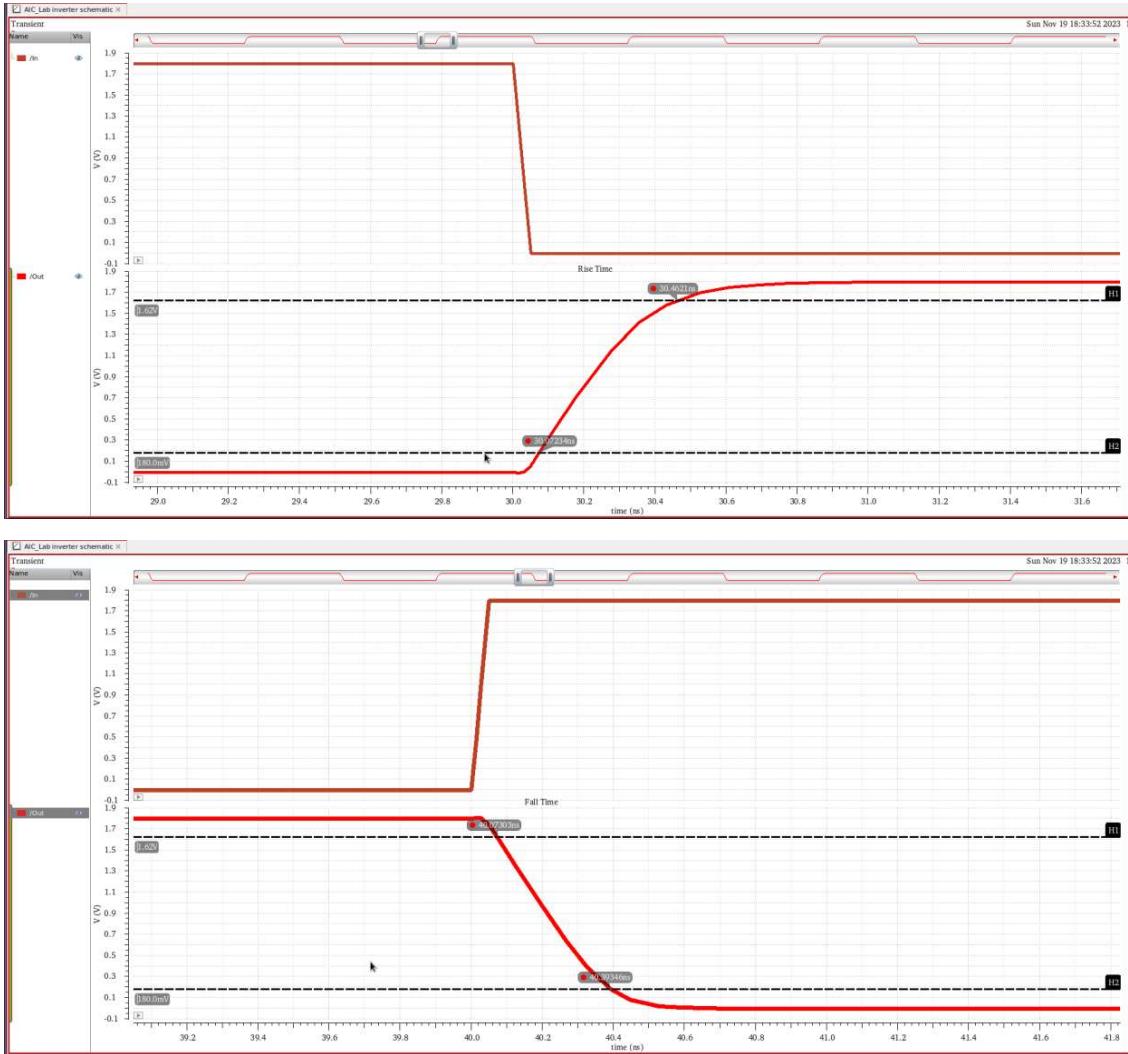
$$t_r = 30.462 \text{ ns} - 30.073 \text{ ns} = 0.389 \text{ ns}$$

$$t_r = 389 \text{ ps}$$

$$t_f = 40.393 \text{ ns} - 40.073 \text{ ns} = 0.32 \text{ ns}$$

$$t_f = 320 \text{ ps}$$

Symmetrical Transient Response – TRise, Tfall:



3. Minimum Propagation Delay:

$$(W/l)_p = \sqrt{r} * (W/l)_n$$

$$w_p = \sqrt{\frac{14.05 k}{4.93 k}} * 2u$$

$$w_p = 674 \text{ nm}$$

From Simulation,

- 1) Propagation delay:

$$t_{plh} = (30.051 - 30.025) \text{ ns} = 0.026 \text{ ns} = 26 \text{ ps}$$

$$t_{phl} = (40.041 - 40.025) \text{ ns} = 0.016 \text{ ns} = 16 \text{ ps}$$

$$t_p = \frac{tplh + tphl}{2} = \frac{26+16}{2} = 21 \text{ ps}$$

$$t_{p0} = 21 \text{ ps}$$

4. For Given $C_L = 50 \text{ fF}$, inverter delay $t_{p0} = t_p$ reference inverter.

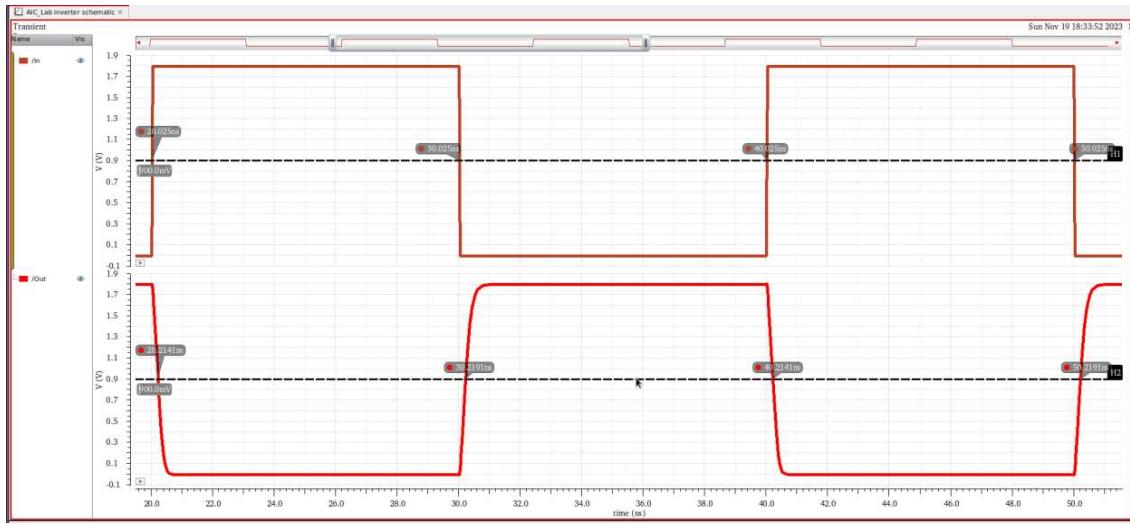
$$T_p = t_{p0} * (1 + (C_L / S C_{inv}))$$

$$C_{inv} = C_{dd} \text{ of nmos} + C_{dd} \text{ of pmos} = 19.5 \text{ fF} + 14.06 \text{ fF} = 33.56 \text{ fF}$$

$$S = 14 \rightarrow t_p = t_{p0}(1.106)$$

By choosing S value we can reduce propagation delay of the inverter for given load

Symmetrical Transient Response – Tpropagation:



Minimum Propagation Delay:



INFERENCE:

1. Inverter provides symmetrical Voltage Transfer characteristics (VTC).
2. High Noise Margins. Voh and Vol are VDD and GND respectively.
3. By scaling the transistor we will adjust rise and fall time of inverter output.
4. It has full rail-to-rail swing. The circuit gives large output swing and only dissipates significant power when the input is switched.
5. There is no static power consumption

RESULT:

Thus, the CMOS inverter circuit is simulated and its VTC and propagation delay is successfully calculated using cadence virtuoso.

Symmetrical VTC Switching Threshold VM = 0.92 V

Propagation Delay = 125.5 ps

Rise Delay = 264 ps

Fall Delay = 141 ps

Minimum Propagation Delay = 21 ps

Ex-No: 4	
DATE:	

DESIGN AND SIMULATION OF DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

AIM:

To simulate the Differential amplifier with active load circuit using Cadence and plot its transient response to calculate CMRR.

SOFTWARE TOOLS REQUIRED:

- Cadence with Linux OS

THEORY:

A differential amplifier is a circuit that has two voltage supplies, whose amplified difference is observed in the output terminal. It is a combination of two common source amplifiers connected in parallel.

Common mode: In this mode both the input voltages are made equal and are in phase with each other. The gain of this mode is given by

$$A_c = V_{out}/(V_1 + V_2)$$

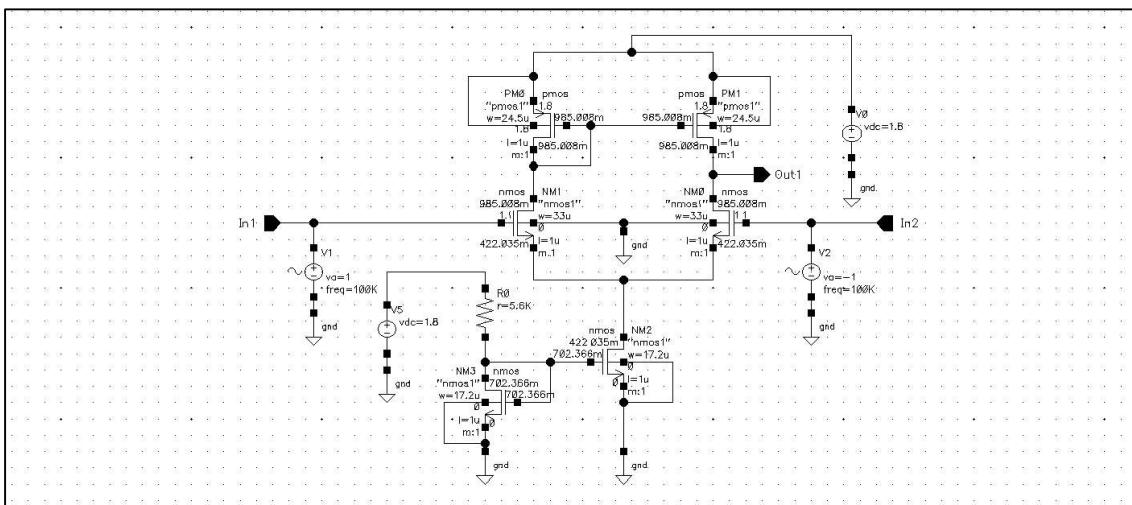
Differential mode: Two input signals will be different and out of phase with each other. The gain of Differential mode of operation is given by

$$A_d = V_{out}/(V_1 - V_2)$$

One of the major characteristics of differential amplifier is the Common Mode Rejection Ratio, which is abbreviated as CMRR. It is the ratio of Differential mode voltage gain to the Common mode voltage gain. The expression for CMRR is given by

$$CMRR = A_d/A_c$$

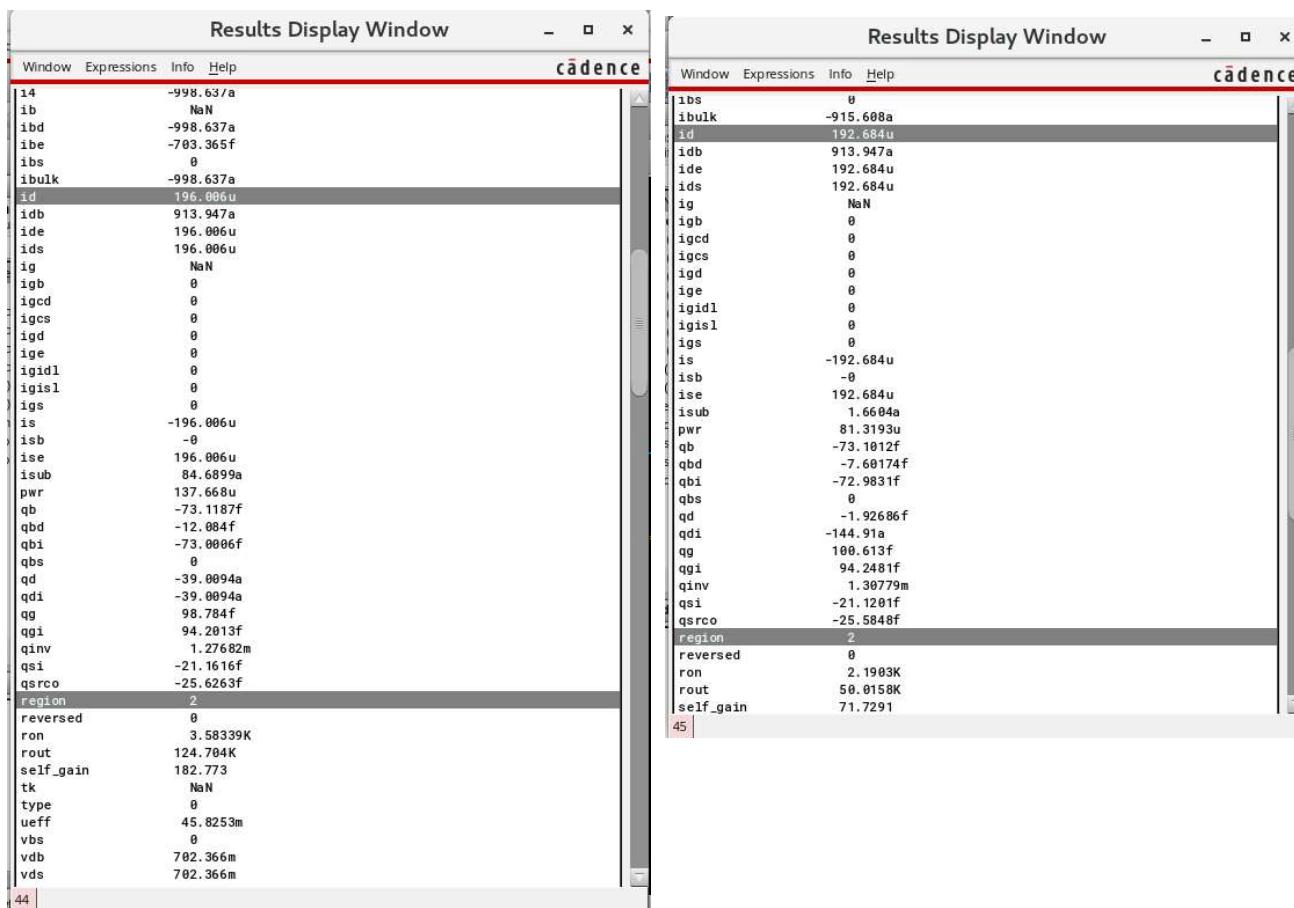
SCHEMATIC:



DC Operating Points:

NM3

NM2



PROCEDURE FOR SIMULATION:

Before beginning any simulation, setup The Simulation directory and model libraries by following the steps;

- Launch → ADEL → Setup → Simulation directory → Click Ok.
- Go to Setup → Model libraries → Select the corresponding gpdk file which is of NN type and click Ok.

TRANSIENT ANALYSIS:

- Launch → ADEL → Analysis → Choose Tran → Set stop time → Click Ok.
- Go to Outputs → To be plotted → Select from design → Select the output terminal → Click Ok.
- Go to Simulation → Netlist and Run to plot the corresponding output graph.

DC ANALYSIS

- Launch → ADEL → Choose DC → Select, "Save DC operating point" and Run.
- Results → Print → DC operating points.
- Select PMOS and NMOS to know its operating points.

AC ANALYSIS:

- Launch → ADEL → Choose AC → Component parameter → Select Component from schematic → Select input voltage source → Select frequency → Click Ok.
- Set start and stop values of frequency for analysis and click Ok.
- Go to Output → To be plotted → Select from design → Select the output terminals
 - → Go to Simulation → Netlist and Run.

NM0

Results Display Window	
Window	Expressions
14	-3.46188f
ib	NaN
ibd	-1.73295f
ibe	-1.4185p
ibs	-1.72893f
ibulk	-3.46188f
id	96.3419u
idb	1.72893f
ide	96.3419u
ids	96.3419u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	0
igisl	0
igs	0
is	-96.3419u
isb	1.72893f
ise	96.3419u
isub	4.01628a
pwr	54.2379u
qb	-168.838f
qbd	-31.0647f
qbi	-168.653f
qbs	-14.4971f
qd	-1.43862f
mdi	-35.4177a
qg	194.911f
qqi	185.049f
qinv	1.05182m
qsi	-16.3608f
qsrho	-24.6337f
region	2
reversed	0
ron	5.84349K
rout	179.149K
self_gain	230.561
tk	NaN
type	0
ueff	45.5378m
47	

NM1

Results Display Window	
Window	Expressions
1bs	-1.72893f
ibulk	-3.46188f
id	96.3419u
edb	1.72893f
ide	96.3419u
ids	96.3419u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	0
igisl	0
igs	0
is	-96.3419u
isb	1.72893f
ise	96.3419u
isub	4.01628a
pwr	54.2379u
qb	-168.838f
qbd	-31.0647f
qbi	-168.653f
qbs	-14.4971f
qd	-1.43862f
mdi	-35.4177a
qg	194.911f
qqi	185.049f
qinv	1.05182m
qsi	-16.3608f
qsrho	-24.6337f
region	2
reversed	0
ron	5.84349K
rout	179.149K
self_gain	230.561
46	

PM0

Results Display Window	
Window	Expressions
1bs	-0
ibulk	63.07f
id	-96.3429u
edb	63.0382f
ide	-96.3429u
ids	-96.3429u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	-0
igisl	-0
igs	0
is	96.3429u
isb	-0
ise	-96.3429u
isub	-31.7262a
pwr	78.5187u
qb	-112.877f
qbd	23.2176f
qbi	112.671f
qbs	-0
qd	-73.9167a
mdi	73.9167a
qg	168.3f
qqi	161.513f
qinv	462.18u
qsi	48.7682f
qsrho	42.1871f
region	2
reversed	0
ron	8.45929K
rout	280.292K
self_gain	134.331
48	

PM1

Results Display Window	
Window	Expressions
1bs	-0
ibulk	63.07f
id	-96.3429u
edb	63.0382f
ide	-96.3429u
ids	-96.3429u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	-0
igisl	-0
igs	0
is	96.3429u
isb	-0
ise	-96.3429u
isub	-31.7262a
pwr	78.5187u
qb	-112.877f
qbd	23.2176f
qbi	112.671f
qbs	-0
qd	-73.9167a
mdi	73.9167a
qg	168.3f
qqi	161.513f
qinv	462.18u
qsi	48.7682f
qsrho	42.1871f
region	2
reversed	0
ron	8.45929K
rout	280.292K
self_gain	134.331
49	

Calculations:

Find R_d to provide $I_d = 200\mu A$

$$V_{ov} = V_{gs} - V_{th} = 0.2, V_{thn} = 0.485V, V_{gs} = 0.685V$$

$$R_d = 5.6Kohm$$

Find V_{in1} and V_{in2} min and max limits;

$$V_{in, Dc} = V_{gs, m1} + V_{ds, m5}$$

$$V_{in, Dc} = 0.88V$$

$$V_{in, Dc, Max} \rightarrow V_{ds} \geq V_{gs} - V_t$$

$$V_{g1} \leq V_{d1} + V_t$$

$$V_{g1} = 1.58V$$

Overdrive Voltage: $V_{ov} = V_{sg} - V_{tp}, V_{tp} = 0.5V, V_{sg} = 0.7V$

$$V_{D, m1} = V_{out, max} = V_{dd} - V_{gs, m4} = 1.8 - 0.7,$$

$$V_{D, m1} = 1.1V$$

 V_{in} -Range (Dc)

$$V_{in, Dc, Min} \leq V_{in} \leq V_{in, Dc, Max},$$

$$0.88V \leq V_{in} \leq 1.58V$$

Find w/l of 5 and 6 to provide 200uA current

$$I_d = \frac{1}{2} k n' \left(\frac{w}{l} \right) (V_{gs} - V_{th})^2$$

$$\left(\frac{w}{l} \right) 5 = 17.24\mu, l = 1\mu m \quad \left(\frac{w}{l} \right) 6 = 17.24\mu, l = 1\mu m$$

Current across each MOSFET.

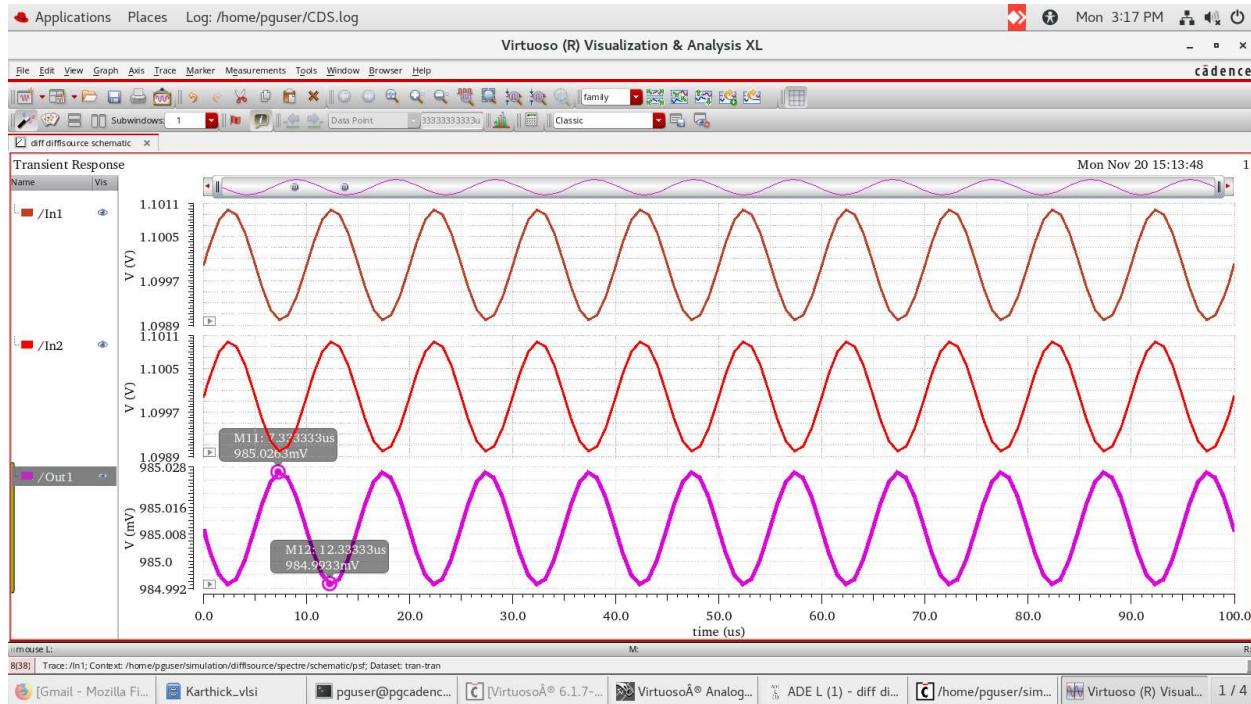
$$I_{d1,2} = 96.341A,$$

$$I_{d3,4} = -96.342A,$$

$$I_{d5} = 192.684A,$$

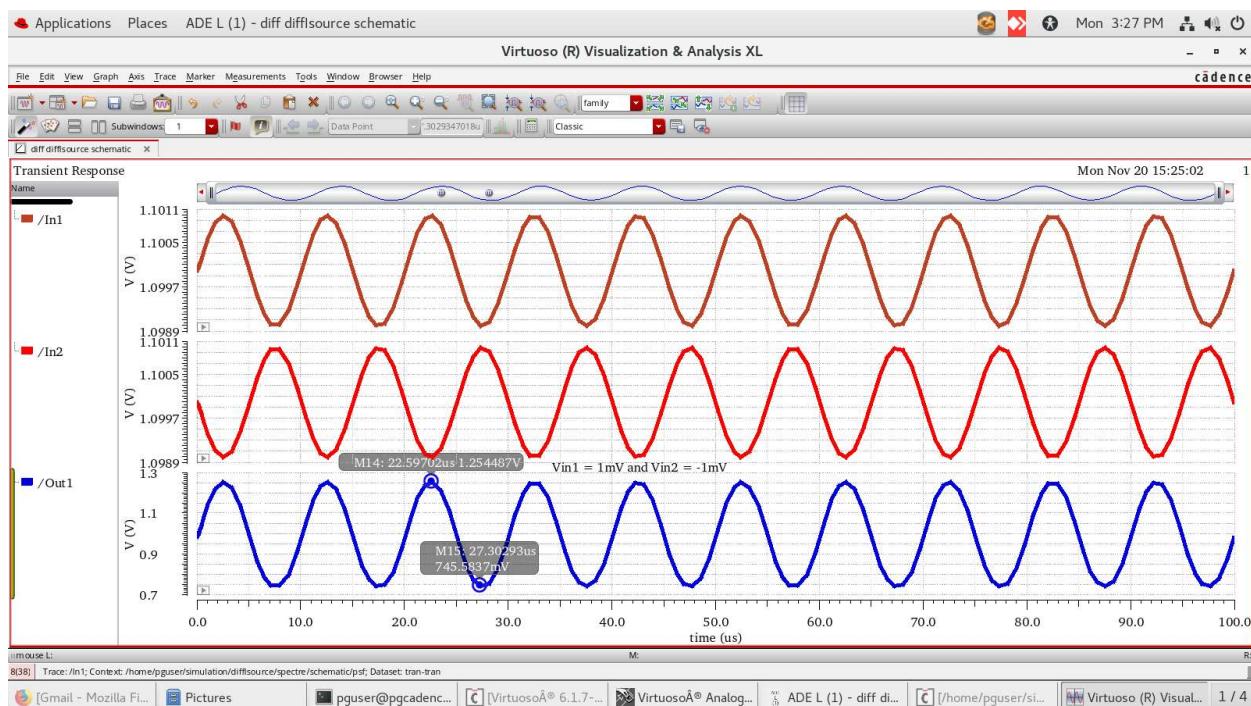
$$I_{d6} = 196.006A$$

Transient Analysis – Common Mode Gain:



Transient Analysis – Differential Mode Gain:

Differential Mode Gain:



$$Ad = \frac{\nabla V_{out}}{V_{in1} - V_{in2}}$$

$$Ad = \frac{1.254 - 0.7455}{2m},$$

$$Ad = 254.25$$

$$Ad \text{ in } db = 20 \log(254.25) = 48.10db$$

Common Mode Gain:

$$Ac = \frac{V_{out}}{\frac{V_{in1} + V_{in2}}{2}}$$

$$Ac = 0.033$$

$$Ac \text{ in } db = 20 \log(0.033)$$

$$Ac, db = -29.62db$$

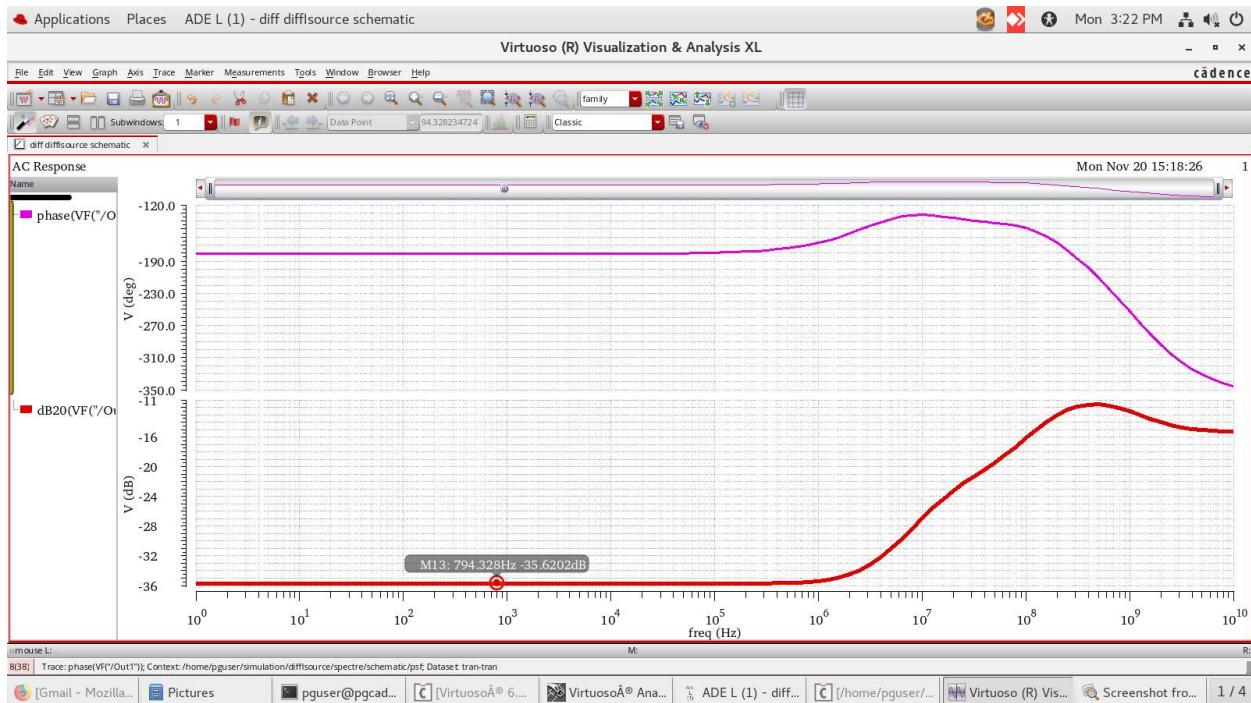
CMRR(Common Mode Rejection Range):

$$CMRR = \frac{Ad}{Ac},$$

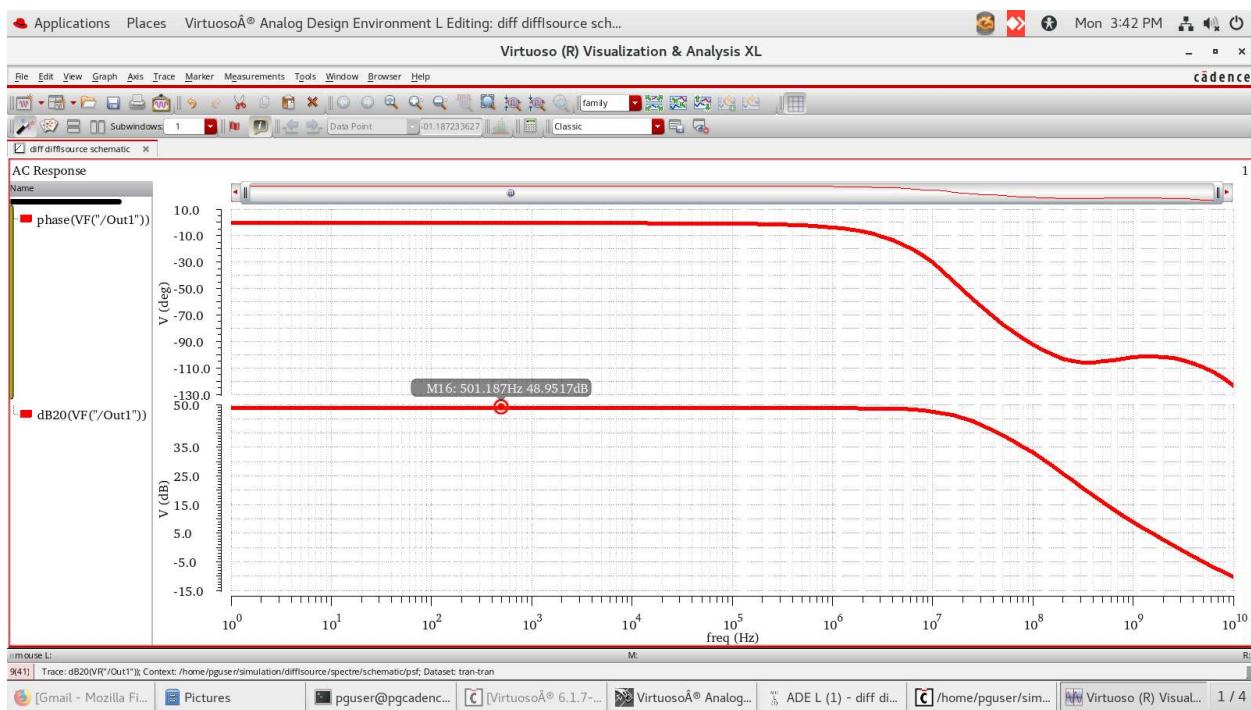
$$CMRR = 7704,$$

$$CMRR, db = 20 \log(7704) = 77.73db$$

AC Analysis – Common Mode Gain:



AC Analysis – Differential Mode Gain:



INFERENCE:

1. Differential amplifier is a versatile and fundamental component in electronic system.
2. Differential amplifiers are thereby able to reduce noise that is common to both inputs, only amplifying the differential signal that we are interested in.
3. we can quantify the differential mode versus common-mode gain in a quantity called the common-mode rejection Ratio (CMRR). High CMRR indicates better rejection of unwanted noise or interference.
4. The ideal differential amplifier should have high gain for differential signals and low gain for common-mode signals.

Result:

Thus, the differential amplifier circuit was simulated its transient and ac plots for common mode, differential mode response was successfully plotted using cadence.

1. Differential mode voltage gain = 254.25
2. Common mode voltage gain = 0.03
3. CMRR = 77.73 dB

Ex-No: 5	STUDY OF CHARACTERISTICS OF TWO STAGE OPAMP WITH AND WITHOUT COMPENSATION
DATE:	

AIM:

To study the characteristics of two stage operational amplifier with and without compensation..

SOFTWARE REQUIRED:

- Cadence software

THEORY:

An two stage operational amplifier generally consists of two stages, namely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain. Two-stage operational amplifiers are the most common used multistage amplifier because it can provide high gain and high output swing.

$$I_d = \frac{1}{2} k_n \left(\frac{w}{l} \right) (V_{g-V_{tn}})^2$$

Gain combining the two stages

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_1} * \frac{V_1}{V_{in}}$$

for this two stage amplifier we have the DC gain of the amplifier

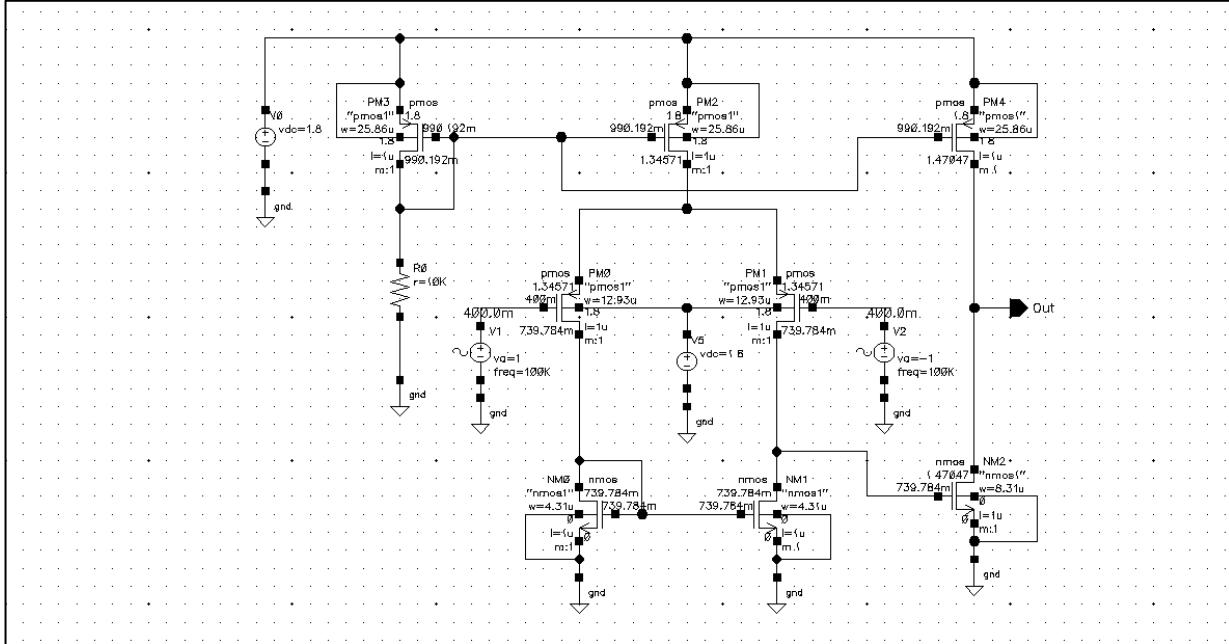
$$A_{dc} = g_m R_1 \times g_m R_2$$

PROCEDURE:-

- Create a folder in desktop → Right click on the folder → Select open interterminal window.
- In the terminal window, enter the following commands to invoke C;
- Type => \$ csh and press enter.
- Type => \$ source /home/install/cshrc and Press Enter key
- Type, “Virtuoso” and press Enter to open the virtuoso window.

SCHEMATIC:

Without compensation:



DC Analysis:

M1 operating values:

gbs	0
gds	2.65047u
gm	241.135u
gmb	69.1559u
gbms	69.1559u
gmoverid	4.96811
i1	-48.5365u
i3	48.5365u
i4	67.9677f
ib	NaN
ibd	33.9885f
ibe	1.58247p
ibs	33.9792f
ibulk	67.9677f
id	-48.5365u
idb	33.9792f
ide	-48.5365u
ids	-48.5365u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	-0
igisl	-0
igs	0
is	48.5365u
isb	33.9792f
ise	-48.5365u
isub	-9.25692a
pwr	29.4096u
qb	-73.0349f
qbd	15.5532f
qbi	72.681f
qbs	7.27853f
qd	-1.53433f
mdi	87.852a
qg	104.187f
qqi	98.3612f
qinv	231.625u
qsi	25.5923f
qsrco	21.5665f
region	2
reversed	0
ron	12.4839K
rout	377.292K
self_main	98.9781

M2 operating values:

gbd	4.32054n
gbs	4.86664p
gds	2.29458u
gm	639.566u
gmb	192.38u
gbms	192.38u
gmoverid	6.76412
i1	94.5533u
i3	-94.5528u
i4	-488.881p
ib	NaN
ibd	-488.88p
ibe	-498.351p
ibs	-62.8357a
ibulk	-488.881p
id	94.5533u
idb	455.388a
ide	94.5533u
ids	94.5528u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	0
igisl	0
igs	0
is	-94.5528u
isb	62.8357a
ise	94.5533u
isub	488.88p
pwr	139.638u
qb	-39.241f
qbd	-11.2645f
qbi	-39.1166f
qbs	-149.229z
qd	2.23715f
mdi	-4.83706a
qg	58.9099f
qqi	58.7576f
qinv	535.885u
qsi	-11.6369f
qsrco	-13.906f
region	2
reversed	0
ron	15.5518K
rout	435.61K

- Click on the following to create a new library:-
 - File -> New -> Library
 - Name is given to the library
 - In the technology file section “ Attach to an existing technology library” is selected.
 - “gdk180” is selected.
- Click on the following to create a cellview:-
 - File -> New -> Cellview
 - Name is given to the cellview.
 - Library created in the previous step is selected.

Two-stage Opamp:-

- Select the option “Create instance” to place the components to form a circuit.
- NMOS and PMOS is selected from “gdk180” i.e “nmos1v” and “pmos1v”.
- Vdc , Idc,, cap,Vsin are selected from “analoglib”library.
- Circuit is created by connecting the components as shown in the circuit diagram.
- Vdd is given 1.8V,Idc = 20uA, Vsin1 = 1V, Vsin2= 1V and Phase for Vsin1= 180degreeand Vsin2= 0 degree.
- Frequency is set to 1KHz.

Simulation Setup:-

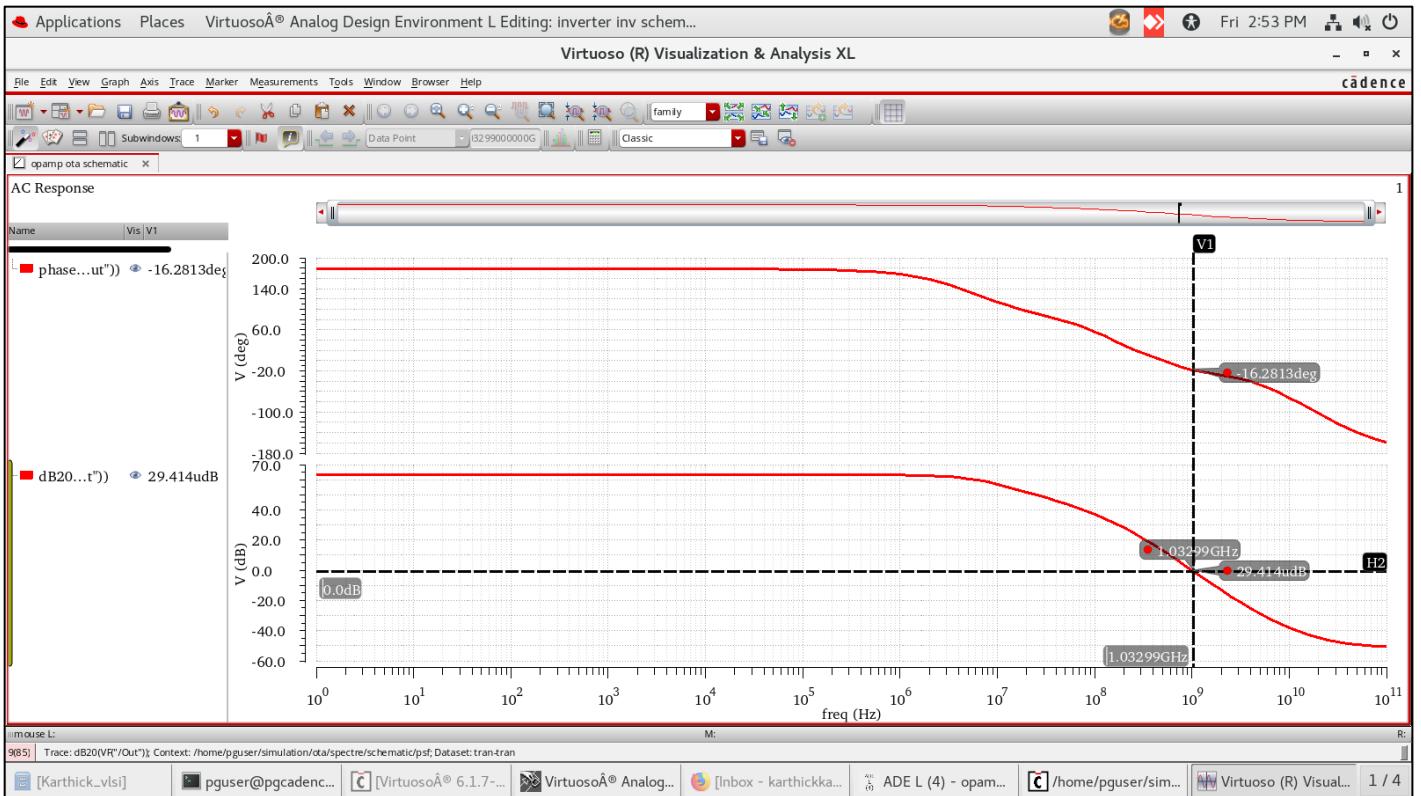
- Click on the following to do the simulation setup:-
- Launch -> ADE L -> Setup -> Simulation directory -> click ok
- Setup -> model libraries -> Select the corresponding gdk file which is of starttype (NN) .

AC Analysis:-

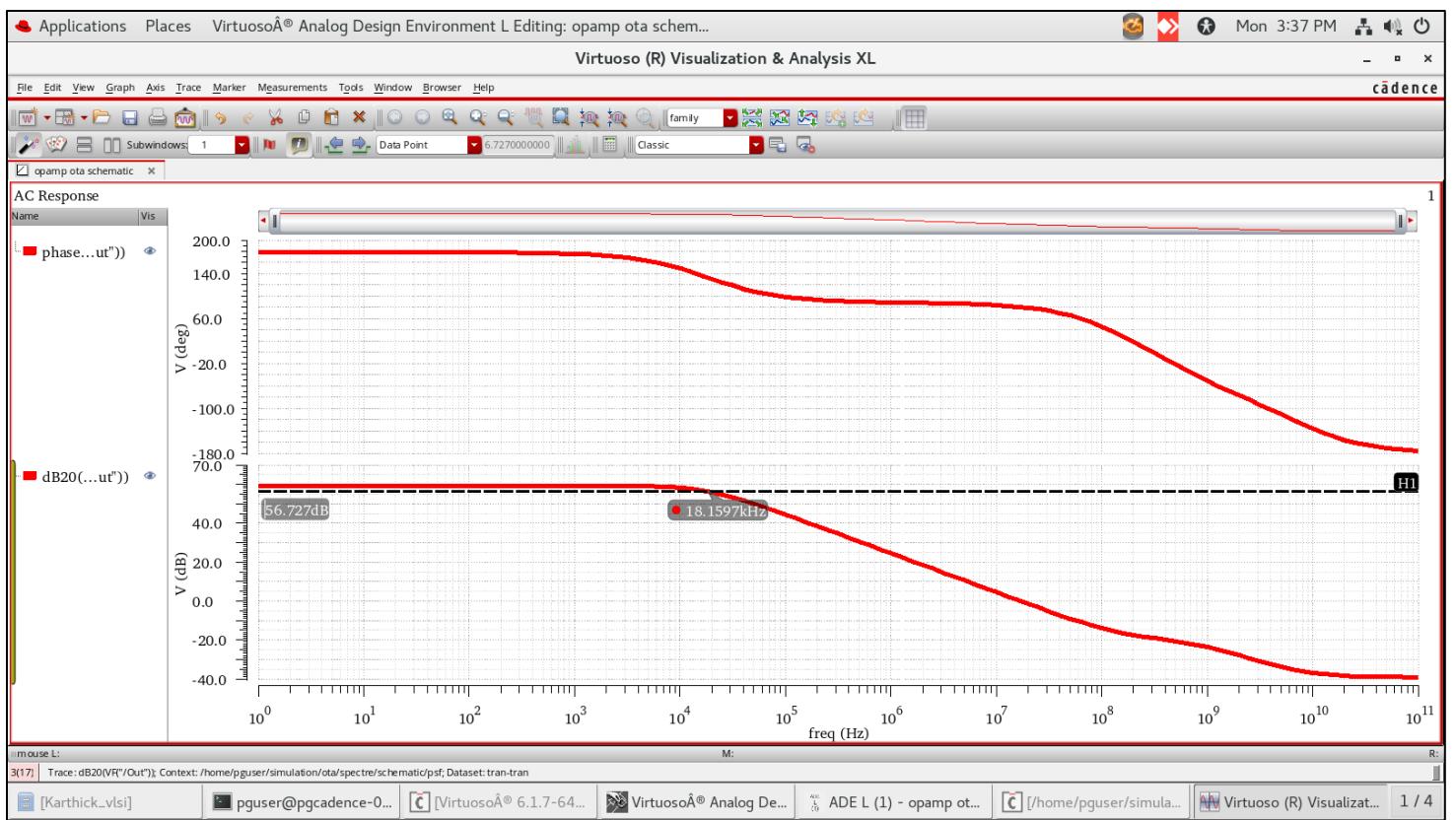
- Click on the following to do AC analysis:-
- Launch -> ADE L -> Analog Design Environment
- Analyses -> Analysis ="ac"
- Sweep variable -> Frequency -> Sweep range -> start 10 and stop 100 GHz
- Sweep type -> Logarithmic -> set points per decade =10-> click ok
- Outputs -> to be plotted -> Select on design -> Select the output terminal -> clickok
- Simulation -> Netlist and Run -> output gets plotted i.e a graph of AC analysis ofthe NMOS.
- Results -> AC magnitude and Phase -> To obtain the graph of magnitude and plot

OUTPUT RESULTS:

AC ANALYSIS:



3dB FREQUENCY:



CALCULATIONS:

FOR PMOS:

$$I_d = \frac{1}{2} k_p \left(\frac{W}{L}\right) (V_{gs} - V_{tp})^2$$

FOR NMOS:

$$I_d = \frac{1}{2} k_n \left(\frac{W}{L}\right) (V_{gs} - V_{tn})^2$$

ASPECT RATIO:

Width of transistors are calculated below:

$$\left(\frac{W}{L}\right)_{1-2} = \frac{2 * I_d}{k_p * (V_{gs} - V_{tp})^2} = \frac{2 * 50 * 10^{-6}}{193.33 * 10^{-6} * (0.2)^2}$$

$$\left(\frac{W}{L}\right)_{1-2} = 12.931/1$$

$$\left(\frac{W}{L}\right)_{3-4} = \frac{2 * I_d}{k_n * (V_{gs} - V_{tn})^2} = \frac{2 * 50 * 10^{-6}}{530 * 10^{-6} * (0.2)^2}$$

$$\left(\frac{W}{L}\right)_{3-4} = 4.31/1$$

$$\left(\frac{W}{L}\right)_{5,6,7} = \frac{2 * I_d}{k_p * (V_{gs} - V_{tp})^2} = \frac{2 * 100 * 10^{-6}}{193.33 * 10^{-6} * (0.2)^2}$$

$$\left(\frac{W}{L}\right)_{5,6,7} = 25.86/1$$

$$2 * \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4}$$

$$2 * \frac{25.86}{25.86} = \frac{\left(\frac{W}{L}\right)_6}{4.31}$$

$$\left(\frac{W}{L}\right)_6 = 8.62/1$$

ICMR Range:

$$-V_{ss} + V_{ov3} + V_{th} - |V_{tp}| \leq V_{ICM} \leq V_{dd} - |V_{tp}| - |V_{ov1}| - |V_{0v5}|$$

$$V_{th} = 0.48V, V_{ov1-8} = 0.2V, |V_{tp}| = 0.51V, V_{dd} = 1.8V, V_{ss} = 0V$$

$$0.17V \leq V_{ICMR} \leq 0.89V$$

THEORETICAL GAIN:

$$|Av| = gm1(ro2||ro4) \times gm6(ro6||ro7)$$

$$|Av| = 1485.26 \frac{v}{v}$$

$$20 \log |Av| = 20 \log(1485.26)$$

$$|Av| = 63.43 db$$

AC ANALYSIS:

From Graph

$$3 db gain = 60.73db$$

$$3 db frequency = 5.573MHz$$

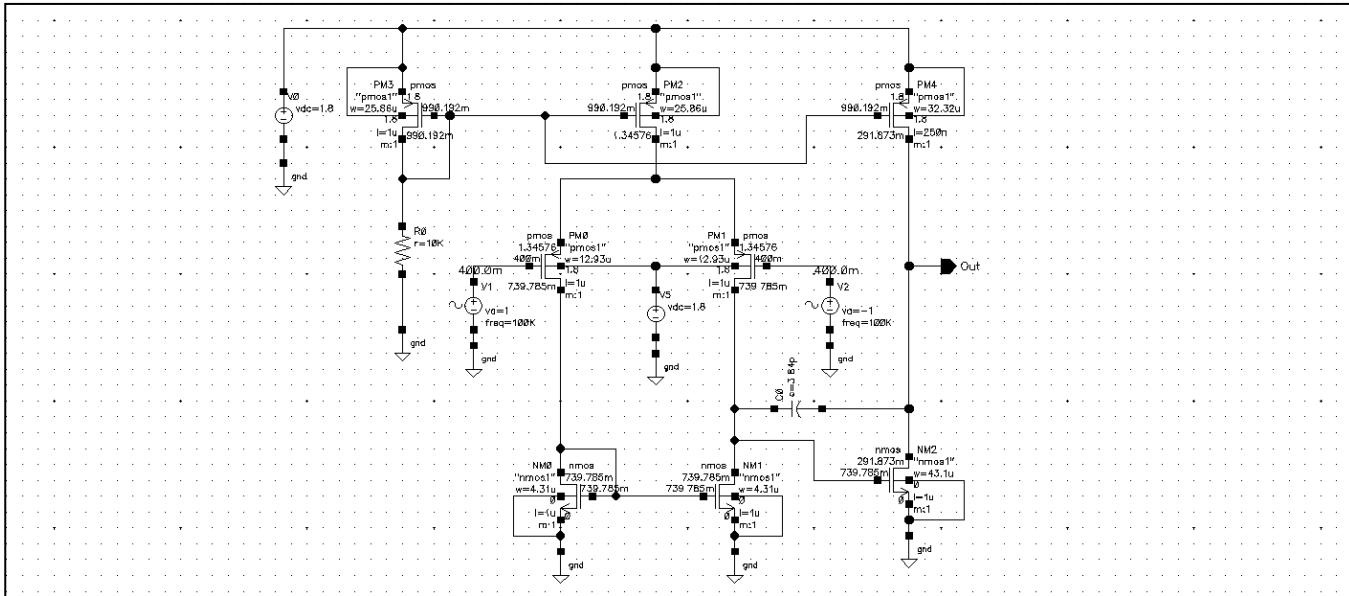
PHASE MARGIN:

$$Phase Margin(\phi_m) = 180 - \phi$$

$$\phi = 196.281deg$$

$$\phi_m = -16.281deg$$

SCHEMATIC: With compensation:



DC Analysis:

M1 operating values:

M2 operating values:

gbd	18.002a
gbs	0
gds	344.062u
gm	3.68396m
gmb	1.08086m
gmb5	1.08086m
gmoverid	6.10462
i1	603.471u
i3	-603.471u
i4	-2.25149f
ib	NaN
ibd	-2.25149f
ibe	-294.125f
ibs	0
ibulk	-2.25149f
id	603.471u
idb	2.24991f
ide	603.471u
ids	603.471u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	0
igisl	0
igs	0
is	-603.471u
isb	-0
ise	603.471u
isub	1.58089a
pwr	176.137u
qb	-186.326f
qbd	-13.3987f
qbi	-186.201f
qbs	0
qd	-8.73811f
mdi	-1.59857f
qg	268.478f
qgi	249.422f
qinv	4.1136m
qsi	-61.6221f
qsco	-73.414f
region	2
reversed	0
ron	483.658
rout	2.98645K
self main	10.7073

gbd	30.9861a
gbs	0
gds	2.65122u
gm	241.169u
gmb	69.1676u
gmbs	69.1676u
gmoverid	4.96725
i1	-48.5519u
i3	48.5519u
i4	67.9677f
ib	NaN
ibd	33.9885f
ibe	1.58242p
ibs	33.9792f
ibulk	67.9677f
id	-48.5519u
ldb	33.9792f
ide	-48.5519u
ids	-48.5519u
ig	NaN
igb	0
igcd	0
igcs	0
igd	0
ige	0
igidl	-0
igisl	-0
igs	0
is	48.5519u
isb	33.9792f
ise	-48.5519u
isub	-9.25989a
pwr	29.4212u
qb	-73.0345f
qbd	15.5532f
qbi	72.6806f
qbs	7.2778f
qd	-1.53435f
qdi	87.8632a
qg	184.192f
qgi	98.3653f
qinv	231.664u
qsi	25.5968f
qsro	21.5708f
region	2
reversed	0
ron	12.481K
rout	377.185K
self_gain	90.9653
+	NaN

DESIGN CALCULATIONS:

Aspect ratio of transistor are choosen from the without compensation technique.

$$\left(\frac{w}{l}\right)1-2 = 12.931/1$$

$$\left(\frac{w}{l}\right)3-4 = 4.31/1$$

$$\left(\frac{w}{l}\right)5-8 = 25.86/1$$

For the compensation technique ,the below conditions have to be satisfied,

$$\frac{GM1}{CC} < \frac{GM2}{C1}$$

so the current in stage 2 is increased, as the GM 2 also increased by this way.

$$\begin{aligned}\left(\frac{w}{l}\right)6 &= \frac{2*Id}{k_n * (V_{gs} - V_{tp})_2} \\ &= \frac{2*500*10^{-6}}{580 * 10^{-6} * (0.2)_2}\end{aligned}$$

$$\left(\frac{w}{l}\right)6 = 43.104/1$$

$$\begin{aligned}\left(\frac{w}{l}\right)7 &= \frac{2*Id}{k_p * (V_{gs} - V_{tp})_2} \\ &= \frac{2*500*10^{-6}}{193.33 * 10^{-6} * (0.2)_2} \\ \left(\frac{w}{l}\right)7 &= 33.324/0.25\end{aligned}$$

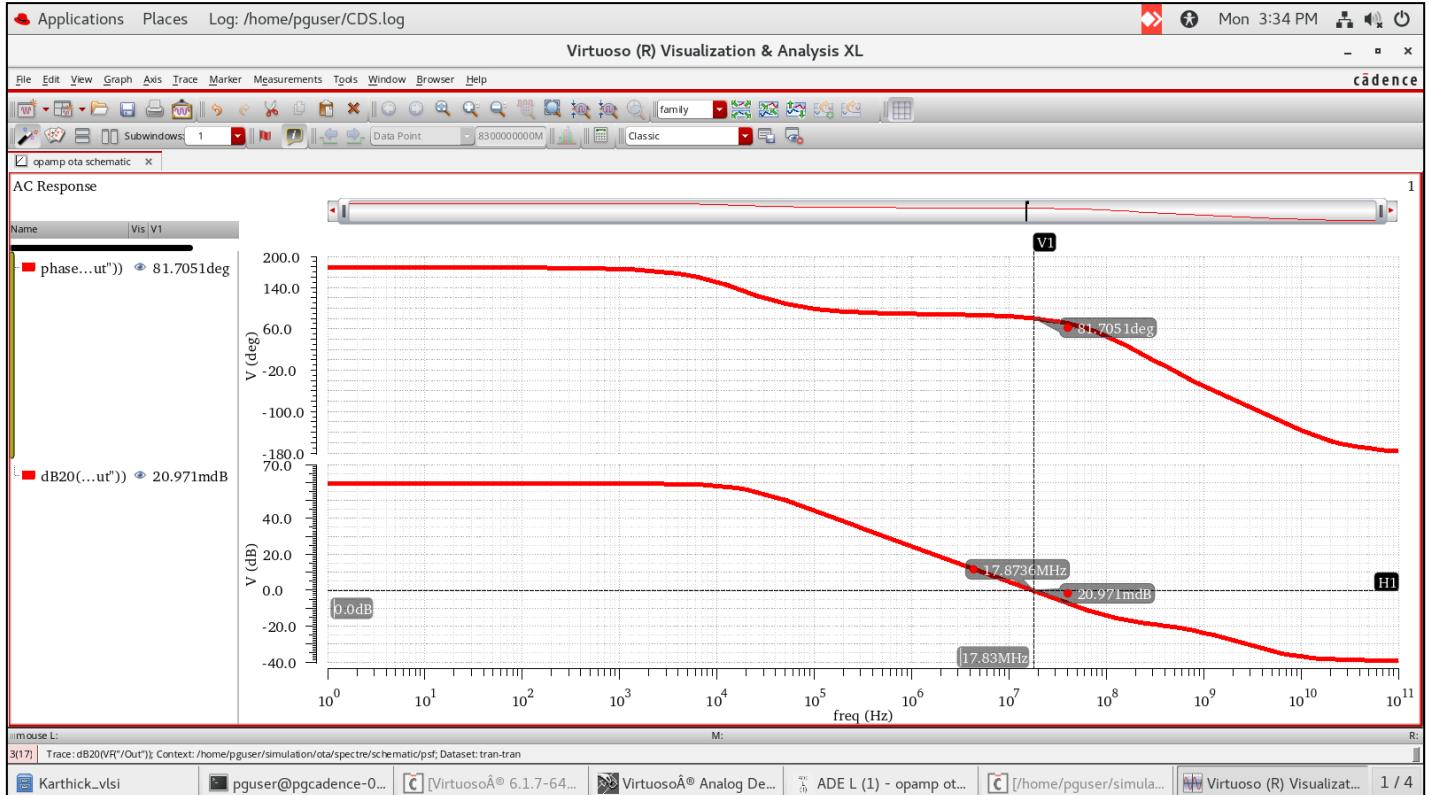
CAPACITOR VALUE

$$Cc = Gm1 / (2\pi f t)$$

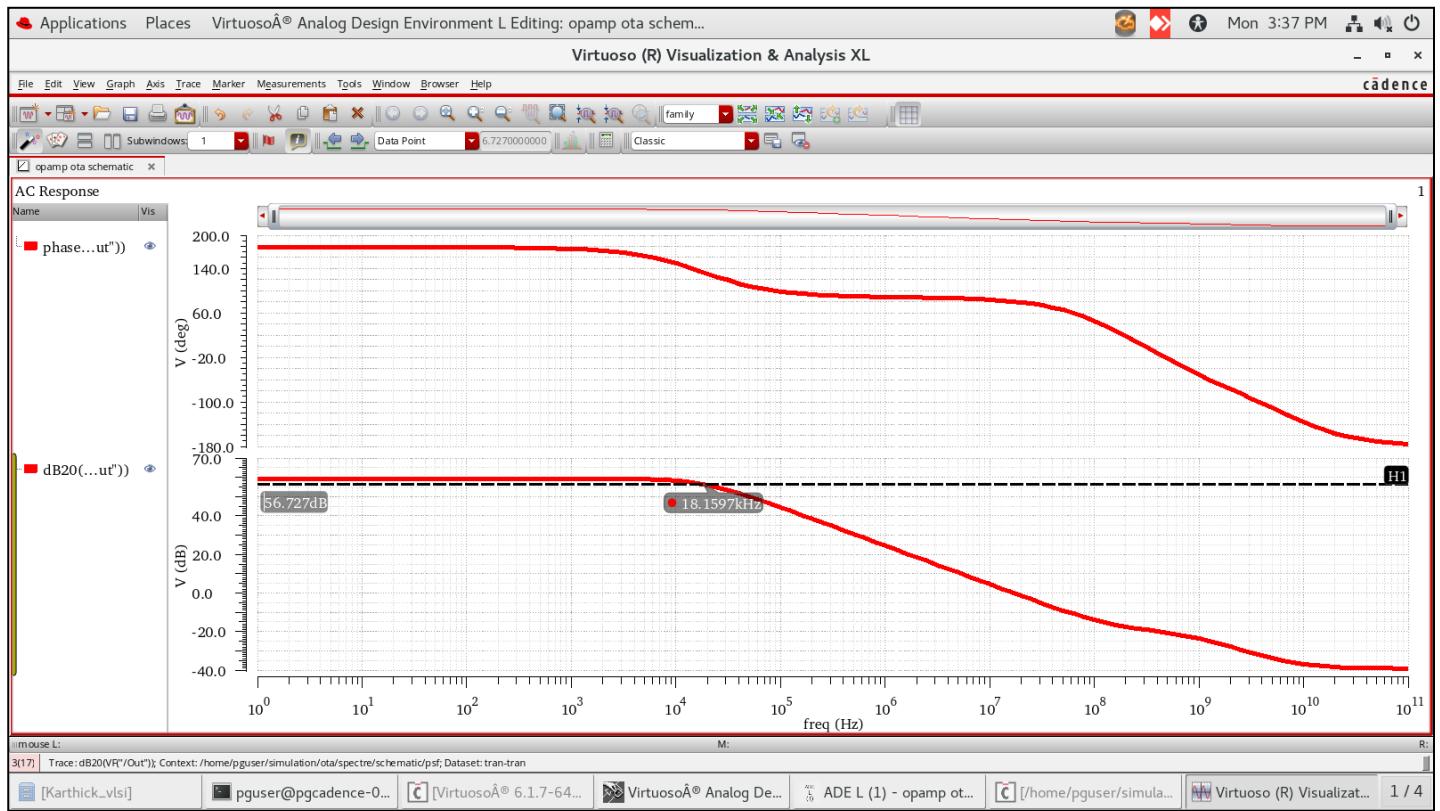
$$Gm1 = gm1 = 241.165 \mu m/v^2$$

$$ft = 10 MHz, Cc = 3.84 pF$$

OUTPUT RESULTS: AC Analysis



3db Frequency:



THEORITICAL GAIN:

$$|Av| = gm1(ro2||ro4) \times gm6(ro6||ro7)$$

$$|Av| = 782.78 \frac{v}{v} ,$$

$$Av, dB = 57.87 dB$$

$$3 db frequency = 18.159 KHz$$

PHASE MARGIN:

$$Phase Margin(\phi_m) = 180 - \phi$$

$$\phi = 98.295 deg$$

$$\phi_m = 81.705 deg$$

INFERENCE:

- Two-stage operational amplifiers are the most common used multistage amplifier because it can provide high gain and high output swing.
- However, an uncompensated two-stage operational amplifier has a two-pole transfer function, and these are located below the unity gain frequency.
- Gain compensation refers to simply reducing the gain by adjusting feedback resistor values.
- By bringing down the gain, the frequency limit where the onset of instability would occur is increased, and one would more stable operation of the circuit even with lower gain.

RESULT:

Thus, the stability analysis of two stage Operational amplifier with and without Compensation is performed and the corresponding phase margin are observed.

Ex-No: 6	LAYOUT DESIGN OF CMOS INVERTER
DATE:	

AIM:

To simulate the Layout of CMOS Inverter perform Design Rules Check (DRC), Layout vs Schematic check (LVS) and extract resistance and capacitance values.

SOFTWARE REQUIRED:

- Cadence software with linux OS.

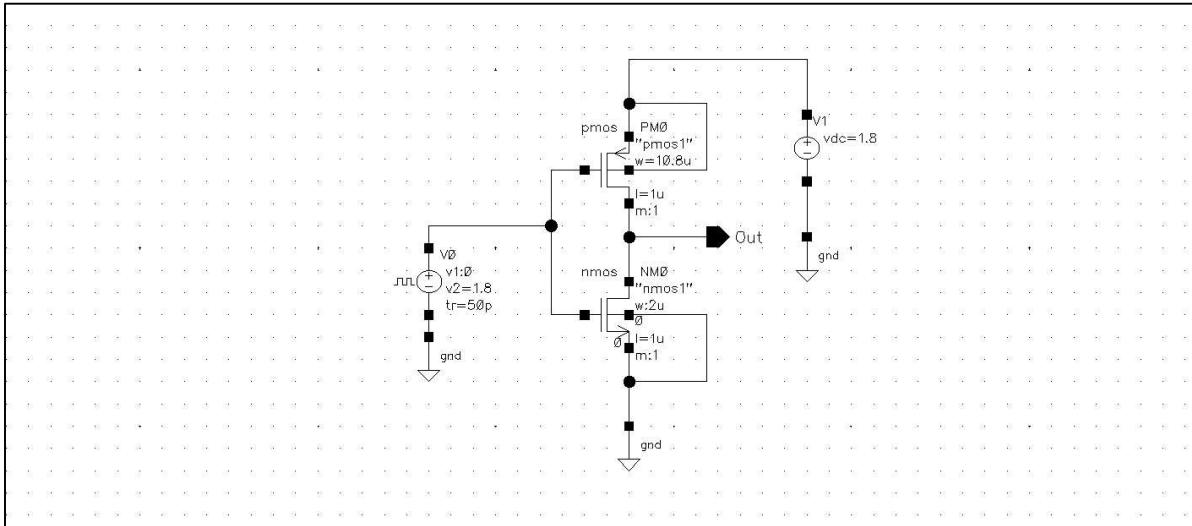
THEORY:

The layout of an integrated circuit defines the geometries that appear on the masks used in fabrication, the geometries include n-well, active, polysilicon, n+ and p+ implants, interlayer contact windows, and metal layers.

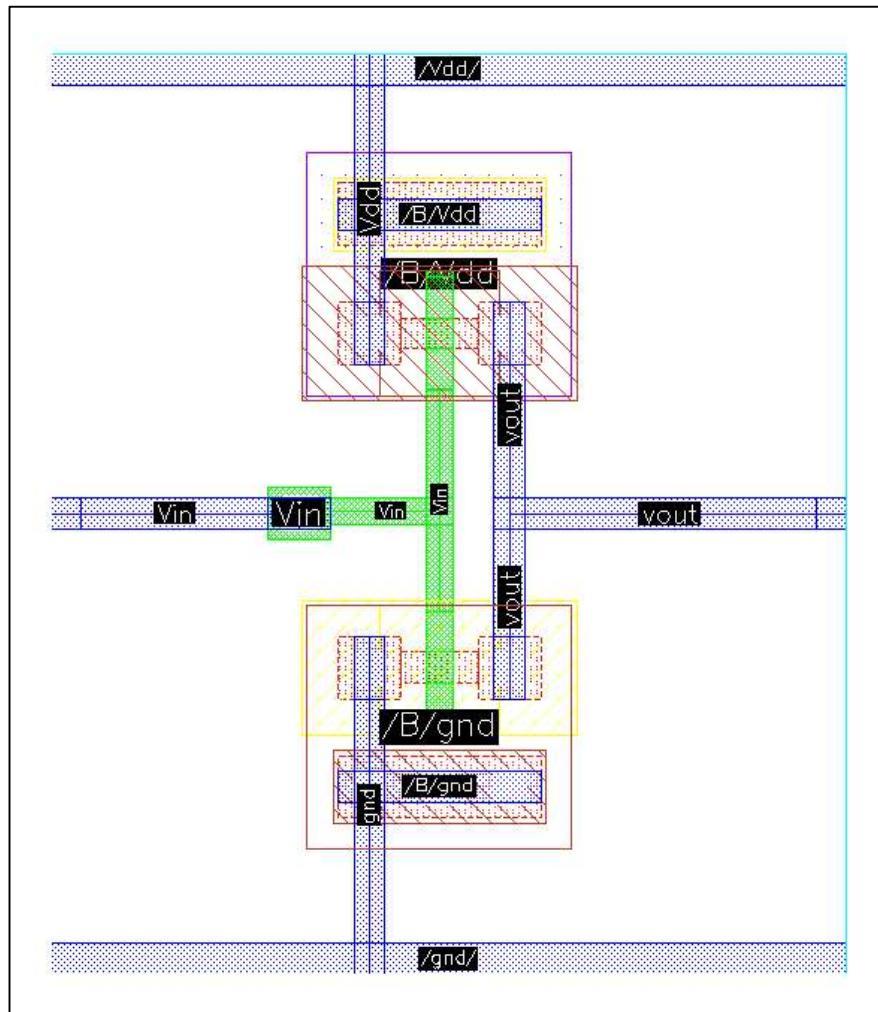
PROCEDURE:-**Virtuoso:-**

- Boot the system using Redhat linux and open the terminal
- Create a directory by typing mkdir “name of the directory”.
- Using command “cd”(change directory) move into the created folder i.e “ cd ‘name of the directory’ ”.
- Type “csh” in terminal to invoke “cshell” in the terminal i.e we are looking into the home
- directory to commands from the “.cshrc” file.
- Now type the command “ source /home/install/cshrc “ in terminal to setup the environment to launch virtuoso.
- Type “virtuoso” to launch the virtuoso suite of cadence software, virtuoso window pops up.
- Click on the following to create a new library:-
- File -> New -> Library
- Name is given to the library
- In the technology file section “ Attach to an existing technology library” is selected.
- “gdk180” is selected.

INVERTER SCHEMATIC:



LAYOUT DESIGN:



- Click on the following to create a cellview:-
- File -> New -> Cellview
- Name is given to the cellview.
- Library created in the previous step is selected.

Designing the circuit:-

- Select the option “Create instance “ to place components to form a circuit:-
 - NMOS is selected from “gpdk90” i.e., “nmos1v”
 - “Vdc,gnd” is selected from “analoglib” library.
 - Circuit is created as per the circuit diagram.

Designing the circuit in layout:

- Select the Launch click on the option Layout XL
 - Startup option appears in layout section click create new
 - In Configuration section click Automatic and click OK “Layout window appears”
 - In Layout window select connectivity and in generate all from sources the devices from “schematic” window will get imported in the “layout XL” windows
 - Connections are made with reference to circuit diagram.

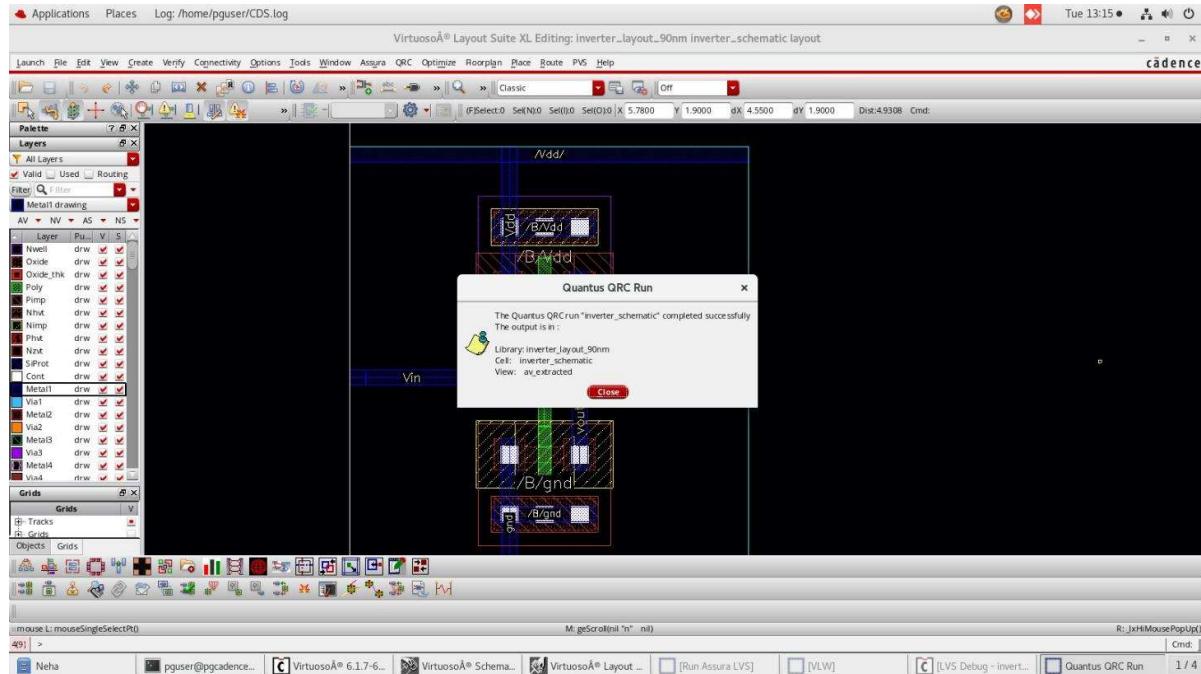
PROCEDURE FOR SIMULATION:

After Designing the layout go to Assura click technology “assura technology Lib Selection window appear in that click view -> In Directory click “Cadance”->”Foundary”->”analog”->”90nm” and in files click “assura tech lib” and then click on apply and ok.

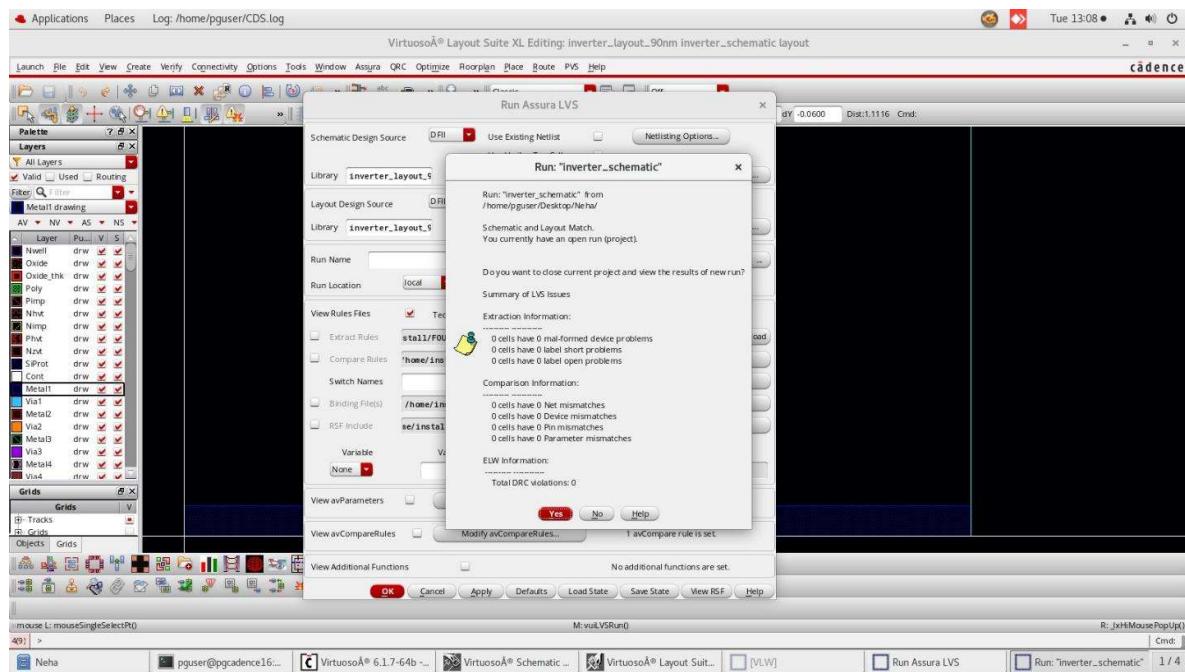
I. DESIGN RULES CHECK(DRC):

- i. Go to Assura and select “Run DRC”
 1. In that window in technology drop down select gpdk 90nm->click apply and ok.
 2. And window will appear which will give tell weather any error is present it not it will display “No DRC is found”.

DRC CHECK:



LVS CHECK:



II. Layout vs Schematic check (LVS):

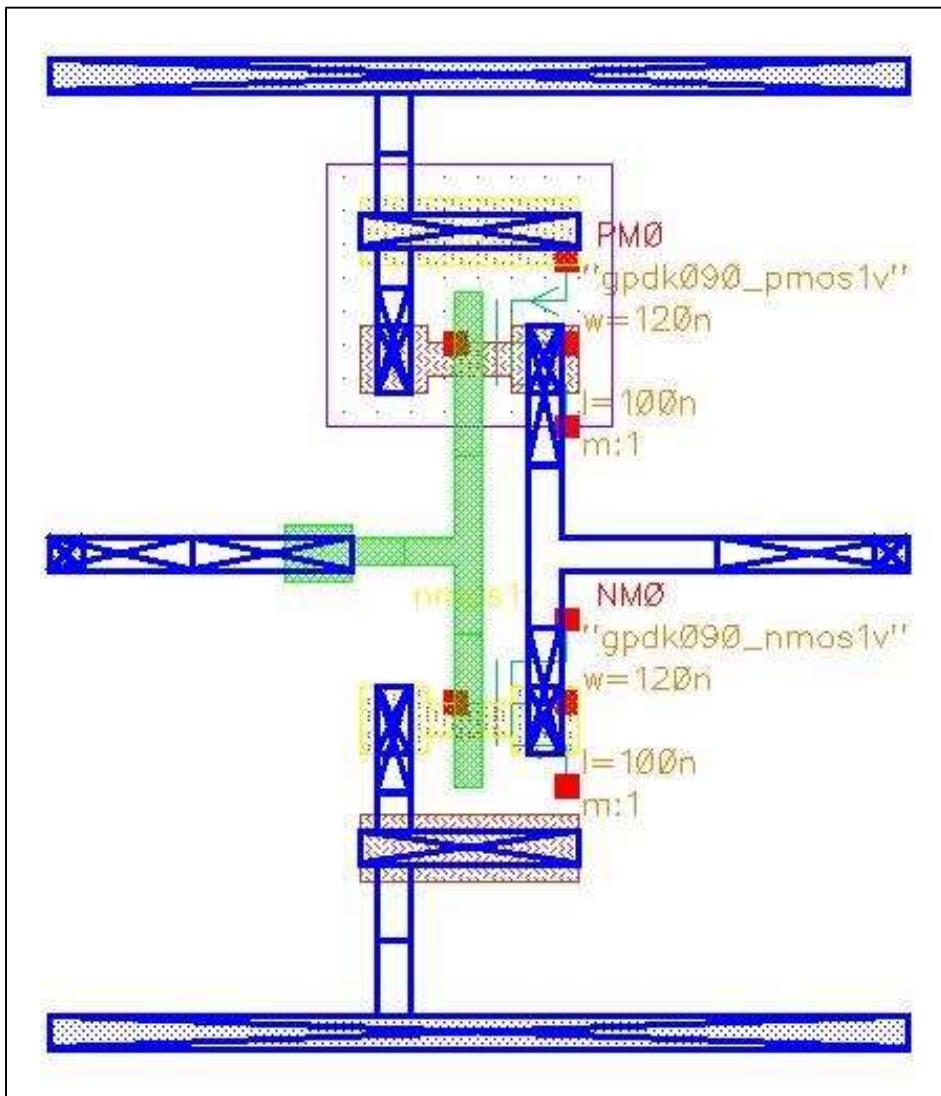
- i. Go to Assura and select “Run LVS”
 1. In that window in Layout Design Source weather the cell and view are schematic and layout
 2. In technology drop down select gpdk 90nm->click apply and ok.
 3. And window will appear which will give tell weather the layout and schematic are same and verify for any violations if not found it will display “Schematic and Layout match”

III. Extract Resistance and Capacitance Values:

- i. Go to the Quantus and click setup quantus
 1. In Set as Default Drop down select the select extracted view and close.
- ii. Go to Assura and click Run Quantus.
 1. In technology drop down select gpdk-90nm.
 2. A dialogue box appears and inform the extraction is down
- iii. To view the extracted view go to “virtuoso” in files select open

In the layout library you can find the extracted view file and opening it you can find the “Resistance and Capacitance values” in the Layout Design.

PARAMETER EXTRACTION (CAPACITANCE AND RESISTANCE):



RESULT:

Thus the design of Layout of CMOS Inverter and Design Rules Check (DRC), Layout vs Schematic check (LVS) and extract resistance and capacitance values are performed and the results are verified.

