Multicycle implementation.

* an instr execution split into multiple steps.

  each step — 1 clock cycle

SCI MCI

* allows a functional unit to be used > more than once per instr in diff cc.

  → reduces amt of h/w required. * (advantage)

Differences from SCD:

1) single mem unit used for both instr & data
2) single ALU rather than an ALU & adders
3) one or more reg are added after every major funct unit to hold the o/p of that unit until the value is used in the subsequent cc.

* at the end of a cc, data used in subsequent cc must be stored.

  ↳① data used by same instr in a later cc — stored in one of the addln reg

  ↳② data used by subsequent instr in a later cc — stored in either PC, Reg file or Mem.

* in MCI, we assume that the cc can accomodate at most one of the foll oprtns — a mem access, reg file access or an ALU oprtn.

∴ data produced by any of these three units must be saved into a temp reg for use in a later cc.

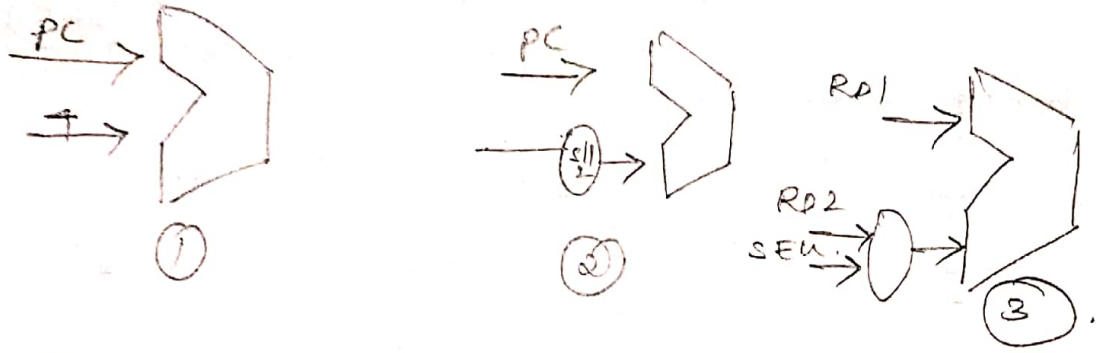
Additional reg :—

1) IR & MDR (Mem Data reg) are added to save o/p of mem for an instr read & data read resp.

2) A & B reg are used to hold reg operand values read from reg file. (RD1 and RD2) (A) (B)

3) ALUOUT reg to hold ~~value~~ o/p of ALU

Replacing ~~single~~ three ALU by a single ALU
— single ALU must accomodate all i/p that used to go to three diff ALU.



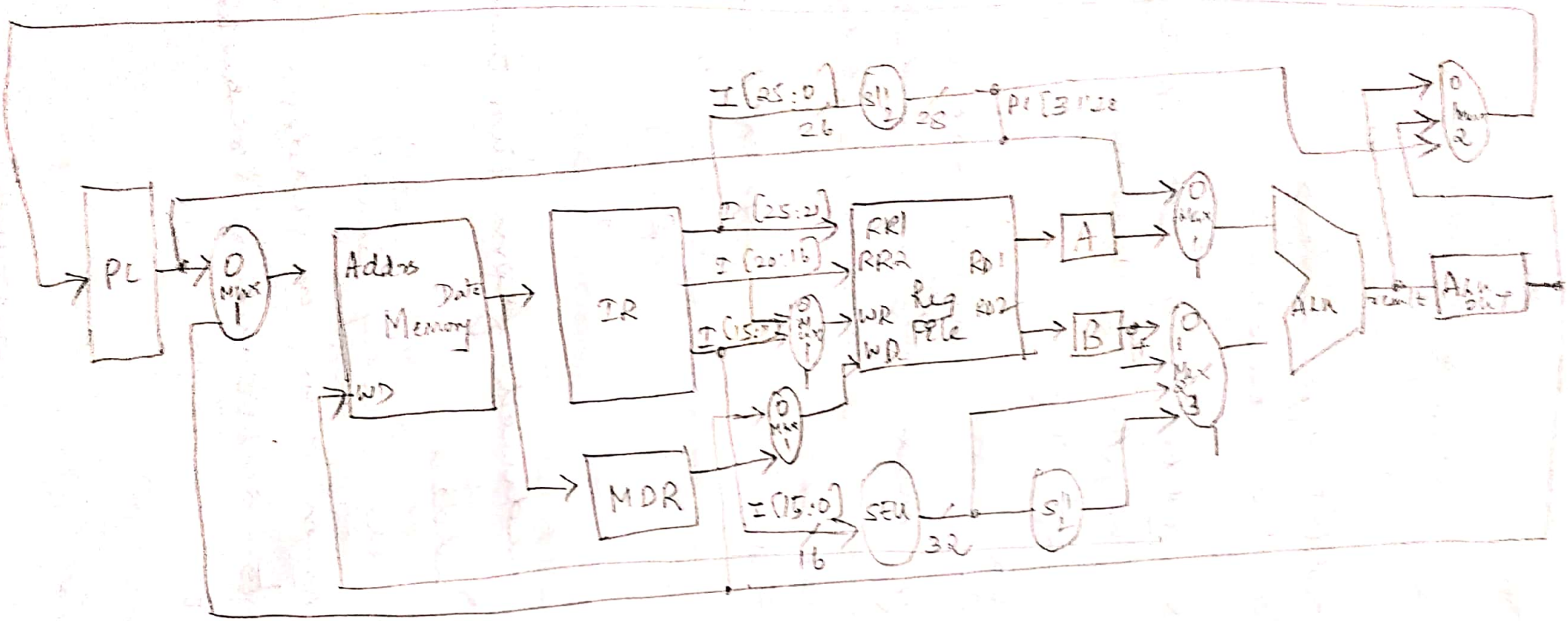
To handle the addln i/ps – two changes to the datapath

① an addln mux added b4 1st i/p to ALU to choose b/w PC & value read from RD1 (A reg)

② mux on 2nd i/p to ALU is changed from 2way to 4way mux. to accomodate 4 i/ps — a) value read from RD2 (B reg
b) const 4
c) SEU (32 bit sign extd val
d) sll 2 (32 bit left shifted offset value).

adv of MCI :

* mem unit reduced from two to a
* eliminates 2 adders
* regs & mux are fairly small compared to mem unit or adders which yields to substantial reduc in h/w cost.



MCI without Control signals.

Breaking instr exec into CC.

1) IF step.

$IR \Leftarrow Mem[PC]$

$PC \Leftarrow PC+4.$

CS.

MemRead – 1
IRWrite – 1
IorD – 0
ALUSrcA – 0
ALUSrcB – 01
ALUOP – 00
PCSource – 00
PCWrite – 1

2) ID.

$A \Leftarrow Reg[IR[25:21]]$

$B \Leftarrow Reg[IR[20:16]]$

$ALUOUT \Leftarrow PC + (sign\ ext(IR[15:0] \ll 2))$

CS: ALUSrcA = 0 ALUOP – 00

ALUSrc B = 11

3) Exec, mem addrs comp a branch completion

(a) Mem ref. for both lw & sw.

$ALUOUT \Leftarrow A + sign\text{-}extend(IR[15:0])$

ALUSrcA = 1 ALUSrcB = 10 ALUOP=00

(b) AL. instr

$ALUOUT = A\ op\ B$

ALUSrcA = 1 ALUSrcB = 00 ALUOP = 10

(c) Branch if $(A == B)$ $PC \Leftarrow ALUOUT$

ALUSrcA = 1
B = 00
ALUOP = 01
PCWriteCond = 1 PCSrc = 01

Jump:

PC ⇐ {PC[31:28], (IR[25:0]), 2'b00)}

PCSource – 10

PCWrite – 1

(4) Mem access a R type completion.

Mem access:

lw: MDR ⇐ Mem[ALUOut]

sw: Mem[ALUOut] ⇐ B

MemRead – 1

IorD – 1

MemWrite – 1

IorD – 1

Arith.:

Reg[IR[15:11]] ⇐ ALUOut

RegDst – 1 RegWrite – 1

MemToReg – 0

(5) Mem Read completion step.

lw: Reg[IR[20:16]] ⇐ MDR

MemToReg – 1 RegWrite – 1

RegDst – 0

Learn Fig NO: 5:30 Page 329.

Chapter - 4 Performance

Consider a comp A that runs a pgm in 10sec & another comp B that runs the same pgm in 15sec. Which comp's perf is better?

Since A completes the same pgm in just 10sec, compared to B which takes 15sec which is more, A's perf is better than B.

∴ we can say

$$Perf = \frac{1}{Exec\ time}$$

$$Perf_A = \frac{1}{Exec\ time_A} = \frac{1}{10} = 0.1$$

$$\approx Perf_B = \frac{1}{15} = 0.06$$

How much faster is A than B?

$$\frac{Perf_A}{Perf_B} = \frac{Exec\ B}{Exec\ A} = \frac{15}{10} = 1.5$$

∴ $Perf_A = 1.5$ times $Perf_B$.

Say a pgm takes following cc for execution.

we can say total execution time

= total no: of cc x time taken for each clock cycle

$$\text{CPU exec time} = \text{No: of cc} \times \text{CC T.}$$

also we have

$$\text{CCR} = \frac{1}{\text{CCT}} \text{ hz (cycles/sec)}$$

clock cycle rate

ie no: of cc/s

$$\therefore \text{CPU exec time} = \frac{\text{No: of cc}}{\text{CCR}}$$

Q) A pgm runs on comp A in 10s with the CR of 4GHz. We want to design a comp B that will run the same pgm in 6s. Is it possible to increase the CR causing comp B to require 1.2 times as many cc as comp A?

we have: CPU exec time$_A$ = 10s

CCR_A = 4GHz

CPU Ex time$_B$ = 6s

No: of cc$_B$ = 1.2 x no: of cc$_A$.

find CCR_B ? i.e $\frac{\text{no: of } CC_B}{\text{Exec time}_B}$ find

$$\text{Ex time} = \frac{\text{no: of CC}}{\text{CR}}$$ we have

$\therefore$ no: of CC_A = $\text{Ex time}_A \times CCR$

= 10 sec x 4 GHz (cycles/sec)

= $10 \times 4 \times 10^9$ cycles

= 4×10^{10} cycles

$K = 10^3$
$M = 10^6$
$G = 10^9$
$P = 10^{12}$
$T = 10^{15}$

$\therefore$ no: of CC_B = $1.2 \times 4 \times 10^{10}$ cycles

= 4.8×10^{10} cycles.

$$\therefore CCR_B = \frac{\text{no: of } CC_B}{\text{Exec time}_B}$$

$$= \frac{4.8 \times 10^{10}}{6} = 8\,GHz$$

8 GHz > 4 GHz

$\therefore$ It is possible to increase the CR of B.

Q) A pgm runs in 10s in comp X with a CR of 2 GHz. If you have to design a new comp Y to run the same pgm in 6 sec, what is the CR required for Y, given Y requires 10% more CC than X to execute the pgm.

given:

Ex time_X = 10 s Ex time_Y = 6 sec

CCR_X = 2 GHz no: of CC of Y = (CC of X) + 10% of CC of X.

find: CCR_Y = $\frac{\text{no: of CC Y}}{\text{Ex time Y}}$ find we have

No: of CCy = CCx + 10% CCx

~~CPU ex time~~

$$CCx = \frac{CPU\ ex\ time_x}{} \times CR_x$$

$$= 10 \times 2 \times 10^9$$

$$= 2 \times 10^{10}\ cc$$

$$\therefore CCy = 2 \times 10^{10} + \frac{10}{100} \times 2 \times 10^{10}$$

$$= 2 \times 10^{10} + 2 \times 10^9$$

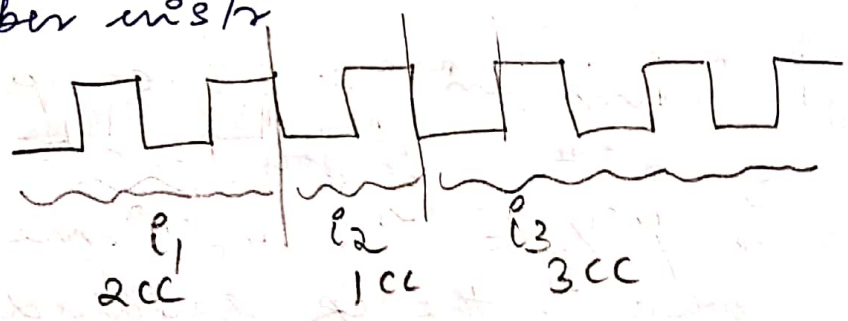
$$= 20 \times 10^9 + 2 \times 10^9$$

$$= 22 \times 10^9\ cc$$

$$\therefore CR_y = \frac{22 \times 10^9}{6} = 3.67\ GHz$$

Total no: of cc for a pgm can be made more specific by finding no: of cc per instr

eg:



Total no: of cc = Total no: of instr × avg cc per instr

$$= 3 \times \frac{(2+1+3)}{3} = 3 \times \frac{6}{3} = 6$$

∴ we can write No: of cc = Ic × CPI

Ic = instr count; CPI = avg cc/instr

$$\therefore \boxed{Ex\ time = Ic \times CPI \times CT}$$

Q) A comp A has a CCT of 250 picose and CPI of 2 for a particular pgm. For the same pgm, comp B has CCT of 500ps and CPI of 1.2. which comp is faster and by how much?

$$\frac{Perf_A}{Perf_B} = \frac{Extime_B}{Extime_A}$$

$$= \frac{IC_B \times CPI_B \times CCT_B}{IC_A \times CPI_A \times CCT_A}$$

since its same pgm $IC_A = IC_B$

$$\therefore \frac{Perf_A}{Perf_B} = \frac{1.2 \times 500}{2 \times 250}$$

$$= 1.2$$

$Perf_A = 1.2$ times $Perf_B$

$\therefore$ A is 1.2 times faster than B.

Q) Consider three processors P_1 P_2 P_3 executing same pgm with CR of 2, 1.5, 3 GHz resp. & CPI of 1.5, 1, 2.5 resp.

a) which proc has highest perf?

b) If each proc executes in 10 s find the no: of CC in each.

~~c) we are trying to reduce extime of a pgm~~

Ans:

a) $Perf_{P1} = \frac{1}{Extime_{P1}} = \frac{CR_{P1}}{IC_{P1} \times CPI_{P1}} = \frac{2}{1.5} = 1.3$

Since its a comparison, we can ignore IC (for same pgm $\therefore IC_{P1} = IC_{P2} = IC_{P3}$)

$P_2 = \frac{1.5}{1} = 1.5$

$P_3 = \frac{3}{2.5} = 1.2$

$\therefore P_2$'s perf is highest.

(5) no: of cc = ?

$\text{Extense} = \frac{\text{no: of cc}}{CCR}$

$\therefore$ no: of cc = Ex tense x CCR

no: of cc $P_1 = 10 \times 2 = \underline{20}$

$P_2 = 10 \times 1.5 = \underline{15}$

$P_3 = 10 \times 3 = \underline{30}$

Q) We are trying to reduce extense of a s/m by 30% which causes the CPI to increase by 20%. what CR should we have to achieve this if the existing CCR is 2 GHz.

$Ex' = Ex - \frac{30}{100} Ex = 0.7\,Ex$

$CPI' = CPI + \frac{20}{100} CPI = 1.2\,CPI$

$CCR = Ex = \frac{Ic \times CPI}{CCR}$

$\therefore CCR = \frac{Ic \times CPI}{Ex}$

$CCR' = \frac{Ic' \times CPI'}{Ex'} = \frac{Ic \times 1.2\,CPI}{}$

now we have

$$Ex' = 0.7\,Ex$$

$$\frac{IC' \times CPI'}{CCR'} = 0.7 \times \frac{IC \times CPI}{CCR}$$

$$\frac{1.2 \times CPI}{CCR'} = \frac{0.7 \times CPI}{CCR}$$

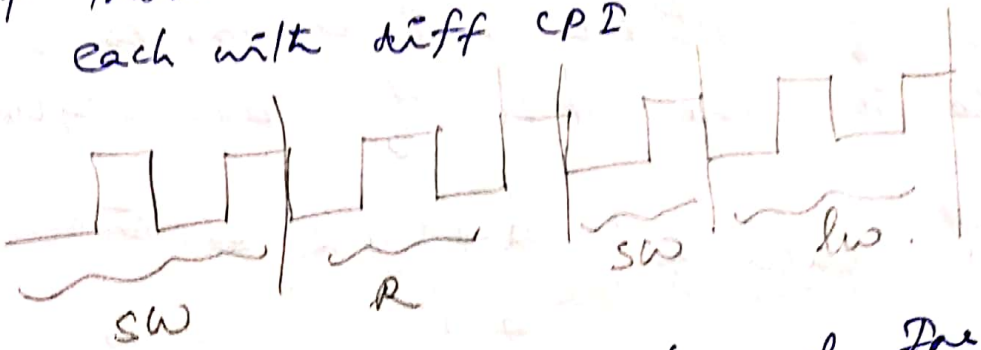
$$CCR' = \frac{1.2}{0.7} \times CCR\,(2\ GHz)$$

$$= 1.7 \times 2 = 3.4\ GHz$$

In the previous eqn of CC

$$CC = CPI \times IC$$

If there are diff classes of Instr each with diff CPI



the count of each class of Instr will be diff.

$$\therefore \text{Total no: of CPU CC} = \sum_{i=1}^{n} (CPI_i \times IC_i)$$

where IC_i = count of no: of instr of class i

CPI_i = avg no: of cc / instr for that Instr class

n = no: of instr classes.

Q) A compiler designer is trying to decide b/w 2 code sequences for a particular comp. Given Instr class

	A	B	C
CPI	1	2	3

Consider the foll code sequence

Instr count for each class

	A	B	C
1	2	1	2
2	4	1	1

which code sequence executes the most instrs ? which will be faster ? what is the CPI of each sequence.

seq 1 executes $2+1+2 = 5$

seq 2 $4+1+1 = 6$

∴ seq 1 has less instrs.

$$CC_1 = \sum_{i=1}^{n} CPI_i \times IC_i$$

$$= 2\times1 + 1\times2 + 2\times3$$

$$= 10$$

$$CC_2 = 4\times1 + 1\times2\times1\times3$$

$$= 9$$

2 requires less CC, ∴ 2 is faster.

seq 2

To find CPI of each sequence.

we have

total no: of CC_1 = $CPI_1 \times IC_1$

$\therefore CPI_1 = \frac{\text{total } CC_1}{IC_1}$

$= \frac{10}{5} = \underline{\underline{2}}$

$\approx CPI_2 = \frac{\text{total } CC_2}{IC_2} = \frac{9}{6} = \underline{\underline{1.5}}$

Q) Consider two s/m that are executing the same applⁿ, the IC for various classes of instr & CPI are given as follows.

CPI for each class

	Int/sw	Acu	branch
1	1.2	0.9	0.8
2	1.5	0.7	0.9

IC for each instr class

	lw/sw	Acu	branch
1	20	15	15
2	18	20	12

which of the two s/m are faster assuming both run at same CR. What happens if s1 runs at 2 GHz & s/m 2 at 2.2 GHz?

No: of $CC_1 = 20 \times 1.2 + 15 \times 0.9 + 15 \times 0.8 = 49.5$

$CC_2 = 18 \times 1.5 + 20 \times 0.7 + 12 \times 0.9 = 51.8$

s/m 1 is faster. since both run at same CR

s/m with CR 2GHz

$$\text{Exectime}_1 = \frac{\text{NO: of CC1}}{\text{CR1}}$$

$$= \frac{49.5}{2\times10^9}$$

$$= 25 \times 10^{-9}\text{s}$$

$$\text{Extime}_2 = \frac{\text{NO: of CC2}}{\text{CR2}}$$

$$= \frac{52}{2.2\times10^9} = 23.6\times10^{-9}\text{s}$$

s/m is faster with diff CR.

Q) s/m 1

IClass	CPI	freq
A	2	40%
B	3	25%
C	3	25%
D	5	10%

s/m 2

A	2	40%
B	2	25%
C	3	25%
D	4	10%

s/m 1 has a CR of 500MHz. Is it possible to improve the perf of s/m with a CR of 600MHz?
Compute CPI for each m/c.
which s/m is faster?

$$CPI = \frac{\text{no: of cc}}{Ic}$$

$$= \frac{\Sigma IC_i \times CPI_i}{Ic}$$

$$= \Sigma \frac{ICi}{Ic} \times CPI_i$$

$\frac{\Sigma ICi}{Ic}$ = freq of instr class i.

$$\therefore CPI_1 = \frac{40}{100} \times 2 + \frac{25}{100} \times 3 + \frac{25}{100} \times 3 + \frac{10}{100} \times 5$$

$$= .8 + .75 + 0.75 + .5$$

$$= \underline{\underline{2.8}}$$

$$\approx CPI_2 = \frac{40}{100} \times 2 + \frac{25}{100} \times 2 + \frac{25}{100} \times 3 + \frac{10}{100} \times 4$$

$$= .8 + 0.5 + 0.75 + .4$$

a) Assume the operation time for major functional unit are the foll:

Memory – 200ps
ALU – 100ps
RF – 50ps.

Compute the length of each instr class, clock cycle time for a m/c with single clock impl for all instr using critical path. Also compute the execution time for 60 instrs.

critical path – path taken by each instr to be executed.

	IM	RR	ALU	DM	RW	Total
R	200	50	100	0	50	400
lw	200	50	100	200	50	600 Max
sw	200	50	100	200	0	550
beq	200	50	100	0	0	350
j	200	0	0	0	0	200

CCT - 600ps - max

CPU exec time = IC x CPI x CCT

= 60x1 x 600

= 36000ps.

Q) Consider an instr mix of 25% load, 10% stores, 11% branch, 2% jump, 52% ALU, Compute the overall CPI if each state in multicycle CPU req 1 CC?

~~No. of CC~~ Instr class	No: of CC
load	5
store	4
branch	3
jump	3
ALU instr	4

$$CPI = \frac{\sum CPI_i \times IC_i}{IC}$$

= .25 x 5 + .1 x 4 + .11 x 3 + .02 x 3 + .52 x 4

= 4.12