Q) For the following instructions what changes do you make to the existing SCP datapath (and control signals)? Depict with diagram.

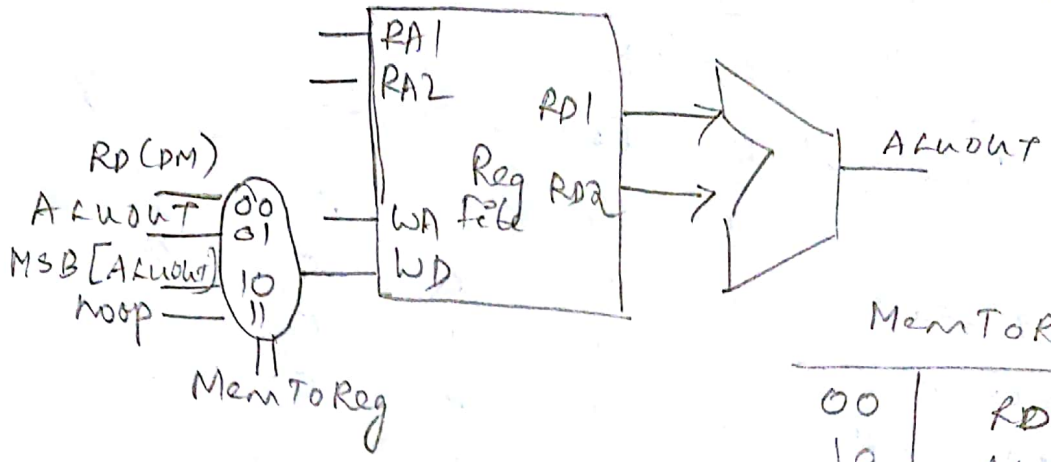
1) slt $t1 $s2 $s4

if ($s2 < $s4) $t1 = 1
else $t0 = 0

∴ check MSB bit of ALUOUT. & write that to reg file directly (WD part)

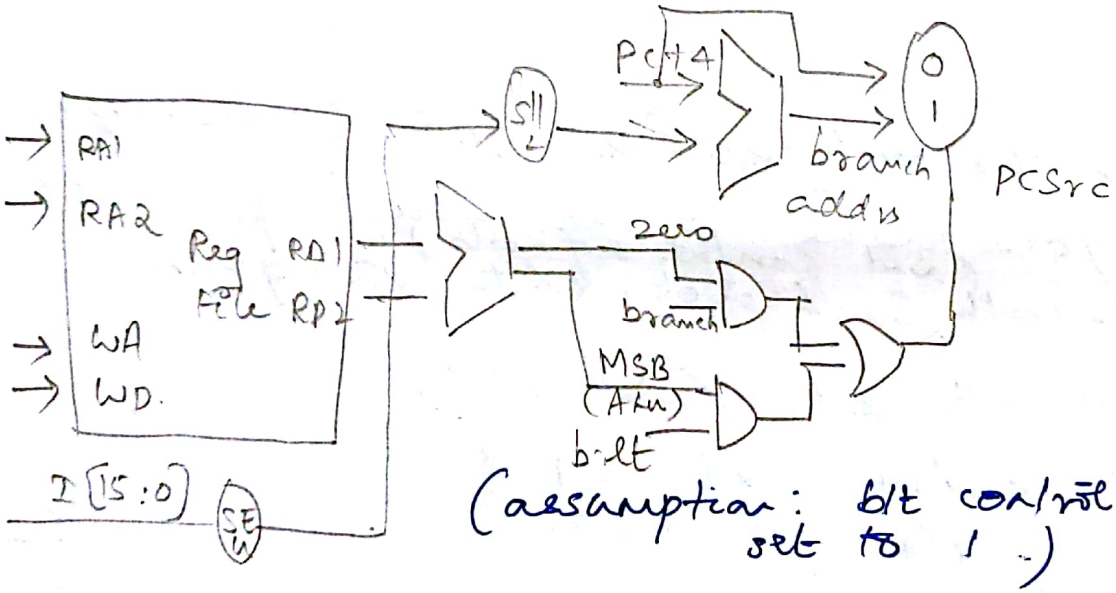
but there are already two values RD (DM) & ALUOUT going to WD of reg file.

One possible change — to modify MemToReg to 2 bit signal & include one more i/p



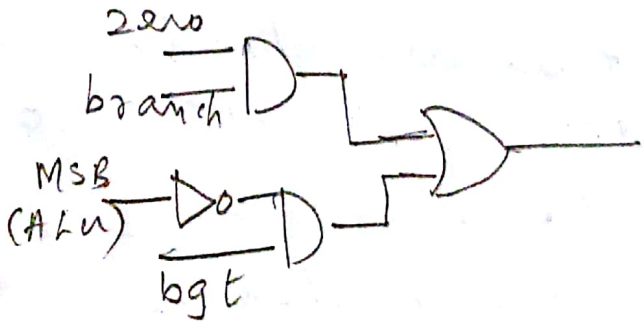
MemToReg	
00	RD(DM) (lw)
10	ALUOUT (R-format)
01	MSB[ALUOUT] slt
11	no op

② blt $s1 $s2 L



(assumption: blt control signal set to 1.)

If bgt $s1 $s2 L, invert MSB



(3) load increment, which increments the contents of index reg after loading word from memory

lw $rt L($rs)
addi $rs $rs 1

Two writes in a single clock.

∴ include one more WA, WD ports and one extra write signal