Fault diagnosis in analog circuit using machine learning

Project-I (IE47007) report submitted to

Indian Institute of Technology Kharagpur

in partial fulfilment for the award of the degree of

Btech-4year

in

Electrical Engineering

by

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Autumn Semester, 2019-20

December 5, 2019

DECLARATION

I certify that

(a) The work contained in this report has been done by me under the guidance of my supervisor.

(b) The work has not been submitted to any other Institute for any degree or diploma.

(c) I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.

(d) Whenever I have used materials (data, theoretical analysis, figures, and text) from other sources, I have given due credit to them by citing them in the text of the thesis and giving their details in the references. Further, I have taken permission from the copyright owners of the sources, whenever necessary.

Date: December 5, 2019 (Aaditya)
Place: Kharagpur (16IE10033)

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

KHARAGPUR - 721302, INDIA

CERTIFICATE

This is to certify that the project report entitled "**Fault diagnosis in analog circuit using machine learning**" submitted by **Aaditya** (Roll No. 16IE10033) to Indian Institute of Technology Kharagpur towards partial fulfilment of requirements for the award of degree of Btech-4year in Electrical Engineering is a record of bonafide work carried out by him under my supervision and guidance during Autumn Semester, 2019-20.

Date: December 5, 2019
Place: Kharagpur

Department of Electrical Engineering
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Kharagpur - 721302, India

Abstract

Name of the student: **Aaditya** Roll No: **16IE10033**

Degree for which submitted: **Btech-4year**

Department: **Department of Electrical Engineering**

Project title: **Fault diagnosis in analog circuit using machine learning**

Month and year of project submission: **December 5, 2019**

Our work is about proposing fault diagnosis method for analog integrated circuits. Our approach is based on Machine Learning Model that is trained beforehand to guide us through diagnosis decisions. The Model is a defect filter that detects failing devices due to gross defects (hard faults) Thus, the defect filter is key in developing a unified hard fault diagnosis approach. hard faults are diagnosed using a multi-class classifier

Acknowledgements

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Contents

Chapter 1

Introduction

1.1 Motivation

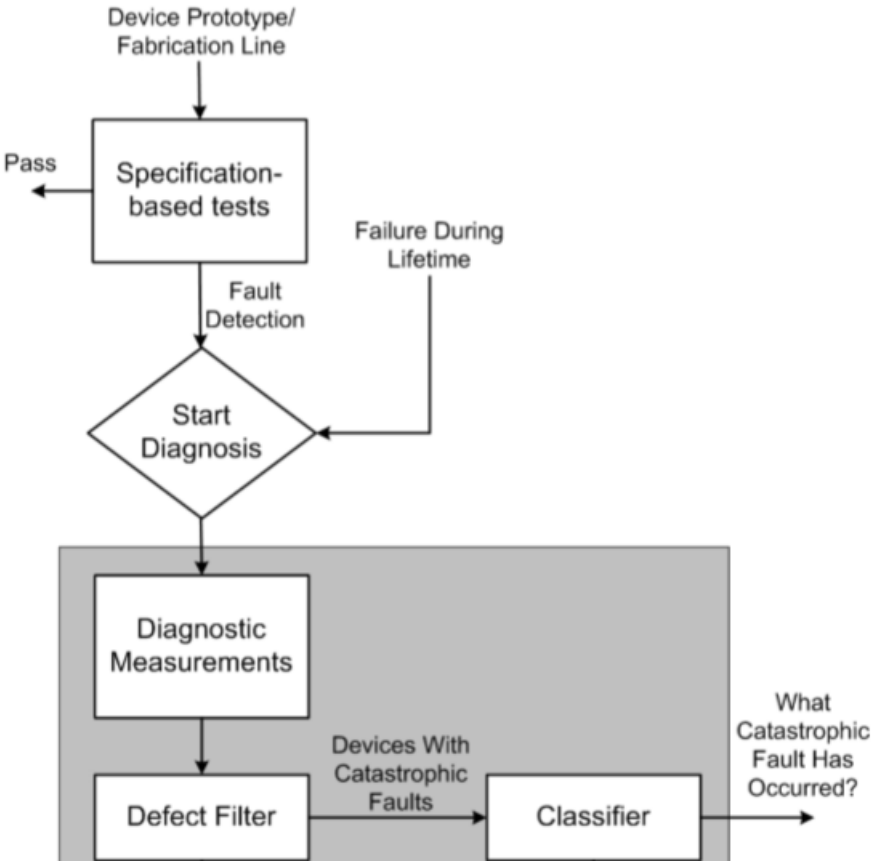
The design of integrated circuits (ICs) typically passes through many silicon iterations before it is finalized. Diagnosing the sources of failure in the rst IC prototypes in a timely fashion is very critical to meet the time-to-market goal. Failure at this stage is related to the incomplete simulation models and the aggressive design techniques that are being adopted to exploit the maximum of performance out of the current technology. A second application of fault diagnosis is in high-volume production where it can assist the designers in gathering information regarding the underlying failure mechanisms. This information constitutes valuable feedback to enhance yield in future product generations. A comprehensive fault diagnosis method is also needed in cases where the IC is part of a larger system that is safety critical (e.g. automotive, aerospace). During its lifetime, an IC might fail due to aging, wear-and-tear, harsh environments, overuse, or due to defects that are not detected by the production tests and manifest themselves later in the eld of operation. Here, it is important to identify the root-cause of failure so as to repair the system if possible, gain insight about environmental conditions that can jeopardize the system's health, and apply corrective actions that will prevent failure re occurrence and, thereby, expand the safety features.

1.2 Challenges

Fault diagnosis is a major challenge that calls for immediate solution. some of the factors that hinder diagnosis are the limited controllability and observability of internal blocks of ICs, the difculty to deal with unanticipated faults, the limited diagnostic information (only one/few IC samples showing the same erroneous behavior are available), and the fault ambiguity (i.e. different faults having the same inuence on the IC behavior) which does not permit case-based reasoning. .

1.3 Proposed Method

The proposed fault diagnosis method belongs to the fault model-based category. It relies on an machine learning model that must be tuned in a pre-diagnosis learning phase. ML models have also been used in the past to implement an adaptive go/no go test. A high-level description of the proposed method is illustrated in Fig. 1.



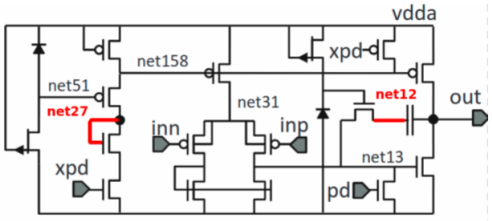
Chapter 2

Related work

Various types of fault diagnosis techniques have been proposed to date for analog circuits Fault-model-based techniques require the apriori generation of fault hypotheses. In this step, an inductive fault analysis is combined with historical defect data to dene a list of hard fault hypotheses at the circuit net-list level. Perhaps the most well-known fault-model-based technique is the fault dictionary [1], [2], [3]. A fault dictionary contains fault hypothesis/diagnostic measurement pattern pairs, which are generated by sequentially simulating the circuit, inserting each time a single fault in the net-list. The same diagnostic measurement pattern is obtained during diagnosis and is compared to those in the faulty dictionary using a similarity measure. The diagnosed fault is the one that pairs up with the most similar diagnostic measurement pattern. This is in essence a pattern recognition (e.g. classication) approach. As such, it is mostly suitable for catastrophic faults

Chapter 3

Datasets



(a) OPMAP1

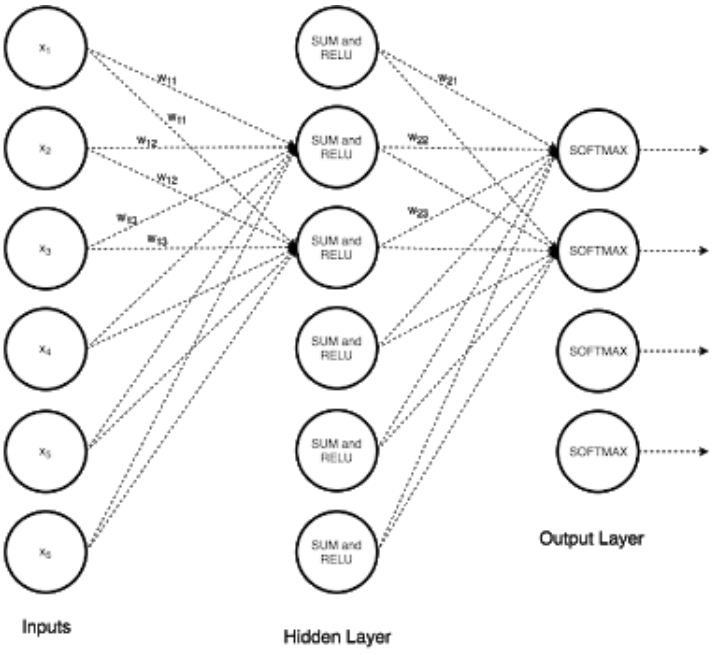
Transistor	Fault Type
mnm12	SG
mnm12	DG
mnm11	SG
mnm11	SD
mnb02	SG

TABLE 3.1: Small example of fault dictionary with 5 faults

each fault from the fault dictionary was injected into the OPAMP circuit (a) one by one (b) taking two at a time, as shown in Table 1, by injecting fault we mean short-circuiting the corresponding source-drain or drain-gate or gate-source by 1 ohm resistor. the resulting fault-injected circuit was then simulated using Cadence Spectre software. each transistors DC Operating point was noted for each simulation run. as a result (a) 40 (b) 780 instances were generated for single fault and double fault simulation runs respectively

Chapter 4

Model Description



We used a Dense neural network classifier for identifying different catastrophic (hard) faults. Dense neural network consists of layers that are fully connected (dense) by the neurons in a network layer. Each neuron in a layer receives an input from all the neurons present in the previous layer—thus, they're densely connected. In other words, the dense layer is a fully connected layer, meaning all the neurons in a layer are connected to those in the next layer.

The choice of Dense Neural network(DNN) over other networks like convolutional neural network(CNN), LSTMs etc was inspired by large functional representation space of DNN over CNN. A densely connected layer provides learning features from all the combinations of the features of the previous layer, whereas a convolution layer relies on consistent features with a small repetitive field. we used keras library in Python to build the DNN. along with the model we employed binary crossentropy as the loss function and used adam optimizer for updating the model weights. the corresponding diagram of DNN is shown in figure 1

Number of neurons in input layer for (a)single fault DNN model (b) double fault DNN model are 10 (corresponding to DC operating values) respectively. whereas the number of neurons in hidden layers for are 64,32 respectively. the number of neurons in output layer are equal to number of faults ie, 40. the output of the output layer will be the set of probabilities for each fault.

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Chapter 5

Results & Conclusion

We trained our Dense Neural Network on the fault injected simulated data set and tabulated the accuracy of the model for (a) single fault simulations and (b) double fault simulations

Fault	Accuracy
Single faults	87%
Double faults	83%

Table 5.1: Model Accuracy

- From the results we conclude that the accuracy for single faults is more that for double faults owing to less number of data examples.
- mostly accuracy mentioned here corresponds to the definition of number of individual correct fault predictions rather than the whole correct fault vector

Chapter 6

Future Work

- we would like to experiment with other IC's like Phase locked loop(PLL) and Comparator (COMP)and try to model their faults.
- we would also like to experiment with other models with different loss functions like MSE, MAE, SVM etc.
- we can also experiment with different optimizers like sgd, adam etc