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DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

End Semester Examination – Summer 2019

Course: B. Tech in Computer Engineering **Sem: III**

Subject Name: Computer Architecture and Organization

Subject Code: BTCOC304

Max Marks: 60 **Date: 31/05/19** **Duration: 3 Hr.**

Instructions to the Students:

1. *Solve **ANY FIVE** questions out of the following.*
2. *The level question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Four of the following.**		**12**
A)	Differentiate between Big and Little endian. Why are transfer of control instructions needed?	Informative/Easy	
B)	A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. (i) How many selection inputs are there in each multiplier? (ii) What sizes of multiplexers are needed? (iii) How many multiplexers are there in the bus?	Synthesis/Logical	
C)	Enlist the design issues of computer organisation with explanation. For move and add instructions, the format is load location1,location 2 and add R1, R0. Is it possible to use fewer instructions to accomplish the task? If yes, then elaborate your answer and give the proper sequence.	Application/ Average Level	
D)	Why a format that allows multiple words to be use for a single instruction would be needed to represent an instruction set? Why there is need of computer organization?	Understanding /Easy	
E)	Represent the decimal values 5,-2,14,-10 as signed seven bit numbers in the following binary formats. a) Signed and Magnitude b) 1's complement c) 2's complement.	Informative/ Average	
Q.2	**Solve Any Four of the following.**		**12**
A)	Why is RISC architecture better suited for pipeline processing than CISC? Which architecture is more common in mobile phones RISC or CISC?	Info/Average	
B)	What is the purpose of integer arithmetic and describe the role of overflow in addition and subtraction operations of integer arithmetic? Calculate (72530-48960) using tens complement arithmetic. Assume rules similar to those for twos complement arithmetic.	Understanding	
C)	A memory byte location contains the pattern 00101100. What does this pattern represents when interpreted as a binary number? What does it represent as ASCII code? How two's complement relates with subtraction	Understanding/	

	rule? Write proper reason and example.	Hard	
D)	Discuss the need of variable length instruction format. How many bits wide memory address have to be if the computer had 16 MB of memory?	Tough Level/ Synthesis	
E)	How do you improve the cache performance? How many check-bits are needed if the hamming error correction code is used to detect single bit errors in a 2048 bit data word?	Application	
Q. 3	**Solve the following.**		12
A)	Discuss difference between dynamic and static RAM in terms of characteristics such as speed,size and cost. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt?	Understanding	
B)	How is the syndrome for the Hamming code interpreted? Suppose that the processor has access to two levels of memory. Level 1 contains 1000 words and has an access time of 0.01 microseconds; level 2 contains 1,00,000 words and has an access time of 0.1 microseconds. Assume that if a word to be accessed in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose 95% of the memory accesses are found in the cache. Then, what should be the average time to access a word?	Info/Average	
Q.4	**Solve Any four of the following.**		12
A)	Differentiate virtual with main memory?	Info	
B)	Consider a cache with a line size of 32 bytes and a main memory that requires 30 ns to transfer a 4 byte word. For any line that is written at least ones before being swapped out of the cache, what is the average number of times that the line must be written before being swapped out for a write-back cache to be more efficient than a write-through cache?	Understanding	
C)	Give the difference between sequential, random and direct access.	Info	
D)	A set associative cache consists of 64 lines or slots divided into four line sets. Main memory contains 8K blocks of 64 words each. Show the format of main memory addresses.	Application	
E)	How the memory is organized?	Info	
Q. 5	Attempt any four of the following.		12
A)	When a DMA module takes control of a bus and while it retains control of the bus, what does the processor do?	Understanding	
B)	What is the difference between isolated I/O and memory mapped I/O? Why does DMA have priority over the CPU when both request a memory transfer?	Info	
C)	When a device interrupt occurs, how does the processor determine which device issued the interrupt?	Average/ Understanding	
D)	How three techniques have defined and differentiated for performing Input/Output?	Info	
E)	What is parity bit? How does SDRAM differ from ordinary DRAM?	Info/Synthesis	

Q. 6 Attempt the following. **12**

A) Explain the difference between hardwired control and micro-programmed control. What are different stages of a pipe? — Informative/ Logical/ Reasoning based

B) Why does an assembly line in a manufacturing plant refer to as pipe-lining?Discuss the need of instruction pipe-lining. — Reasoning/Info

C) Many pipelined processors use four to six stages. Others divide instruction execution into smaller steps and use more pipeline stages and a faster clock.
Considering the above scenario, for fast operations what would you suggest in terms of pipeline stages? How we relate instructions and micro-operations? What is the overall function of a processor's control unit? — Application/ Understanding

END