DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE – RAIGAD -402 103

Winter Semester Examination – Dec - 2019

Branch: B.Tech. (Computer Engineering)	**Sem: III**
Subject with Subject Code: Computer Architecture & Organization[BTCOC304]	**Marks:60**
Date:- 17-12-2019	**Time: 3 Hrs**

Instructions to the Students:

1.Each question carries 12 marks.
2. Attempt **any five** questions of the following.
3. Illustrate your answers with neat sketches, diagram etc., wherever necessary.
4. If some part or parameter is noticed to be missing, you may appropriately assume it and should mention it clearly.

Q.1	**Solve any following questions.**	
(A)	What, in general terms, is the distinction between computer organization and computer architecture?	**06**
(B)	Explain the computer: the top level structure with structural component with neat sketch diagram.	**06**
Q. 2	**Attempt the following questions.**	
(A)	Enlist and explain any two addressing modes. Given the following memory values and a one-address machine with an accumulator, what values do the following instructions load into the accumulator? • Word 20 contains 40. • Word 30 contains 50. • Word 40 contains 60 • Word 50 contains 70. a. LOAD IMMEDIATE 20 b. LOAD DIRECT 20 c. LOAD INDIRECT 20 d. LOAD IMMEDIATE 30	**06**
(B)		
I.	Convert the following instruction into Accumulator based CPU, Register based CPU. Instruction:(A*B)-(R+Z)/T	**03**
II.	Is RISC better than CISC? Illustrate your answer with example of processor.	**03**
Q.3	**Attempt the following questions.**	
(A)	Given x = 1011 and y = 1001 in twos complement notation (i.e., x = -5, y = - 7), draw and compute the product p = x * y with Booth's algorithm flowchart.	**06**
(B)	Show how the following floating-point additions are performed (where significants are	**06**

	truncated to 4 decimal digits). Show the results in normalized form. a. $5.566 \times 10^{2} \times 7.777 \times 10^{3}$ b. $3.344 \times 10^{1} + 8.877 \times 10^{-2}$ c. $6.21 \times 10^{5} \div 8.877 \times 10^{1}$	
Q.4	**Attempt the following questions.**	
(A)	What are the differences among direct mapping, associative mapping, and set-associative mapping?A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.	**06**
(B)	Elaborate the concept of SRAM and DRAM memory with typical memory cell structure.	**06**
Q.5	**Attempt the following questions.**	
(A)	What is the overall function of a processor's control unit?A stack is implemented.show the sequence of micro-operations for a. popping b. pushing the stack PUSH 10 PUSH 70 PUSH 8 ADD PUSH 20 SUB MUL	**06**
(B)	What is the difference between a hardwired implementation and a microprogrammed implementation of a control unit?	**06**
Q.6	**Attempt any two questions.**	
(A)	In virtually all systems that include DMA modules, DMA access to main memory is given priority than CPU access to main memory. Why?	**06**
(B)	What is the meaning of each of the four states in the MESI protocol? Can you foresee any problem with the write-once cache approach on bus-based multiprocessors? If so, suggest a solution.	**06**
(c)	How does instruction pipelining enhance system performance? Elaborate your answer using RISC instruction stages.	**06**

**********End of Paper**********