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Charts and Tables located in aap75_jbs55_Project2_Data.pdf

From the data we received in Experiment 1, we tested different cache and block sizes to see their general trends. The easiest to see is that whenever you increase the size of the cache, both the L1 miss rate and the total number of cycles will decrease. The other relevant information from this data is that whenever the byte size of the blocks increased, it tended to decrease the number of cycles as well as the L1 miss rate. However, having a bigger block size when your cache is small (256 Byte block size with a 1KB cache), the miss rate was large since there were not many blocks to be placed in the cache so it will cause a lot of thrashing which can be seen in the high miss rate. However, if you have enough room with a larger cache, increasing the block size will usually help because of spatial locality. Also, the trends for the cycle times mirrored the miss rate for the L1 cache because there is a steep penalty of 100 cycles for missing the cache rather than hitting it.

In experiment 2 we looked at the impact an L2 cache had on cycle counts and how different block and cache sizes impacted the L1 and L2 miss rates. The L1 miss rates were the same as those in Experiment 1 and the data overall showed the consistent correlation that Increasing cache sizes would result in lower miss rates in the cache whose size was increased and lower cycle counts. L2 miss rates trended up when the size of the L1 cache was increased. There were less misses since the L1 miss rates went down so more of the L2 cache accesses were ***first time*** L2 accesses which are always misses. With the different traces the results jumped around a bit. For example with a 1KB L1 cache long trace 2 performed much better with 4B and 256B block sizes and worse with 16B and 64B block sizes. This suggests that either picking and choosing with little regard for spacial locality or taking a lot more in each block is a better strategy than taking middle amounts for some processes. If you know what processes will be using a certain design choosing cache and block sizes will be easy using this data.

Experiment 3 compared L1 miss rates when L1 associativity was changed. Overall we saw that miss rates trended down when the associativity decreased though not by huge margins. The jump from an associativity of 1 to 4 was also much more impactful than the jump from 4 to 8 suggesting that maybe a lower associativity is fine as long as it is greater than 1. If increasing associativity is expensive in price or complexity it is probably not worth increasing it above 4.