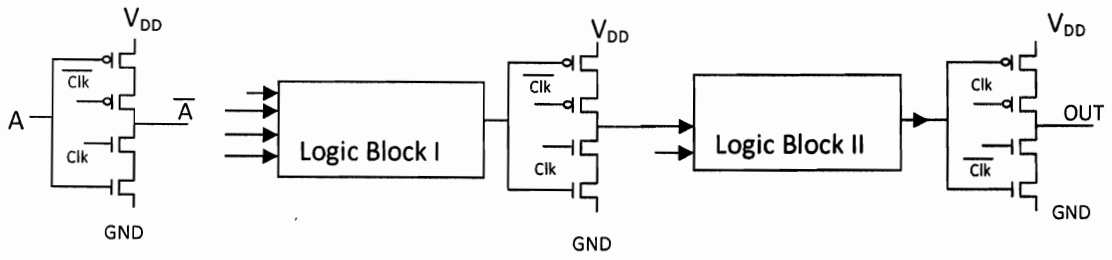
Electrical Engineering Department

EEL329 **Major** **Time:2hrs Marks:40 Date:6/5/2010**

Q1. All five inputs A, B, C, D and E are taken through appropriate C^2MOS latch and applied to logic blocks. One example is shown for input A. OUT=(AB+CD)+E. Design the pipe line for maximum clock frequency.
Design the logic blocks using (a) Static CMOS circuits and (b) Dynamic logic circuits.
Compare the two realizations in terms of (i) speed, (ii) area and (iii) power dissipation.

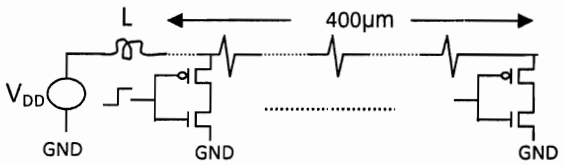


[4+5+4+2+4=19]

Q2. (a) Does the Mirror full adder circuit have static power dissipation?

(b) Given $t_{carry}=t_{add}$ find the condition when carry save multiplier will be faster than array multiplier.

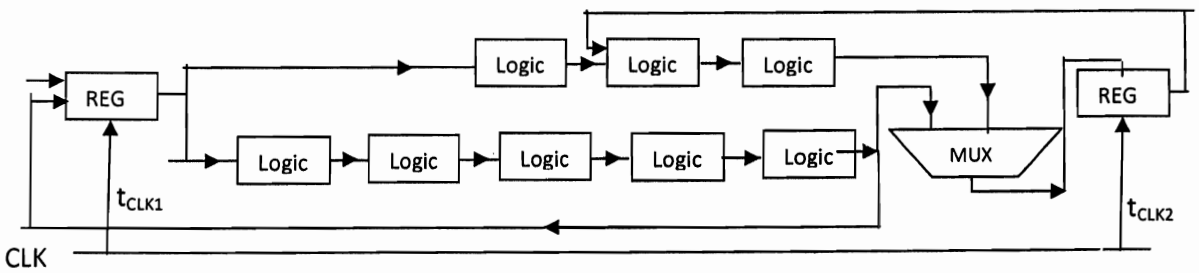
(c) A 0.4 μm wide wire of length 400 μm is used for power bus. The inductance L=2 nH is associated with V_{DD} pin. 32 inverters (with W_p =1.3 μm and L_p=0.13 μm) are connected are connected to the power bus. Half of which is switching high simultaneously in 100 psec time. What is the worst case power drop near the 32nd inverter? Given: Metal wire thickness =0.8 μm and sheet resistivity R□ = 54 mΩ/□, V_{DD}=1.8V and K_p' =27 μA/V^2.



(d) Given a long wire of length 20mm you have to insert buffers. Would you insert equal sized buffer?

[2+3+5+2=12]

Q3.



Given: $t_{c\text{-}q}=t_{logic}=t_{setup}$ =1unit time and t_{MUX} =2 unit time. Determine

(a) Minimum clock period when clock skew is zero.

(b) Maximum positive clock skew that can be tolerated before the circuit fails.

(c) Maximum negative clock skew that can be tolerated before the circuit fails.

[3+3+3=9]