Operating Systems

EEL 602

Major (2008)

F.M=40 Time: 2 hr

1 (a) Some DMA controllers support direct virtual memory access, where the targets of I/O operations are specified as virtual addresses and a translation from virtual to physical address is performed during the DMA. What are the advantages of providing this functionality? (2)

1 (b) Sometime code to be executed in response to an interrupt from a device controller is broken into two parts. How are these parts executed? What is the advantage of this design? (3)

2 Provide a schematic design of a block device driver for an OS of UNIX flavor. (5)

3. Compare the performance of C-SCAN and SCAN scheduling assuming a uniform distribution of requests. Consider the average response time, variation in response time and effective bandwidth for data transfer. How does performance depend on the relative sizes of seek time and rotational latency? (5)

4 (a) Rate monotonic scheduling works with the assumption that every time a process acquires the CPU, the duration of the CPU burst is the same. Is this statement true? Illustrate your answer with the help of examples. (3)

4 (b) Can we achieve 100% processor utilization with EDF scheduling? (2)

S (a) Open-file table is used to keep track of files which are currently open. How is this table organized? What information should be maintained in this table? (3)

5(b) A designer proposes to store name of the creating program with the file's attributes. Is there any justification for his proposal? (2)

6. (a) Assume that we have a demand-paged memory. The page table is in registers. It takes 8 ms to service a page fault if an empty-frame is available or if the replaced page is not modified., and 20 ms if replaced page is modified. Memory access time is 100 ns. Assume that the page to be replaced is modified 70% of time. What is the maximum acceptable page fault rate so that effective memory access time is no more than 200 ns? (3)

6 (b) What kind of hardware support is required for implementing demand paging? (2)

7. A single lane bridge connecting two villages X and Y can become deadlocked if X-bound cart and Y-bound cart get on the bridge at the same time. Design an algorithm that prevents deadlock using semaphores.

8 (i) How can you use message passing for process synchronization?

8 (ii) What are the steps involved in creation of a process? (2.S x2)