EEL 832	CAD of VLSI	Major	100 marks	120 minutes

Answer briefly and to the point.

Q. 1. The channel has pins as follows: TOP = (1, 1, 3, 2, 3, 4, 5. 3, 5, 7, 7, 3), BOT = (2, 6, 4, 1, 6, 3, 3, 7, 8, 8, 5). The channel is to be routed in two layers with restricted doglegging and the reserved wiring model.

(a) Write the HCG and VCG for the channel, as matrices. Mark the node numbers on the left and top of the matrices (marks will be deducted if this is not done).

(b) Determine lower bounds on the number of tracks using the HCG and VCG.

(c) How would this bound change if restricted doglegging was not permitted ?

(40 marks)

Q. 2. A 1 GHz clock is used to latch the output of a MAC unit on a 4-cycle path. The flip-flops used all have setup and hold times of 0.1ns and 0.05 ns, respectively. If the MAC unit gets an input at t=0, determine the latest time of arrival of the MAC output, as well as the time till which it is required to be available for proper operation.

(5 marks)

Q. 3. The AND gate shown drives an interconnect and the output is latched. If V_{dd} is 1V, $\sigma_N^2 = 0.0322$, and the capacitance driven by the gate is 1 pF, what is the maximum frequency at which the gate can be operated for reliable operation ?

(10 marks)

Q. 4. What is the entropy of the output Y that is described by the following Karnaugh map ?

	00	01	11	10
0	0	0	X	1
1	X	1	1	0

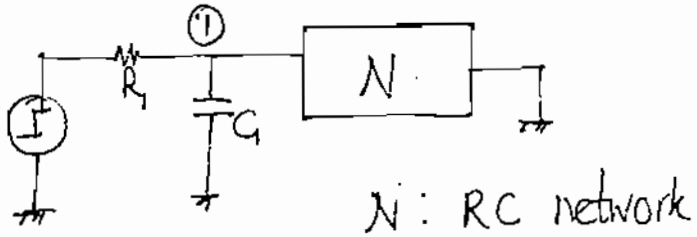
(5 marks)

Q. 5. A slicing floorplan tree has N nodes, including the root and operators. How many blocks are there in the floorplan ?

(5 marks)

Q. 6. In figure FQ6, the AWE approximation for the homogeneous part of V_1, i.e. $V_{h1}(t)$ is given by $V_{h1}(t) = 2e^{-t} + 3e^{-3t}$. What is the magnitude of the step input ?

(5 marks)



Q. 7. Two subtrees T1 and T2 have delays t_1 and t_2, and need to be driven by a clock. The skew needs to be balanced by adding two interconnect pieces from the source. Tree T1 is connected to the source by a piece with size L_1 x W_1, while Tree T2 is connected to the source by a piece with size L_2 x W_2. The trees have root capacitance of C1 and C2, respectively. Determine a relation between L_1, W_1, L_2, and W_2 for the skew to be zero. The interconnect has a resistivity of ρ, the oxide thickness is t_{ox}, and the dielectric constant of the oxide is ε.

(20 marks)

Q. 8. It is required to route the signal ***s*** to all 6 points in Fig. FQ8 so that the delay from ***s*** to any point is at most 13.26 L. What would be the maximum length of such a tree ? Explain your answer briefly.

(10 marks)

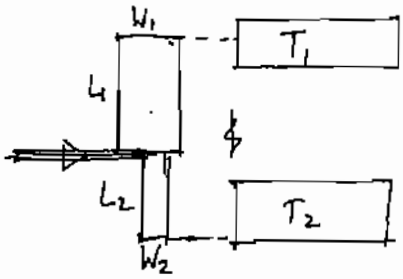


Fig. FQ7.

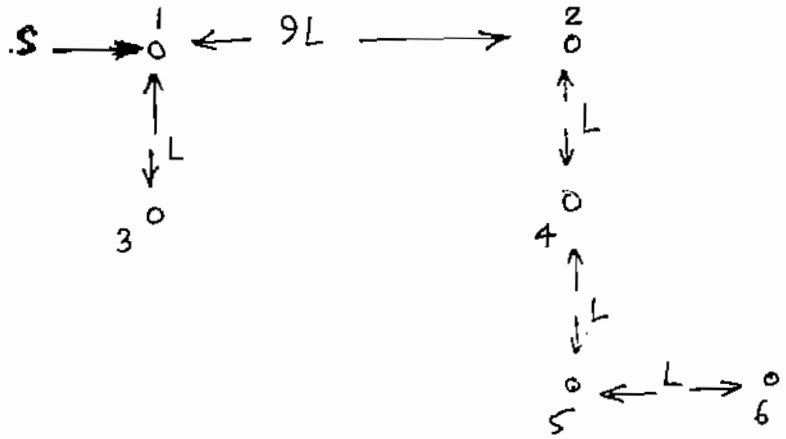


Fig. FQ8.

P.T.O.