ELECTRICAL ENGINEERING DEPARTMENT

EE734 MOS LSI

Date: December 1, 2006 Time: 1:00PM to 3:00PM

Q1. a) We discussed about the address multiplexing in a DRAM. Draw a block diagrammatic set up for generating the relevant Row Address and Column Address signals/clocks to carry out READ and WRITE operations after a Address Transition is detected and the memory operation is enabled.

b) In order to reduce the overhead on address decoding one of the schemes used is to detect the address transmission. This is useful in page mode of operation when the x-address remains the same while the y address is changed. Propose a scheme that can be used to detect the address transition and give its CMOS realization. Hint: Detection of address transition means detection of non identical values at successive clock instants.

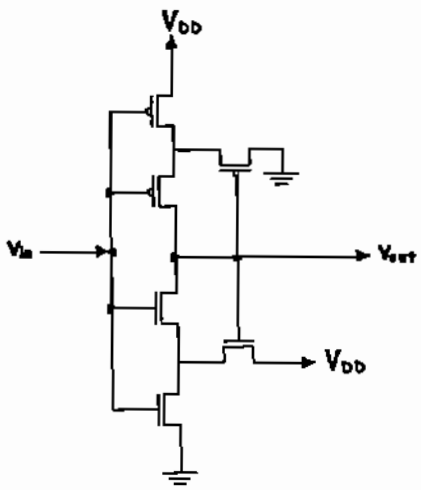
— (20)

Q2. a) You are to design a six transistor CMOS SRAM cell. In designing the W/L ratios of the various transistors enunciate the criterian to be used and explain.

b) Draw the transfer characteristics of the CMOS logic circuit shown below and identify its function.

(c) We discussed dynamic and static combinational circuits in the class, write a few words on static and dynamic sequential circuits with examples.

c) Design a CMOS gate that gives at the output $\overline{A}BC + \overline{A}BD$ and identify its logical effort.



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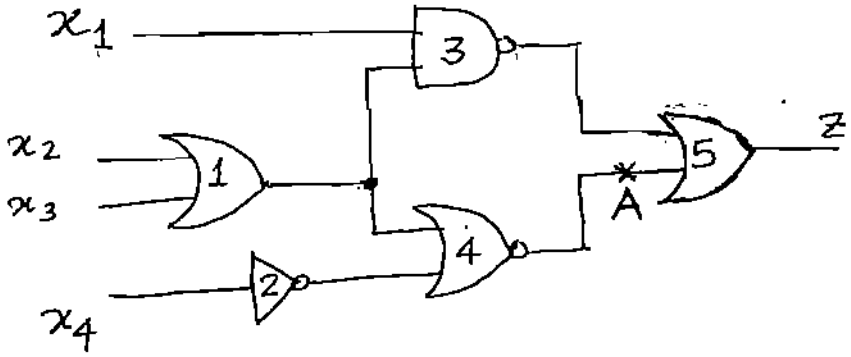
Q3. For the combinational circuit find the input test vector to detect s-a-0 and s-a-1 faults at the node A.

— (10)



BEST OF LUCK