CSL 812 - System Level Design and Modelling
29 April 2008, 3:30 PM to 5:30 PM
Major Exam

1. (20 Marks) An application has a frequently executed loop of the form:

```
for (i = 0; i < 10000; i++)
  a = a + x[i] + y[i+1] + z[i+2] + w[i+3] + v[i+4];
```

   Analyse the advantages and disadvantages of extending a standard RISC processor with a single instruction that executes the one statement in the loop body.

2. (15 Marks) Explain why several types of processes are present in SystemC whereas they are not present in HDLs such as VHDL.

3. (10 Marks) What semantic issues need to be clarified when concurrency and hierarchy are introduced into FSMs?

4. (30 Marks) Given a C program and a processor, we would like to estimate the energy consumed when the program is executed on the processor. Discuss in detail three different strategies for doing this energy modelling, and the advantages and disadvantages of each.

5. (15 Marks) State three different program features that can lead to non-determinism in KPNs, along with clear examples of why non-determinism is caused when the feature is present.

6. (15 Marks)

   In HW/SW partitioning, we are evaluating whether to map a SystemC process to HW or SW. If low power is the objective, where should we map the process? Explain your decision.

7. (15 Marks)

   Consider the following loop:

```
int a[1024], b[1024], c[1024];
...
for (i = 0; i < 1024; i++)
  a[i] = b [c[i]];
```

   Assume we have a scratch pad memory and a data cache in our embedded architecture, both with size = 1024 integers. What data should we store in the scratch pad memory and what data should we bring through the data cache? Justify your decision.