*Name:*_____ *Entry Number:*_____

Major Examination: EEL843

Max. Marks: 50
Time: 2 Hours

Note: *(i) Answer all the questions*
(ii) Draw neat waveforms to scale
(ii) Assume suitable data, if required.
(iii) In case of design problems justify the converter topology selection and assumptions made in the design process.

1. Design a switeh-mode de-dc boost converter to meet the following speeifieations: Load voltage of 42 V and supplying a power demand of 20 Watts; DC battery voltage is 24 V; switehing devices will give better performance @ 10 kHz frequency; Average inductor current should not be more than 150% of constant load current; Inductor ripple current is 2.5 times the average inductor current, load voltagc ripple should be less than 5 %; switching deviees utilization becomes poor for the active duty ratio beyond 0.4. Final design parameters must satisfy the constraints mentioned in the problem. (8)

2. What should be constraint on the number of turns of the reset winding of the forward converter? Justify why this constraint needs to be fulfilled in the design stage. Establish a mathematical relationship that supports your justification. (8)

3. Design an isolated converter to meet the following specifications: Dc battery voltage is 24 V, Load power: 200 Watts; Load voltage should be 20 V when it is supplying 10 A. Converter switching frequeney is 40 kHz, maximum allowable inductor eurrent ripple is 5 % of average load current, maximum load voltage ripple is 2 %. (Constraints: Use of additional reset winding is not allowed, the switeh voltage stress should not exceed 24 V, load side energy transfer diode voltage rating should not be more than input de battery voltage). (12)

4. Design an isolated converter topology to meet the following specifications:
DC load voltage=225 V @ 4.44 A, DC input source voltage is 180 V. Assume continuous inductor current and isolation transformer turns ratio N_p: N_s= 1:1; Switching frequency= 50 kHz, Maximum load voltage ripplc= 2 %; Maximum inductor eurrent ripple= 10%, Transformer core utilization must be 100 %. (12)

5. Compare the capabilities of the circuit and system level simulators, which are commonly used in the power electronie circuit's simulation. (10)

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