ELECTRICAL ENGINEERING DEPARTMENT

EEL 329 MAJOR.

TIME : 2hr
MARKS : 35
DATE : 8/5/2009

Q1.

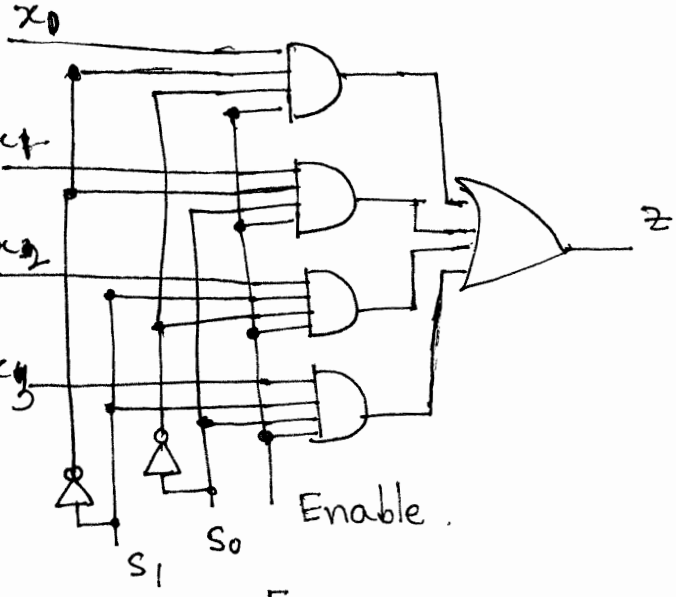


Fig 1 shows a gate implementation of a 4 input MUX. Realize the mux with (a) DOMINO CMOS and (b) static CMOS. Compare their performances in terms of delay and power dissipation. (5 + 5 + 2 = 12)

Fig 1.

Q2.

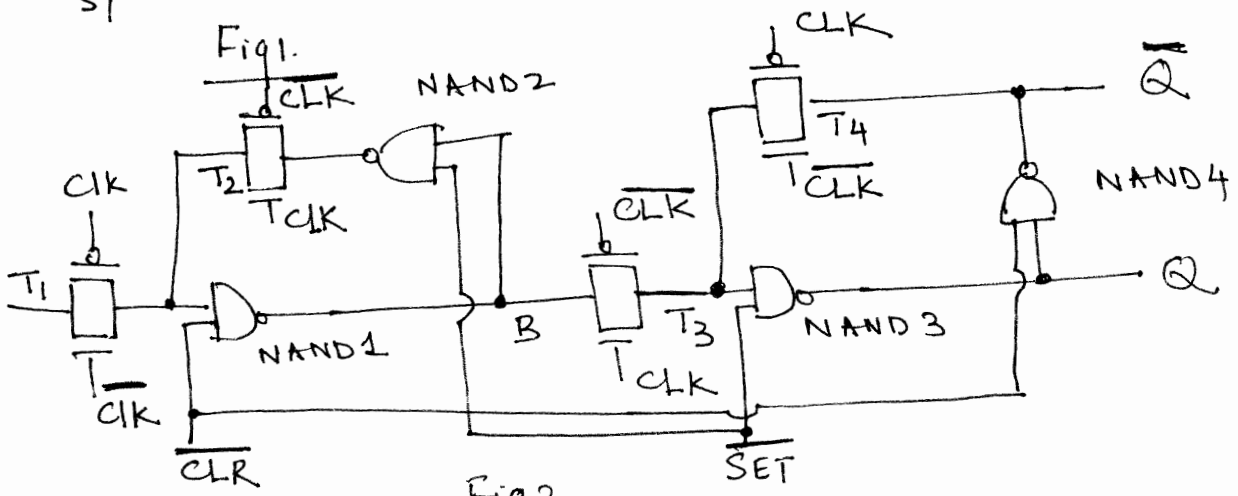


Fig 2

Fig 2 shows an edge-triggered D flipflop. Find (i) setup time (ii) hold time and propagation delay time of the flipflop. Draw the wave form of clk and Q. (2 + 2 + 2 + 1 = 7)

Q3.

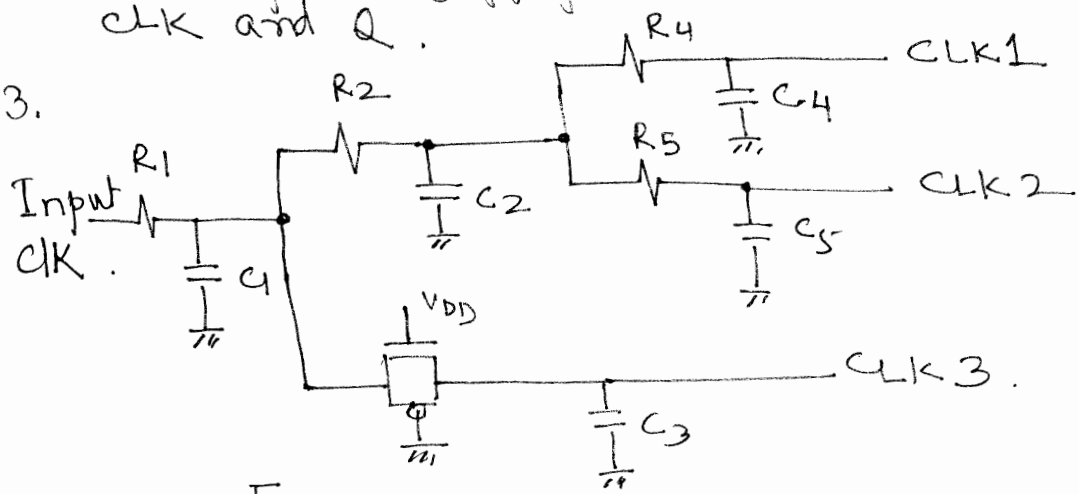


Fig 3

Fig 3 shows a clock distribution network.

(a) Write the expressions for the time constants associated with CLK1, CLK2 & CLK3

(b) If $R_1 = R_2 = R_4 = R_5 = R$ and $C_1 = C_2 = C_3 = C_4 = C_5 = C$ what value of R_3 is required to balance delays of CLK1, CLK2 and CLK3

(c) For $R = 750\Omega$, $C = 2000$ fF what (W/L) is required for the transmission gate to eliminate skew? Given: $K_n' = 80\mu A/V^2$, $K_p' = 27\mu A/V^2$ and $V_{DD} = 1.8V$.

(3 + 2 + 3)

Q4 (a)

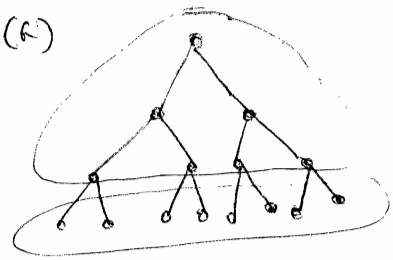
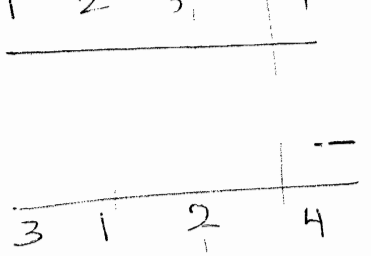


Fig 4

Consider the binary tree shown in Fig 4. Apply Kernighan-Lin Algorithm to this graph. The initial partition is given ___ all the leaves are in one partition and the rest of the nodes are in the other partition

(b)



A channel with a side pin is shown. Draw the HCG and VCG of the channel.

(4 + 4)