EEL308: Computer Architecture

MAJOR

Answer all questions *Max. Marks: 40;* *Time: 2hrs*
Note that all parts of a question must have the answers together.

Q1 Here is a series of address references given as word addresses:
1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17

Assuming a direct- mapped cache that is initially empty, with four-word blocks and a total size of 16 words, label each reference in the list as a hit or a miss and show the final contents or *final state* of the cache. (4+2)

Q2 For each pipeline register in Fig.6.25 label each portion of the pipeline register with the name of the value that is loaded into the register. Determine the length of each field in bits. For example, the IF/ID pipeline register contains two fields, one of which is an instruction field that is 32 bits wide. (3+2)

Q3 A friend is proposing that the control signal MemtoReg to be eliminated. The multiplexor that has MemtoReg as an input will instead use the control signal MemRead Will your friends' modification work? Consider both datapaths.

Determine whether any of the control signals (other than MemtoReg) in the single-cycle implementation can be eliminated and replaced by another existing control signal. Why or why not? (3+3)

Q4 Consider executing the following code on the pipelined datapath of Fig.6.46 (See Notes) :

Add $1, $2, $3
Add $4, $5, $6
Add $7, $8, $9
Add $10, $11, $12
Add $13, $14, $15

(a) At the end of 5th cycle of execution, which register is being read and which register will be written?
(b) Explain what the forwarding unit is doing during the 5th cycle of execution. If any comparisons are being made, mention them.
(c) Explain what the hazard detection unit is doing during the 5th cycle of execution. If any comparisons are being made, mention them. (2x3=6)

Q5 You have been given **18** (you may not need all of them) **32K x 8**-bit (32K byte) SRAM chips to build a cache memory for a processor with a 32-bit address. Find out the largest size (i.e. the largest size of the data storage area in bytes) of cache memory that you can build for the following two cases using components given to you.

(a) Direct -mapped cache with one-word (=32-bit) blocks?
(b) Direct -mapped cache with four-word blocks?

$2^2 8 + 15^3 + 14^4 + 15^5 + 14 + 12 + 7$

$= 105$

Give breakdown of the address into its cache access components (i.e. number of bits for tag, index, block offset, and byte offset). How many chips are required for data area and how many chips for overhead storage are required for the above two cases?

Give your final answer in the following format:

Case(a) :

Address breakup, No. of Chips for data area =? No. of Chips for overhead storage = ?

Case(b) :

Address breakup, No. of Chips for data area =? No. of Chips for overhead storage = ?

(3+3)

Q6 Assume that we change the delays of the following major functional units in **single cycle implementation** (See Fig 5.29) by using a different type of adder:

ALU: 2 nanoseconds (ns)

Adder for PC+4: X ns

Adder for branch address computation: Y ns.

The delay of the multiplexors, control unit, PC access, sign extension unit, and wires is considered to be negligible.

(a) What would the cycle time be if X=3 and Y=3? (b) What would the cycle time be if X=5 and Y=5? (c) What would the cycle time be if X=1and Y=8?

(6)

Q7. Add comments to the following MIPS code and describe in one sentence what it computes. Assume that $a0 is used for the input and initially contains n, a positive integer. Assume that $v0 is used for the output. (4+1)

```
begin:   addi $t0, $zero, 0
         addi $t1, $zero, 1
loop:    slt $t2, $a0, $t1
         bne $t2, $zero, finish
         add  $t0, $t0, $t1
         addi $t1, $t1, 2
         j   loop
finish:  add $v0, $t0, $zero
```