Computer Architecture (EEL 601)

Major (2006)

F.M = 40 Time: 2hr

Q1. (a) What are the differences between super-scalar and SIMD processors?
(b) How can circular addressing mode be supported in hardware?
(c) What are the advantages of hierarchical bus structure?
(d) Can code re-ordering effect performance of cache memory? How?
(e) What is a 'barrier'?

(2x5 = 10)

Q.2 Assume a directory-based cache coherence protocol. The directory currently has information that indicates that processor P1 has the data in exclusive mode. If the directory now gets a request for the same cache block from processor P1, what could this mean? What should directory controller do?

(6)

Q.3 A dynamically scheduled superscalar processor, having deep pipeline, will be unlikely to ensure performance enhancement for simultaneous multi-threading. Is this statement true? Discuss considering different architectural variants.

(4)

Q.4. 21264 uses virtually addressed instruction cache. Is it that virtually addressed caches need to have more tag bits ~~that~~ than physically addressed cache? Why?

(4)

Q.5 Consider the following loop: for (i = 6; i <= 100; i = i+1) {

Y[i] = Y[i-5] + Y[i]; }

Can this loop be unrolled for exploiting ILP? How? (4)

Q.7 A single predictor predicting a single branch instruction is more accurate than is that same predictor serving more than one branch. Discuss. by providing examples of (i) 1-bit predictor sharing that reduces misprediction rate & (ii) 1-bit predictor sharing that increases misprediction.

(6)

Q.8 (a) Explain RAID organisation of disc
(b) Describe different techniques for hit time ~~reduction~~, reduction of cache

(3+3)