MAJOR PART

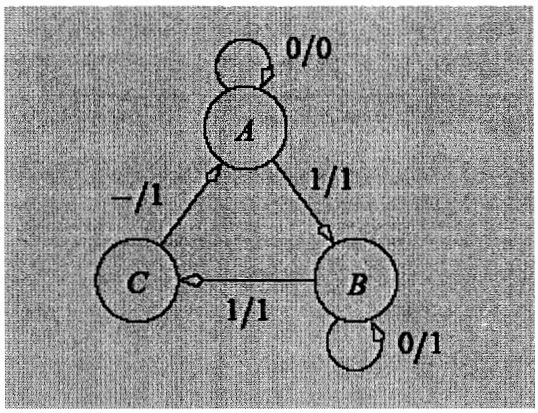
EEL324 Digital Hardware Design

Time: 2 Hour **Max. Marks: 40**

NAME: **Entry No.**

N. B.:- Do all rough work in the continuation sheet provided. This is **open book / notes examination**, but no **transfer** of notes to each other. Write calculation and result neatly on this sheet at appropriate places and return.

Q1 (a): - Convert the following Mealy machine to Moore machine:



Answer: Draw the diagram below:

b): For the following state assignment and transition table (Of synchronous sequential machine) construct excitation and output maps for D flip-flop. Draw the diagram (using D flip-flop) of resulting circuit. **(2 + 5)**

y_1y_2	$(y_1y_2)^+,z$ X = 0	x = 1
A→00	01,0	00,0
B→01	01,0	10,0
D→11	01,0	10,1
C→10	11,0	00,0

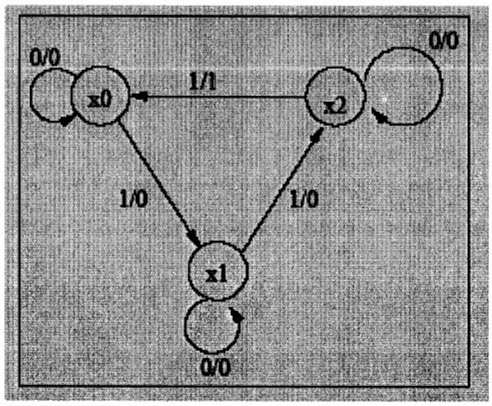
Answer:

Q2:-For the finite state machine M = ($\sum$, Δ, X, x_2, g, f) where:

$\sum = \{0, 1\}$ $\Delta = \{0, 1\}$ $X = \{x_0, x_1, x_2\}$

$g(x_0, 0) = x_0$, $g(x_0, 1) = x_1$, $g(x_1, 0) = x_1$, $g(x_1, 1) = x_2$, $g(x_2, 0) = x_2$, $g(x_2, 1) = x_0$

$f(x_0, 0) = 0$, $f(x_0, 1) = 0$, $f(x_1, 0) = 0$, $f(x_1, 1) = 0$, $f(x_2, 0) = 0$, $f(x_2, 1) = 1$



Find a corresponding Petri-Net. **(5)**

Answer:

Q3:- The following VHDL program is a structural description of a circuit that uses NOR2, AND2 and NOT components. In the port map statements the output signal is the last signal. Draw the circuit that is described and give the function table for the circuit.

(5)

```
LIBRARY  IEEE;
Use IEEE. Std._logic_1164. ALL;

ENTITY   mystry_ckt IS
PORT (
      D, C          : IN Std_logic;
      Q, Q_b        : OUT Std_logic);
END  mystry_ckt;

ARCHITECTURE structural OF mystry_ckt IS
SIGNAL R. S, D_b : Std_logic;
BGIN
AND_1      : AND2 port map (D, C, S);
AND_2      : AND2 port map (C, D_b, R);
NOT_1      : NOT port map (D, D_b);
NOR_1      : NOR2 port map (S, Q, Q_B);
NOR_2      : NOR2 port map (Q_b, R, Q);
END structural;
```

Answer:-

Q4:- A sequential system is the controller for stamp vending machine as shown in the diagram. There is one selector to select between two choices of stamps. The values of stamps are Rs. 1.0 and Rs. 1.50. The machine can accept Rs. 0.50, Rs. 1.00 and Rs. 2.00 coins only. Machine starts automatically by insertion of first coin and goes to initial states.

The digital circuit attached with the sequential machine computes the incoming coins and gives this information as shown to the machine. If customer changes mind and presses push button switch he gets back his money. He also gets the information about the availability of change and in case he pushes the activation switch in absence of change he gets the stamp but loses the change. If change is there (and sum is more than the cost of stamp) he gets it along with the desired stamp on pressing activation switch. One stamp only can be obtained at a time and maximum Rs. 2.00 can be inserted.

Give a state diagram for controller. Also assume that coins can be inserted in any order. Clearly mention any new assumption which you make to have simplicity. Neat and clear state-diagram will get better marks. Use the following notations for your controller:

INPUTS: - MR → money return, **CT** (coin type) → € (0.50, 1.00, 2.00), **ST** (stamp type) → (1.00, 1.50), **AC** (activation switch input), **CA** (change available input)

OUTPUTS: - RS_1 (release stamp 1 Rs. 1.00), **RS_2** (release stamp 2 Rs. 1.50),

RC → return change,

RAC → return all coin (on MR returns all coins as the person might have changed the mind). **(7)**

Q5:- Write the collision vector for the reservation table below: **(6)**

Stages	→ Time							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
S_1	X			X				
S_2		X			X			
S_3	X					X		
S_4		X					X	
S_5	X		X					X

Answer: **(a) Collision vector (in C_7 C_6 …C_1 format) =**

(b) Draw the state diagram for this pipeline below:

(c) Simple cycles:

(d) Greedy cycles:

(e) Find a latency sequence that can achieve the MAL. Is delay needed here?

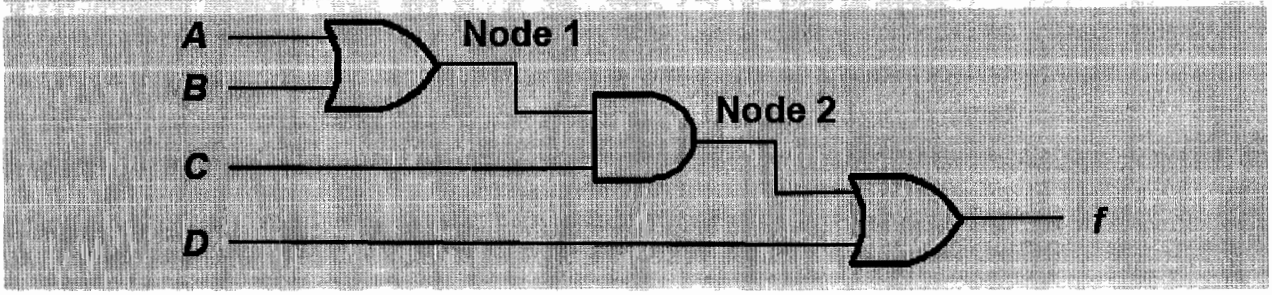
Q6 (a):- If a function is as below:

F (w, x, y, z) = ∑m (5, 7, 8, 10, 14, 15). Represent as complete **BDD** below:

(b):- Write the above function's **ROBDD** in the space below:

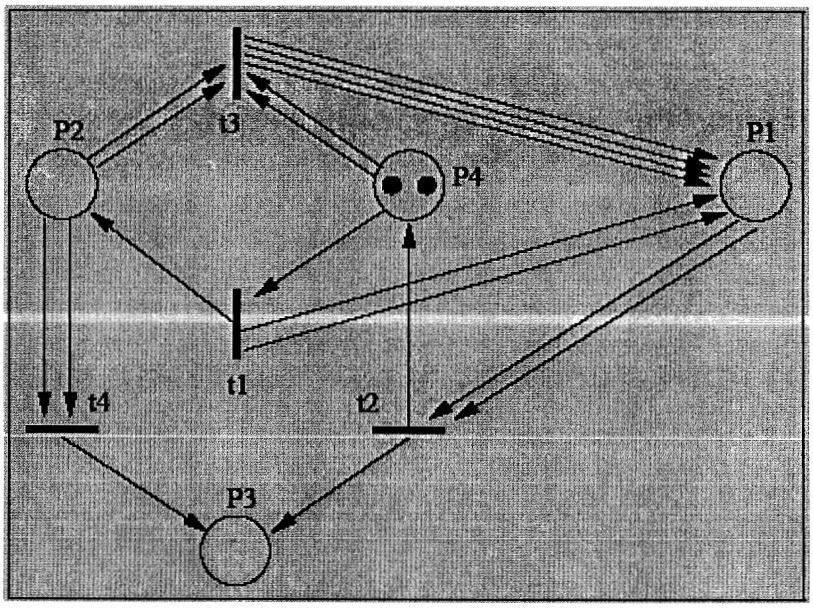
(c): **(2 +2 + 2)**

For the following circuit, give a test vector that will detect a "stuck at 1" fault on Node 2.



Answer:

Q7: - For the following Petri net construct the coverability-tree. **(4)**



ANSWER: