Indian Institute of Technology, Delhi
EEL782: Analog Integrated Circuits
Final, May 4, 2009

Answer all the questions. Read the instructions carefully. No books or notes allowed. You should have a working calculator. Full marks is 80. Approximate answers are ok. Incompatible units or unrealistic answers will invoke the wrath of the examiner. Good luck!

Part A: Objective type questions (1 to 12)

Each question or fill-in-the-blank carries 1 mark. Total 20 marks.

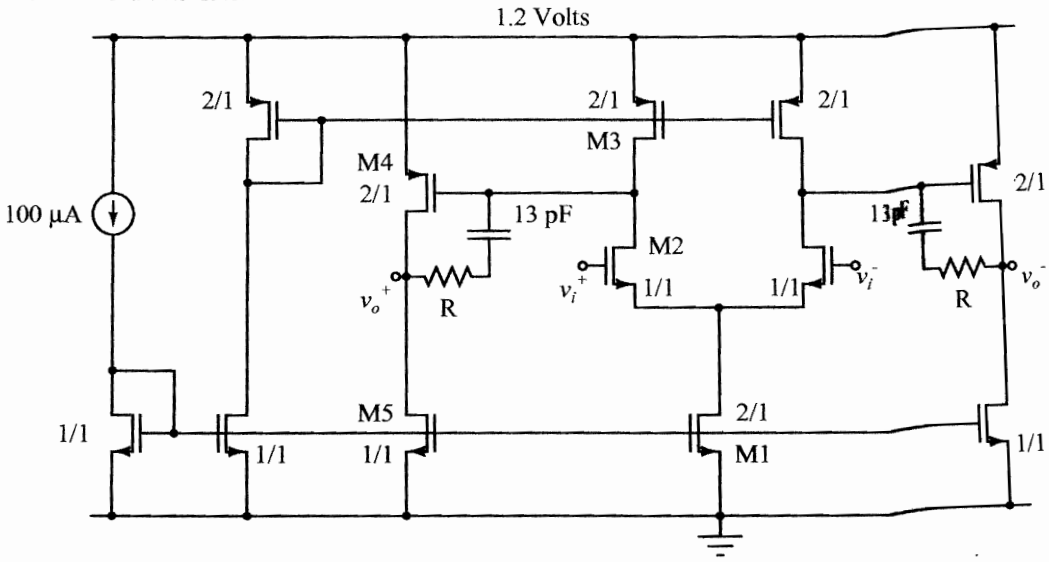
1. The approximate gain for a single stage amplifier, assuming an infinite load impedance is _____.
2. The effect of designing an MOS device with multiple fingers is a reduction in: (a) C_{overlap} (b) C_{junction} (c) C_{gs} (d) C_{gd}
3. Through fingering, the above parasitic capacitance can at most be reduced by a factor of _____.
4. To match two capacitors, both their _____ and _____ need to be matched.
5. A capacitor of 100 fF has dimensions of 10 μm $\times$ 10 μm. A 200 fF capacitor matched to the previous capacitor will be of dimensions _____$\times$ _____.
6. If an opamp designed with an input differential pair of size 10 μm $\times$ 1 μm shows an input offset voltage of 5 mV, the expected input offset voltage of an opamp with an input differential pair of size 20 μm $\times$ 2 μm is _____.
7. To minimize the effect of a linear oxide gradient, the most commonly used layout technique is _____ layout.
8. The unit for root mean squared noise voltage per unit frequency is _____.
9. Common mode feedback is mandatory for any opamp design. (True / False)
10. Common mode feedback is needed only when we intend to place the opamp in a closed loop configuration. (True / False)
11. A feedback loop senses the current at the output and feeds back a voltage. The units for gain of the forward block are _____, and the units for gain of the feedback block are _____. The output impedance of the closed loop system will _____ by a factor of (1+loopgain), and the input impedance of the closed loop system will _____ by a factor of (1+loopgain).
12. The two halves of a fully differential circuit are excited by the same input signal. The currents through the wires connecting the two half circuits to each other will have components only at _____ and the _____ harmonic frequencies, and the voltages on those wires will have components only at _____ and the _____ harmonic frequencies.

Part B: Regular questions (13 to 18)

(60 marks)
For all MOS devices in this section, assume they are in strong inversion and in saturation. The current, I_D, through an nMOS device, as a function of V_{GS} and V_{DS} is given by:

$$I_D = \mu C_{ox}/2 \cdot W/L \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Modify the above equation appropriately for your own purposes for pMOS devices. V_T is 0.3 Volts, $\mu C_{ox}/2$ is 10 mAmp/Volt^2 for nMOS devices, 5 mAmp/Volt^2 for pMOS devices. λ is 0.5 Volt^{-1} for all devices.



13. Assume both the input and output nodes of the circuit to be at 0.6 Volts. Evaluate the DC operating point voltages at all the different nodes in the circuit. Assume body effect of the devices to be negligible. Are all the devices indeed in strong inversion and saturation? Find out the small signal g_m and r_{ds} of M_1, M_2, M_3, M_4 and M_5. (4 + 1 + 0.5×10 = 10 marks)

14. Draw the differential mode small signal half-circuit. Compute the differential mode gain of the circuit. (3 + 7 = 10 marks)

15. Draw the common mode small signal half-circuit. Compute the common-mode gain given by $A_c - (v_o^+ + v_o^-)/(v_i^+ + v_i^-)$. (3 + 7 = 10 marks)

16. Evaluate the unity-gain bandwidth of the OTA circuit. Compute the phase margin of the circuit, if the load capacitance is 7.5 pF on each output node. Assume all other parasitic capacitances are negligible. Also assume that the value of R is such that it cancels out any zero in the transfer function. Use appropriate engineering approximations and intuitions. (5 + 10 = 15 marks)

17 Propose a common-mode feedback circuit for the given OTA. (5 marks)

18. Compute the root-mean-squared input referred noise voltage per unit frequency. For each individual MOS device, the mean squared noise current per unit frequency is given by $8/3 \cdot kT/g_m$. Use the small signal differential mode half-circuit for this purpose. (10 marks)