CSL 719 - Synthesis of Digital Systems
22 November 2008
Major Exam. Maximum Marks: 120

1. (15 Marks) Give an appropriate modification of the technology mapping algorithm discussed in class for doing an efficient covering of a combinational netlist (assumed to be a tree) while optimising for delay. That is, the mapped netlist should have minimum delay. (Hint: the way the cost would be combined would be different now, but other parts of the algorithm might be similar).

2. (10 Marks) Explain why the division algorithm based on polynomial algebra is a legal solution to the boolean division problem.

3. (5+5=10 Marks) Explain the significance of functions f under the following conditions:

   (a) $f_x = f_{x'} = g$ (co-factors with respect to x and x' are equal)

   (b) $f_x = 0$ and $f_{x'} = 1$

4. (5+5+10=20 Marks)
   (a) What property of the OBDD graph ensures that it is acyclic?
   (b) Given an ROBDD for function f, explain how to efficiently generate the ROBDD for f'.
   (c) Given ROBDDs for functions $f(a, b, c)$ and $g(d, e, f)$ give a strategy for constructing the ROBDDs for $f + g$ and $f.g$.

5. (10 Marks)
   In the optimisation loop for 2-level logic, could we have replaced the REDUCE-EXPAND-IRREDUNDANT order by EXPAND-IRREDUNDANT-REDUCE? Explain.

6. (5+5 = 10 Marks)
   (a) In multilevel logic optimisation, explain why the quotient f_i/f_j is guaranteed to be NULL if there is a path in the logic network from i to j.
   (b) What happens to the quotient f_i/f_j if there is a path from j to i?

7. (10 Marks) Explain the advantages and disadvantages of using one-hot encoding for FSM state assignment.

8. (20 Marks) In behavioural synthesis, it is possible that after Datapath and FSM generation, the generated circuit does not meet the clock cycle timing constraints – i.e., there are some combinational paths that do not complete within the clock cycle. Explain why this may happen, and give some suggestions for overcoming them.

9. (15 Marks) Explain the difference in the Common Subexpression Elimination as it is applied to Behavioural Synthesis vs. Logic Synthesis.