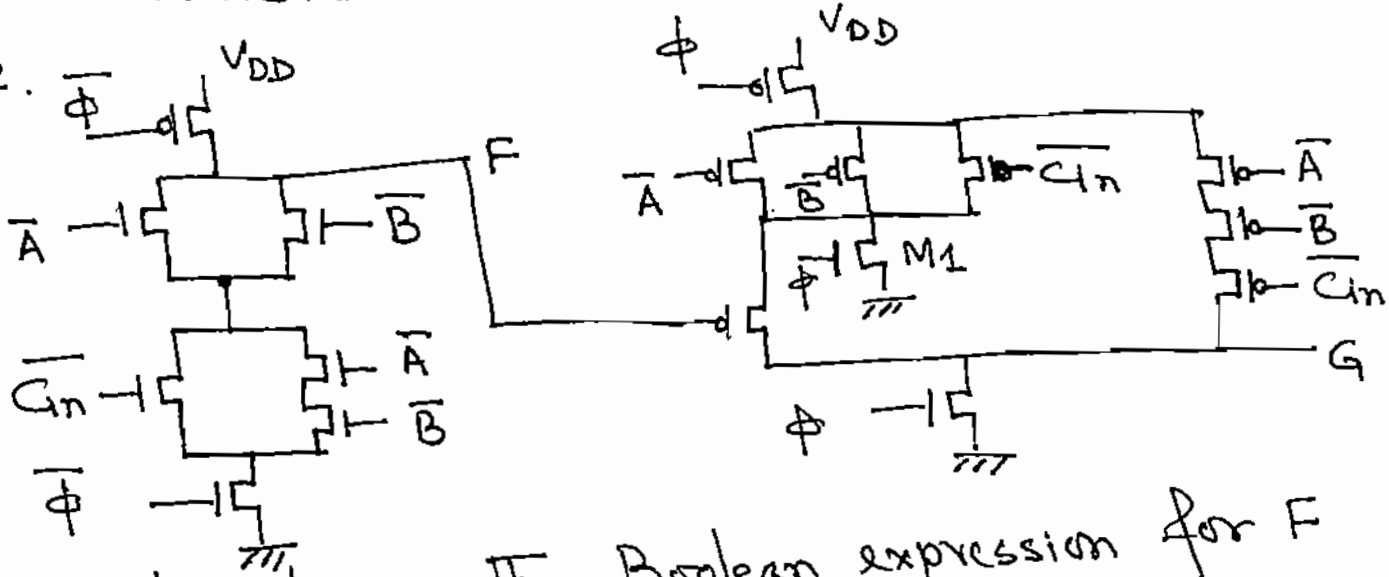
Electrical Engg Department

EE L 329 MAJOR EXAM

MARKS = 35
TIME = 2 hrs
Date : 30/4/08

Q1. Realize $F = \overline{A\bar{B} + A\bar{C} + \bar{A}CD}$ using a static complimentary CMOS gate. Find the $(\frac{W}{L})$ ratio of the NMOS and PMOS transistors. (2+2+2=6)

Q2.



(a) Write down the Boolean expression for F and G.

(b) How can the evaluation phase of F can be speeded up by rearranging transistors? No transistors should be added or deleted or resized.

(c) What is the purpose of transistor M1? Can you achieve this by another way without loading ϕ? (3+2+3 = 8)

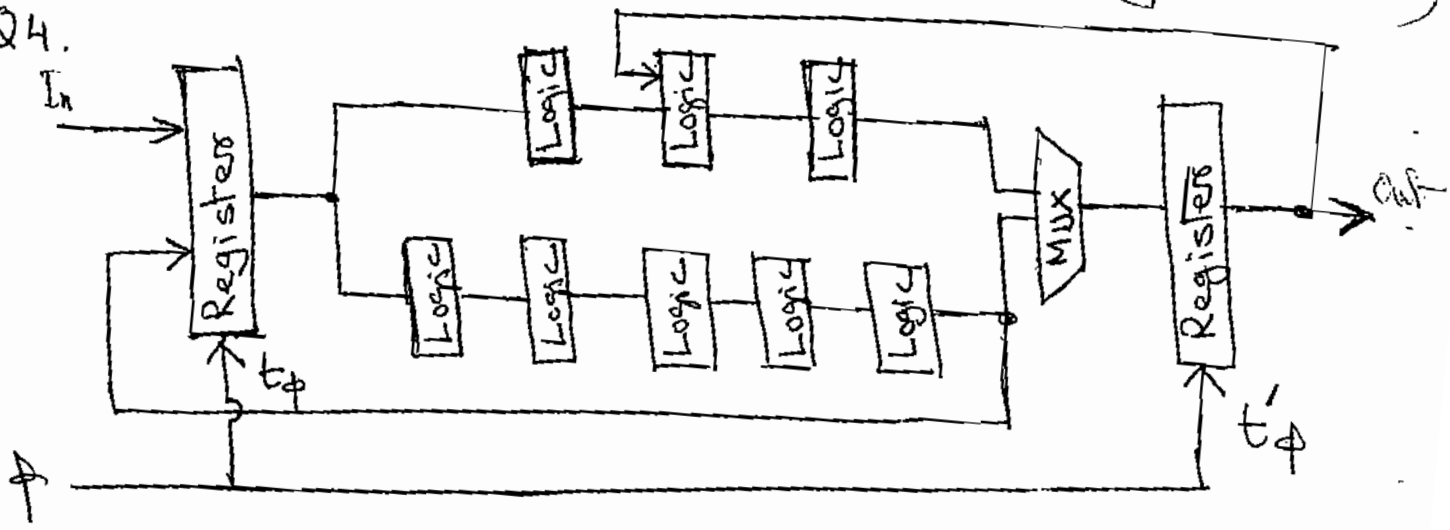
Q3. A two stage buffer is to drive a metal wire of length 1 cm. The first inverter input capacitance $C_i = 10$ ff and propag-ation delay $t_{p0} = 175$ psec when loaded with an identical gate. The width of the metal layer is 3.6 μm. The sheet resistance

(a) What is the propagation delay tw over the metal wire.

(b) Compute the optimal size of the second inverter.

(2'5+2'5 = 5)

Q4.



Assume registers delay, t_r = logic delay, t_L = 1 and MUX delay, $t_{MUX} = 2$.

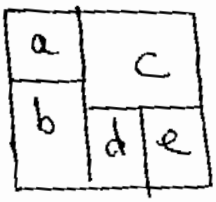
(a) Determine minimum clock period when skew $\delta = t'_\phi - t_\phi = 0$

(b) Determine the maximum positive clock skew that can be tolerated before the circuit fails.

(c) Determine the maximum negative skew that can be tolerated. (2+3+3 = 8)

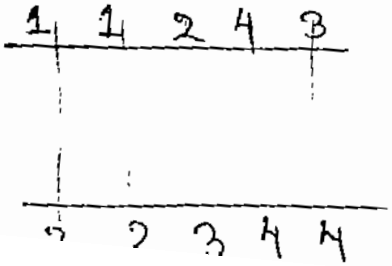
Q5 (a) Given the normalized Polish expression 12 − 34 − 15− obtain the expression 12 − 3 − 4 − 5 −

(b)



Draw the Horizontal dependency graph for the given floor plan.

(c)



Draw the Horizontal and Vertical constrain graphs for the given channel. Can you determine the number of tracks required from the