EEL 832	CAD of VLSI	Major	100 marks	100 minutes

Q. 1. A channel with pins TOP = (1, 2, 3, 0, 3, 5, 3), BOT = (2, 1, 4, 1, 4, 4, 5) is required to be routed in two layers using the reserved wiring model; doglegging is permitted. From the global router, we know that nets 1, 2, and 3 enter from the left, and nets 3, 4, and 5 exit from the right. Route the channel and determine the order of entering and leaving nets. **(15)**

Q.2. Route the channel with pins TOP = (1, 2, 3, 0, 3, 5, 3), BOT = (2, 1, 4, 1, 4, 4, 5) using the NIRVANA wiring model in two layers with restricted doglegging. **(15)**

Q. 3. For Fig. Q3, write the state space equations for the currents in the form $\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{i}_3 \end{bmatrix} = [A] \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + [B] \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$. Determine the values of m_{-1} for the three loop currents.

(15)

Q.4. Write the Lagrangian and the K.K.T. conditions for the problem $\text{Min } x_1^2 + 3x_2^2$ subject to $x_1 + x_2 \leq 9$. Is the problem convex ? **(10)**

Q. 5. The blocks in Fig. Q5 need to be compacted from right to left. Treat the **left edge** of each block as the variable used. Blocks are of fixed sizes as indicated. The spacing between any two edges that are adjacent, i.e. can "see each other", is 5λ, but constraints on crosstalk require that the closest edges of blocks 2 and 5 are at least 32 λ apart. If interconnect delay requires that the closest edges of blocks 1 and 3 are not separated by more than 22λ. Draw the compaction graph and find the critical path. Identify any cycles in the graph. Mark the x-positions of all blocks on the compacted graph (draw a SEPARATE figure). **(15)**

Q.5. A full-adder has input X = (a_i, b_i, c_{i-1}) and output Y = (c_i, s_i), where c and s denote carry and sum bits, and a and b are input operands. Determine H(X), H(Y|X), H(X|Y), and H(Y). **(10)**

Q.6. Answer/comment briefly in about 5 lines each.

(a) An AND gate with a t_p of 4 ns is connected through a short interconnect to a flip-flop with a setup time of 6 ns and a hold time of 2 ns. What is W_{ch} for the equivalent channel ?
(b) Draw the global routing graph for Fig. Q6b.
(c) Indicate the order in which channels/switchboxes should be routed in Fig. Q6b. Identify the switchboxes.
(d) If a clock tree is to be connected to N sinks, what is the complexity of Jackson, Srinivasan, and Kuh's minimum skew clock tree routing algorithm ?
(e) It is not possible to find the AWE approximation for a tank (LC) circuit.
(f) One dimensional compaction can be solved optimally in polynomial time.
(g) BRSTs can be used to route clock trees.
(h) What is the longest possible VCG path for a channel that has no edges in the HCG ?

(5 + 3 + 4 + 2x4)

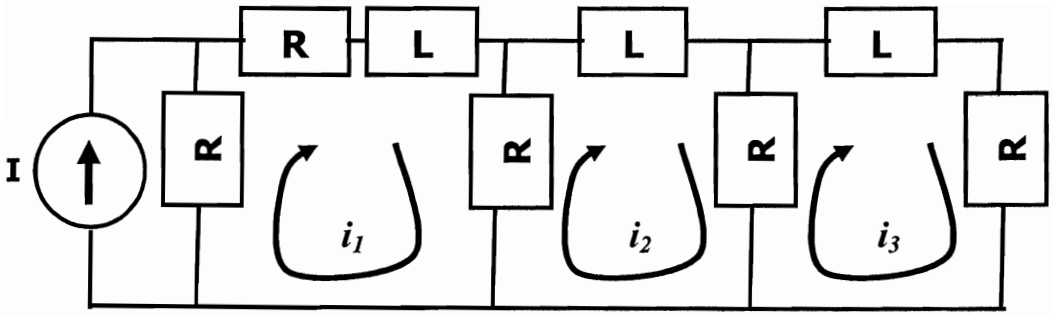

Fig. Q3

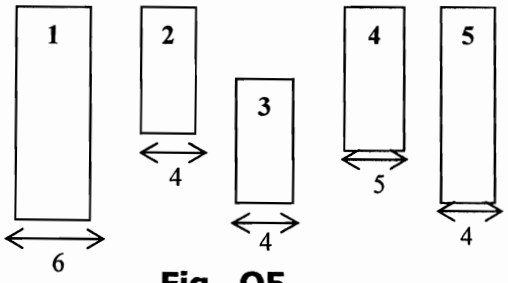

Fig. Q5

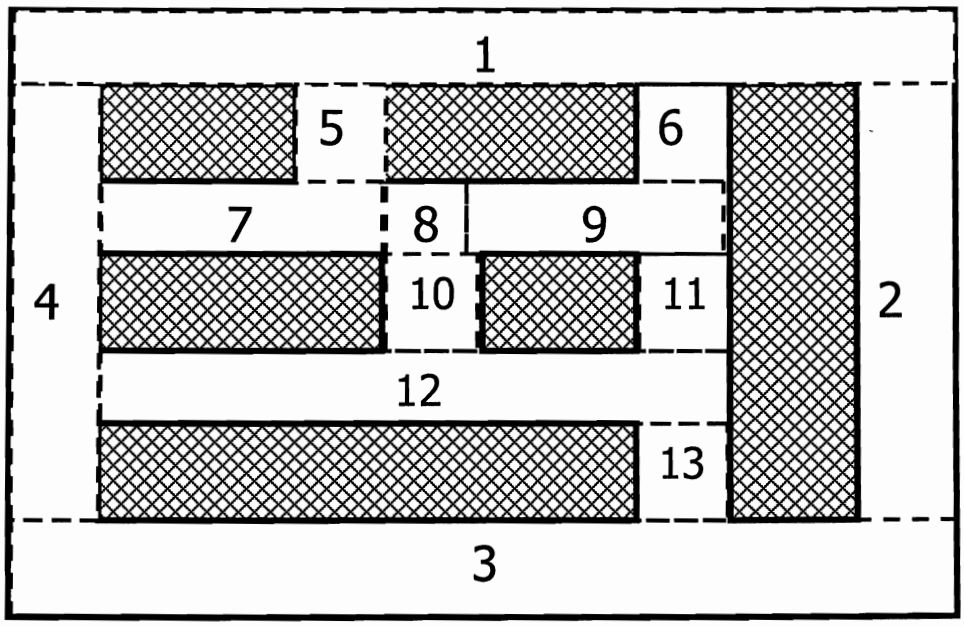

Fig. 6b