CSL 719 - Synthesis of Digital Systems
28 November 2006, 10:30 AM to 12:30 AM
Major Exam. Maximum Marks = 120

Name: **Entry Number:**

[5 Marks] One-hot encoding of FSMs is said to lead to circuits with lower delay. Explain why.

[5 Marks] Is the common sub-expression elimination algorithm guaranteed to always give better results? Explain.

[10 Marks] Consider a 4-to-1 MUX structure with 4 data inputs, 2 select inputs, and one output. Show clearly how to use the MUX to implement a general boolean function $f(a, b, c)$ - i.e., derive the expressions for the data and select inputs in terms of f.

[10 Marks] Clearly indicate what happens in each step of the algebraic division process when the expression $(a + b')$ is divided by a'.

[15 Marks] In the retiming formulation, we used the condition: "if $D_{ij} > \phi$ then $W'_{ij} \geq 1$". Explain why it is sufficient to use this condition (instead of: "$W'_{ij} \geq D_{ij}/\phi$").

[15 Marks] The Boolean *satisfiability* problem refers to the task of finding an assignment of boolean values of variables such that the expression becomes TRUE. An ROBDD representation of the expression can be used to answer this question. Explain how. (*Hint: search for a path between suitable nodes in the ROBDD.*)

[15 Marks] Give an algorithm to determine the critical path of a netlist, assuming that all the nets (including the output net) have been annotated with their signal arrival times. It should be accurate, handle all special cases and should be as close as possible to an actual C implementation; just an overall idea is not sufficient (and will fetch zero marks).

[20 Marks] An SRAM based FPGA features a 4-bit SRAM in each logic block. It is to be used for either of two purposes:

- implementation of the logic function $y = a + b'$
- storage space for 4 bits

The choice of the functionality, however, is to be done dynamically, through an input port C to the logic block. a and b are inputs to the block. If $C = 1$, then it implements $y = a + b'$. There is another one-bit input R, which is used when $C = 0$; when $R = 1$ the data stored in the memory is sent to y (READ operation); when $R = 0$, the data from a 1-bit input *data* is stored in the memory (WRITE operation). Both READ and WRITE operations use the concatenation of $\{a, b\}$ bits to form the memory address.

Draw a detailed circuit that will achieve the above functionality. Assume that the programming of the logic block's function will be done by a *bit-stream* (sequence of bits). Make any reasonable assumptions.

[10 Marks] Explain the difference in the objectives of the EXPAND and IRREDUNDANT operators in two-level logic synthesis.

[15 Marks] Consider the VHDL code snippet below:

```
signal a : BIT := '0';
signal b : BIT := '0';
process
  a <= NOT b after 5 ns;
  wait for 4 ns;
  b <= NOT a after 5 ns;
  a <= '1' after 2 ns;
end process
```

Draw the waveform when the above process is simulated from 0ns to 12ns. Clearly indicate all *transactions* and *events* that occur during the simulation.