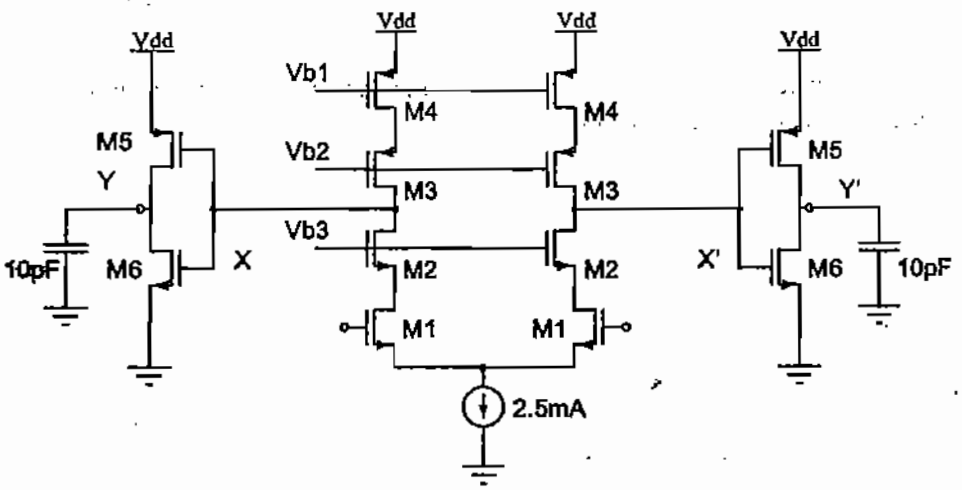
Indian Institute of Technology, Delhi
Analog Circuits, Final, May 5 2007

Instructions:
Full marks: 45
Total time: 120 min
You can ask the instructor for hints at the cost of 1 mark for every hint that he gives out. (e.g, if the examiner gives you 10 hints through the duration of the exam, you will have a -10 penalty.)
Please make intelligent approximations.



The figure above is a basic two stage OTA, with the first stage being a cascode amplifier. Vdd is 3 Volts, the current through the tail current source is 2.5 mA, as indicated. The common-mode voltage level at nodes X and X' is 1.5 Volts. The nMOS and pMOS devices are all in saturation and strong inversion, with the basic governing relationship given by:

$$I_D = \mu C_{ox}/2 \cdot W/L \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

For the nMOS, $\mu = 0.03$ m^2/V/s, for the pMOS, $\mu = 0.01$ m^2/V/s. $C_{ox} = 4$mF/sq.m. $\lambda = 0.1$/V. $|V_T| = 0.5$V. All pMOS devices are of size 150μm/0.5μm, all nMOS devices are of size 50μm/0.5μm. For all the devices, the capacitance C_{GS} is given by $2/3 \cdot W \cdot L \cdot C_{ox}$. The capacitance C_{GD} is given by $W \cdot C_{gdo}$ where $C_{gdo} = 0.3 \times 10^{-9}$ F/m.

1. Compute the DC bias current through M5 and M6. (2)

2. Compute the total power consumption of the circuit. (2)

3. Compute the DC small signal circuit parameters (g_m, r_o) of all the devices. (10)

4. Compute the DC small signal differential gain of the circuit. (5)

5. Which are the nodes in the OTA that are responsible for poles? (3)

6. Compute the effective small signal resistance, and the lumped capacitance at the above nodes. Compute the pole frequencies of the OTA. (6)

7. Draw the Bode gain and phase plot for the above DC gain, and the computed poles. (5)

8. I require a phase margin of 75°. What compensation capacitor (and series resistor) will you use? (15)