Department of Computer Seience & Engineering
CSL718 Architecture of High Performancc Computers
Major Test

Date: 30.4.2008 Time: 0800 – 1000 Max. Marks: 35

1. Compare instruction scheduling in the following architecture classes - static superscalar, dynamic superscalar, pure VLIW and EPIC. In which class does the IA-64 architecture fall and how is a program for this architecture coded independent of execution resources?

(5)

2. Consider performance improvement in a VLIW processor using the following approaches - a) loop unrolling or b) software pipelining. What are the limiting factors in the two cases? Point out which factors are same and which are different.

(5)

3. Illustrate the use of poison bits in speculative execution in a VLIW processor. Can this approach be used with a superscalar proccssor?

(5)

4. Consider a cache controller implementing the simple 3 state invalidation based coherenee protocol. What steps does it take when a write hit occurs or a write miss occurs? At which steps does the bus need to be locked and unlocked? State the memory consistency model assumed.

(5)

5. Bandwidth analysis of a bus shared by n homogeneous proeessors was done in the class. Extend this analysis for heterogeneous processors.

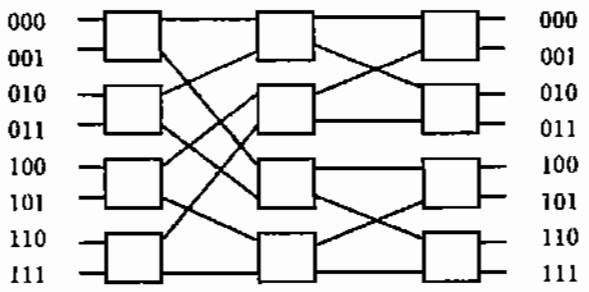
(5)

6. The following code for barrier synchronization uses shared variables `X`, `count` and `release`. Identify the conditions under which it would fail. Give a solution which overcomes this problem.

```
lock (X)
if(count=0)release ← 0
count++
unlock(X)
if(count=total){count←0;release←1)
else spin(release=1)
```

(5)

7. Consider the 3 stage interconnection network shown for connecting 8 sources to 8 destinations. When two sources simultaneously request for connections, what is the probability that blocking would occur? Does it depend on which two inputs are making requests? Assume that a source may request connection for any destination with equal probability.



(5)