Electrical Engineering Department
EEL404/EEL894 Flexible AC Transmission System
Major Test

Time allowed- 2 hour | Maximum Marks- 50

Answer all questions in the sequence given in the question

Q.1

i. Obtain with justification the transport delay present in a 'f' Hz, p-pulse TCR. Mark=2

ii. Explain the need of integral gain reduction in the voltage control loop of SVC. Mark=2

iii. Explain in (ii) why not we should go for a low value from the designing stage itself. Mark=2

iv. Explain the necessity of susceptance regulator in case of SVC. Mark=2

v. Explain the operation of a PLL with schematic. Mark=2

vi. What is the function of an anti-parallel diode across the IGBT valve. Mark=2

vii. Draw the phasor diagram of a type-1 converter system. Mark=2

viii. Explain in (vii) how to vary magnitude and phase angle of the output voltage. Mark=2

ix. Under which circumstance SSSC will be SSR neutral and why. Mark=2

x. Explain the need of other types of controller apart from PID. Mark=2

xi. Write the differential equations that will govern the current I_d and I_q respectively for the circuit given in Fig.1. Mark=2

xii. Find out the real and reactive power loss in Fig.1. Mark=2

xiii. Find the reactive power involved in any one side in Fig.1. Mark=2

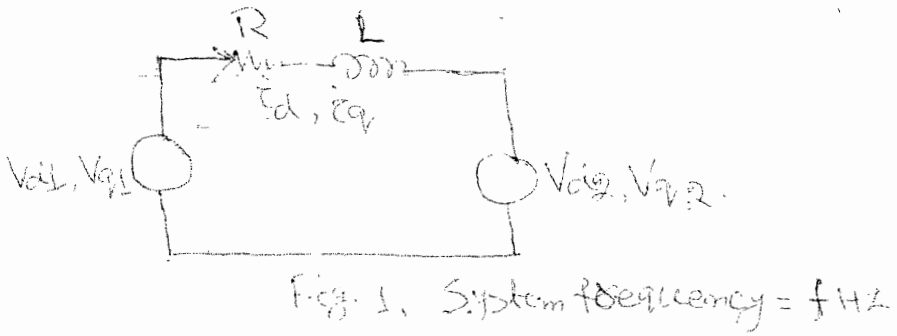

Fig. 1, System frequency = f Hz

Q.2

i. Explain from the power angle characteristics that inclusion of a shunt reactive power source with speed feedback will improve first swing stability. Marks = 8

ii. Derive from the basic the load injection model of an UPFC. Marks = 8

iii. Draw the control block diagram of a Type-2 SSSC. Explain from the block diagram clearly indicating by point how we can regulate the magnitude of injected voltage. If the injected voltage is increased by 1% what will be the phase difference between the line current and the injected voltage at steady state. Marks= 4+3+1