EEL 322, IC Technology, Major Exam, 06 May 2009.

Time: 2 hours. Maximum marks: 100.
Closed book exam with one handwritten A4 sheet (both sides) allowed as notes.

1. **Answer very briefly.** *(7*5 marks)*

   (a) Quartz, Sapphire, Alumina and Silica are all insulating oxides. When these oxides are used as gate dielectrics or passivation dielectrics, give as many differences between them as you know of (with explanations).

   (b) Arrange the following in decreasing order of importance for achieving the fastest switching speed of a transistor: technology (bipolar/CMOS), operating temperature, doping level, majority carriers (electrons/holes), carrier mobility. Give justifications for your answer.

   (c) Why do you need isolation in BJT's and not in CMOS transistors? Draw cross-section diagrams of at least two isolation schemes for BJT's.

   (d) SiC (silicon carbide) is an insulator at room temperature with $E_g \approx 3eV$. But it is used as a semiconductor at high temperatures. Explain how this is possible? Guess what temperature range this will be true.

   (e) Calculate the ratio of resonant frequencies of two crystalline-Si cantilever beams of dimensions $10\mu \times 100\mu \times 0.1\mu$ and $100\mu \times 10\mu \times 0.01\mu$. Repeat if the cantilevers are made of amorphous-diamond, which has a Young's modulus twice that of Si.

   (f) Roughly, how big is a DNA molecule in width? A carbon nanotube? A single H atom?

   (g) How is light produced in old CRT monitors? How is light produced in an LCD screen for a present-day laptop? What fraction of useful light comes out of the screen?

2. **NMOS and CMOS Inverter** *(6+8+6 marks)*

   (a) Give the circuit diagrams for an NMOS inverter and a CMOS inverter.

   (b) Give the top layout views for an NMOS inverter and a CMOS inverter.

   (c) Finally, draw the cross-sections of the layout views of the NMOS inverter and the CMOS inverter.

3. **SUPREM program.** *(20 marks)*

   Explain the following SUPREM program and the structure it simulates.

```
option quiet
set echo
mode one.dim
line x loc=0.0 spacing=0.01 tag=top
line x loc=1.0 spacing=0.01
```

```
line x loc=20 spacing=0.25 tag=bottom
region gaas       xlo=top  xhi=bottom
boundary exposed  xlo=top  xhi=top
boundary backside xlo=bottom xhi=bottom
init carbon conc=1e15
implant beryllium dose=1e14 energy=100 pearson
deposit nitride thick=.3
select z=log10(beryllium)
plot.1d x.min=0 x.ma=2 y.mi=14 y.max=20
line.type=4
method fermi init=1e-5
method full.fac
diffuse time=15 temp=800 argon
select z=log10(beryllium)
plot.1d x.mi=0 x.ma=2 y.mi=14 y.ma=20 cle=f axi=f
line.typ=2
quit
```

4. **Doping in semiconductors.** *(10 marks)*

   You are the plant manager of the crystal growing unit. One day an employee reports that while he was working with the molten Si, his gold wedding ring weighing 5g fell into the 100kg melt. He thinks it is ok to proceed since the amount of gold ($\rho = 19.3g/cc$, $A = 79$) is very small. Roughly estimate what is the doping level caused by the gold contamination. What kind of problems, if any, will this cause? For Si, $N_0 = 5\times10^{22}/cc$, $\rho = 2.33g/cc$, $A = 14$. For intrinsic Si, $E_g = 1.1eV$. It is known Au introduces an acceptor level at 0.54eV and a donor level at 0.35eV.

5. **Organic Electronics.** *(5+2+8 marks)*

   (a) Sketch all fabrication steps for dual gate organic thin film transistor (2D cross sectional view).

   (b) Write down the name of an n-type and p-type organic semiconductor material (except pentacene) and organic dielectric.

   (c) Consider a p-channel OTFT with $W = 500\mu m$, $L = 200\mu m$ and gate oxide thickness $t_{ox} = 500nm$. Assume that the drain current in the linear region for $V_{DS} = 10V$ is $I_{DS} = 5\mu A$ at $V_{GS} = 5V$ and $I_{DS} = 15\mu A$ at $V_{GS} = 7.5V$. $\epsilon_0 = 8.85 \times 10^{-12}$, $\epsilon_{r,SiO_2} = 3.9$. Calculate the carrier mobility from this data without help of threshold voltage.