MAJOR PART 'A'

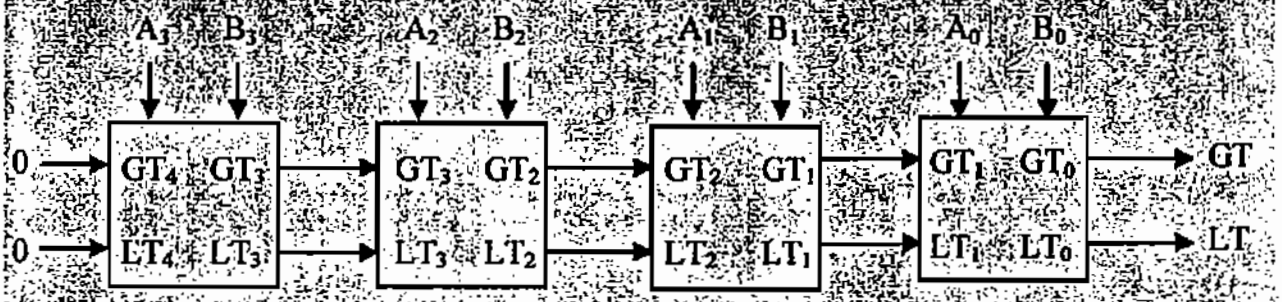
EEL324 Digital Hardware Design

Time: 1 Hour **Max. Marks: 20**

N. B.:- This is **open notes examination. Transfer** of notes to each other is strictly **prohibited.** Write in the answer script. Attach part 'B' in main answer script.

Q 1:- Write the answer in the main answer script. (5)

It is required to model a 4-bit comparator that compares two 4-bit numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$, and produces two outputs GT, and LT. If A>B, then the output signal GT is set to 1 and LT is set to 0. If A<B, then the output signal LT is set to 1, and GT is set to 0. Otherwise both signals will be set to 0, which indicates that the two numbers are equal (i.e. A=B). The 4-bit comparator circuit can be designed in a modular way as shown below:



The equations for the 1-bit magnitude comparator can be found to be:

$$GT_i = GT_{i+1} + \overline{LT_{i+1}}\, A_i \overline{B_i}$$

$$LT_i = LT_{i+1} + \overline{GT_{i+1}}\, \overline{A_i} B_i$$

(i) Describe an Entity **COMP** for a 1-bit magnitude comparator.

(ii) Model an Architecture **Conc** for this 1-bit COMP using concurrent statements.

(iii) Describe an Entity **COMP4** for a 4-bit magnitude comparator.

(iv) Model Architecture **Struct** for the 4-bit magnitude comparator (**COMP4**) using instantiations of the Entity **COMP.**

Q2:- A sequential circuit has two inputs, **w** and **x**, and one output, **z**. Its function is to compare the input sequences on the two inputs. If **w** equals **x** during any four consecutive clock cycles, the circuit produces **z** equal '**1**'; otherwise, **z** equals '**0**'. For example:

w:	**0**	**1**		**1**	**0**		**1**	**1**	**1**	**0**		**0**	**0**	**1**	**1**		**0**	**1**
x:	**1**		**1**	**1**	**0**		**1**	**0**	**1**	**0**		**0**	**0**	**1**	**1**		**1**	**0**
z:	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**		**0**	**1**	**1**	**1**		**0**	**0**		

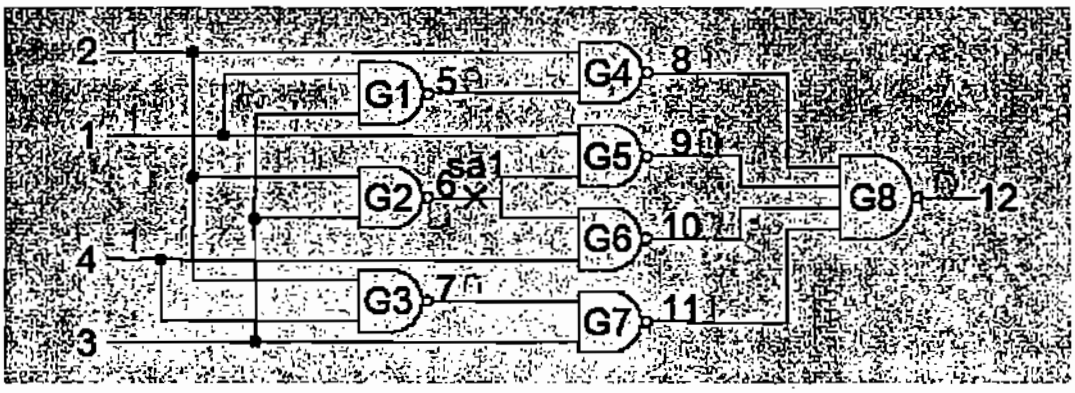
Does this finite state machine (FSM) correspond to a Mealy machine or a Moore machine? Give a reason why you chose your answer (in less than 20 words).

Give a suitable (Neat) state transition graph that implements the described functionality from above. Label your states A, B, C, etc. (Can make proper assumptions to reduee number of states.)

(4)

Q3 (a):- For the following eircuit diagram find the fault 6 s-a-1 using D-algorithm. Draw a **neat** table and discuss the forward drivc and line justifieations.

(4)



(b):- For the expression of **F** given below show the **ROBDD** and **ROBDD** in complement form.

(2)

(Variable ordering is a ≤ b ≤ c ≤ d and a is top variable.)

$$a \cdot \bar{c} + \bar{a} \cdot \bar{b} \cdot c + \bar{b} \cdot \bar{c}$$

(c):- Discuss in **less than 30** words thc non-restoring division algorithm for the **signed** integers (for **n = 3**) as compared to signed numbers.

(2)

(d):- In less than 40 words write the difference between signals and variables in VHDL? Where can signals and variables be used within a typical VHDL model?

(3)

MAJOR PART 'B'

EEL324 Digital Hardware Design

Time: 1 Hour **Max. Marks: 20**

NAME: **Entry No.**

N. B.:- Do all calculations/derivations and rough work in the main answer script with question numbers. This is open notes examination, but no transfer of notes to each other. Return this part.

Q5 (a):- Draw a state diagram corresponding to the VHDL program shown below. (3)

```
Entity foo is
        port (b, clk: in STD_LOGIC; u, v: out STD_LOGIC);
end foo;
Architecture bar of foo is
  signal state: state_type;
  begin
        process (clk) begin
              if clk'event and clk = '1' then
                    if state = baseball and b = '1' then
                          state <= birdie;
                    elsif state = puck and b = '0' then
                          state <= baseball;
                    elsif state = puck and b = '1' then
                          state <= birdie;
                    elsif state = birdie and b = '0' then
                          state <= baseball;
                    elsif state = birdie and b = '1' then
                          state <= puck;
                    end if;
              end if;
  end process;
  u <= '1' when state = baseball or state = puck else '0';
  v <= '1' when state = birdie else '0';
end architecture bar;
```

Answer:- **---DIAGRAM---**

(b):- Consider the two VHDL processes below, each of which will be implemented hy a D flip-flop during logic synthesis. How will the two resulting flip-flops differ, and why? Be specific. (Answer in less than 35 words total.)

(3)

1st

```
PROCESS
BEGIN
    WAIT UNTIL ( Clock' EVENT AND Clock = '1' );
        IF reset = '1' THEN
            Q2 <= '0';
        ELSE
            Q2 <= D;
        END IF;
END PROCESS;
```

2nd

```
PROCESS (Reset, Clock)
BEGIN
        IF Reset = '1' THEN
            Q3 <= '0';
        ELSEIF ( Clock' EVENT AND Clock = '1' ) THEN
            Q3 <= D;
        END IF;
END PROCESS;
```

ANSWER:-

Q6 (a):- For the given state table as below assume the following input sequence with the machine initially in state A:

(3)

10011101011001

P.S.	Next State		OUT PUT	
	X=0	X=1	X=0	X=1
A	B	G	0	0
B	B	H	1	1
C	F	D	1	0
D	B	H	0	0
E	F	D	1	0
F	F	C	0	1
G	E	A	0	0
H	E	A	0	0

Determine the resulting sequence.

ANSWER:-

Input	1	0	0	1	1	1	0	1	0	1	1	0	0	1
Present state	A													
Output														

(b):- A state machine has a single input N and a single output D. Four-bit messages arrive at the input. The purpose of the circuit is to detect when a 4-bit message is not a BCD word. That is, D = 1 whenever the 4-bit word is not a decimal number in BCD code. Assume that the circuit returns to its initial (reset) state at the end of each 4-bit word. Construct a neat state diagram below.

(3)

ANSWER:-

Q7:- Division circuits usually include logic to detect a dividend-divisor combination that will cause the quotient to overflow. Suppose that a divider for n-bit unsigned integers has a double-word (2n-bit) dividend **D** and a single-word divisor **V**. What general condition must be satisfied for quotient overflow to occur? By choosing **n = 3** and taking numerical values of **D** and **V** explain the condition. **(3)**

Answer: Condition for overflow =

Discuss your answer in less than 25 words:

Q8:- For the following reservation table find the Collision vector (in $C_7\ C_6 \ldots C_1$ format). Determine MAL associated with the shortest greedy cycle. Find the lower bound on the MAL. **(5)**

	Time →					
OPERATIONS	**1**	**2**	**3**	**4**	**5**	**6**
S_1	X					X
S_2		X		X		
S_3			X			
S_4				X	X	

ANSWER: **Collision vector (in $C_7\ C_6 \ldots C_1$ format) =**

MAL = **Lower bound on MAL =**

If you are allowed to insert one non compute delay stage to make a latency of 1 permissible in the shortest greedy cycle for the purpose of achieving optimal latency equal to lower bound.

Complete the new reservation table below with delay below:

	Time →					
OPERATIONS	**1**	**2**	**3**	**4**	**5**	**6**
S_1						
S_2						
S_3						
S_4						
D						

In new table: New collision vector (in $C_7\ C_6 \ldots C_1$ format) =

Simple cycles:-

Greedy cycle:- **New MAL:-**