Electrical Engg Department

EEL 832 MAJOR

Date : 8/5/2007
Total : 45
Time : 2hrs

Q1. A floorplan and sizes of the modules are shown in Fig1 and Table1 respectively.

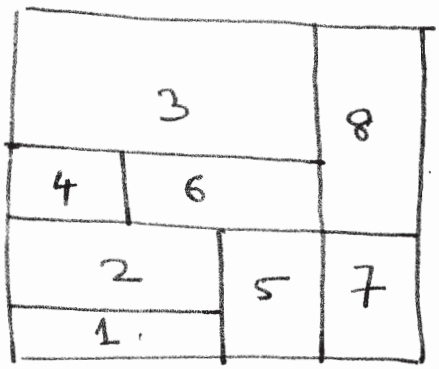

Fig1.

Module NO	Width	Height
1	2	1
2	2	2
3	4	3
4	1	1
5	1	3
6	2	1
7	3	3
8	2	4

Table 1

(a) Draw the horizontal and vertical dependency graph of the given floor plan.

(b) Use the graphs to determine the minimum required width and height of the floor plan.

(c) Draw the slicing tree corresponding to the above floor plan.

(d) Determine the normalized Polish expression

(e) Determine the area from the normalized Polish expression.

(f) Draw the Global routing graph for the given floor plan.

(4+2+4+3+3+3)

Q2.(a) For the PLA Personality Matrix given below fold the PLA using the algorithm taught in the class.

r_1	1	2	2	2	0	1
r_2	2	1	2	1	1	0
r_3	1	2	2	1	0	1
r_4	2	2	1	2	0	1
r_5	2	1	2	2	1	0
	x_1	x_2	x_3	x_4	y_1	y_2

(b) Can you fold the PLA given below using the same algorithm? If not devise your own method.

r_1	1	2	2	2	0	1
r_2	2	0	2	0	1	0
r_3	1	2	2	0	0	1
r_4	2	2	1	2	0	1
r_5	2	0	2	2	1	0
	x_1	x_2	x_3	x_4	y_1	y_2

(7+4)

Q3. Draw the gate matrix layout of the function $X = A.B + B.C + C.A$.

(a) Find the net-gate set and the gate-net set.

(b) Apply the technique taught in the class to optimize the gate matrix layout. (8)

Q4. Design a greedy algorithm to order channel in a given placement so as to minimize the number of switch boxes. (7)