Major Test

SEMICONDUCTOR DEVICE TECHNOLOGY: PHL704

II Semester 2009-10

Max. Marks 55 Time : 2 Hr

Attempt all questions.

1. Answer in brief. **Each question carries 3 marks.**

   a. Why do we prefer 100 orientation Si for CMOS devices and 111 orientation in bipolar?
   b. There are interstitial and vacancy diffusion mechanisms in Si. For fast diffusant, such as Cu in Si has activation energy of 1.5 eV, which type of diffusion mechanism is dominant in this case and why?
   c. Why do we anneal after ion implantation? Does annealing temperature depend on the mass of implanted ion?
   d. How do water(steam), sodium and chlorine affect the oxidation rate of Silicon?
   e. How can we minimize channeling effect in Silicon?

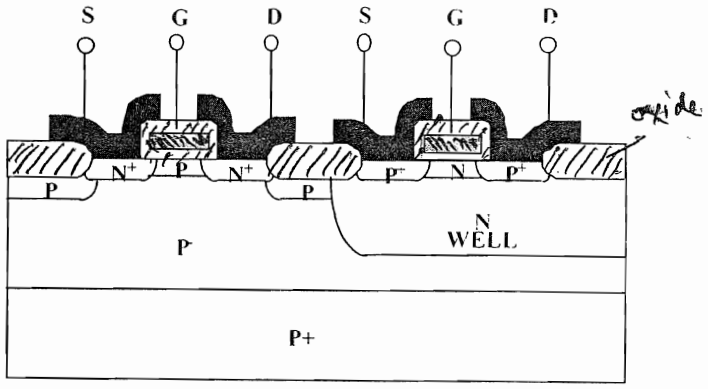
2a. What are the various methods of depositing or growing insulating films? Explain APCVD method for growing oxide with diagram..

b. Compare the quality of silicon oxide grown by Plasma, thermal oxidation and LPCVD method. 3+4+3=10

3a. Show the diffusion profiles of B and P at Si/SiO2 interface and both sides of it. 5

b. How does the diffusivity affected under high dopant concentration? 5

4. Sketch a process flow that would result in the structure shown below by drawing process steps involved. Show the mask and name of the process used. 8



5a. Discuss in brief the mechanisms of ion stopping in silicon.

b. Show the ion implantation profiles (along depth) of B, As,and Sb at same dose..

c. How does channeling affects the profile in the case of Boron, P, and As ion implanted at different energies? 4+4+4=12