EEL 4768
Computer Architecture

Memory, Cache and Virtual Memory Examples

Outline

- Example 1: Direct–mapped cache Design
- Example 2: MIPS Memory size and cache parameters
- Example 3: cache organization and internal main memory organization
- Example 4: Cache memory accesses/references scenario
- Example 5: Fully Associative cache
- Example 6: Associative cache parameters
- Example 7: Virtual Memory / TLB & cache parameters

Example 1: Direct–mapped cache Design

Design a direct–mapped cache that has 2KB and 16 bytes per block. Assume a 32 bit address.

a) How many bits are used for the byte offset?

- 3
- 4
- 8
- 6
- 16

b) How many bits are used for the (index) field?

- 10
- 8
- 13
- 7
- 9
- 16

Example 1: Direct–mapped cache Design

Design a direct–mapped cache that has 2KB and 16 bytes per block. Assume a 32 bit address.

c)How many bits are used for the tag?

- 20
- 21
- 31
- 11
- 17
- 18

d) How many total bits in this cache? Compare the size of the cache to that needed just for the storage of the data?

- 19 1/4 Kbits, 1.03
- 19200, 1.027
- 18 3/4 Kbits, 1.172
- 2Kbits, 1.172
- 16Kbits , 1.271
- 19 2/4 Kbits, 1.037

Example 1: Direct–mapped cache Design

Design a direct–mapped cache that has 2KB and 16 bytes per block. Assume a 32 bit address.

e) To what block number does byte address 18200_{ten} map?

- 223
- 113
- 13
- 1137
- 137
- 37

Example 2: MIPS Memory size and cache parameters

Given: A MIPS computer system with 1 GB of main memory. It has a 4K-Byte direct-mapped cache with a block size of 4 words.

a) How many bits wide is the address bus?

b) How many lines are in the cache?

c) How many bits wide is the tag field?

d) Show the bit field encoding for memory addresses.

a. In order to address 1GiB of memory, a total of $\log_2\left(2^{10} \times 2^{10} \times 2^{10}\right) = 30$ bits are required.

b. Because the cache is 4KiB in size, and there are 4 words per block, then, the cache must have
$$\frac{4\text{KiB}}{4\text{wrd blk}^{-1} \times 4\text{B wrd}^{-1} \times 1\text{blk line}^{-1}} = 256 \text{ lines.}$$

c. $t = 30 - (8 + 2 + 2) = 18\text{bit}.$

d. Figure 1 shows the address bus encoding.

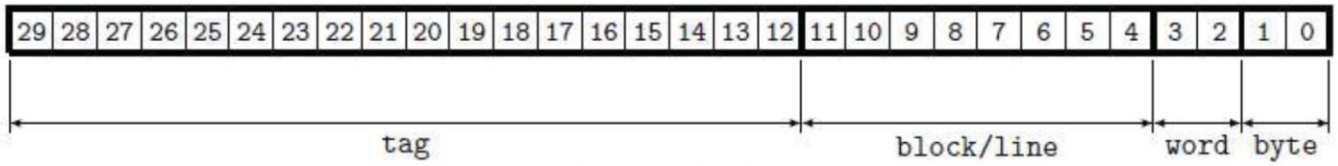
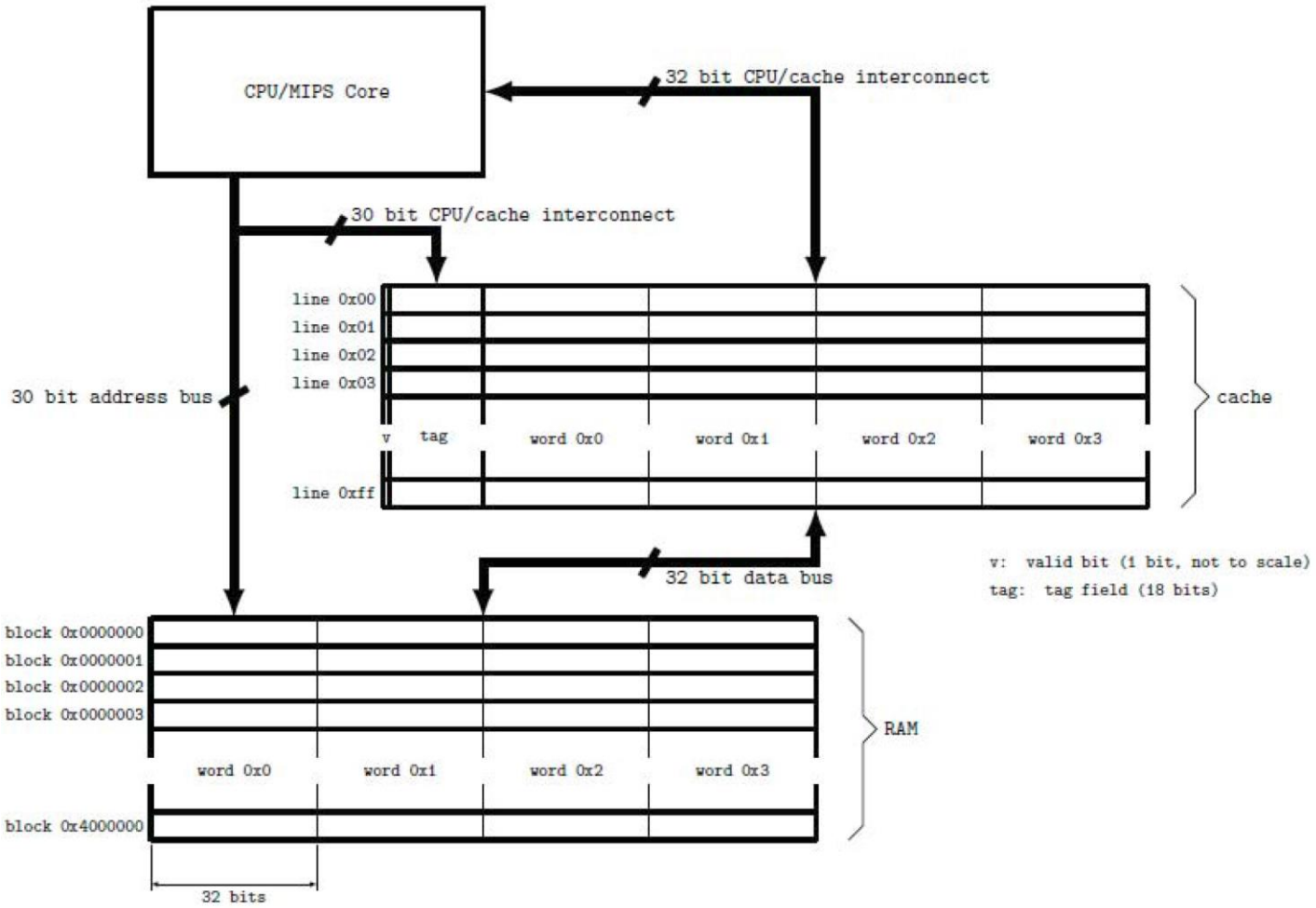


Figure 1: Address bus encoding for problem 2d.

Example 3: cache organization and internal main memory organization

Given the system described in Example 2). Draw a diagram showing address and data buses, bus widths, and bus directions.

Show internal cache organization and internal main memory organization.



Example 4: Cache memory accesses/references scenario

Consider a system with the following characteristics. The main memory size is 16 bytes, the cache size is 4 words, the block size is one word, and the word width is one byte. Assume cache is initially empty. Calculate the hit rate for the reference string of decimal addresses {7,8,2,11,8,3,11,11}. Express your answer as a percent.

Assuming a directly mapped cache, the cells hit are 3, 0, 2, 3, 0, 3, 3 and 3. The first three are compulsory misses, the fourth address is a miss on the grounds that a different address is stored in that cache line. The next referenced address produces a hit, then a miss, then a miss, and then a hit. This means that out of 8 addresses, only two hits occur, or a 25%.

Example 5: Fully Associative cache

Given a MIPS system with 4GB bytes of main memory, a fully associative-mapped cache, and block size of 64 words.

How many bits are in the tag field?

The address bus size is 32 bits wide. Since there are 64 words per block, 6 bits are required to index them, since each word is 4 bytes wide, 2 bits are required to index them. Thus the size of the tag field is given by $32 - (6 + 2) = 24$ bits wide.

Example 6: Associative cache parameters

Given a MIPS system with 16MB bytes of main memory, a 4-way set associative-mapped cache containing 32K lines,

and a block size of 8 words.

a) How many bits are in the set field?

b) How many bits are in the tag field?

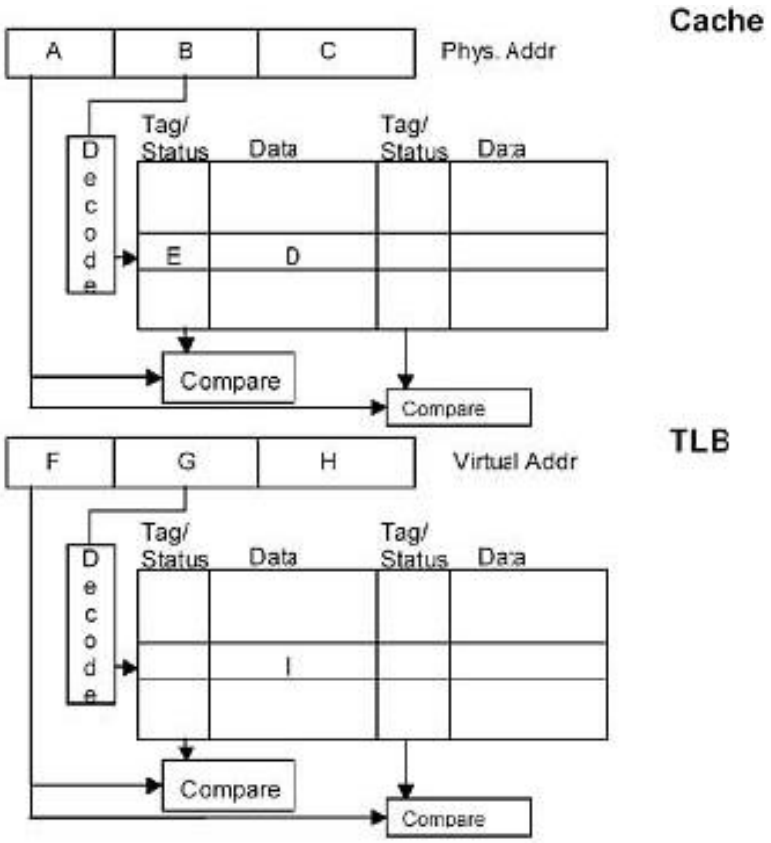
a. The cache contains $32 \times 2^{10} = 32768$ lines (blocks), structured in sets of 4 blocks, each block containing 8 words, each word containing 4 bytes. The total number of sets on the cache is thus given by $32768/4 = 8192$, thus a total of 13 bits is needed to address them.

b. The address bus is $\log_2(16 \times 1024 \times 1024) = \log_2\left(2^4 \times 2^{10} \times 2^{10}\right) = 24$ bits wide. Three bits is needed to address the words in the block and 2 bits are needed to address the bytes in the word. Thus, the size of the tag field is given by $24 - (13 + 3 + 2) = 6$ bits.

Example 7: Virtual Memory / TLB & cache parameters

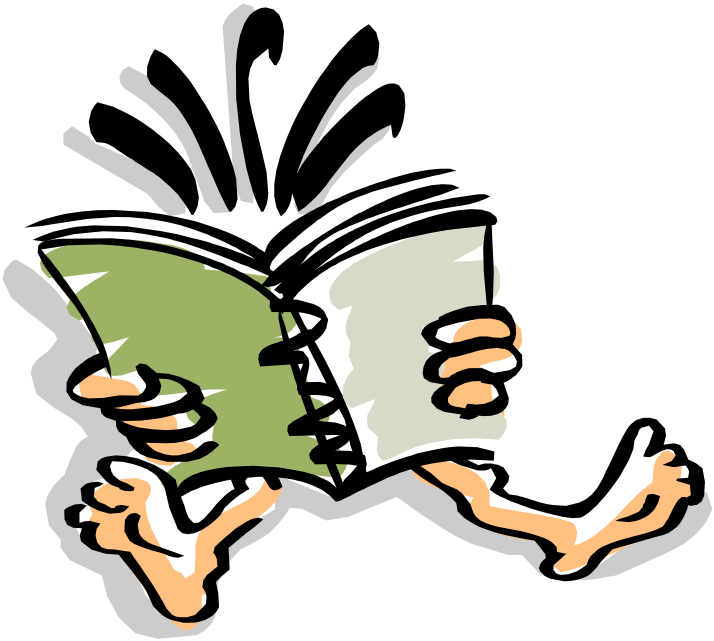
Consider a memory system with the following parameters:

- Translation Lookaside Buffer has 128 entries and is 2-way set associative.
- 64Kbyte L1 Data Cache has 64 byte lines and is also direct mapped.
- Virtual addresses are 42-bits and physical addresses are 30 bits.
- 16KB page size
- Below are diagrams of the cache and TLB. Please fill in the appropriate information in the table that follows the diagrams (assume 3 for status bits):



L1 Cache		TLB	
A=	Bits	F=	Bits
B=	Bits	G=	Bits
C=	Bits	H=	Bits
D=	Bits	I=	Bits
E=	Bits		

Readings



- P&H Comp Org & Design
  - Ch5