MIPS64 Reference

Load/store instructions

LD, LW, LH, LB	LWU, LHU, LBU	SD, SW, SH, SB	*integer*
L.S, L.D,	S.S, S.D	LI.S, LI.D	*floating-point*

Arithmetic & logical

DADD, DADDI, DADDU, DADDIU	DSUB, DSUBU	DMUL, DMULU	DDIV, DDIVU	*64-bit*
ADD, ADDI, ADDU, ADDIU	SUB, SUBU	MUL, MULU	DIV, DIVU	*32-bit*
SLT, SLTI, SLTU, SLTIU				*32-bit & 64-bit*
AND, OR, NOR, XOR	ANDI, ORI, XORI			*32-bit & 64-bit*

Shift & rotate

DSLL, DSLL32, DSLLV	DSRL, DSRL32, DSRLV	DSRA, DSRA32, DSRAV	DROTR, DROTR32, DROTRV	*64-bit*
SLL, SLLV	SRL, SRLV	SRA, SRAV	ROTR, ROTRV	*32-bit*

Branch & jump

BEQ, BNE, BLT, BLE, BGT, BGE	*compare integer registers*
J, JAL, JALR	

Load a 64-bit immediate

LUI, AUI, DAHI, DATI

Floating-Point Compare & Branch

C.EQ.S, C.NE.S, C.LT.S, C.LE.S, C.GT.S, C.GE.S	*floating-point registers (32-bit)*
C.EQ.D, C.NE.D, C.LT.D, C.LE.D, C.GT.D, C.GE.D	*floating-point registers (64-bit)*
BC1T, BC1F	

Move operations between GPRs and FPRs

DMTC1, DMFC1	*64-bit*
MTC1, MFC1	*32-bit*

Integer/Floating-Point conversion (W: 32-bit int) (L: 64-bit int) (S: 32-bit FP) (D: 64-bit FP)

CVT.D.S, CVT.D.W, CVT.D.L	CVT.S.D, CVT.S.W, CVT.S.L
CVT.L.S, CVT.L.D	CVT.W.S, CVT.W.D

Floating-point operations

ADD.S, ADD.D, ADD.PS	SUB.S, SUB.D, SUB.PS
MUL.S, MUL.D, MUL.PS	DIV.S, DIV.D, DIV.PS
MOV.S, MOV.D, MOV.PS	

Pair of Singles (PS) operations

CVT.PS.S F0, F1, F2		// Merge two SPs into one PS
PLL.PS F0, F1, F2	PLU.PS F0, F1, F2	// Merge two SP into one PS
PUL.PS F0, F1, F2	PUU.PS F0, F1, F2	// Merge two SP into one PS
CVT.S.PL F0, F1	CVT.S.PU F0, F1	// Extract a SP from a PS