Exam2 review Part2 No submission

Please write legibly or type. Show your work to the extent possible.

1. Answer the following questions based on the following table. All different datapaths support the following four instruction types with listed delay of each component. Assume no hazard is detected in the pipelined datapath. Please explain your answer.

Instruction class	Instruction fetch	Register read	ALU operation	Data access	Register write	Total time
Load word (`lw`)	200 ps	100 ps	200 ps	200 ps	100 ps	800 ps
Store word (`sw`)	200 ps	100 ps	200 ps	200 ps		700 ps
R-format (`add`, `sub`, `and`, `or`, `slt`)	200 ps	100 ps	200 ps		100 ps	600 ps
Branch (`beq`)	200 ps	100 ps	200 ps			500 ps

a) What should clock cycle time be for the single-cycle, multi-cycle and pipelined datapaths? Please explain your answer.
b) What is the latency (defined as the delay from when the instruction enters the datapath until it finishes) of an R-format instruction in the single-cycle, multi-cycle and pipelined datapaths?
c) What is the latency (defined as the delay from when the instruction enters the datapath until it finishes) of load word (lw) instruction in the single-cycle, multi-cycle and pipelined datapaths?
d) What is the averaged throughput (defined as the number of instructions executed in 1 nanosecond in this case) of the single-cycle, multi-cycle and pipelined datapaths? Assume the frequency of four different instruction types are the same.

2. Suppose that an unpipelined processor has a cycle time of 25 ns, and its datapath consists of modules with the latencies of 2, 3, 4, 7, 3, 2, and 4 ns (in this specific order). In pipelining this processor, it is not possible to rearrange the order of the modules (for example, putting the register read stage before the instruction decode stage) or to divide a module into multiple pipeline stages (for complexity reasons). Note that, this is not standard five-stage pipeline design.

a) What is the minimum clock cycle time that can be achieved by pipelining this processor? Please explain your answer.
b) If you are limited to a 2-stage pipeline, what is the minimum clock cycle time? Please explain your answer.

3.The following codes run on the five-stage pipelined datapath. For each piece of code, answer the following questions.

a) Without forwarding, insert the necessary number of 'nops' for the code to execute correctly.
b) With the forwarding unit available (only supports forwards MEM-> EX and WB->EX), show how the code will execute. Mention the data that's forwarded between the stages. Use 'nops' only when necessary.

```
Code 1:
sub t1, t2, t3
add t1, t4, t5
or t4, t2, t6

Code 2:
and t2, t5, t1
sub t3, t2, t0
nor t7, t1, t5
```

```
Code 3:
and t2, t5, t1
sub t3, t2, t0
nor t7, t2, t1

Code 4:
lw t1, 22(t0)
and t2, t1, t3

Code 5:
lw t1, 22(t0)
sub t6, t0, t2
xor t3, t1, t5
```

4. For the standard five-stage pipelined datapath, there are three different branch handling mechanisms below. Explain each strategy for the two approaches of implementing the 'beq' (i.e., in ID stage or in MEM stage). Also, for each strategy, answer the following questions:

- How many 'nops' are used if the branch is taken?
- How many 'nops' are used of the branch is not taken?
- Is this solution always applicable? Explain.

a) *stall-on-branch* strategy for implementing the 'beq' instruction.
b) *branch prediction* strategy for implementing the 'beq' instruction.
c) *delayed branch* strategy for implementing the 'beq' instruction.

5. If the 'beq' instruction is implemented in the ID stage, how do the codes below execute correctly? Use forwarding and minimal number of 'nops'. Clearly place 'nops' within the codes and explain where do forwarding(s) take place.

```
Code 1:
sub t1, t2, t3
beq t1, t2, label

Code 2:
sub t1, t2, t3
add t0, t2, t3
beq t1, t2, label

Code 3:
lw t1, 5(s0)
beq t1, t0, label
```

6. (10 points) For five-stage pipelined datapath, please explain each line of the following code and fill "_____":

```
if ( EX/MEM.RegWrite==1 and
     EX/MEM.RegisterRd != 0 and
     EX/MEM.RegisterRd == ID/EX.RegisterRs )
then, forward from _____(which stage?) to _____(which operand of
which stage?)
```

7. For five-stage pipelined datapath, please explain each line of the following code and fill "_____":

```
if ( MEM/WB.RegWrite==1 and
     MEM/WB.RegisterRd != 0 and
     EX/MEM.RegisterRd != ID/EX.RegisterRs and
     MEM/WB.RegisterRd == ID/EX.RegisterRs )
then, forward from _____(which stage?) to _____(which operand of
which stage?)
```

8. The figure below shows how the forwarding unit sets the multiplexers to forward from the MEM or WB stages to the EX stage.

a) What are the values of "ForwardA" and "ForwardB" when the "sub" instruction in EX stage:

```
add $2, $1, $4
sub $3, $2, $1
```

b) What are the values of "ForwardA" and "ForwardB" when the "and" instruction in EX stage:

```
lw $2, 5( $0)
sub $1, $3, $4
and $5, $2, $4
```