Overrun_error

REG

framing_error

REG

data_ready

REG

rx-data   7:0

REG

PRDATA   7:0

REG

n_rst

Data_read   PSLVERR

PENABLE

PSEL

2:0   PADDR

PWRITE

Address Mapping

read_select

write_select

7:0   PWDATA

REG   7:0   Bit_period[7:0]

REG   5:0   Bit_period[13:8]

REG   3:0   Data_size

Address Mapping Logic:
reg error = {ovrerun,framing}
if (pwrite)
if(psel && penable)
if (paddr == 0x2)
write_select = 0x1
else if(padder == 0x4)
write_select == 0x2
else
pslverr = 1
else if pwrite == 0
if (paddr == 0x0)
read_select = 0x1
else if (paddr == 0x1)
read_select = 0x0
else if (paddr == 0x2)
read_select = 0x3
else if (paddr == 0x4)
read_select = 0x4
else if (paddr == 0x6)
read_select = 0x2