ASIC Design Laboratory

Lab 11

Evaluation Sheet

Spring 2020

Student Name: ABDULRAHMAN AJIBADE

Mg Account: MG133

Section: 04

Lab Setup TA Initials Date Score

Lab 11 folder and provided files in Git /1

Layout Process Analysis TA Initials Date Score

What layers are used for supply ring bars /1

Horizontal? metal1 Vertical? metal2

What are the widths of the supply ring bars and their

spacing: /1

Bar Width? 0.01mm Bar Spacing? 0.01mm

What is the spacing between the inner supply ring and the

core area, and which prior command controls this /1

0.01mm

Addring -spacing\_Left -spacing\_Right

How did the design change after running ’place\_cells.tcl’ /1

Cells were in placed in the core

What is a rough estimate for the core utilization /1

80-90%

What changed after running ’sroute’ /1

The cells were connected to ground and power supply rings

1

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In what ways are the three metal layers typically used in the

routing /1

The red metals(2) are used to connect to the pad cells outside the core, the blue metals(1) are used for power and ground connections and the green metals are used for connection between cells

What percentage of the core appears to be filled with cells

after running ’final\_route.tcl’ /1

95%

And which command do you think primarily resulted in the

change /1

setOptMode -MaxDensity

Performing Layout Timing Analysis TA Initials Date Score

What are the starting and ending gate-level components of

the critical path /1

Starting – waddr\_reg[2]

Ending – fiforeg\_reg[2][0]

How many combinational logic cells are in between /1

14

What are the starting and ending blocks (design modules) of

the critical path /1

Starting – DFFSR

Ending – DFFPOSX1

Is the synthesis critical path similar to the layout one? What

are their respective delays /1

No they aren’t. Synthesis arrival – 5.422

layout arrival – 4.61

Pad/Pin Placement based Timing Adjustment TA Initials Date Score

Reduced negative slack after IO-frame adjustment /4

What change(s) were made and why do you think they

resulted in the reduction /2

The U1(d\_minus) and U2(d\_plus) IO pads were put much closer to the U7(transmit) IO pad. The write\_data, write\_enable, fifo\_full and fifo\_empty IO pads were also pushed much closer to each other. This resulted in the reduced slack because there is now less distance between the wiring connection of dedicated IO, hence much faster data transfer time.

Total points for lab /20

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