Ayaz Akram

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Research Interests: Computer Architecture, High Performance Computing, Confidential Computing, Hardware Security, Machine Learning

Education

University of California Davis, CA USA

PhD Computer Science, September 2018 - continued
- Thesis Topic: "Hardware/Software Co-Design for Secure HPC Systems"
- CGPA: 4.0/4.0

Western Michigan University, Kalamazoo, Michigan USA

MS Computer Engineering, January 2015 - August, 2017
- Thesis Topic: "A Study on the Impact of ISAs on Performance of a Processor"
- CGPA: 3.94/4.0

University of Engineering and Technology Lahore, Pakistan

BS., Electrical Engineering, September 2009 - May, 2013
- Thesis Topic: "Android Based ECG Monitoring System"
- CGPA: 3.65/4.0

Research Experience

Research Assistant **September, 2018 - continued**

Working with Prof. Jason Lowe-Power as an RA in DArchR research group at UC Davis, CS Deptartment.
- Working on building hardware/software co-designed architectures for secure HPC.
- Working on DRAM cache models and heterogeneous memory systems.
- Contribute to gem5art, a tool for reproducible and structured experiments with gem5.
- Contribute to gem5 simulator and gem5 resources.
- Instructor for gem5 Bootcamp 2022.

Research Affiliate **January, 2019 - continued**

Collaborating with Dr. Sean Peisert at Usable Data Systems Group at Lawrence Berkeley National Lab (LBNL).
- Working on building confidential computing architectures for HPC.
- Studied the usability of trusted execution environments for HPC.

Computer Architecture Intern **June, 2021 - September, 2021**

Worked as a computer architecture intern with Dr. Steven Woo at Rambus Labs, San Jose, CA.
- Did research on future memory system architecutres for Datacenter systems.
- Worked on building DRAM cache models in gem5 and studying the impact of caching in future disaggregated memory system architectures.
- Presented the above work, alongwith related literature in weekly lab-wide meetings.

Research Assistant **February, 2018 - August, 2018**

Worked as an RA with Dr. Khurram Bhatti at Embedded Computing Lab at Information Technology University, Lahore.
- Built techniques for the detection of microarchitectural side channel attacks.

- Explored the possible research opportunities in the domain of approximate computing.

Research Assistant **January, 2015 - January, 2017**
Worked as an RA with Dr. Lina Sawalha in Computer Architecture and Systems Research Lab (CASRL), WMU.
- Performed an empirical comparative study of various computer architectural simulators and their accuracy with reference to real hardware.
- Investigated the impact of instruction set architectures on performance and power.
- Worked on building new instruction prefetching techniques.

Research Officer **July, 2013 - December, 2014**
Worked at High Performance Computing and Networking Lab (HPCNL), Al-Khwarizmi Institute of Computer Science (KICS), UET Lahore, Pakistan.
- Ported QEMU (system mode emulation) to Cavium Octeon MIPS64 processors
- Helped in writing a proposal to port Xen (famous open source bare-metal hypervisor) to MIPS architecture
- Ported Contiki OS (famous OS for IoT) to stm32f4 discovery board

Teaching Experience

Teaching Assistant **Februaruy 2018 - June 2018**
Worked as a TA at Electrical Engineering Dept. ITU Lahore for Embedded Systems Class.

Lab Instructor/Teaching Assistant **January, 2015 - December, 2017**
Worked as a lab instructor and TA for various classes:
- ECE 2500 Digital Logic.
- ECE 3570 Computer Architecture.
- ECE 2510 Intro. to Microprocessors.

Lab Engineer **September 2013 - November 2013**
Worked as a lab instructor at Electrical Engineering Dept. UET Lahore for the introductory course to Electronics.

Internship

Rambus Labs, Rambus Inc. San Jose, CA **Summer 2021**
Worked as a memory architect intern in the Rambus Labs.

Open Silicon Pvt. Ltd. Lahore, Pakistan **Summer 2012**
Worked on a project of DDR3 Memory Controller's IP Design and Verification.

Research Works

Analyzing Google Workload Traces in gem5, **Ayaz Akram**, Maryam Babaie, Jason Lowe-Power, 5th gem5 Users' Workshop associated with ISCA, June 2023.

What not to do when simulating large workloads!, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power, 5th gem5 Users' Workshop associated with ISCA, June 2023.

Enabling Design Space Exploration of DRAM Caches in Emerging Memory Systems, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2023), April, 2023. arXiv version: `https://arxiv.org/pdf/2303.13029.pdf`

A Cycle-level Unified DRAM Cache Controller Model for 3DXPoint Memory Systems in gem5, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power. arxiv: `https://arxiv.org/pdf/2303.13026.pdf`

HammerSim: A Tool to Model Rowhammer, Kaustav Goswami, **Ayaz Akram**, Hari Venugopalan,

Jason Lowe-Power. Young Architect Workshop (YArch), colocated with ASPLOS 2023.

Toward Rethinking Management Techniques in Emerging Memory Systems, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power. Career Workshop for Inclusion and Diversity in Computer Architecture (with MICRO 2022).

SoK: Limitations of Confidential Computing via TEEs for High-Performance Compute Systems, **Ayaz Akram**, Venkatesh Akella, Sean Peisert, Jason Lowe-Power. IEEE International Symposium on Secure and Private Execution Environment Design (SEED), September 2022.

Toward High-Fidelity Heterogeneous Memory System Modeling in gem5, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power. Workshop on Modeling & Simulation of Systems and Applications (ModSim), August 2022. [**Sudha Award Finalist**].

A Cycle-level Unified DRAM Cache Controller Model in gem5, Maryam Babaie, **Ayaz Akram**, Jason Lowe-Power. 4th gem5 Users' Workshop associated with ISCA, June 2022.

Modeling HBM2 Memory Controller, **Ayaz Akram**, Maryam Babaie, Wendy Elsasser, Jason Lowe-Power. 4th gem5 Users' Workshop associated with ISCA, June 2022.

Data Enclaves for Scientific Computing, **Ayaz Akram**, Venkatesh Akella, Jason Lowe-Power, Sean Peisert. DOE Data Days Workshop, LLNL 2022.

Simulating Trusted Execution Environments in gem5, Workshop on Modeling & Simulation of Systems and Applications (ModSim), August 2021.

Enabling Design Space Exploration for RISC-V Secure Compute Environments, **Ayaz Akram**, Venkatesh Akella, Sean Peisert, Jason Lowe-Power. Fifth Workshop on Computer Architecture Research with RISC-V (CARRV 2021), with ISCA 2021, June 2021.

Performance Analysis of Scientific Computing Workloads on Trusted Execution Environments, **Ayaz Akram**, Anna Giannakou, Venkatesh Akella, Jason Lowe-Power and Sean Peisert, 35th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2021), May, 2021 (preprint available on Arxiv: `https://arxiv.org/pdf/2010.13216.pdf`).

Architectures for Secure High-Performance Computing, **Ayaz Akram**, Young Architect Workshop (YArch '21) held in conjunction with the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April, 2021.

Trusted Execution for High-Performance Computing, **Ayaz Akram**, 15th EuroSys Doctoral Workshop (EuroDW 2021), April 2021.

Enabling reproducible and agile full-system simulation, Bobby Bruce, **Ayaz Akram**, Hoa Nguyen, Kyle Roarty, Mahyar Samani, Marjan Fariborz, Trivikram Reddy, Matt Sinclair, Jason Lowe-Power, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2021), March, 2021. [**Best paper nominee**]

The Tribes of Machine Learning and the Realm of Computer Architecture, **Ayaz Akram**, and Jason Lowe-Power, arXiv preprint: `https://arxiv.org/pdf/2012.04105.pdf`, December, 2020.

Artifact, Reproducibility and Testing Framework for gem5, **Ayaz Akram**, and et al. In Workshop on Modeling & Simulation of Systems and Applications (ModSim'2020), August 2020.

The gem5 Simulator: Version 20.0+, Jason Lowe-Power, Abdul Mutaal Ahmad, **Ayaz Akram**, and

et al., arXiv preprint: `https://arxiv.org/pdf/2007.03152.pdf`, July 2020.

gem5art: Zen and the Art of gem5 Experiments, **Ayaz Akram**, and et al. In gem5 Users' Workshop in conjunction with ISCA 2020, June 2020.

WHISPER A Tool for Run-time Detection of Side-Channel Attacks, M Mushtaq, J Bricq, MK Bhatti, **Ayaz Akram**, V Lapotre, G Gogniat, P Benoit, In IEEE Access, May 2020.

Meet the Sherlock Holmes' of Side Channel Leakage: A Survey of Cache SCA Detection Techniques, **Ayaz Akram**, M Mushtaq, MK Bhatti, V Lapotre, G Gogniat, In IEEE Access, April 2020.

Validation of the gem5 Simulator for x86 Architectures, **Ayaz Akram**, and Lina Sawalha, In IEEE/ACM Performance Modeling, Benchmarking and Simulation of High Performance Computer Systems (PMBS) in conjunction with Supercomputing Conference (SC19), November 2019.

A Study of Performance and Power Consumption Differences Among Different ISAs, **Ayaz Akram**, and Lina Sawalha, In IEEE 21st Euromicro Conference on Digital System Design (DSD), August 2019.

Using Trusted Execution Environments on High Performance Computing Platforms, **Ayaz Akram**, Anna Giannakou, Venkatesh Akella and Jason Lowe-Power and Sean Peisert, In Open-source Enclaves Workshop (OSEW 2019), July 2019.

A Survey of Computer Architecture Simulation Techniques and Tools, **Ayaz Akram**, and Lina Sawalha, In IEEE Access, May 2019.

Sherlock Holmes of Cache Side-Channel Attacks in Intel's x86 Architecture, Maria Mushtaq, **Ayaz Akram**, Muhammad Khurram Bhatti, Usman Ali, Vianney Lapotre, and Guy Gogniat, In IEEE Conference on Communications and Network Security (CNS), June 2019.

FlexCPU: A Configurable Out-of-Order CPU Abstraction, Bradley Wang, **Ayaz Akram**, and Jason Lowe-Power, IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2019.

Machine Learning For Security: The Case of Side-Channel Attack Detection at Run-time, Maria Mushtaq, **Ayaz Akram** et al, In Proceedings of 25th IEEE International Conference on Electronics Circuits and System (ICECS), December 2018.

Run-time Detection of Prime+Probe Side-Channel Attack on AES Encryption Algorithm, Maria Mushtaq, **Ayaz Akram** et al, In Proceedings of Global Information Infrastructure and Networking Symposium (GIIS), October 2018.

NIGHTs-WATCH: A Cache-based Side-channel Intrusion Detector Using Hardware Performance Counters, Maria Mushtaq, **Ayaz Akram** et al, In Proceedings of the 7th International Workshop on Hardware and Architectural Support for Security and Privacy (HASP) in conjunction with ISCA-45, June 2018.

Cache-Based Side-Channel Intrusion Detection using Hardware Performance Counters, Maria Mushtaq, **Ayaz Akram** et al, In 16th CryptArchi Workshop, Lorient France, June 2018.

A Study on the Impact of Instruction Set Architectures on Processor's Performance, **Ayaz Akram**, Master's Thesis. Url: https://scholarworks.wmich.edu/masters_theses/1519.

The Impact of ISAs on Performance, **Ayaz Akram** and Lina Sawalha, In 14th Annual Workshop

on Duplicating, Deconstructing, and Debunking (WDDD) in conjunction with ISCA-44, June 2017.

Emulating an Octeon MIPS64 based Embedded System on X86 in QEMU, Muhammad Amir Mehmood, Qurrat ul Ain, **Ayaz Akram**, Abdul Qadeer and Abdul Waheed, In IEEE 19th International Multi-topic Conference (INMIC), December 2016.

A Comparison of x86 Computer Architecture Simulators [Poster Paper], **Ayaz Akram** and Lina Sawalha, In ACM/IEEE Supercomputing Conference (SC16) November, 2016.

x86 Computer Architectural Simulators: A Comparative Study, **Ayaz Akram** and Lina Sawalha, In IEEE 34th International Conference on Computer Design (ICCD), October 2016.

Android Based ECG Monitoring System, **Ayaz Akram**, Raheel Javed and Awais Ahmad, In International Journal of Science and Research (IJSR), November 2013.

Comparison of Edge Detectors, **Ayaz Akram** and Asad Ismail, In International Journal of Computer Science and Information Technology Research (IJCSITR), October 2013.

Skills

- Programming Languages: C, C++, Java, MATLAB, Python, Bash, Assembly Programming (x86, MIPS, ARM, HCS12, Alpha, RISCV), OpenGL
- Hardware Description Languages: Verilog HDL, VHDL
- Architectural Simulators and Emulators: gem5, Sniper, ZSim, Marssx86, Multi2Sim, QEMU, FireSim, McPAT, DynamoRIO, Wireshark.
- Tools: Xilinx ISE, Xilinx Vivado, ModelSim, Keil, Proteus, ORCAD, Diptrace, Visual Studio, Eclipse, Code Compser Studio, Netbeans, IAR Embedded Workbench, gdb, COOJA simulator, Valgrind, MentorGraphics EDA tools
- Benchmarks: SPEC, NPB, GAPBS, Cloudsuite, MiBench, lmbench, CoreMark, BigDataBench
- Microcontrollers: Atmel89c51, Msp430, stm32f4
- Documentation Tools: Latex, Microsoft Word, Microsoft Visio
- Operating Systems: Unix/Linux, Windows, Contiki OS
- Others: Linux kernel programming, device drivers development, Android app. development.

Awards and Grants

- Graduate Student Travel Grant ($700) from Grauate College WMU for attending SC16.
- Graduate Student Travel Grant ($700) from Graduate College WMU for attending ICCD 2016.
- Graduate Student Travel Grant ($500) from CEAS WMU for attending ICCD 2016.
- Department Level Graduate Research and Creative Scholar Award for 2015-2016.
- Merit based Scholarship by Punjab Govt. for bachelors degree.
- Winner of Microcontroller Interface Competition at SOFTEC FAST NU Lahore 2012.
- Winner of Control the Controller competition at TECHNOFEST UET Lahore 2012.

Academic Projects

- Design of a 4 bit ALU, 8 bit Shifter and a Dual 4*4-Bit Register Bank at transistor level using MentorGraphics EDA tools (for class of Digital Electronics)
- Simulator for state machine of a robotic arm with gui, generic simulator for DFA (for class of Theory Foundations)
- Simulator for different types of branch predictors, simulator for an out of order pipeline, addition of an instruction prefetcher in gem5 (for class of High Performance Computer Architecture)
- Design of frequency meter, design of conveyer belt controller interfaced with LCD using stm32f4 microcontroller (for class of Microcontroller Applications)
- Android based portable ECG monitoring system(Undergraduate Final Year Project)
- 2 DOF Robotic arm interfaced with a pc
- Torch Light Following Robotic Vehicle
- Automatic Traffic Lights Control System with provision of Emergency vehicles