DIGITAL LOGIC SYSTEMS : ASSIGNMENT 6

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Exercise 1.
Prove that every output bit of a decoder depends on all the inputs.

Solution 1.
If possible, let an output bit of a decoder, DECODER(n), be independent of one of the inputs.
Therefore, WLG, let the k^{th} bit of the output be independent of the l^{th} bit of the input.
Let the input be $i[1:n]$ and the output be $o[1:2^n]$.
Therefore, $o[k]$ is unchanged by $flip_l(i)$.
Let o_1 be the output of DECODER(n) for some i_1, such that $o_1[k] = 1$.
Therefore, $o_1[k] = 1$ for $flip_l(i_1)$.
Therefore, either $wt(o_1) \neq 1$, or the output of DECODER(n) is the same for i_1 and $flip_l(i_1)$.
If $wt(o)$, it contradicts the definition of the decoder.
If the outputs for i_1 and $flip_l(i_1)$ are the same, it contradicts the fact that any decoder is one-to-one.
Hence, every output bit of DECODER(n) must be dependent on all the input bits.

Exercise 2.
Prove that the logical connective that corresponds to a MUX-gate is complete. (Hint: Implement a complete set of connectives using only a MUX and constants.)

Solution 2.
Let $D[0]$, $D[1]$, and S be the inputs of a MUX-gate. Let Y be the output of the MUX-gate.
Therefore,

$D[0]$	$D[1]$	$S = X_1$	Y
1	0	0	1
1	0	1	0

Therefore, if $D[0] = 1$, $D[1] = 0$, $S = X_1$, $Y = \neg X_1$.

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$D[0]$	$D[1] = X_1$	$S = X_2$	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

Therefore, if $D[0] = 1$, $D[1] = X_1$, $S = X_2$, $Y = X_1 \wedge X_2$.

$D[0] = X_1$	$D[1]$	$S = X_2$	Y
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

Therefore, if $D[0] = X_1$, $D[1] = 1$, $S = X_2$, $Y = X_1 \vee X_2$.
Therefore, as the complete set of connectives { NOT , AND , OR } can be constructed using a MUX-gate only, it is a complete set of connectives.

Exercise 3.
Design a combinational circuit $JO(n)$ (just one) specified as follows:

Input	$x \in \{0,1\}^n$
Output	$y, z \in \{0,1\}$
Functionality	$z = 1 \iff x = 0^n$, $y = 1 \iff wt(x) = 1$

(1) Prove the correctness of your design.
(2) Analyze the asymptotic cost of your design.
(3) Analyze the asymptotic propagation delay of your design.
(4) Prove asymptotic lower bounds on the cost and propagation delay of $JO(n)$.

Solution 3.

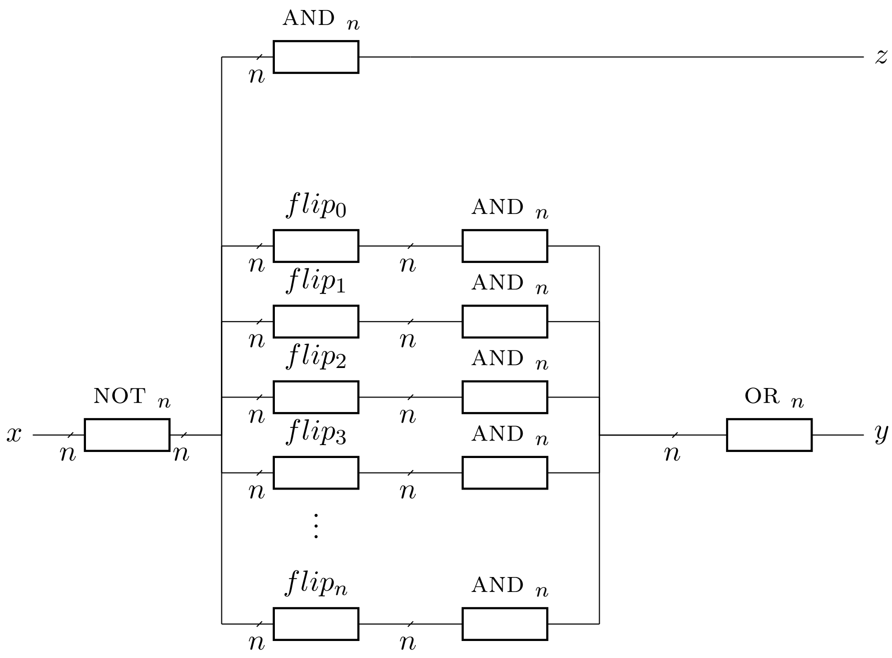

FIGURE 1. $JO(n)$

Where AND $_n$ is AND of n bits, implemented using an optimized AND tree, OR $_n$ is OR of n bits, implemented using an optimized OR .
NOT $_n$ and $flip_i$ are implemented as shown.

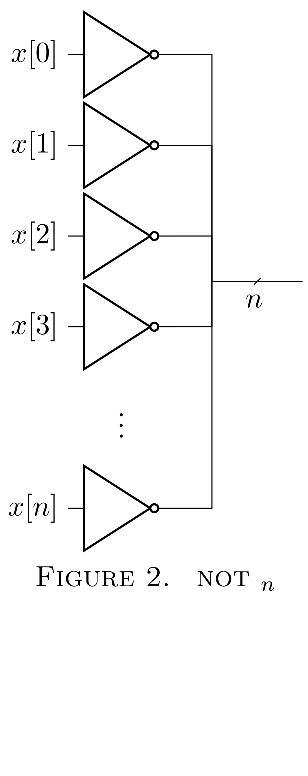

FIGURE 2. NOT $_n$

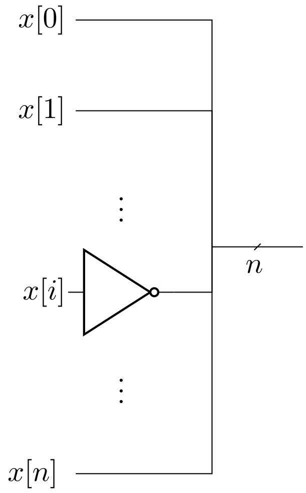

FIGURE 3. $flip_i(x)$

(1)

$$y = \bigoplus_{i=0}^{n-1} \overline{x[0]} \wedge \ldots \wedge x[i] \wedge \ldots \wedge \overline{x[n-1]}$$
$$z = \bigwedge_{i=0}^{n-1} \overline{x[i]}$$

If $n = 1$,

$$y = x[0] \oplus \overline{x[1]}$$
$$z = \overline{x[0]} \wedge \overline{x[1]}$$

Therefore,

$x[0]$	$x[1]$	y	z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	0

Therefore, the circuit $JO(2)$ works as intended.
If possible let $JO(n)$ work as intended.
Therefore,

$$y_n = 1 \iff wt(x_n) = 1$$
$$z_n = 1 \iff x_n = 0^n$$

Therefore,

$$
\begin{aligned}
y_{n+1} &= \bigoplus_{i=0}^{n} \overline{x[0]} \wedge \ldots \wedge x[i] \wedge \ldots \wedge \overline{x[n]} \\
&= \bigoplus_{i=0}^{n} \left(\overline{x[0]} \wedge \ldots \wedge x[i] \wedge \ldots \wedge \overline{x[n-1]}\right) \wedge \overline{x[n]} \\
&= \left(\bigoplus_{i=0}^{n-1} \left(\overline{x[0]} \wedge \ldots \wedge x[i] \wedge \ldots \wedge \overline{x[n-1]}\right) \wedge \overline{x[n]}\right) \\
&\quad \oplus \left(\overline{x[0]} \wedge \ldots \wedge \overline{x[n-1]} \wedge x[n]\right) \\
&= y_n \wedge \overline{x[n]} \oplus \left(\overline{x[0]} \wedge \ldots \wedge \overline{x[n-1]} \wedge x[n]\right)
\end{aligned}
$$

If $x_{n+1}[n] = 0$,

$$
\begin{aligned}
y_{n+1} &= (y_n \wedge 1) \oplus (z_n \wedge 0) \\
&= y_1 \oplus 0 \\
&= y_1 \\
&= wt(x_n) \\
&= wt(x_{n+1})
\end{aligned}
$$

If $x_{n+1}[n] = 1$,

$$
\begin{aligned}
y_{n+1} &= (y_n \wedge 0) \oplus (z_n \wedge 1) \\
&= 0 \oplus z_n
\end{aligned}
$$

$x_n = 0^n$ if and only if $z_n = 1$.
If and only if,

$$
\begin{aligned}
y_{n+1} &= 0 \oplus 1 \\
&= 1
\end{aligned}
$$

Therefore, $y_{n+1} = 1$ if and only if $x[n] = 1$ and $z_n = 1$, i.e. $x[0] = \cdots = x[n-1] = 0$.
Therefore, $wt(x_{n+1}) = 1$.
$x_n \neq 0^n$ if and only if $z_n = 0$.
If and only if,

$$
\begin{aligned}
y_{n+1} &= 0 \oplus 0 \\
&= 0
\end{aligned}
$$

Therefore, $y_{n+1} = 0$ if and only if $x[n] = 1$ and $z_n = 0$, i.e. at least one of $x[0], \ldots, x[n-1]$ is 1. Therefore, $wt(x_{n+1}) > 1$.
Therefore, $y_{n+1} = 1$ if and only if $wt(x_{n+1}) = 1$.

$$\begin{aligned} z_{n+1} &= \bigwedge_{i=0}^{n} \overline{x_{n+1}[i]} \\ &= \left(\bigwedge_{i=0}^{n-1} \bar{[i]} \right) \wedge \overline{x_{n+1}[n]} \\ &= z_n \wedge \overline{x_{n+1}[n]} \end{aligned}$$

If $x_{n+1}[n] = 0$,

$$\begin{aligned} z_{n+1} &= z_n \wedge 1 \\ &= z_n \end{aligned}$$

Therefore, $x_{n+1} = 0^{n+1}$ if and only if $x_n = 0^n$.
If $x_{n+1}[n] = 1$,

$$\begin{aligned} z_{n+1} &= z_n \wedge 0 \\ &= 0 \end{aligned}$$

Therefore, $x_{n+1} \neq 0^{n+1}$ if and only if $x_{n+1}[n] = 1$.
Hence, by induction, $JO(n)$ works as intended, $\forall n \geq 2$. $\square$

(2)

$$\begin{aligned} c(y) = &\quad c(\text{ NOT }_n) \\ &+ n \cdot c(flip) \\ &+ n \cdot c(\text{ AND }_n) \\ &+ c(\text{ OR }_n) \\ = &\quad n \cdot c(\text{ NOT }) \\ &+ n(n-1)c(\text{ NOT }) \\ &+ n(n-1)c(\text{ AND }) \\ &+ (n-1)c(\text{ OR }) \end{aligned}$$

$$\text{cost}(z) = (n-1)\text{cost}(\text{ OR }) + \text{cost}(\text{ NOT })$$

Therefore,

$$\begin{aligned} c(y) &= O\left(n^2\right) \\ c(z) &= O(n) \\ \therefore \text{cost} &= O\left(n^2\right) \end{aligned}$$

(3)

$$\begin{aligned} d(y) &= d(\text{ NOT }_n) + d(flip_i) + d(\text{ AND }_n) + d(\text{ OR }_n) \\ d(z) &= d(\text{ NOT }_n) + d(\text{ AND }_n) \end{aligned}$$

Therefore,

$$\begin{aligned}\text{delay} &= \max\left\{d(y), d(z)\right\} \\ &= d(\text{ NOT }_n) + d(flip_i) + d(\text{ AND }_n) + d(\text{ OR }_n) \\ &= \Theta(\log_2 n)\end{aligned}$$

(4) As the cone of the output is all the inputs, the number of elements in the cone are n.
Therefore, the asymptotic lower bound on the cost is $O(n)$ and the asymptotic lower bound on the delay is $\Theta(\log_2 n)$.