Shivaji University , Kolhapur

Question Bank For Mar 2022 (Summer) Examination

Subject Code: 83856

Subject Name: B.Tech. CBCS of Part IV Semester 7 – Advanced Computer Architecture

Unit 01:

1. List and explain the parallel processing mechanisms in uniprocessor computers.
2. Explain how to evaluate the cost of an Integrated Circuit.
3. Explain the Flynn's classification of computer architectures with neat diagrams.
4. Define the two states of service with respect to an SLA. Explain the two main measures of dependability.
5. Explain the functional structure of SIMD array processor.
6. Why understanding of cost and its factors is essential for designers? Explain the major factors that influence the cost of a computer.
7. Explain functional design of an MIMD Multiprocessor System.
8. Explain the dynamic and static power consumption in CMOS chips.
9. Explain the Flynn's classification of computer architectures with neat diagrams.
10. Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side, assuming a defect density of 0.4 per cm2 and α is 4.

Unit 02:

1. Explain basic concept of pipelined processors with space-time diagrams.
2. Explain Handler's classification of pipeline processor according to levels of processing.
3. Explain the basic structure of linear pipeline processor
4. Explain Ramamoorthy and Li's classification of pipeline processor according to pipeline configurations and control strategies.
5. Explain any four performance evaluation factors for pipeline processors.
6. Draw and explain S-access memory organization.
7. What is the advantage of Interleaved Memory Organizations? Define memory bandwidth and explain the factors affecting on memory bandwidth?

8. Illustrate three classes of data-dependent hazards according to various data update patterns.
9. Draw and explain C-access memory organization.
10. Explain in short how basic scheduling and loop unrolling is used to increase the ILP.

Unit 03:

1. What is principle of locality? Explain the typical memory hierarchy.
2. Explain the set associative scheme of placing the block in a cache.
3. What is Miss rate? Explain three categories of cache misses in three Cs Model.
4. List and explain six basic cache optimizations in short.
5. What is way prediction? How it is used to reduce the cache hit time?
6. Explain the use of loop interchange to reduce the miss rate with example.
7. Explain the use of nonblocking caches to increase the cache bandwidth.
8. Explain the use of blocking to reduce the miss rate with example.
9. Explain the use of write merging to reduce the cache miss penalty with neat figure.
10. Explain the use of compiler-controlled prefetching to reduce the miss penalty or miss rate.

Unit 04:

1. What is Vector Operand? Explain the classification of vector instructions into four primitive types with example.
2. State the three types of pipelined vector processing methods and explain the horizontal vector processing method with example.
3. Explain the three special vector instructions with example: i) Compare ii) Compress iii) Merge
4. State the three types of pipelined vector processing methods and explain the vertical vector processing method with example.
5. Explain the different approaches to enhance to vector processing capability.
6. What are Associative memories? Why they are called as content addressable?
7. Explain the architecture of a typical vector processor with multiple functional pipes with neat diagram.

8. Explain bit serial and bit parallel architectures.
9. Explain the basic structure of a vector architecture, VMIPS.
10. Illustrate the use of associative memory for the storage and retrieval of student file containing Name, Sex, Department, Age & Class, and query given below: Query: Search for those students whose ages are in the range (21, 31).

Unit 05:

1. Explain the data routing and masking mechanisms for processing elements in SIMD computers.
2. Explain NVIDIA GPU Computational Structure.
3. Explain the architectural configuration of SIMD array processors.
4. Explain the programming in GPU with CUDA.
5. Explain the set of parameters defining the SIMD computer.
6. Write note on conditional branching in GPU.
7. Explain the components of Processing Element (PE) in SIMD computer.
8. List and explain the fundamental decisions that determines the architecture of an interconnection network for a SIMD machine.
9. Compare Configuration -I and Configuration -II of SIMD computer.
10. With neat diagram, explain the calculation of the summation S(k)= $\sum A\ ki$= 1 i , k= 0, 1, … ,7 in a SIMD machine.

Unit 06:

1. Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip.
2. What is cache coherence protocol? Explain the two classes of cache coherence protocols.
3. Explain the basic architecture of a distributed-memory multiprocessor.
4. What are the challenges of parallel processing?
5. What is Multiprocessor Cache Coherence?

6. With neat diagram, explain a write invalidate cache coherence protocol for a private write-back cache.
7. Explain the two snooping coherence protocols.
8. Explain directory based cache coherence protocol.
9. What is cache coherence protocol? Explain the two classes of cache coherence protocols.
10. With neat diagram, explain a write invalidate cache coherence protocol for a private write -back cache.