CH-6 **semiconductor**

semiconductors are the substance that has the resistance level between conductors and insulators. It has an electrical conductivity that falls between conductor such as a metallic copper, and an insulator such as glass. Its resistance falls as its temperature rises. The bandgap is smaller in semiconductors (0.6eV - 4eV). They have

- Negative temperature coefficient.
- Resistivity in range roughly 10^7 to 10^{-3} Ω cm.
- Generally high thermo-electric power.
- Rectifying effects.
- High sensitivity to light.

Intrinsic Semiconductors

An intrinsic semiconductor, also called an undoped semiconductor or i-type semiconductor, is a pure semiconductor without any significant dopant species present. The number of charge carriers is therefore determined by the properties of the material itself instead of the amount of impurities. In intrinsic semiconductors, the number of excited electrons is equal to the number of holes; n = p. Silicon and germanium are examples of intrinsic-type semiconductors. It behaves as an insulator at absolute zero. Electrons are excited by thermal energy.

Electron concentration in Intrinsic Semiconductor

In this type of semiconductor, there is a transfer of an electron from the valence band to the conduction band. It leaves the hole behind in the valence band. Then, the number of electrons in the conduction band is equal to the total number of holes in the valence band.

If ‘n’ is the density of electrons, i.e. the number of electrons per unit volume in the conduction band, then in the equilibrium condition,

$$n = \int_{E_c}^{\infty} g(E)F(E)dE \qquad 1$$

where g(E) is the density of states in conduction band.

$$g(E) = \frac{4\pi}{h^3}.\,(2m^*)^{3/2}.\,(E - E_c)^{1/2} \qquad 2$$

Now, the Fermi-Dirac distribution function is given by,

$$F(E) = \frac{1}{1+exp^{\frac{(E-E_F)}{KT}}} \approx exp^{\frac{(E-E_F)}{KT}} \quad for\ (E - E_F) \gg KT$$

Therefore,

$$n = \frac{4\pi}{h^3}.\ (2m^*)^{3/2}.\int_{E_c}^{\infty}(E - E_c)^{1/2} exp^{\frac{(E-E_F)}{KT}}.dE$$

$$n = \frac{4\pi}{h^3}.\ (2m^*)^{3/2}.\int_{E_c}^{\infty}(E - E_c)^{1/2} exp^{\frac{(E_F-E_c)}{KT}}\ exp^{\frac{-(E-E_c)}{KT}}.dE$$

$$n = \frac{4\pi}{h^3}.\ (2m^*)^{3/2}.exp^{\frac{(E_F-E_c)}{KT}}\ \int_{E_c}^{\infty}(E - E_c)^{1/2}\ exp^{\frac{-(E-E_c)}{KT}}.dE$$

put $\frac{(E-E_c)}{KT} = x$ or $E - E_c = KT.x$

then dE= KT dx

when $E = E_{c,}\ x = 0$ & $E = \infty, x = \infty$

now, $n = \frac{4\pi}{h^3}.\ (2m^*)^{3/2}.exp^{\frac{(E_F-E_c)}{KT}}\ \int_0^{\infty}(KT)^{1/2}(x)^{1/2}\ exp^{-x}.KTdx$

$$n = \frac{4\pi}{h^3}.\ (2m^*KT)^{3/2}.exp^{\frac{(E_F-E_c)}{KT}}\ \int_0^{\infty}(x)^{1/2}\ exp^{-x}dx$$

Using standard integration $\int_0^{\infty}(x)^{1/2}\ exp^{-x}dx = \frac{\sqrt{\pi}}{2}$

$$n = \frac{4\pi}{h^3}.\ (2m^*KT)^{3/2}.exp^{\frac{(E_F-E_c)}{KT}}\ .\frac{\sqrt{\pi}}{2}$$

$$n = 2.\left(\frac{2\pi m^*KT}{h^2}\right)^{3/2}.exp^{\frac{(E_F-E_c)}{KT}}$$

$n = N.exp^{\frac{(E_F-E_c)}{KT}}$ where, $N = 2.\left(\frac{2\pi m^*KT}{h^2}\right)^{3/2}$ is the effective density of state at the conduction band edge.

Hole Concentration in Intrinsic Semiconductors

It is the state of energy in the valence band unoccupied by an electron. F (E) gives the probability of occupation for the energy states. There is the probability that it may be unoccupied by an electron is [1-F (E)]. It is the same as that it may be occupied by a hole.

Therefore, the concentration of holes in the valence band is,

$$p = \int_{-\infty}^{E_V} g(E)[1 - F(E)]dE \qquad 1$$

where g(E) is the density of states in conduction band.

$$g(E) = \frac{4\pi}{h^3}.\,(2m^*)^{3/2}.\,(E_V - E)^{1/2} \qquad 2$$

Now, the Fermi-Dirac distribution function is given by,

$$1-\ F(E) = 1-\ \frac{1}{1+exp^{\frac{(E-E_F)}{KT}}} = \frac{exp^{\frac{(E-E_F)}{KT}}}{1+exp^{\frac{(E-E_F)}{KT}}}$$

As $E << E_F$ on the valance band, the term $exp^{\frac{(E-E_F)}{KT}}$ in the denominator can be neglected in comparison to 1.

Therefore, $[1- F(E)] = e^{\frac{(E-E_F)}{KT}}$ 3

$$p = \frac{4\pi}{h^3}.\,(2m^*)^{3/2} \int_{-\infty}^{E_V} (E_V - E)^{1/2}\, e^{\frac{(E-E_F)}{KT}} dE$$

$$p = \frac{4\pi}{h^3}.\,(2m^*)^{3/2}.\int_{-\infty}^{E_V} (E_V - E)^{1/2} e^{\frac{(E_V-E_F)}{KT}}\, e^{\frac{-(E_V-E)}{KT}}.dE$$

$$p = \frac{4\pi}{h^3}.\,(2m^*)^{3/2}.e^{\frac{(E_V-E_F)}{KT}} \int_{-\infty}^{E_V} (E_V - E)^{1/2}\, e^{\frac{-(E_V-E)}{KT}}.dE$$

put $\frac{(E_V-E)}{KT} = x$ or $E_V - E = KT.x$

then dE= - KT dx

when $E = E_{V,}\ x = 0$ & $E = -\infty, x = \infty$

now, $p = \frac{4\pi}{h^3}.\,(2m^*)^{3/2}.e^{\frac{(E_V-E_F)}{KT}} \int_{\infty}^{0} (KT)^{1/2} (x)^{1/2}\, e^{-x}.(-KT)dx$

$$P = \frac{4\pi}{h^3}.\,(2m^*KT)^{3/2}.e^{\frac{(E_V-E_F)}{KT}} \int_{0}^{\infty} (x)^{1/2}\, e^{-x} dx$$

Using standard integration $\int_0^\infty (x)^{1/2}\, exp^{-x} dx = \frac{\sqrt{\pi}}{2}$

$$p = \frac{4\pi}{h^3}.(2m^*KT)^{3/2}.e^{\frac{(E_V-E_F)}{KT}}.\frac{\sqrt{\pi}}{2}$$

$$p = 2.\left(\frac{2\pi m^*KT}{h^2}\right)^{3/2}.e^{\frac{(E_V-E_F)}{KT}}$$

$p = N.e^{\frac{(E_V-E_F)}{KT}}$ where, $N = 2.\left(\frac{2\pi m^*KT}{h^2}\right)^{3/2}$ is the effective density of state at the valence band edge. [m^*- be the effective mass of hole.]

Fermi-Level in Intrinsic Semiconductor

For an intrinsic Semiconductor, the number of electrons in the conduction band 'n' is equal to the number of holes in the valence band p. This is because the electrons and holes are in pairs.

$$n = p$$

$$2.\left(\frac{2\pi m_e^*KT}{h^2}\right)^{3/2}.e^{\frac{(E_F-E_C)}{KT}} = 2.\left(\frac{2\pi m_h^*KT}{h^2}\right)^{3/2}.e^{\frac{(E_V-E_F)}{KT}}$$

$$(m_e^*)^{3/2}.e^{\frac{(E_F-E_C)}{KT}} = (m_h^*)^{3/2}.e^{\frac{(E_V-E_F)}{KT}}$$

$$e^{\frac{(2E_F-E_C-E_V)}{KT}} = \left(\frac{m_h^*}{m_e^*}\right)^{3/2}$$

If we take natural log on both sides, we get,

$$\frac{(2E_F - E_c - E_V)}{KT} = \frac{3}{2}ln\left(\frac{m_h^*}{m_e^*}\right)$$

$$E_F = \frac{(E_c + E_V)}{2} + \frac{3}{4}ln\left(\frac{m_h^*}{m_e^*}\right)$$

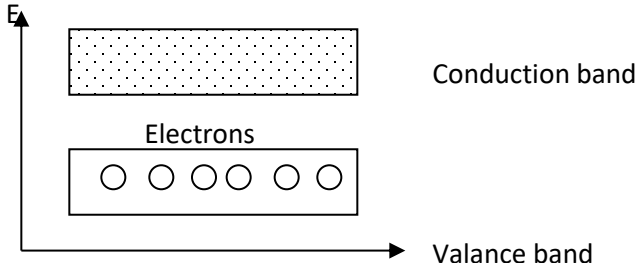
At T= 0

$$E_F = \frac{(E_c + E_V)}{2}$$

So, at absolute zero temperature, the Fermi level lies exactly halfway between the top of the valence band and bottom of the conduction band.

Extrinsic Semiconductors

An intrinsic semiconductor is one which is made of the semiconductor material in its extremely pure form. Common examples of such semiconductors are pure germanium and silicon which have small energy gaps. The energy gap is so small that even at ordinary room temperature; there are many electron which possess sufficient energy to jump across the small energy gap between the valance and the conduction bands. However, it is worth noting that for each electron liberated into the conduction band, a positively charged hole is created in the valance band

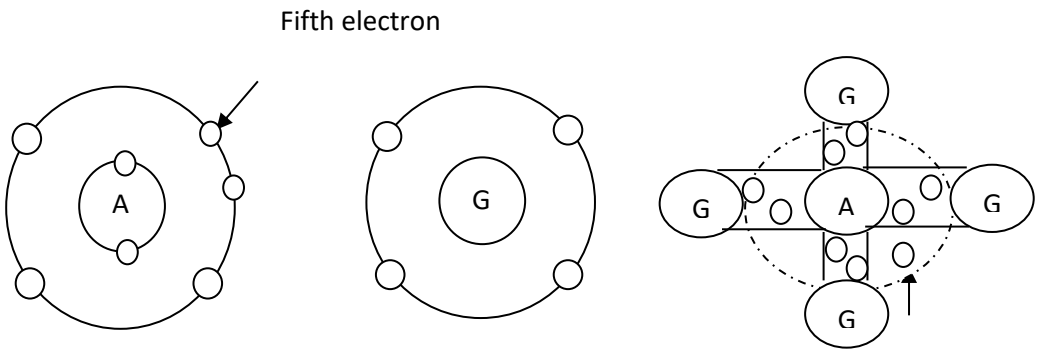


When an electric field is applied to an intrinsic semiconductor (i.e. battery is connected) at a temperature greater than OK, conduction electrons move to the cathode. Hence, semiconductor current consists of movement of electrons and holes in opposite directions.

An extrinsic semiconductor makes the semiconductor electronic devices such as diodes, transistors, etc. Devices that enable current switching also make use of extrinsic semiconductors such as transistors. Bipolar junction transistors are the types of transistors. Field-effect transistors are also the type of transistors. We use extrinsic semiconductors for making these.

N-type Semiconductors

Semiconductors that has been doped with a pentavalent impurities is called an n type semiconductors, where N stands for negative, the figure shows what happens when antimony is doped to the germanium. As shown in figure, each antimony atom forms covalent bonds with the surrounding four germanium atoms with the help of four of its five electrons. The fifth electron is extra and is loosely bound to the antimony atom.



Hence, it can be easily excited from the valence band to the conduction band by the application of electric field or increase in thermal energy. Thus, practically every antimony atom introduce into the germanium lattice, contributes one conduction electron into the germanium lattice without creating a positive hole. Antimony is called donor impurity and makes the pure germanium an N type (N for negative) extrinsic semiconductor.

Even through N type semiconductor has excess of electrons, still it is electrically neutral. It is so because by addition by donor impurity, number of electrons available for conduction purposes becomes more than the number of semiconductor doesn't change because the donor impurity brings in as much negative charge (by may of electrons) as positive charge (by way of proton in its nucleas).

P-type Semiconductors

P-type semiconductors are those extrinsic semiconductors doped with a trivalent impurity element which consists of three electrons in its valence shell. These pentavalent impurities increase the number of electrons for the conduction. The trivalent impurities added provides extra holes known as the acceptor atom. The majority carriers in a p-type semiconductor are holes.

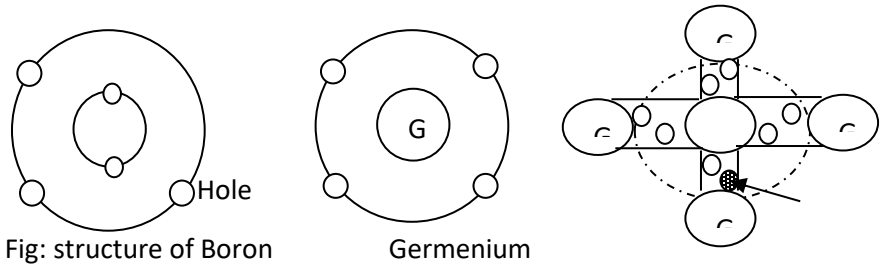


Fig: structure of Boron Germenium

Fig: Adding proces

Carrier concentration in extrinsic semiconductor

The intrinsic carrier concentration is the number of electrons in the conduction band or the number of holes in the valence band in intrinsic material.

Let,

n_0: thermal-equilibrium concentration of electrons

p_0: thermal-equilibrium concentration of holes

n_d: concentration of electrons in the donor energy state

p_a: concentration of holes in the acceptor energy state

N_d: concentration of donor atoms

$N_{a:}$ concentration of acceptor atoms

N_d^+: concentration of positively charged donors (ionized donors)

N_a^-: concentration of negatively charged acceptors (ionized acceptors)

By definition,

$N_d^+ = N_d - n_d$

$N_a^- = N_a - P_a$

by the charge neutrality condition,

$n_o + N_a^- = P_o + N_d^+$

or $n_0 + (N_a - P_a) = P_o + (N_d - n_d)$

assume complete ionization,

$$P_a = n_d = 0$$

then, $n_0 + N_a = P_o + N_d$

From Mass-Action law ($n_o P_o = n_i^2$)

$n_o = \frac{1}{2}[(N_d - N_a) + \sqrt{(N_d - N_a)^2 + 4n_i^2}\,]$, where $N_d > N_a$ (n-type)

$P_o = \frac{1}{2}[(N_a - N_d) + \sqrt{(N_a - N_d)^2 + 4n_i^2}\ ]$, where $N_a > N_d$ (p-type)

$n_o = P_o = n_i$, where $N_a = N_d$ (intrinsic type)

conductivity of semiconductor

In semiconductor, the conduction band electron and valance band hole participate in electrical conduction. To obtain expression for electrical conductivity consider an intrinsic semiconductor bar wchich is connected to external battery as shown in fig

The electric field exist along x direction. The field accelerate electrons (conduction electrons) along negative X-direction and holes along positive X-direction. They starts moving with a constant velocity called Drift velocity vd

The total current in the semiconductor (due to both electron and hole)

I = $I_e + I_h$

or total current density

J = $J_e + J_h$ .....(1)

In order to find the current density of electrons, let the concentration of electrons are 'n' , charge is 'e' and drift velocity is 've', Then

Je = nev_e. .....(2)

The drift velocity produced per unit electric field is called 'mobility' , Thus

$\mu_e = \frac{v_e}{E}$ or $\mu_e E = v_e$

So, $J_e = ne\ \mu_e E$ ….3

From ohms law,

$$J_e = \sigma_e E = ne\ \mu_e E$$

And conductivity of electrons

$\sigma_e = ne\ \mu_e$ ….5

Similarly, current density for holes

$J_p = \sigma_p E = ne\ \mu_p E$

And conductivity of holes

$\sigma_p = ne\,\mu_p$ ….6

From eq 1,5&6

J = $J_e + J_h = ne\,\mu_e E + ne\,\mu_p E$ = ne ($\mu_e + \mu_p$)E …7

And σ = ne ($\mu_e + \mu_p$) ….8

Also, $n_i = \left(\frac{2\pi m^* KT}{h^2}\right)^{3/2} . e^{\frac{-E_g}{2KT}}$

= C $(T)^{3/2} . e^{\frac{-E_g}{2KT}}$

Therefore,

$\sigma = n_i$e ($\mu_e + \mu_p$) = C $(T)^{3/2} . e^{\frac{-E_g}{2KT}}$. e ($\mu_e + \mu_p$) ..9

The mobilities of carrier

$\mu \propto \frac{1}{T^{3/2}}$

for electron $\mu_e = \alpha\, T^{-3/2}$ and for holes $\mu_p = \beta\, T^{-3/2}$

$\mu_e + \mu_p$ = (α + β) $T^{-3/2} = \gamma\, T^{-3/2}$ ..10

So, from eq 9

σ = C $(T)^{3/2} . e^{\frac{-E_g}{2KT}}$. e γ $T^{-3/2}$

σ = C e γ. $e^{\frac{-E_g}{2KT}}$

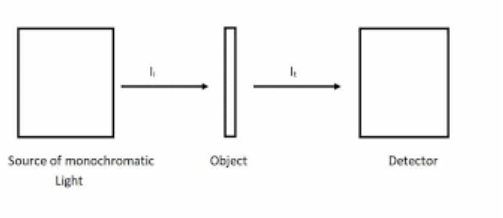
$\sigma = B . e^{\frac{-E_g}{2KT}}$

Photoconductivity

Photoconductivity is an electrical and optical phenomenon in which a material becomes conductive and electric due to the absorption of electromagnetic radiation such as infrared light, ultraviolet light, visible light, or gamma radiation. As soon as

a semiconductor material absorbs light, the number of charge carriers and its electrical conductivity increases. It is the tendency of a substance to conduct electricity to an extent that depends on the intensity of the light radiant energy impinging on the surface of a sample. Most semiconductor materials have this property.

In the semiconductor's energy-band diagram, the number of charge carriers like electrons within the conduction band is significantly low as compared to conductors. But, there are also charge carriers like holes within the valence band. These are known as vacancies which are left by electrons and moved to the conduction band. The following diagram shows charge carriers within a semiconductor. The conduction of the current within a semiconductor takes place by electrons & holes within the valence band.



Once the light rays drop on the semiconducting material, then the electrons in the valence band absorb the photons & jump immediately into the conduction band by leaving holes. So the increased number of electrons & holes within both the bands will increase the material's conductivity. So the conductivity increase is mainly because of the light dropping on the material, which is known as photoconductivity.

These materials are mainly used

- to sense infrared radiation within military-based applications from guiding missiles to heat-generating targets.
- used in the process of xerography or photocopying, which formerly used selenium however now it relies on photoconductive polymers.
- used in street lights, camera light meters, clock radios, nanophotonic systems, infrared detectors & photo-sensors devices with low-dimensional.
- used for X-Ray image detectors
- These are used for relay control
- These are used to switch on & off transistors.

- These can be used with an op-amp-based Schmitt trigger circuit.
- These are used to control the level of current flow within an LED.

Metal - Metal Junction

When two metals with differing fermi energies and work functions come into contact, electrons from the higher fermi level metal begin to cross across to the lower fermi level metal. Metal that has lost electrons is positively charged, while metal that has gained electrons is negatively charged. As a result, a potential difference known as contact potential develops at the junction.

The overall energy of electrons in the metal-metal system is reduced by this electron transfer from one metal to another. This process is repeated until the voltage is high enough to prevent further electron transfer. As a result, the system achieves equilibrium. The fermi levels of both atoms will be the same at equilibrium.

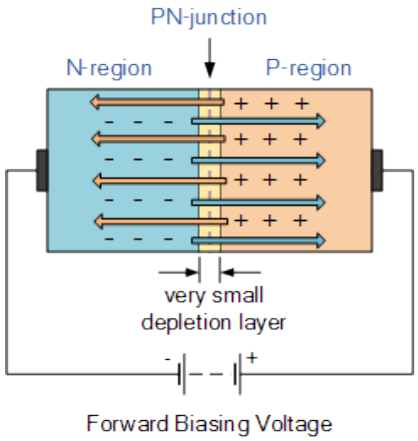
P-N junction semiconductor diode

A p-n junction diode is two-terminal or two-electrode semiconductor device, which allows the electric current in only one direction while blocks the electric current in opposite or reverse direction. If the diode is forward biased, it allows the electric current flow. On the other hand, if the diode is reverse biased, it blocks the electric current flow. P-N junction semiconductor diode is also called as p-n junction semiconductor device. In n-type semiconductors, free electrons are the majority charge carriers whereas in p-type semiconductors, holes are the majority charge carriers. When the n-type semiconductor is joined with the p-type semiconductor, a p-n junction is formed. The p-n junction, which is formed when the p-type and n-type semiconductors are joined, is called as p-n junction diode.

Forward Biased PN Junction Diode

When a diode is connected in a Forward Bias condition, a negative voltage is applied to the N-type material and a positive voltage is applied to the P-type material. If this external voltage becomes greater than the value of the potential barrier, approx. 0.7 volts for silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow.

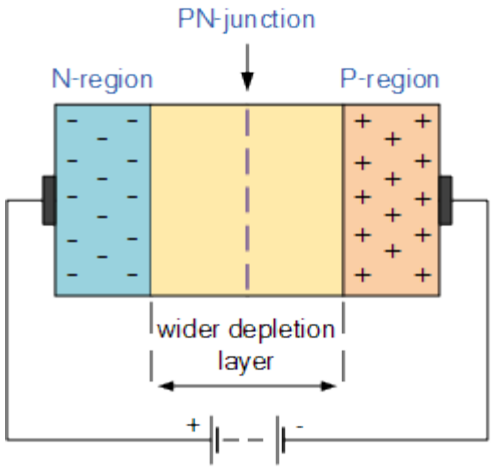
This is because the negative voltage pushes or repels electrons towards the junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage. This results in a characteristics curve of zero current flowing up to this voltage point, called the “knee” on the static curves and then a high current flow through the diode with little increase in the external voltage as shown below.



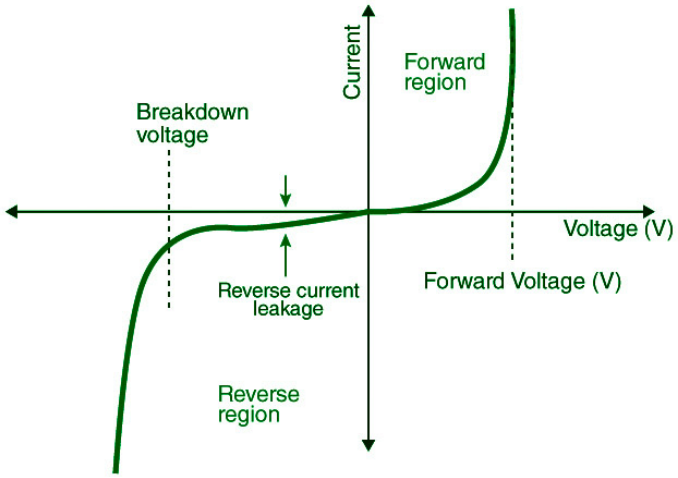
Reverse Biased PN Junction Diode

When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material. The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.

The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator and a high potential barrier is created across the junction thus preventing current from flowing through the semiconductor material.



Reverse Biasing Voltage



Bipolar junction Transistor

A bipolar junction transistor is a semiconductor device made of three layers of p and N type semiconductors. Depending upon the layers formed there are two types of transistor PNP and NPN. In PNP transistor a thin layer of n semiconductor is sandwiched between two thicker layers of p type semiconductors. Similarly, in NPN transistor a thin layer of p type semiconductor is sandwiched between two

thicker layers of n type semiconductors. The structural diagrams and circuit diagram symbols of pnp and npn transistor are depicted in Fig.

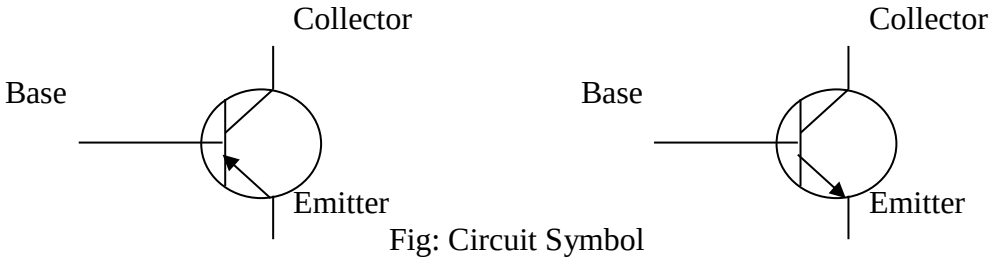


Fig: Circuit Symbol

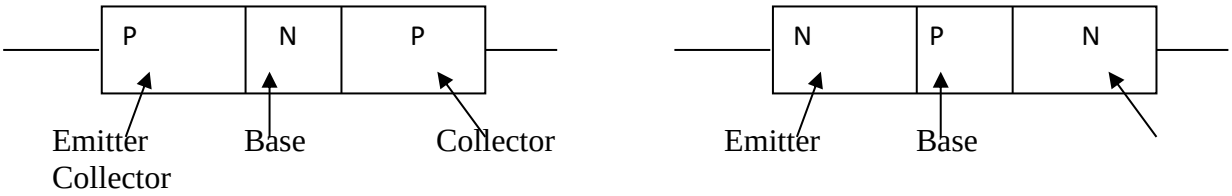


Fig: Structural Diagram

The first layer is called EMITTER. It is highly doped and its function is to supply charges to make current flow in the device. The third or last layer is called COLLECTOR. It is moderately doped. It is to collect charges coming from emitter. The middle section is called BASE. It is lightly doped and its function is to control the charges following from emitter to collector. In other words bade controls the collector current.

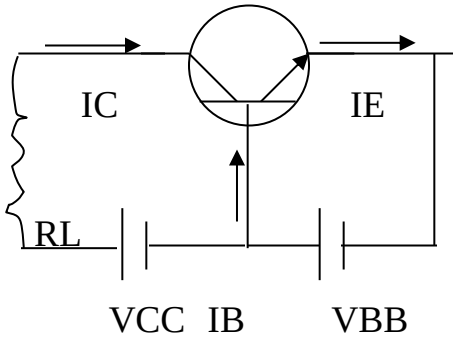
The PN junction between the emitter and base is called emitter-base junction and the PN junction that exists between the collector and base is called collection-base junction. For normal operation of the transistor i.e. to operate the transistor, as an amplifier the emitter-base junction must be forward biased and the collector-base junction must be reverse biased.

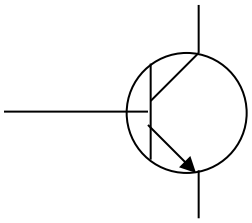
Transistor operation circuits:- The transistor can be connected in the following three different circuit configurations.

1. Common Base Circuit
2. Common Emitter Circuit
3. Common Collector Circuit

1. Common Base Circuit:- In this circuit connection emitter is the input terminal. The input signal to be amplified is fed to the emitter. Collector is the output. The load RL is connected at the collector terminal. The base terminal is common to both the input and output terminals.

2. Common Emitter Circuit:- In this circuit connection Base is the input terminal. The input signal needed to be amplified is fed between the emitter and Base. Collector is the output. So the load RL is connected between the collector and Emitter. Emitter is the common to both the input and output terminals.
3. Common Collector Circuit:- In this circuit connection Base is the input terminal and Emitter is the output terminal. The input signal is fed between the Base and Collector and the output signal is received between Emitter and Collector. So the load RL is connected to the Emitter terminal. Collector is the common to both the input and output terminals.





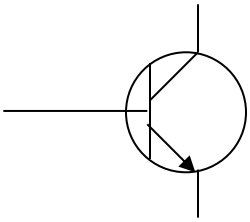


Fig: Common Base circuit Fig: Common Emitter circuit Fig: Common Collector circuit

Characteristics curves of CE transistor circuits

Input characteristics

The curve drawn between base current Ib and base emitter voltage Vbe for a given value of collector emitter voltage Vce is known as the input characteristics.

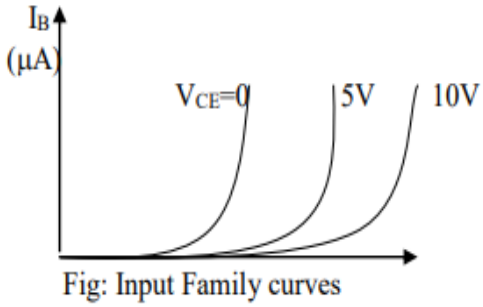


Fig: Input Family curves

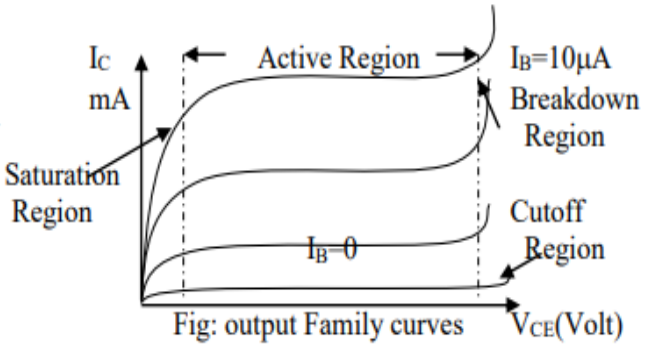


Fig: output Family curves

Output characteristics

it is the curve between collector current Ic and collector emitter voltage Vce for a given value of base current Ib.

a) Saturation region: in this region Vce<1 and collector base junction becomes forward biased. As it is obvious from the output family curves that the collector current changes greatly with Vce.

b) Active region: in this region Vce greater than 1 and less than Vbr. collector current practically does not depends upon Vce. As it is obvious from the curves Ic depends upon the input current Ib. The transistor should operate in this region.

c) Breakdown region: when the voltage between collector and emitter Vce becomes greater than Vbr (Breakdown voltage) the transistor enters into the breakdown region. The transistor should not be operated in this region.

Common Emitter Amplifier

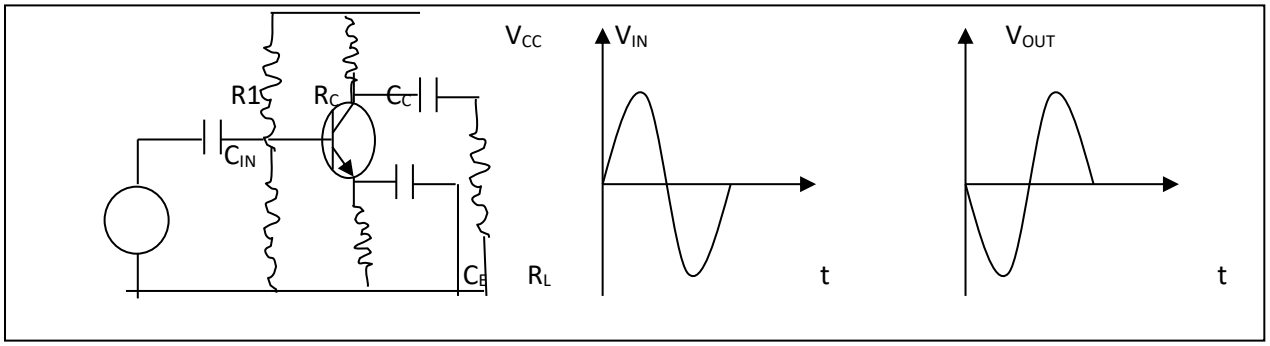


Fig. Shows the circuit of a single Stage CE amplifier using an NPN transistor. Here, Base is the driven element. The input signal is injected into the base emitter circuit where output signal is taken out from the collector-Emitter circuit. The EB junction is forward biased by VBB, CB junction is reverse biased by VCC.

Circuit operation: -when positive half cycle of the signal is applied: -

(1) VBE is increased because it is already positive w.r.t. the ground as per biasing rule.
(2) It leads to increase in forward bias of base-Emitter junction.
(3) IB is increased somewhat.

(4) IC is increased by β times the increased in IB.
(5) Drop ICRC is increased considerably & consequently.
(6) VCE is decreased as seen from the fig, VCE = VCC- ICRC.

Hence, negative half cycle of the output is obtained. It means that a positive going input signal becomes a negative going output signal. Similarly, in -ve half cycle input +ve half cycle output is obtained.

Various Gains of a CE amplifier

(1) Rin = RB// βre ≈ βre , where βre is the ac resistance viewed from base.(1k to 2K)
(2) Rout = RC, if the RL is connected across RC then, rout = RC//RL.(50K or So)
(3) Current gain A; = β is high.
(4) Voltage Gain AV is high about 1500 or so.
(5) Power Gain (Ap) is very high (10000 times or 40 dB).
(6) It produces phase reversal of input signal.

Field Effect Transistor (FET)

A Field Effect Transistor (FET) is a three-terminal semiconductor device. Its operation is based on a controlled input voltage. By appearance JFET and bipolar transistors are very similar. However, BJT is a current controlled device and JFET is controlled by input voltage. Most commonly two types of FETs are available.

Junction Field Effect Transistor (JFET)
Metal Oxide Semiconductor FET (IGFET)
Junction Field Effect Transistor

The functioning of Junction Field Effect Transistor depends upon the flow of majority carriers (electrons or holes) only. Basically, JFETs consist of an N type or P type silicon bar containing PN junctions at the sides. Following are some important points to remember about FET −

Gate − By using diffusion or alloying technique, both sides of N type bar are heavily doped to create PN junction. These doped regions are called gate (G).

Source − It is the entry point for majority carriers through which they enter into the semiconductor bar.

Drain − It is the exit point for majority carriers through which they leave the semiconductor bar.

Channel − It is the area of N type material through which majority carriers pass from the source to drain.

There are two types of JFETs commonly used in the field semiconductor devices: N-Channel JFET and P-Channel JFET.

N-Channel JFET

It has a thin layer of N type material formed on P type substrate. Following figure shows the crystal structure and schematic symbol of an N-channel JFET. Then the gate is formed on top of the N channel with P type material. At the end of the channel and the gate, lead wires are attached and the substrate has no connection.

When a DC voltage source is connected to the source and the drain leads of a JFET, maximum current will flow through the channel. The same amount of current will flow from the source and the drain terminals. The amount of channel current flow will be determined by the value of VDD and the internal resistance of the channel.

A typical value of source-drain resistance of a JFET is quite a few hundred ohms. It is clear that even when the gate is open full current conduction will take place in the channel. Essentially, the amount of bias voltage applied at ID, controls the flow of current carriers passing through the channel of a JFET. With a small change in gate voltage, JFET can be controlled anywhere between full conduction and cutoff state.

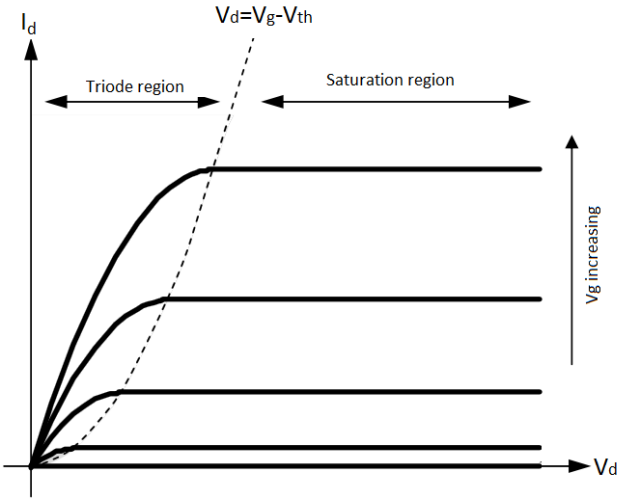
P-Channel JFETs

It has a thin layer of P type material formed on N type substrate. The following figure shows the crystal structure and schematic symbol of an N-channel JFET. The gate is formed on top of the P channel with N type material. At the end of the channel and the gate, lead wires are attached. Rest of the construction details are similar to that of N- channel JFET.

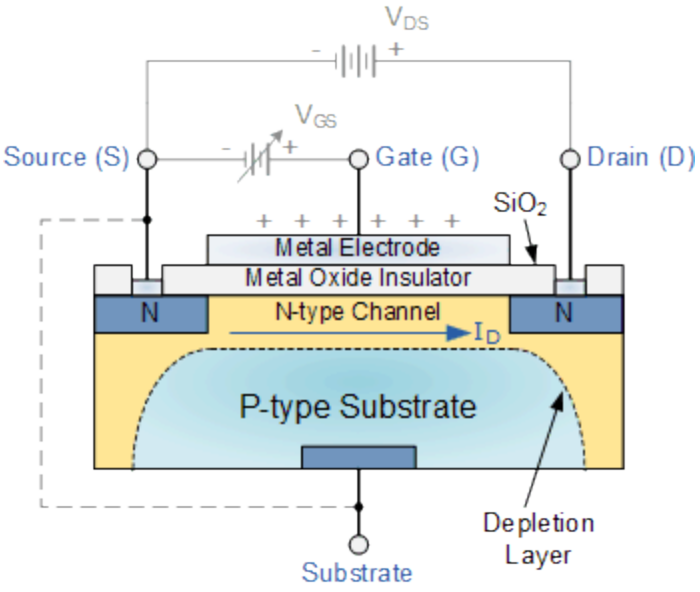
Normally for general operation, the gate terminal is made positive with respect to the source terminal. The size of the P-N junction depletion layer depends upon fluctuations in the values of reverse biased gate voltage. With a small change in gate voltage, JFET can be controlled anywhere between full conduction and cutoff state.

Output Characteristics of JFET

The output characteristics of JFET are drawn between drain current (ID) and drain source voltage (VDS) at constant gate source voltage (VGS) as shown in the following figure. Initially, the drain current (ID) rises rapidly with drain source voltage (VDS) however suddenly becomes constant at a voltage known as pinch-off voltage (VP). Above pinch-off voltage, the channel width becomes so narrow that it allows very small drain current to pass through it. Therefore, drain current (ID) remains constant above pinch-off voltage.

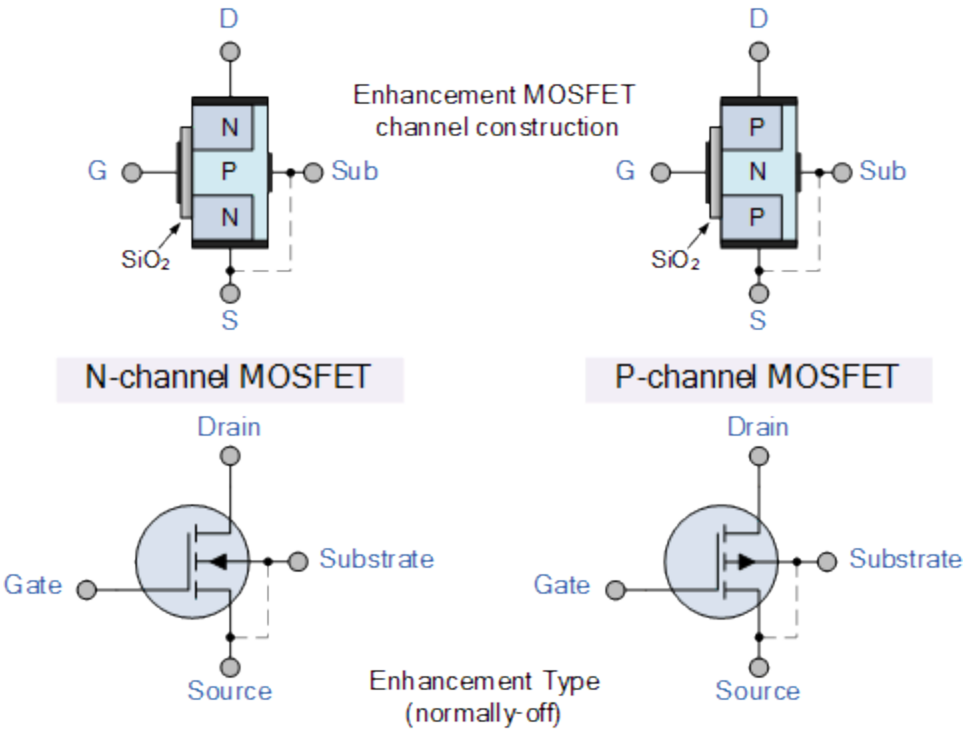


Metal Oxide Semiconductor Field Effect Transistor [MOSFET]



The construction of the Metal Oxide Semiconductor FET is very different to that of the Junction FET. Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel. The gate electrode is placed on top of a very thin insulating layer and there are a pair of small n-type regions just under the drain and source electrodes.

We saw in the previous tutorial, that the gate of a junction field effect transistor, JFET must be biased in such a way as to reverse-bias the pn-junction. With a insulated gate MOSFET device no such limitations apply so it is possible to bias the gate of a M OSFET in either polarity, positive (+ve) or negative (-ve).



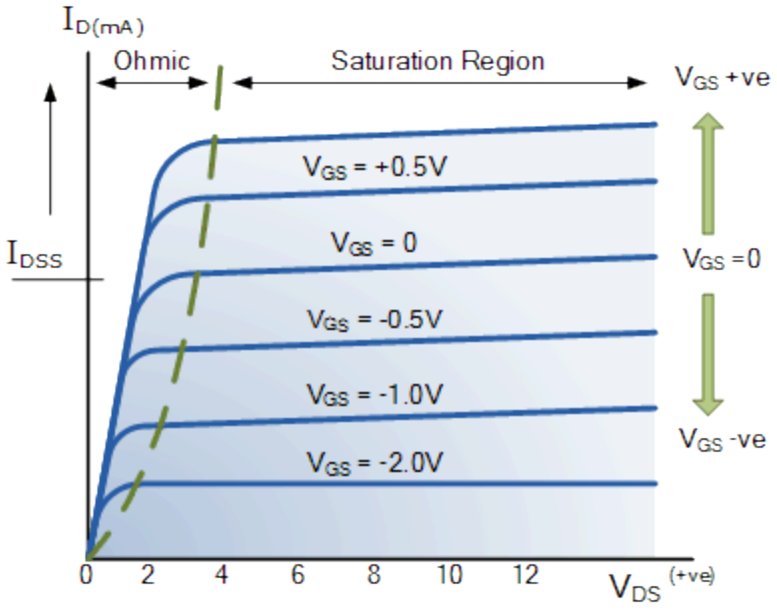
MOSFET Regions of Operation

The operation of this device happens mainly in three regions and those are as follows:

Cut-off Region – It is the region where the device will be in the OFF condition and there zero amount of current flow through it. Here, the device functions as a basic switch and is so employed as when they are necessary to operate as electrical switches.

Saturation Region – In this region, the devices will have their drain to source current value as constant without considering the enhancement in the voltage across the drain to source. This happens only once when the voltage across the drain to source terminal increases more than the pinch-off voltage value. In this scenario, the device functions as a closed switch where a saturated level of current across the drain to source terminals flows. Due to this, the saturation region is selected when the devices are supposed to perform switching.

Linear/Ohmic Region – It is the region where the current across the drain to source terminal enhances with the increment in the voltage across the drain to source path. When the MOSFET devices function in this linear region, they perform amplifier functionality.


$I_{D(mA)}$
Ohmic
Saturation Region
V_{GS} +ve
V_{GS} = +0.5V
V_{GS} = 0
V_{GS} =0
I_{DSS}
V_{GS} = -0.5V
V_{GS} = -1.0V
V_{GS} -ve
V_{GS} = -2.0V
0
2
4
6
8
10
12
V_{DS} (+ve)