POWER ELECTRONICS LABORATORY

Wireless Class D Resonant Converter

Instructor:
Lei GU
Assistant Professor
Dept. of Electrical and Systems Engineering
200 South 33rd Street
Philadelphia, PA 19104-6314
E: leigu@seas.upenn.edu
T: (215) 898-3827

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1 Introduction

The objective of this lab is to analyze the operating behaviour of a wireless Class D resonant dc-dc converter. You will use simulations in LTSPICE and experiments to obtain the power transfer characteristics at different frequencies and loads as well as their waveforms.

A simplified schematic of the Class D converter you will be implementing in the lab is shown in Fig. 1.

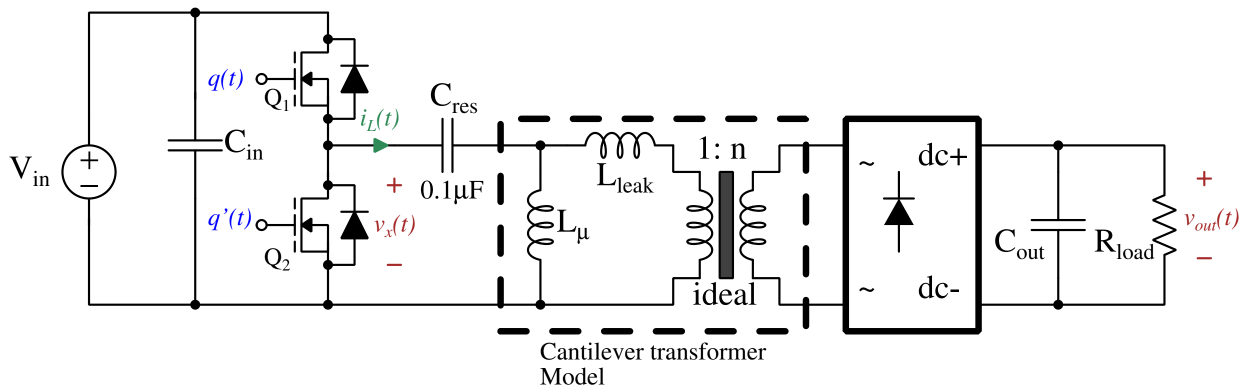


Figure 1: Schematic of the Class D converter.

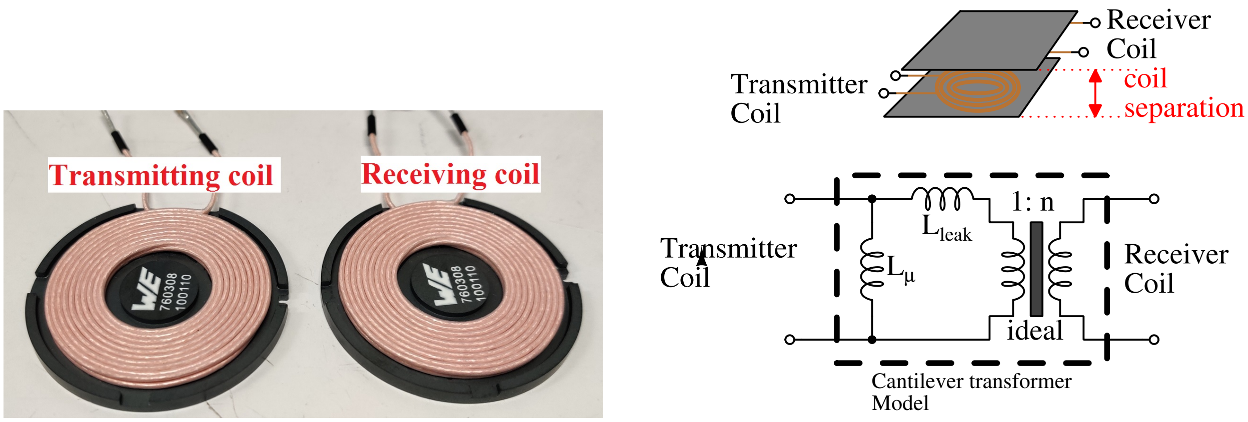
Primary-Side Inverter Board: We will use a half-bridge resonant inverter for the primary side. You will need to assemble the inverter on a pre-designed printed circuit board (PCB). We still use the half-bridge driver SI8274 from Skyworks to drive the two switches in the half-bridge circuit. Similarly, we use an isolated dc-dc converter (ADUM5028) to provide power for the high-side gating in this lab. Using an isolated dc-dc converter avoids the diode voltage drop in a bootstrap based high-side switch gate driver, which reduces the on-state resistance and conduction losses of the high-side switch.

Secondary-Side Rectifier Board: We do not have a PCB for this board. You will need to make a rectifier using bare FR4 boards and schottky diodes like you did in ESE5800. Don't forget to put enough filtering high-frequency capacitors across the dc output terminal. You will connect the electronic load at the dc output of your converter.

In all of these boards, there are no additional safety or protection circuitry other than the ones internally present in the integrated circuits. The reason for this is simplicity. You will be expected to understand the complete operation of the boards and have the tools necessary to repair it if something fails.

2 Wireless Receiver and Transceiver Coil Characterization

The transformer you'll be using to send power wirelessly consist an identical receiver and transmitter coil. The transmitter and receiver coils are shown in Fig. 2a. As shown in Fig. 2b, the



(a) Tx-Rx coils **(b)** Cantilever model

Figure 2: (a)Transmitter and receiver coils. (b) Equivalent cantilever model of the T_X/R_X coils

T_X/R_X coils can couple energy by placing one of the coils on top of the other. As explained in lecture, the electrical behavior of arrangement can be modeled using the cantilever transformer model. The converter's resonant tank consists of capacitor C_{res} and inductors L_μ and L_{leak} of the cantilever model of Fig. 2b. Hence, the magnetizing inductance L_μ and leakage inductance L_{leak} of the T_X/R_X coils are part of the components in your resonant tank. The parameters of the cantilever model will be a function of the distance between the T_X/R_X and their alignment.

In order to properly simulate this circuit, you'll need to determine the parameters of the cantilever model as the separation between the T_X/R_X changes.

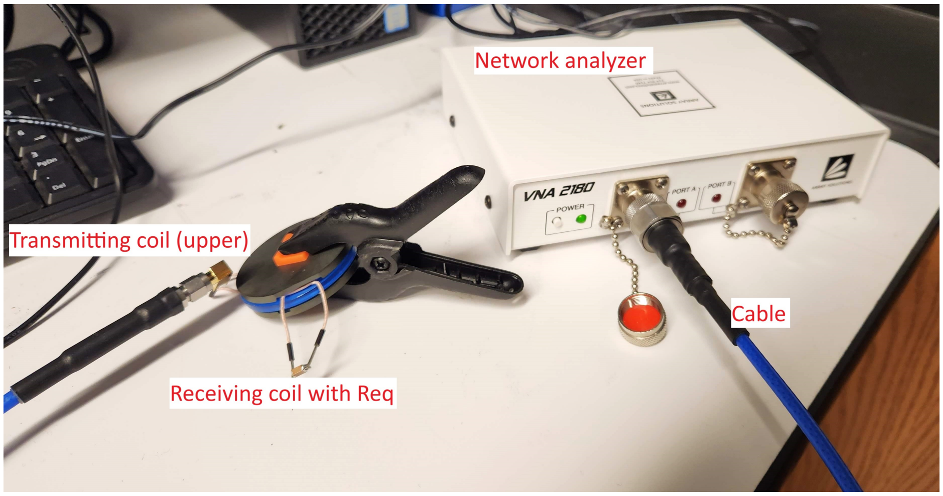
You can use the VNA 2180 impedance analyzer on station 6 in the maker space (Fig. 3). To get accurate measurements, you will need to properly calibrate the analyzer before you measure the actual coil (calibrating at short, open, and 50 Ω). The operating manuals of the VNA 2180 impedance analyzer can be found in the coursework site.

List and/or plot the parameters of the cantilever model (L_μ, L_{leak}, n) when the T_X/R_X are aligned. Use the Acrylic spacer shown in Fig. 8 and clamp to hold the T_X/R_X together.

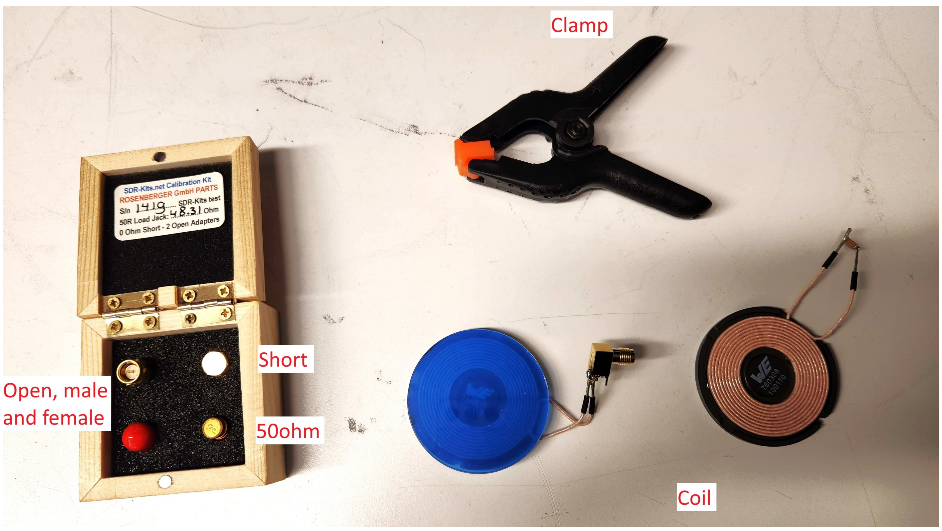
The output dc load of the converter of Fig. 1 is 5 Ω connected at the output of the rectifier. But to see how the load affects the resonant tank, we will use a low power $4\ \Omega$ resistor connected to the R_x coil to measure the impedance at the input of the resonant tank (Fig. 4). **This is a small signal measurement, Do not connect the coils to the main power circuit when the low power resistor is connected to the R_x coil. If you do, the low power resistor may quickly burn and damage your circuit. It may even glow! e.g. `http://www.youtube.com/watch?v=sI5Ftm1-jik`, PLEASE DO NOT attempt.**

Remember that at the fundamental frequency, the equivalent resistance at the input of a full wave rectifier with voltage filter is:

$$R_{eq} = \frac{8}{\pi^2} R_{out}$$



(a)



(b)

Figure 3: Impedance analyzer with probe and calibration standards

Using the VNA 2180 impedance analyzer, measure the impedance as a function of frequency (Bode plot) at the input of the resonant tank as shown in Fig. 4. Compare to an LTspice simulation that models the same conditions.

This measurement will help you to determine at which frequencies the converter will be operating "below resonance" or "above resonance", and how much you can vary the switching frequency of the converter.

3 Board Construction

The boards for this lab were laid out using KiCad PCB Design Software. The software is open-source and free. The schematic and board files of the PCB boards of this lab are available in the coursework site. You will use KiCad to help you during the assembling of the PCB. Specifically, you will be able to select a component in a schematic and locate it on the board.

Please take some time to familiarize with the KiCad PCB Design Software by looking at the tutorials and videos available on the KiCad website.

https://www.kicad.org/help/learning-resources/

3.1 Primary-side board constructions

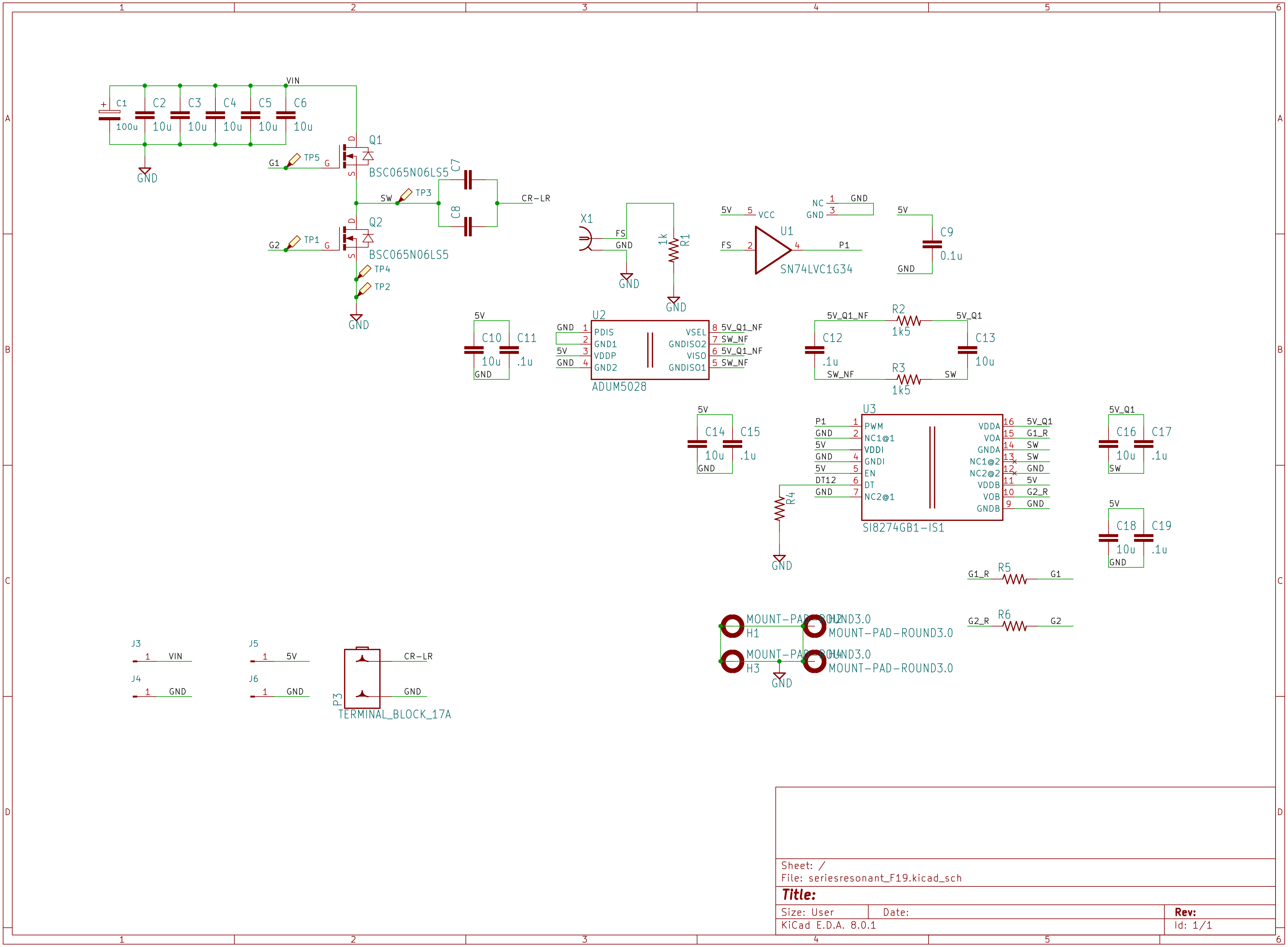
The half-bridge resonant inverter requires two complimentary gate signals to function, and the gate signal needed by the high-side switch of the half-bridge is not referenced to the input ground. Hence, we need to provide an isolated gating signal (not referenced to the input ground) that is connected between the gate and source terminals of the high-side MOSFET. SI8274 has internal isolation betwen the PWM input signal and the high-side gate driver output terminal (VOA-GNDA), but we still need to provide an isolated 5V supply between its supply terminal (VDDA and GNDA). For this lab we will use an i-Coupler device (ADUM5028) to achieve this. ADUM5028 can generate an isolated 5V and provide 60 mA output current.

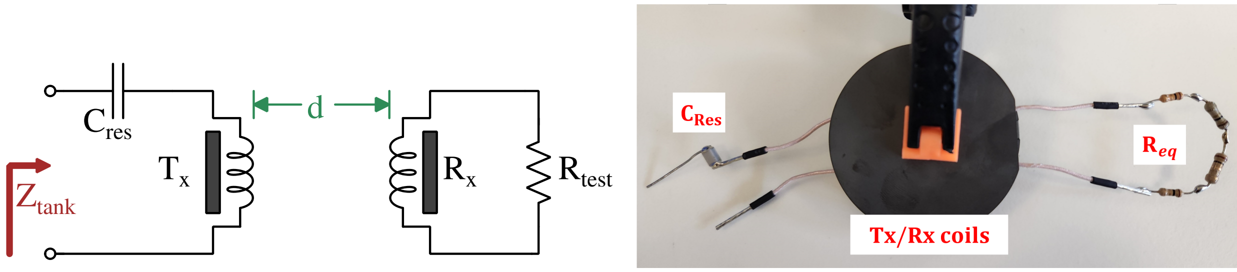
We will be using the Agilent 33521A waveform generator to provide our PWM input signal through the BNC connector X1. An issue with a half-bridge circuit is that we need to avoid having both MOSFETs simultaneously ON, creating a shoot-through condition and effectively shorting the input voltage. Therefore, we need a dead-time in a half-bridge circuit when both switches are off. The dead-time is usually a small fraction of the switching period. The SI8274 allows you to set the dead-time for a PWM signal using a single resistor. Refer to the data sheet of SI8274 for more details, and select the correct resistance to generate a dead-time around 40 ns.

There are parasitic inductance between the gate-driver output and the gate-to-source terminal of the MOSFETs. To avoid large ringing during transient which may damage the gate oxide or pseudo turn on the switch when the switch is supposed to be off, you will pick suitable gate resistors R_5 and R_6 at the output of the high-side and low-side gate drivers to damp the circuit.

Populate the inverter board with the components Table 1 by referring to the KiCad schematic (page 5), Fig. 5a, and KiCad board files found on Canvas.

Remember that if you use the hot plate to pre-heat the board before soldering, make sure to solder all through-hole components at the very end because the protruding terminals may prevent effective preheating. A stencil is provided to help you populate the Class D resonant inverter board.


VIN
C1 100u
C2 10u
C3 10u
C4 10u
C5 10u
C6 10u
GND
Q1 BSC065N06LS5
Q2 BSC065N06LS5
G1 TP5
G2 TP1
SW TP3
TP4
TP2
C7
C8
CR-LR
X1
FS
GND
R1 1k
U1 SN74LVC1G34
5V 5 VCC
FS 2
4 P1
NC 1 GND
GND 3
C9 0.1u
U2 ADUM5028
PDIS
GND1
VDDP
GND2
VSEL
GNDISO2
VISO
GNDISO1
5V_Q1_NF
SW_NF
C10 10u
C11 .1u
C12 .1u
C13 10u
R2 1k5
R3 1k5
5V_Q1
U3 SI8274GB1-IS1
PWM
NC1@1
VDDI
GNDI
EN
DT
NC2@1
VDDA
VOA
GNDA
NC1@2
NC2@2
VDDB
VOB
GNDB
P1
DT12
G1_R
G2_R
R4
C14 10u
C15 .1u
C16 10u
C17 .1u
C18 10u
C19 .1u
R5
R6
G1
G2
H1 MOUNT-PAD-ROUND3.0
H2 MOUNT-PAD-ROUND3.0
H3 MOUNT-PAD-ROUND3.0
H4 MOUNT-PAD-ROUND3.0
J3 1 VIN
J4 1 GND
J5 1 5V
J6 1 GND
P3 TERMINAL_BLOCK_17A
Sheet: /
File: seriesresonant_F19.kicad_sch
Title:
Size: User
Date:
Rev:
KiCad E.D.A. 8.0.1
Id: 1/1



(a) Schematic **(b)** Z_{tank} measurement setup

Figure 4: Impedance measurement for the resonant tank

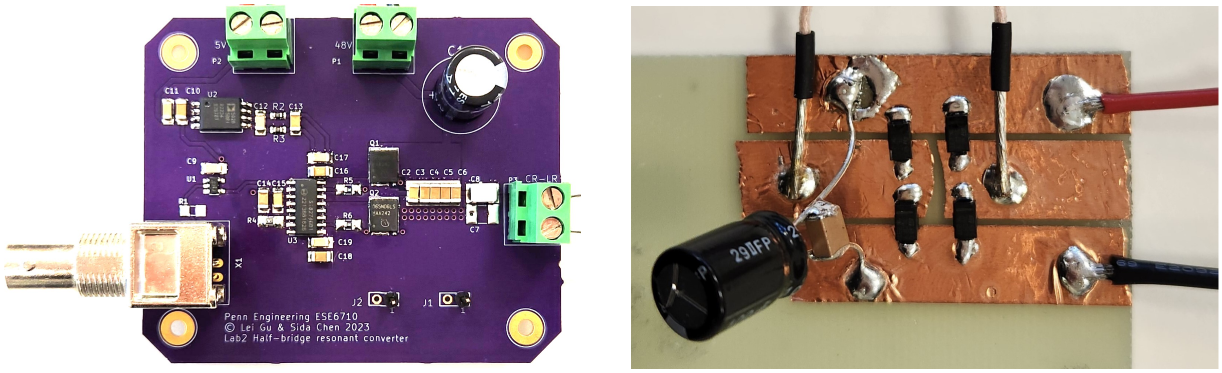
Table 1: List of components of the gate driver circuits

Part Number	Device	Value	Schematic Number
ESH107M100AH4AA	Electrolytic Capacitor, 100V	100 μF	C_1
CC1206JKX7R0BB104	Ceramic Capacitor	.1 μF	C_9, C_{11}, C_{12}, C_{15}, C_{17}, C_{19}
UMK316BBJ106KL-T	Ceramic Capacitor	10 μF	C_{2-6}, C_{10}, C_{14}, C_{16}, C_{18}
BSC065N06LS5	Si MOSFETs 60V		$Q_{1,2}$
TDK Cap Kits	**C0G** Ceramic Capacitor	0.1 μF in total	$C_7 + C_8$
SI8274GB1-IS1	Half-bridge gate driver		U_3
1206 Lab Resistor kits	Gate resistor	**Design choice**	$R_{5,6}$
1206 Lab Resistor kits	Dead-time resistor	**Design choice**	R_4
ADUM5028-5BRIZ	Isolated 5 V Power		U_2
BLM18HE152SN1D	Ferrite Beads		$R_{2,3}$
SN74LVC1G34DBVR	IC Non-inverting Buffer		U_1
1206 Lab Resistor kits	Pull-down resistor (Optional)	1kΩ	R_1
	BNC connector		X_1
	Test Points		TP_{1-4}
	Banana Jacks		J_{3-6}
	Terminal block		P_3
760308100110	Transmitting coil		Connected through P_3

After soldering the surface mount components, make sure there are no shorts on the board. Look for loose solder balls between the leads of the IC that can ”short” out terminals, carefully clean the board with an alcohol wipe. Remember to wear gloves when doing surface mount solder work.

3.1.1 Resonant Inverter Initial Test

Once the gate board is assembled, test the gate drive board by doing the following



(a) Half-bridge resonant inverter board.

(b) Example full-bridge rectifier board.

Figure 5: Resonant inverter and rectifier boards. The actual inverter you will make is slightly different from Fig. 5a.

1. **Make sure the polarized capacitors on your board are not connected backward!**
2. Using the continuity settings of the DMM make sure you don't have obvious shorts on your board.
3. Connect the dc input terminal J_3 to +24 V and J_4 to GND, and dc input terminal J_5 to +5 V and J_6 to GND. **Pay attention to the polarity and do NOT turn on the +24 V supply**.
4. Set the function generator to provide a square signal at $f_s = 200$ KHz with voltages between 0 V and 5 V. *Make sure the output impedance setting of the function generator is High Impedance. If this is not the case you may damage the digital gate IC.*
5. Keep the dc input shorted by keeping +24 V off (the power supply shorts the output internally when it is off) and only turn on +5V supply. Use the probes of the oscilloscope to check the gate-to-source voltages of Q_1 and Q_2. Make sure you should see two out-of-phase 5V gate voltages. **You can only directly measure the gate-to-source voltages of all the MOSFETs when the dc input is shorted so the switch node is at 0 V.**
6. Measure the gate voltages of the half-bridge switch pair $Q_1 - Q_2$ at the same time. Make sure you have enough dead-time ($>$ 25ns) between the two signals.
7. Turn on the +24 V supply, use the probe of the oscilloscope to measure the switched node corresponding to SW in the KiCad schematic. You should see a 200 kHz square waves toggling between 0 and 24V.
8. Verify your circuit works as you vary the frequency f_s anywhere between 100 kHz and 500 kHz.

3.2 Secondary-Side Rectification Board

The secondary-side of the rectification board can be implemented using diodes, capacitors, copper tapes on bare FR4 boards. The electronic dc load will take the role of the output resistor R_{out}.

Fig. 5b shows an example board for the full-bridge rectifier.

Table 2: List of components of the rectifier circuit.

Part Number	Device	Value
STPS360AF	Diode Schottky 60V 3A	
All the ceramic caps we have	Output bypass capacitors	**Design choice**
760308100110	Receiving coil	

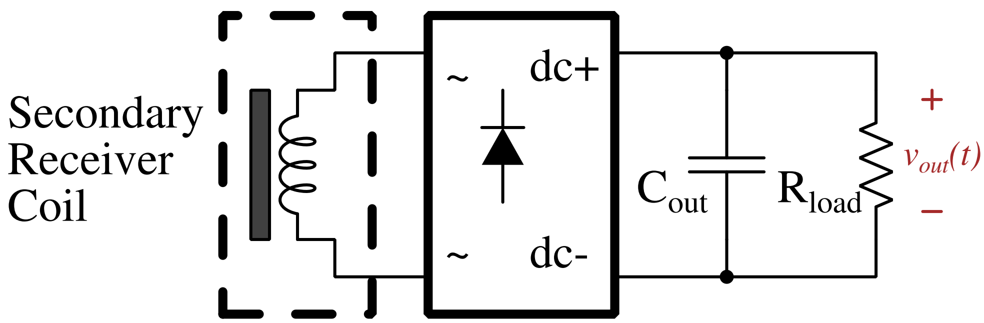


Figure 6: Schematic of the Secondary-side Rectification Board

3.3 DC-AC-DC Converter Assembly and Initial Check

Assemble the inverter, coils, and rectifiers together as shown in Fig. 7. For holding the wireless coils, use the spacer we 3D printed, shown in Fig. 8 and the plastic clamps. Once the whole dc-dc converter is assembled, check your circuits by doing the following before connecting to the power supply.

1. **Make sure the polarized capacitors on your board are not connected backward!**
2. Use the continuity settings of the DMM to make sure you don't have obvious shorts on your board.
3. Check which measurement test points (TP_{1-5}) on the board you can use.
4. Put the transceiver and receiver coils on top of each other. Makes sure that as you run the tests with the coils remain aligned.

4 Experimental procedures

4.1 Converter at Constant Load at varying frequencies

Make the following measurements and in your report, comment and compare to your simulation.

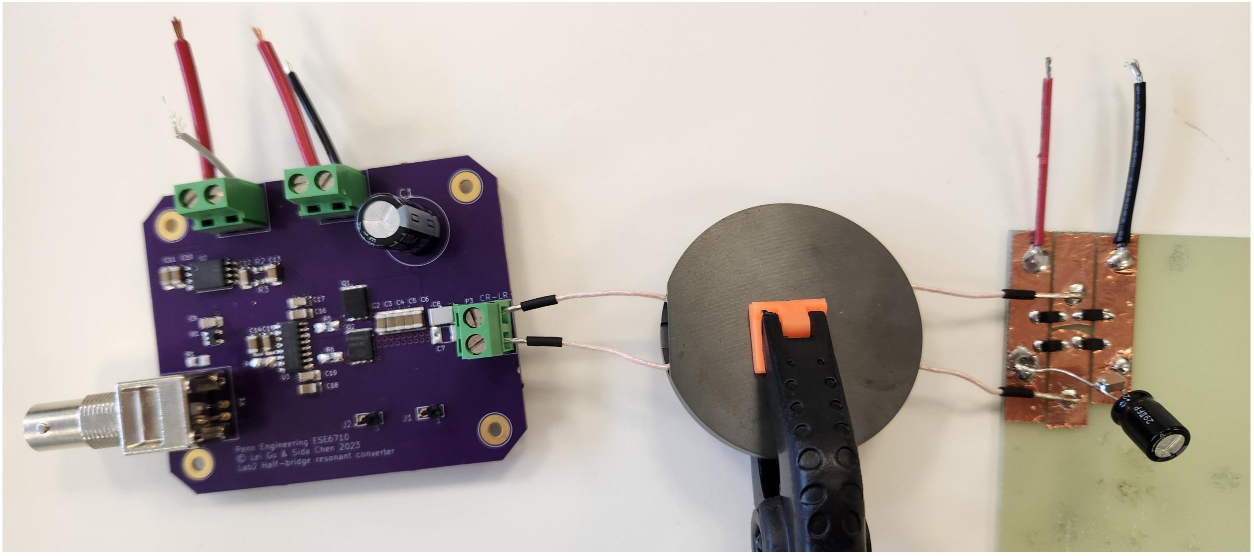


Figure 7: Assembled primary-side, WPT coils, and secondary-side power board.

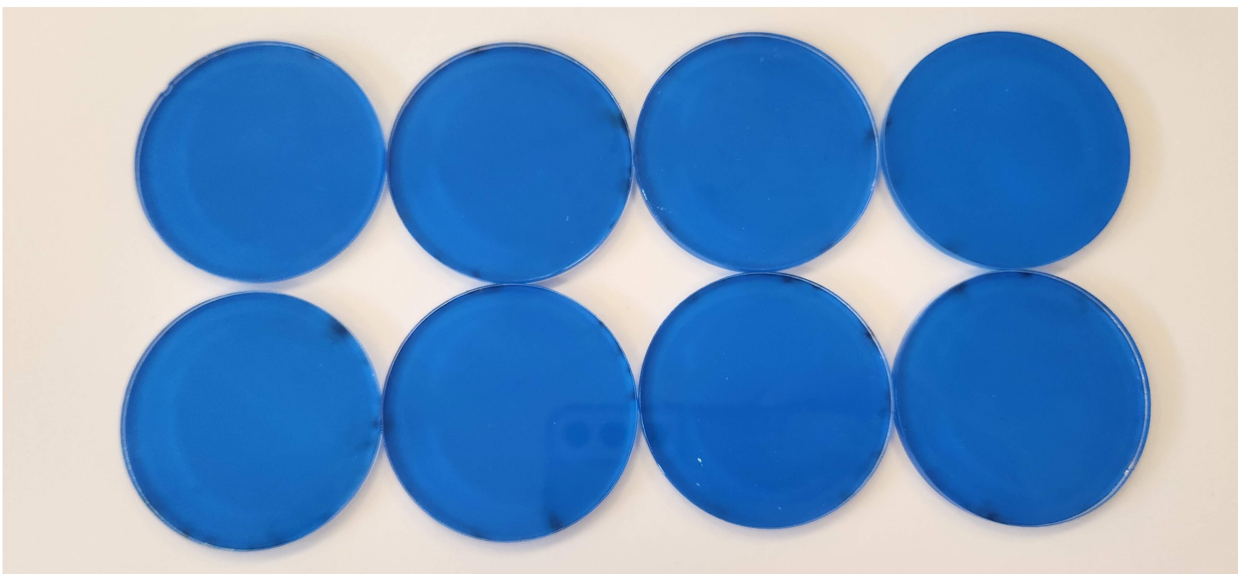


Figure 8: Acrylic spacer for separating wireless coils.

1. Connect J_5 to $+5$ V and J_6 to GND, and J_3 to 24 V and J_4 to GND. 24V will be the input voltage V_i throughout all the measurements.

2. Set the electronic load to be in constant resistance mode, and set the resistance value to $5\ \Omega$.

3. Do the following measurements for at least 7 values of frequencies where three frequencies are above the resonant frequency of the tank (Assuming L_μ is very large), one at the resonant frequency, three frequencies below f_0. *Note: For the peak to peak ripple measurements do not use the automated measurement function in the scope, but use the manual cursors instead. The reason for this should be obvious once you look at your waveforms.* Duty Cycle should always be 50%.

   (a) Plot I_p (Primary Current) peak-to-peak vs. Frequency f_s.
   (b) Plot V_o (Output Voltage) vs. Frequency f_s.
   (c) Plot $\frac{V_o}{V_i}$ vs. Frequency f_s.
   (d) Plot P_{out} vs. Frequency f_s.
   (e) Plot η vs. Frequency f_s.

4. In your report show a screen capture of the waveforms of the primary current $I_p(t)$, the output voltage $v_o(t)$ and the switched node (SW) voltage of the bottom MOSFET at a frequency below, at, and above the resonant frequency of the tank.

4.2 Converter operating at Constant Frequency and varying loads

Make the following measurements and in your report, comment and compare to your simulation.

1. Set the electronic load to be in constant resistance mode, and set frequency slightly above your resonant frequency.

2. Do the following measurements for at least 6 values of output resistance values. How does it compare to your simulation?

   (a) Plot V_o (Output Voltage) vs. I_o (Output Current)
   (b) Plot η vs. I_o.

5 Acknowledgment

Thanks to Sida Chen for helping update the lab and the PCB.

Penn Engineering