Fab Design Rule Set: OSHPark

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	PSR-4000BN	1.00mil	4.5	
1	Top Layer	Copper	1.38mil		
	Dielectric 1	Kingboard KB6167F	59.00mil	4.5	
2	Bottom Layer	Copper	1.38mil		
	Bottom Solder	PSR-4000BN	1.00mil	4.5	
	Bottom Overlay				

Symbol	Count	Hole Size	Hole Tolerance	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
	5	13.00mil (0.330mm)		PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
	5	43.00mil (1.092mm)		PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
	6	19.69mil (0.500mm)		PTH	Slot	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	11	12.00mil (0.305mm)		PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v61h30
	13	12.00mil (0.305mm)	+/-2.00mil	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
	20	40.00mil (1.016mm)		PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	60 Total								

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Title: J-Link Cortex with VCOM Adapter.PcbDoc

Desc: Adapter for Segger J-Link to Cortex
Also adds VCOM UART support, 3.3V LDO, and breakouts for power and ground
*

Size: Letter | Auth: Andrew Katz | Proj: J-Link-Cortex-VCOM

Date: 5/31/2020 Time: 9:23:20 PM Sheet 1 of 1

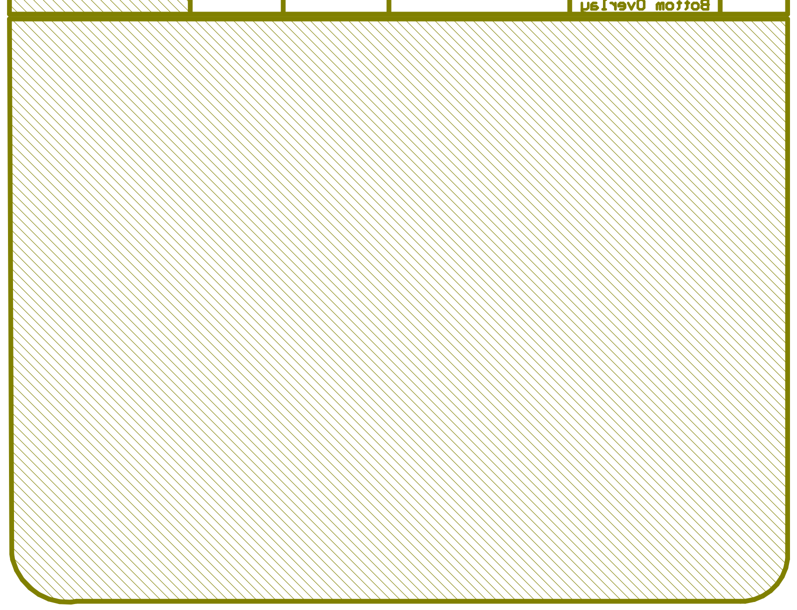
Repo: https://github.com/aakatz3/J-Link-Cortex-VCOM

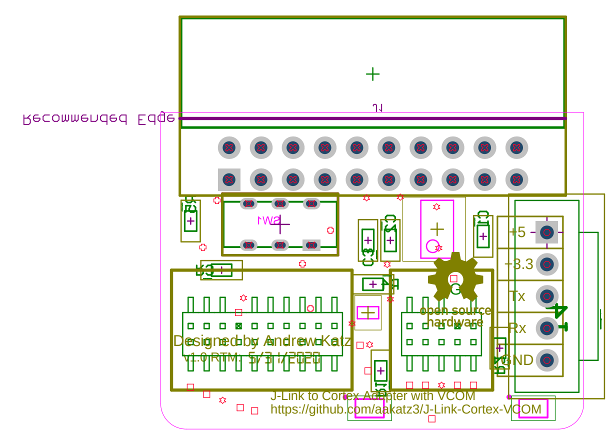
File: C:\git\Segger J-Link Cortex Adapter Board\J-Link Cortex with VCOM Adapter.PcbDoc

open source hardware

Fab Design Rule Set: OSHPark

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	PSR-4000BN	1.00mil	4.5	
1	Top Layer	Copper	1.38mil		
	Dielectric 1	Kingboard KB6167F	59.00mil	4.5	
2	Bottom Layer	Copper	1.38mil		
	Bottom Solder	PSR-4000BN	1.00mil	4.5	
	Bottom Overlay				





Symbol	Count	Hole Size	Hole Tolerance	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
⊕	5	13.00mil (0.330mm)		PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
○	5	43.00mil (1.092mm)		PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
⌘	6	19.69mil (0.500mm)		PTH	Slot	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
✲	11	12.00mil (0.305mm)		PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v61h30
□	13	12.00mil (0.305mm)	+/-2.00mil	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)
⊠	20	40.00mil (1.016mm)		PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	60 Total								

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

open source hardware

Title:J-Link Cortex with VCOM Adapter.PcbDoc

Desc: Adapter for Segger J-Link to Cortex
Also adds VCOM UART support, 3.3V LDO, and breakouts for power and ground
*

Size:Letter | Auth: Andrew Katz | Proj:J-Link-Cortex-VCOM

Date: 5/31/2020 | Time: 9:23:20 PM | Sheet 1 of 1

Repo: https://github.com/aakatz3/J-Link-Cortex-VCOM

File: C:/git/Segger J-Link Cortex Adapter Board/J-Link Cortex with VCOM Adapter.PcbDoc