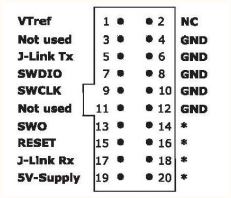
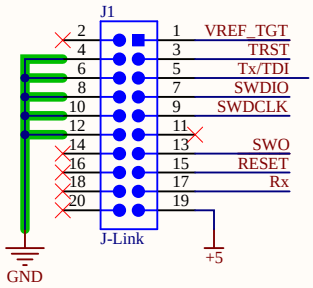
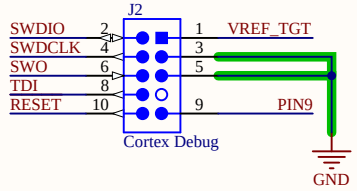
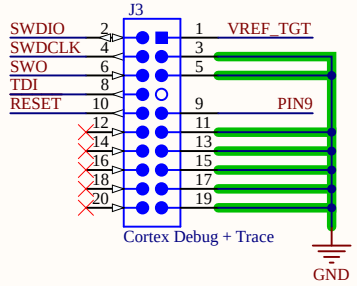


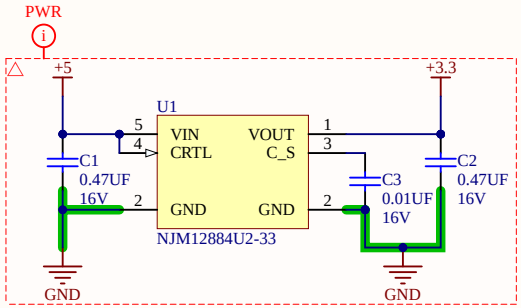
PIN	SIGNAL	TYPE	Description
1	VTref	Input	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.
2	Not connected	NC	This pin is not connected in J-Link.
3	Not used	NC	This pin is not used by J-Link. If the device may also be accessed via JTAG, this pin may be connected to nTRST, otherwise leave open.
5	J-Link Tx	Output	This pin is used as VCOM Tx (out on J-Link side) in case VCOM functionality of J-Link is enabled. For further information about VCOM, please refer to *Virtual COM Port (VCOM)* .
7	SWDIO	I/O	Single bi-directional data pin. A pull-up resistor is required. ARM recommends 100 kOhms.
9	SWCLK	Output	Clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK of the target CPU.
11	Not used	NC	This pin is not used by J-Link. If the device may also be accessed via JTAG, this pin may be connected to RTCK, otherwise leave open.
13	SWO	Input	Serial Wire Output trace port. (Optional, not required for SWD communication.)
15	nRESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called "nRST", "nRESET" or "RESET". This signal is an active low signal.
17	J-Link Rx	Input	This pin is used as VCOM Rx (in on J-Link side) in case VCOM functionality of J-Link is enabled. For further information, please refer to *Virtual COM Port (VCOM)* .
19	5V-Supply	Output	This pin can be used to supply power to the target hardware. Older J-Links may not be able to supply power on this pin. For more information about how to enable/disable the power supply, please refer to *Virtual COM Port (VCOM)* .

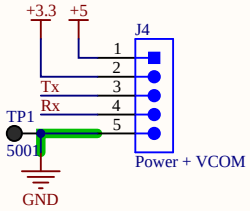
UART VCOM is defined in reference to J-Link

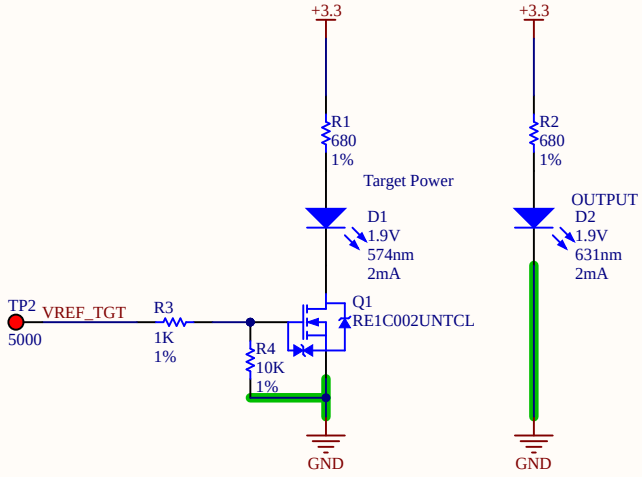




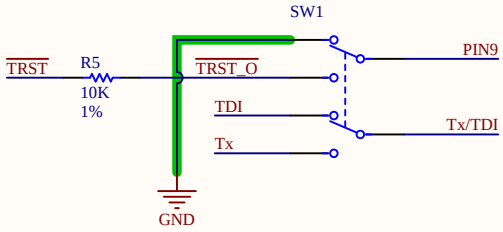








Some devices offer JTAG \TRST on Pin 9, others use it as GND Detect, to detect the presence of a debugger. Therfore, A switch is used to select function. Since this is only used in JTAG mode, and TDI is also only used in JTAG mode, and conflicts with VCOM, a DPDT switch is used to select the configuration. For safety, a 10K resistor is in series with the \TRST option.



Title: *J-Link Cortex with VCOM Adapter.SchDoc*		
Desc:		
Size: Letter	Auth: Andrew Katz	Proj: J-Link Cortex + VCOM
Date: 6/2/2020	Time: 10:59:47 PM	Sheet * of *
Repo: https://github.com/gakatz3/J-Link-Cortex-VCOM		
File: C:\git\Segger J-Link Cortex Adapter Board\J-Link Cortex with VCOM Adapter.SchDoc		