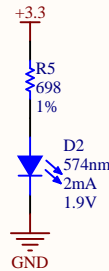
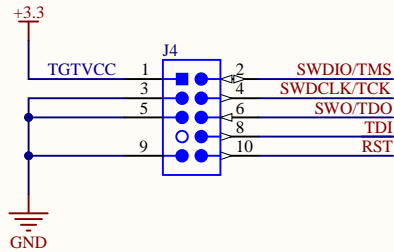
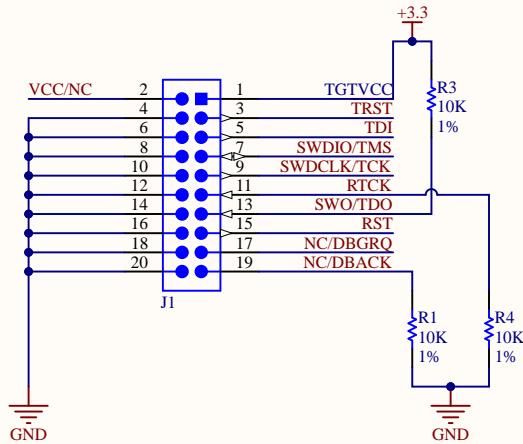
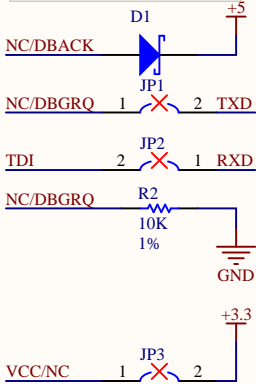


⚠ The Segger J-Link devices with their 20 Pin connector supply 5V on pin 19. D1 allows the J-Link to power the microcontroller, but not short to ground with other programmers. If the programmer expects the DBGACK signal, it is tied low to indicate no support for this, via a 10kΩ resistor.

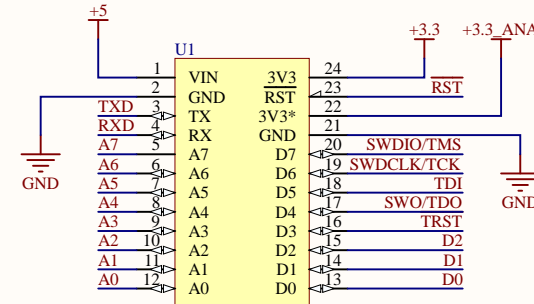
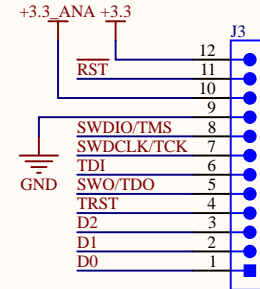
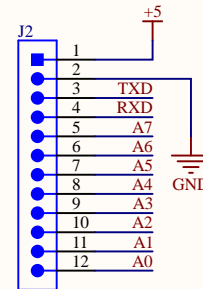
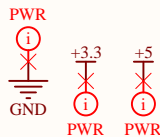
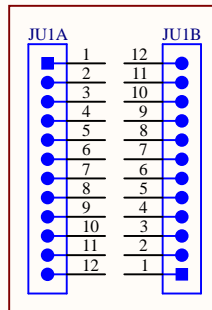
⚠ If you are using a Segger J-Link in SWD mode instead of JTAG, and wish to use the VCOM functionality, close jumpers JP1 and JP2, install D1 (default) and remove R2 (if installed)

⚠ If your JTAG programmer or debugger expects DBGQ and DBGACK to be pulled low, install R2, and ensure JP and JP2 are open (default). D1 can be safely ignored.

⚠ If your programmer supports target powering on Pin 2 of the JTAG port, close JP3



Mechanical (U1 Socket)



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Title: **programmer-shield.SchDoc**

Desc: :

Size: Letter Auth: Andrew Katz Proj: Core J-Link Shld

Date: 5/20/2020 Time: 10:54:05 PM Sheet 1 of 1

Repo: <https://github.com/aakatz3/spark-programmer-jlink>

File: C:\git\spark-programmer-jlink\programmer-shield.SchDoc