Assignment 2 :: Report

Organization of Digital Computers Lab
EECS 112L
University of California, Irvine
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Team CTRL-C CTRL-V
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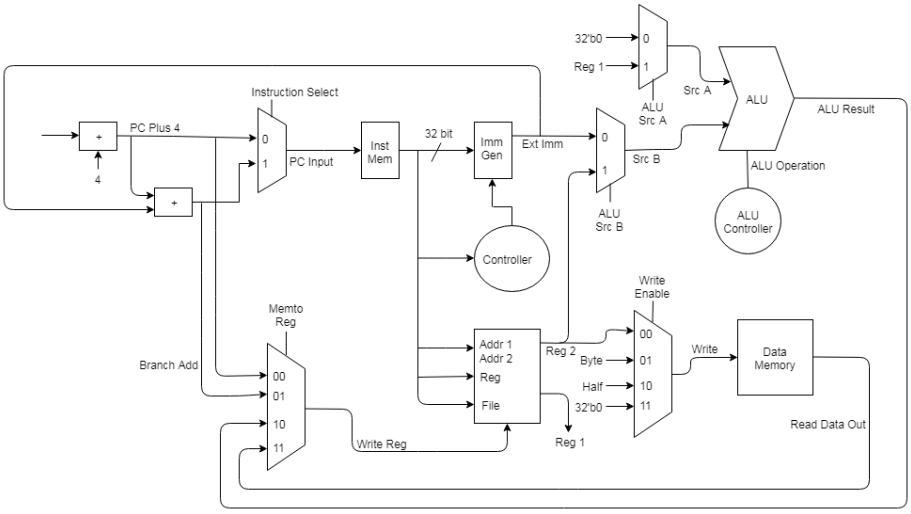
1 Block Diagram

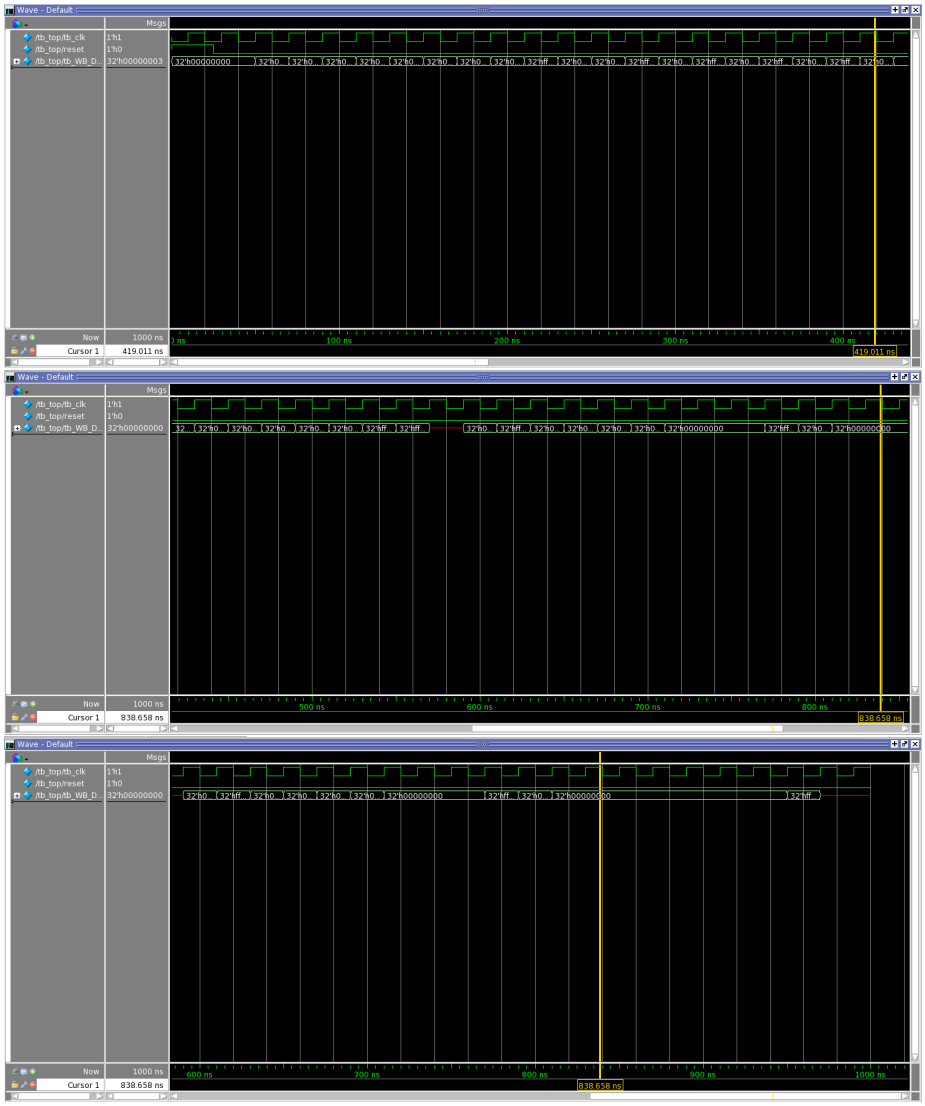


In the original block diagram, the RISC V processor implemented did not support any B type (branching), J type (jumping), or U type (unsigned) instructions. Our newly implemented design now features these instructions, and the following changes were made to support them:

- For the Immediate Generator, new outputs were included to support reading immediate values from B type, U type, and S type instructions.
- For the ALU, the actual instructions were implemented (e.g. AND = input_1 & input_2).
- For the Data Memory, the ability to load and store half words and bytes was implemented.
- For the Controller, new signal outputs were added to support the different types of U type instructions, the different types of J type instructions, and the B type instructions.
- For the Datapath, new multiplexers were added to support the new signals from the Controller and actually perform the jumps in the program counter given by the B type and J type instructions.

2 Module Simulation

2.1 Screenshots of Waveform



2.2 Complications

We faced multiple challenges when adding the new signals to the Datapath from the Controller. One such was an iteration error, because the program counter was not able to jump properly in ac-

cordance to what the instruction was asking. We faced some issues that were not solvable, such as the implementation of a JALR instruction, as for some reason, the 4-1 multiplexer was not able to assign data to the proper output.

3 Module Synthesis

3.1 Power

```
****************************************
Report : power
        -hier
        -analysis_effort medium
        -verbose
Design : riscv
Version: J-2014.09-SP4
Date   : Fri Mar  1 15:29:14 2019
****************************************


Library(s) Used:

    saed32lvt_tt1p05vn40c (File: /users/ugrad2/2012/spring/pooriam/libraries/saed32lvt_tt1p0


Operating Conditions: tt1p05vn40c   Library: saed32lvt_tt1p05vn40c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
riscv                 ForQA              saed32lvt_tt1p05vn40c
Controller            ForQA              saed32lvt_tt1p05vn40c
ALUController         ForQA              saed32lvt_tt1p05vn40c


Global Operating Voltage = 1.05
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                   Switch   Int      Leak     Total
Hierarchy                          Power    Power    Power    Power    %
--------------------------------------------------------------------------------
riscv                                 5.466    4.768 3.21e+07   42.305 100.0
  ac (ALUController)                  1.875    1.798 1.63e+07   19.940  47.1
  c (Controller)                      3.241    2.970 1.58e+07   22.015  52.0
```

3.2 Area

```
****************************************
Report : area
Design : riscv
Version: J-2014.09-SP4
Date   : Fri Mar  1 15:29:14 2019
****************************************

Library(s) Used:

    saed32lvt_tt1p05vn40c (File: /users/ugrad2/2012/spring/pooriam/libraries/saed32lvt_tt1p05vn40c.db)

Number of ports:                           34
Number of nets:                            68
Number of cells:                            3
Number of combinational cells:              0
Number of sequential cells:                 1
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       3

Combinational area:                100.641025
Buf/Inv area:                       20.331520
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:             16.040373

Total cell area:                   100.641025
Total area:                        116.681397

Information: This design contains black box (unknown) components. (RPT-8)

The above information was reported from the logical library. The following are from the physical library:

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------  --------------------------
Hierarchical cell                 Absolute   Percent  Combi-    Noncombi-  Black-
                                  Total      Total    national  national   boxes   Design
--------------------------------  ---------  -------  --------  ---------  ------  -------------
riscv                              100.6410    100.0    0.0000     0.0000  0.0000  riscv
ac                                  44.2211     43.9   44.2211     0.0000  0.0000  ALUController
c                                   56.4200     56.1   56.4200     0.0000  0.0000  Controller
--------------------------------  ---------  -------  --------  ---------  ------  -------------
Total                                                  100.6410     0.0000  0.0000
```

3.3 Clock Frequency

```
****************************************
Report : qor
Design : riscv
Version: J-2014.09-SP4
Date   : Fri Mar  1 15:29:14 2019
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:               1.00
  Critical Path Length:          0.00
  Critical Path Slack:         uninit
  Critical Path Clk Period:       n/a
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:          2
  Hierarchical Port Count:         36
  Leaf Cell Count:                 57
  Buf/Inv Cell Count:              16
  Buf Cell Count:                   0
  Inv Cell Count:                  16
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:        57
  Sequential Cell Count:            0
  Macro Count:                      0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      100.641025
  Noncombinational Area:     0.000000
  Buf/Inv Area:             20.331520
  Total Buffer Area:             0.00
  Total Inverter Area:          20.33
  Macro/Black Box Area:      0.000000
  Net Area:                 16.040373
  -----------------------------------
```