

**Batch:**                      **Roll No.:**

**Experiment / assignment / tutorial No. \_\_\_\_\_**

**TITLE:** Study of PCI and SCSI.

**AIM:** To Study and learn PCI and SCSI

**Expected OUTCOME of Experiment : (Mention CO/CO's attained here )**

**Books/ Journals/ Websites referred:**

1. <https://www.techopedia.com/definition/8815/peripheral-component-interconnect-bus-pci-bus>
2. <https://www.techopedia.com/definition/331/small-computer-system-interface-scsi>
3. [http://www.csun.edu/~edaasic/roosta/BUS\\_Structures.pdf](http://www.csun.edu/~edaasic/roosta/BUS_Structures.pdf)
4. W.Stallings William “Computer Organization and Architecture: Designing for Performance”, Pearson Prentice Hall Publication, 7th Edition. C.

**Pre Lab/ Prior Concepts:**

Microcomputer buses which communicate with a peripheral devices or a memory location through communication lines called buses.

The major parts of microcomputers are central processing unit (CPU), memory, and input and output unit. To connect these parts together through three sets of parallel lines, called buses. These three buses are Address bus, data bus, and Control bus.

**Address Bus:**

The address bus consists of 16, 20, 24, or more parallel signal lines, through which the CPU sends out the address of the memory location. This memory location is used for to written to or read from. The number of memory location is depends on 2 to the power N address lines. Example, a CPU with 16 address lines can address  $2^{16}$  or 65,536 memory locations. When the CPU reads data from or writes data to a port. The port address is also sent out on the address bus. This is unidirectional. This means that the CPU can send data to a memory location or I/O ports.

**Data Bus:**

The data bus consists of 8, 16, 32 or more parallel signal lines. The data bus lines are bidirectional. This means that the CPU can read data from memory or from a I/O port as well as send data to a memory location or to a I/O port. In a system, many output devices are connected to the data bus, but only one device at a time will be enabled to the output.

**Control Bus:**

The control bus consists of 4-10 parallel signal lines. The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or port devices. Typically control bus signals are memory read, memory write, I/O read and I/O write. To read a data from a memory location, the CPU sends out the address of the desired data on the address bus and then sends out a memory read signal on the control bus. The memory read signal enables the addressed memory device to output the data onto the data bus where it is read by the CPU.

### **PCI Bus**

### **SCSI bus:**

**Post Lab Descriptive Questions**

**Q1 . Differentiate between PCI and SCSI Bus**

**Q2. List two applications each of PCI and SCSI Bus**

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