Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2015

Homework 9 **Due on April 16, 2015 at 5:00 PM**

Suggested Readings:

a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 9.1: (Designing a cascode transconductance amplifier)

A transconductance (voltage to current) amplifier requires a large input resistance, a large output resistance and a large transcoductance gain. Suppose we require an output resistance greater than 10MΩ, a transconductance gain of at least 1 mS, and an infinite input resistance. The 2 μm FET technology available to us has the following specifications. We also have a single stable current source available on a chip.

$L = 2\ \mu\text{m}$

$\mu_n C_{ox} = 50\ \mu A/V^2$

$\mu_p C_{ox} = 25\ \mu A/V^2$

$\lambda_n = 0.05\ 1/V$

$\lambda_p = 0.02\ 1/V$

$V_{DD} = 5.0\ V$

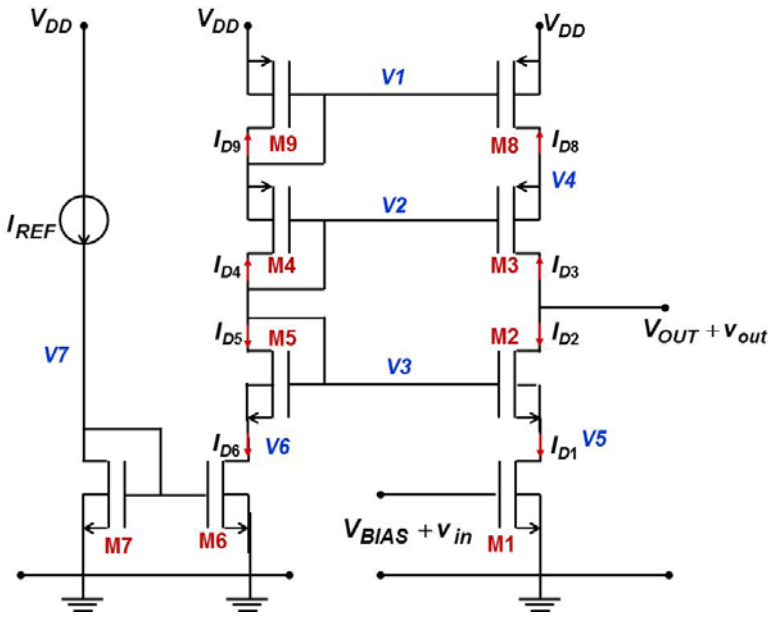
$V_{TN} = 1.0\ V$

$V_{TP} = -1.0\ V$

$I_{REF} = 100\ \mu A$

How do we choose a good design? The simplest idea would be to try a single or multistage cascade of CS stages. It will not be difficult to get a transconductance gain of 1 mS using CS stages. However, getting a large output resistance of 10 MΩ will not be easy. For example, suppose the final stage is a CS stage with a 100 μA current going through a NFET. The output resistance of the NFET, which will set the upper limit for the output resistance of the amplifier, will be $\sim (\lambda_n I_D)^{-1}$ which equals 200 kΩ. Therefore, using single or cascaded CS stages one can never hope to meet the design specs. A different design is required. A cascode design can work. The design of a cascode transconductance amplifier is shown below.

Suppose we choose the current I_{D1} to equal 100 μA. Rest of the design process follows step by step after making this choice.



a) Assuming that the resistance looking into the PFET biasing source on top of the cascode is very large, what value should one choose for the width W_1 of M1 such that the transconductance of the cascode amplifier is around 1 mS?

b) What are the output resistances of M1 and M2 at the chosen bias point? What are the output resistances of M3 and M8 at the chosen bias point?

c) Assuming that the resistance looking into the PFET biasing source on top of the cascode is very large, what value should one have for the transconductance g_{m2} of M2 such that the output resistance of the cascode amplifier is around 20 MΩ?

d) Assuming for a moment that:

$$I_{D2} \approx \frac{k_n}{2}(V_{GS2} - V_{TN})^2$$

what value should one choose for the width W_2 of M2 such that the transconductance g_{m2} of M2 has the value found in part (c)?

e) Suppose we want the resistance looking into the PFET biasing source on top of the cascode to be 100 MΩ (i.e. very large). What value should one have for the transconductance g_{m3} of M3?

f) Assuming for a moment that:

$$I_{D3} \approx -\frac{k_p}{2}(V_{GS3} - V_{TP})^2$$

what value should one choose for the width W_3 of M3 such that the transconductance g_{m3} of M3 has the value found in part (e)?

Now we choose $W_3 = W_8$

g) To bias the circuit properly, what should be the widths of M5, M4, and M9?

Next, we choose $W_6 = W_1$.

h) Now what should be W_7 ?

i) Find the voltages V1, V2, and V3.

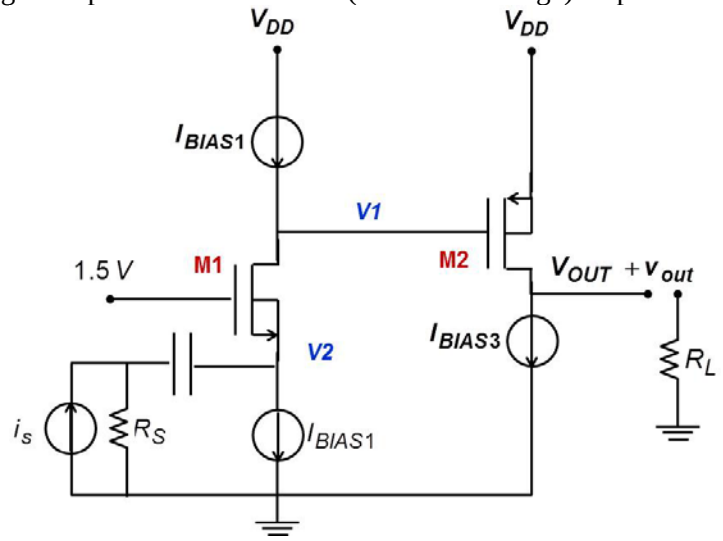
j) Find the voltages V4, V5, V6 and V7.

k) What should be V_{BIAS} ?

l) Suppose the on chip current source I_{REF} is no longer available. But you are allowed to choose a resistor in its place. What value resistor would you use to keep the rest of the circuit functioning as before?

Problem 9.2: (Designing a cascade transresistance amplifier)

Consider the following attempt at a transresistance (current to voltage) amplifier.



A current to voltage amplifier requires a small input resistance and a small output resistance. Assume the following parameter values:

$L = 4\ \mu m$

$\mu_n C_{ox} = 50\ \mu A/V^2$

$\mu_p C_{ox} = 25\ \mu A/V^2$

$\lambda_n = 0.02\ 1/V$

$\lambda_p = 0.05\ 1/V$

$V_{DD} = 5.0\ V$

$V_{TN} = 0.7\ V$

$V_{TP} = -1.0\ V$

$I_{BIAS1} = 200\ \mu A$

$I_{BIAS3} = 500\ \mu A$

$r_{oc1} = r_{oc3} = \infty$

$R_S = 10\ k\Omega$

Assume that $V_{OUT} = 2.5\ V$

a) Identify the two stages in the cascade (e.g. CE, CC, CS, etc).

b) Suppose that the voltage *V2* is needed to be at least 0.5 V so that the FET making up the current bias I_{BIAS1} in the source of M1 does not go into the linear region. Calculate the width W_1 of the FET M1 needed to ensure that *V2* is 0.5 V.

c) Suppose we need *V1* to be 3.0 V. Find the width W_2 of the FET M2 needed to achieve this.

d) Find an expression for and calculate the value of R_{in} for this cascade amplifier.

e) Find an expression for and calculate the value of R_{out} for this cascade amplifier.

f) Find an expression for and calculate the value of the transresistance $R_m = v_{out}/i_s$ of this amplifier assuming that the output is open (i.e $R_L = \infty$) and the resistance R_S is also infinite.

g) The value of R_{out} for this cascade amplifier found in part (e) is fairly large. Transresistance amplifiers need to have a small output resistance. Suppose you can use one more FET (PFET or NFET) and one more infinite output resistance bias current source to modify the design shown above. Suppose you need, as a design spec, R_{out} less than 5 kΩ and V_{OUT} greater than 1.5 V. Choose the FET type, together with its width in microns, and the value of the bias current source, and redesign the amplifier such that it keeps the previous values of the R_{in} and the open circuit $R_m = v_{out}/i_s$ but meets the specs on R_{out} and V_{OUT}. Show that your design works.

Problem 9.3: (A BICMOS Amplifier)

Consider a BICMOS (BIpolar and CMOS mix technology) amplifier (on the next page). The parameter values are as follows.

$L_n = L_p = 4\ \mu\text{m}$
$\mu_n C_{ox} = 50\ \mu A/V^2$
$\mu_p C_{ox} = 25\ \mu A/V^2$
$\lambda_n = 0.02\ 1/V$
$\lambda_p = 0.05\ 1/V$

$V_{DD} = 5.0\ V$
$V_{TN} = 0.7\ V$
$V_{TP} = -0.7\ V$
$W_n = 20\ \mu\text{m}$
$W_n = 40\ \mu\text{m}$

$V_A = 50V$
$V_{BE-ON} = 0.7V$
$V_{CE-SAT} = 0.2V$
$\beta_{FO} = 100$
$\beta_F = \beta_{FO} e^{|V_{CE}|/V_A}$

a) What is the current through each leg of the amplifier?

b) What is the total power dissipation?

c) What ought to be the value of V_{BIAS} such that M1 sinks the current provided by M7 and M6?

d) Identify each stage of the amplifier (e.g. CE, CS, CD, CG, etc) and specify what type of amplifier is this (e.g. current amplifier, transimpedance amplifier, etc).

e) Find the voltage at each node of the amplifier (V1, V2, V3, V4, V5, VX, V_{OUT}).

f) What is the maximum value V_{OUT} can take such that no FET/BJT in the amplifier goes out of the saturation/forward active region of operation?

g) What is the minimum value V_{OUT} can take such that no FET/BJT in the amplifier goes out of the saturation/forward active region of operation?

h) Estimate the open circuit voltage gain of the amplifier.