ECE 3150: Microelectronics

Spring 2015

Homework 11 **Due on May 06, 2015 at 5:00 PM**
(But one-day extension to all - without asking - is available due to the ECE day)

Suggested Readings:

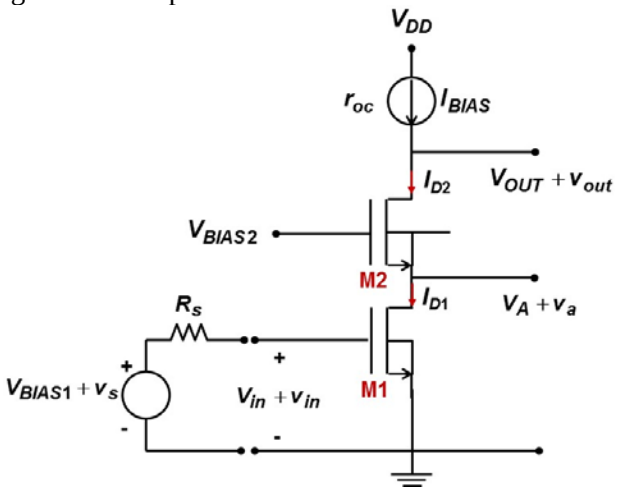
a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 11.1: (Frequency performance of a cascode amplifier vs a common source amplifier)

Consider the following cascode amplifier:



$W = 10\ \mu\text{m}$
$L = 0.5\ \mu\text{m}$
$\mu_n C_{ox} = 200\ \mu A/V^2$
$\lambda_n = 0.02\ 1/V$
$V_{DD} = 3.0\ V$
$V_{TN} = 0.5\ V$

$I_{BIAS} = 4\ mA$
$C_{gd} = 10\ fF$
$C_{gs} = \frac{2}{3} C_{ox} WL = 30\ fF$
$r_{oc} \approx r_{o2} = r_{o1}$

Assume that V_{BIAS1} and V_{BIAS2} have been adjusted such that the drain current of the both the FETs is 4 mA. Suppose $R_S = 2\text{k}\Omega$.

Synopsis: A good voltage amplifiers needs to have a large input resistance, a small output resistance, a large gain, and a large gain bandwidth (i.e. the bandwidth over which the gain is flat and at the DC value is large). A common source amplifier has a large gain and a large input resistance, but suffers from the Miller effect which compromises the gain bandwidth. A common gate amplifier has a large gain, and a large gain bandwidth, but has a small input resistance. A casacade of the two, i.e. a cascode, has a large input resistance, a large gain, and a large gain bandwidth. These characteristics make the cascode an attractive stage for circuit designers. In this problem you will explore this in detail.

a) Draw the small signal model of the cascode shown above.

b) At the bias point, find the (numerical) values of g_m and g_o for both the FETs (these should be identical for the two FETs since they are both biased with the same DC current). How big is g_m compared to g_o?

c) Using KCL at the drain end of M2 in the small signal model, show that:

$$\frac{v_{out}}{v_a} \approx \frac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}$$

The above expression is the open circuit voltage gain of the second common gate stage. At low frequencies (~DC), the above expression gives the familiar near-DC open circuit voltage gain of a common gate amplifier: $g_{m2}(r_{oc} \,||\, r_{o2})$.

d) Plot $10\log_{10}\left|\frac{v_{out}}{v_a}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency in Hz (not rad/s). The matlab function "logspace" will be useful when making the frequency array for plotting.

e) Using KCL at the drain end of M1 in the small signal model, show that:

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + g_{o2} + g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2}\left[\frac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}\right]}$$

If the input impedance looking into M2 from the source end were assumed to be infinite, the above expression would reduce to,

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{o1} + j\omega(C_{gd1})}$$

which is the just the open circuit voltage gain of a common source amplifier with a low frequency value equal to $-g_{m1}r_{o1}$. However, the input impedance of the common gate amplifier is not infinite and is in fact very small. After making suitable approximations, the above expression simplifies to,

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1} + j\omega C_{gd1}}{g_{m2} + j\omega(C_{gd1} + C_{gs2}) - g_{o2}\left[\frac{g_{m2}(r_{oc} \,||\, r_{o2})}{1 + j\omega C_{gd2}(r_{oc} \,||\, r_{o2})}\right]}$$

The near-DC value of the above expression is,

$$\frac{v_a}{v_{in}} \approx -\frac{g_{m1}}{g_{m2}}\left(1+\frac{r_{oc}}{r_{o2}}\right) = A_{v1}\frac{R_{in2}}{R_{out1}+R_{in2}}$$

$$\begin{cases} A_{v1} = -g_{m1}r_{o1} \quad R_{out1} = r_{o1} \quad R_{in2} \approx \dfrac{1}{g_{m2}}\left(1+\dfrac{r_{oc}}{r_{o2}}\right) \end{cases}$$

v_a/v_{in} at near-DC is of the order of unity. What the above analysis shows is that the first stage, the common source stage, does not really provide much gain at all. All the gain comes from the second stage, the common gate stage. The first stage does not provide much gain because it is loaded with the small input resistance of the second stage. And so the loaded voltage gain of the first stage (not the open circuit voltage gain) is pretty small, near unity! Now here comes the punch line: *since the first common source stage does not really provide much gain, the Miller effect does not make the gate-to-drain capacitance of the first stage look terribly big and therefore the Miller effect does not destroy the high frequency performance of the first common source stage!*

f) Plot $10\log_{10}\left|\frac{v_a}{v_{in}}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

g) Do a KCL at the gate of M1, used previously obtained results, and show that,

$$\frac{v_{in}}{v_s} \approx \frac{1}{1+j\omega(C_{gs1}+C_{gd1})R_s - j\omega C_{gd1}R_s\left[\dfrac{-g_{m1}+j\omega C_{gd1}}{g_{m2}+j\omega(C_{gd1}+C_{gs2})-g_{o2}\left[\dfrac{g_{m2}(r_{oc}\,||\,r_{o2})}{1+j\omega C_{gd2}(r_{oc}\,||\,r_{o2})}\right]}\right]}$$

h) Plot $10\log_{10}\left|\frac{v_{in}}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

i) Based on the results in part (d) and (f) and (h), which stage, first or second or the input part, limits the overall frequency bandwidth of the amplifier?

j) Now using your results from parts (c), (e), amd (g), Plot $10\log_{10}\left|\frac{v_{out}}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency.

k) If you now just consider a simple common source amplifier (assume that the FET M2 is replaced by a wire) then from the lecture notes (without making approximations):

$$\frac{v_a}{v_{in}} \approx \frac{-g_{m1}+j\omega C_{gd1}}{g_{o1}+g_{oc}+j\omega(C_{gd1})}$$

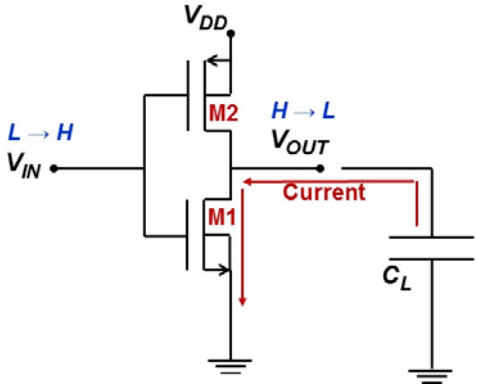
$$\frac{v_{in}}{v_s} \approx \frac{1}{1+j\omega(C_{gs1}+C_{gd1})R_s - j\omega C_{gd1}R_s\left[\dfrac{-g_{m1}+j\omega C_{gd1}}{g_{o1}+g_{oc}+j\omega(C_{gd1})}\right]}$$

Plot $10\log_{10}\left|\frac{v_a}{v_s}\right|^2$ (i.e. in dB units) on a log-frequency scale from 1e6 Hz to 1e12 Hz. Note the 3dB corner frequency. Compare the plot to your answer in part (j) for the cascode amplifier. You should see that the cascode does better in terms of the frequency bandwidth while providing at the same time few dB larger near-DC gain.

l) There is still a problem with using the cascode as a voltage amplifier; it has a large output resistance. This can be fixed by using a common drain stage as the final output stage. Do you think that adding a common drain stage would significantly spoil the frequency performance of the overall amplifier? Why or why not? Does a common drain stage suffer from the Miller effect?

Problem 11.2: (CMOS Logic: Fall times)

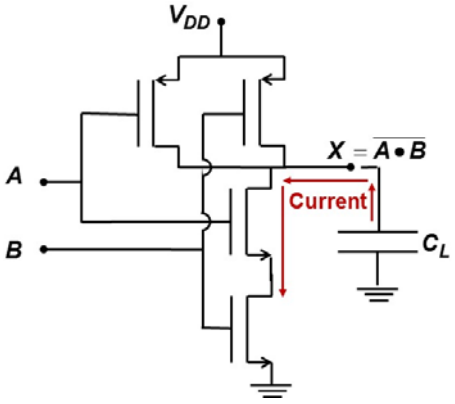
a) Consider the following inverter from the lecture handouts:



Suppose the output capacitor was charged HIGH ($\sim V_{DD}$) at time zero. The input transitioned from LOW to HIGH. The output capacitor will discharge through the FET M1. For simplicity we will define the fall time t_f to be the time in which the output goes from V_{DD} to $0.1V_{DD}$. Show that the fall time is:

$$t_f \approx \frac{2C_L}{k_n(V_{DD}-V_{TN})}\left\{\frac{V_{TN}}{V_{DD}-V_{TN}}-\frac{1}{2}\ln\left[\frac{0.1V_{DD}}{2(V_{DD}-V_{TN})-0.1V_{DD}}\right]\right\}$$

b) Now consider the following NAND gate:



Suppose the output capacitor was charged HIGH (~V_{DD}) at time zero. Both the inputs transitioned from LOW to HIGH. The output capacitor will discharge through the NFETs. For simplicity we will define the fall time t_f to be the time in which the output goes from V_{DD} to $0.1V_{DD}$. Find an expression for the fall time.

c) In part (b), does the bottom NFET ever go into the linear region during the discharge process? Explain?

d) In part (b), does the top NFET ever go into the linear region during the discharge process? Explain?

Problem 11.3: (CMOS Logic: The XOR gate)

a) Design a CMOS XOR gate using the minimum number of PFETs and NFETs (do not Google the answer). The truth table for the XOR gate is:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0