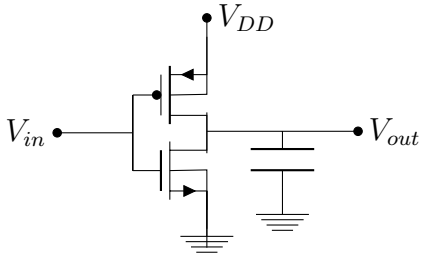
ECE 3150 Lab 2

Aalaap Narasipura

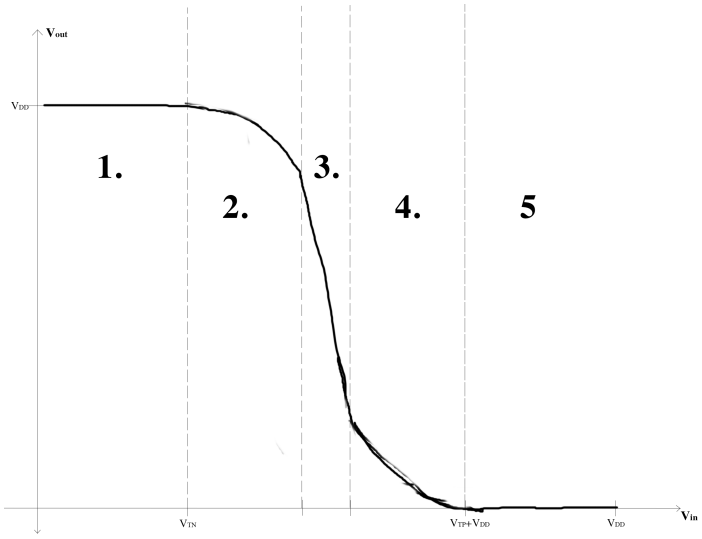
Febuary 26, 2016

1 Pre-Lab Work

CMOS Logic Inverter



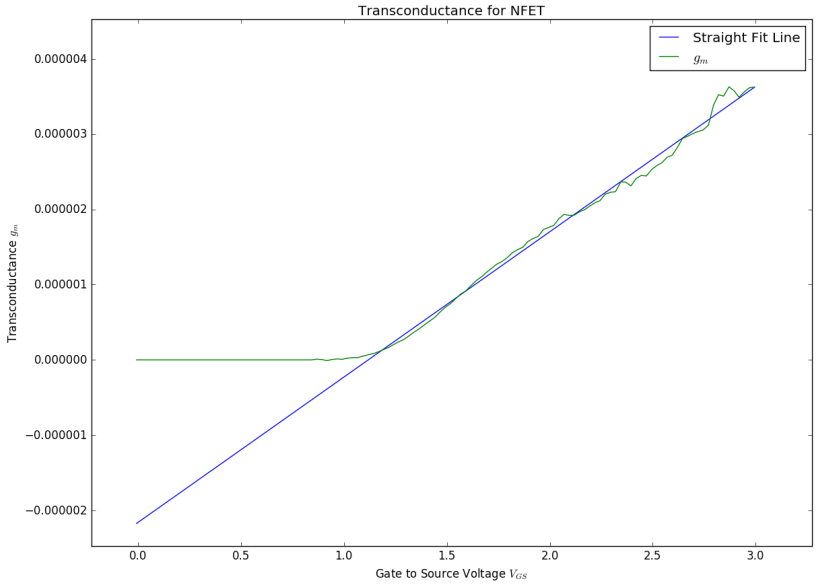
a) $V_{OUT} < V_{IN} - V_{TN}$
b) $V_{OUT} > V_{IN} - V_{TN}$
c) $V_{IN} < V_{TN}$
d) $V_{OUT} > V_{IN} - V_{TP}$
e) $V_{OUT} < V_{IN} - V_{TP}$
f) $V_{IN} > V_{TP} + V_{DD}$
g $V_{DD} = 5.0V$, $V_{TN} = 1.5V$, $V_{TP} = -1.5V$, finally, $k_n = k_p$



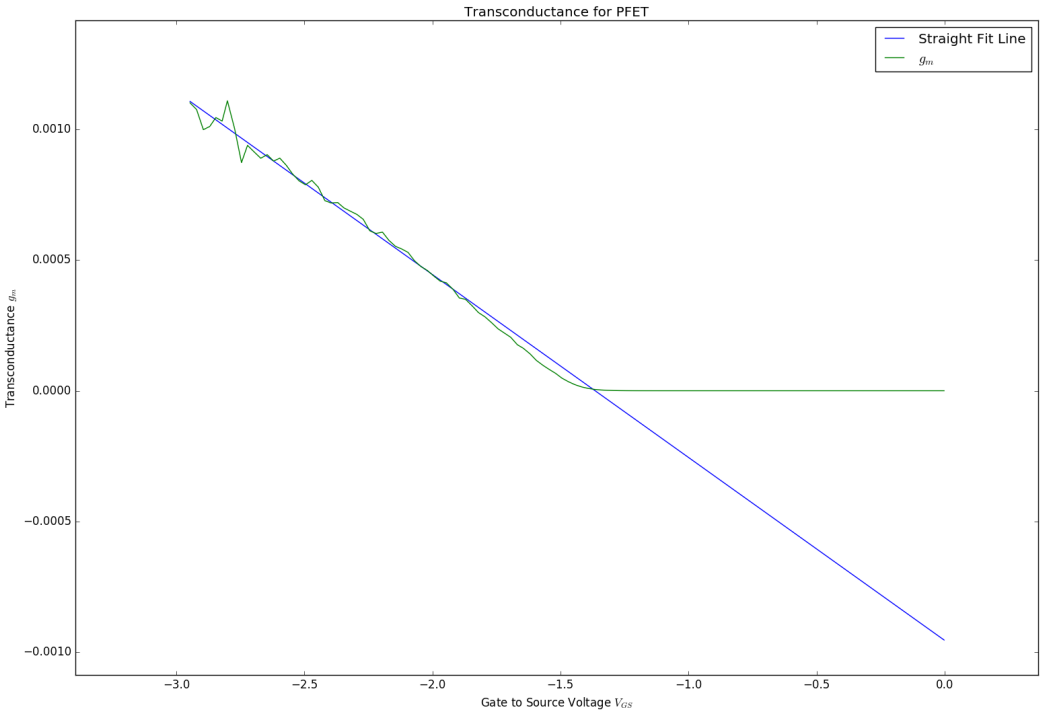
1. NFET in cutoff region, PFET is in linear region
2. NFET in saturation region, PFET is in linear region
3. Both are in saturation
4. NFET in linear region, PFET is in saturation region
5. NFET in cutoff linear, PFET is in cutoff region

2 Post Lab Work

2.1 Transconductance



Equation of line fit $= y = 1.93177 * 10^{-6}x - 2.1607 * 10^{-6}$



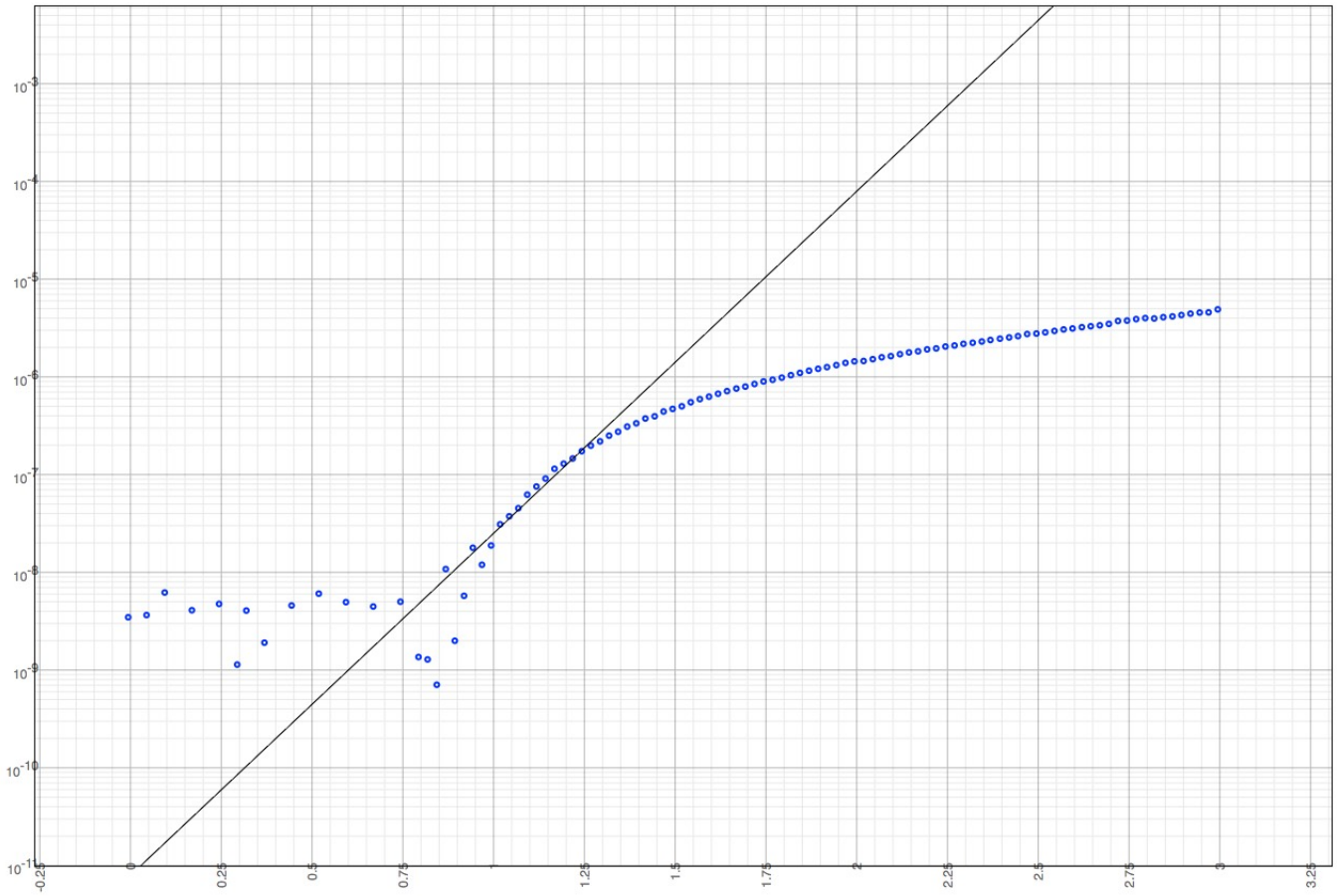
Equation of line fit $= y = -.0006996x - .0009546$

$V_{tn} = 1.118V$, $k_n = 1.93177 * 10^{-6} \frac{A}{V^2}$

$V_{tp} = -1.42V$, $k_n = -.0006996 \frac{A}{V^2}$

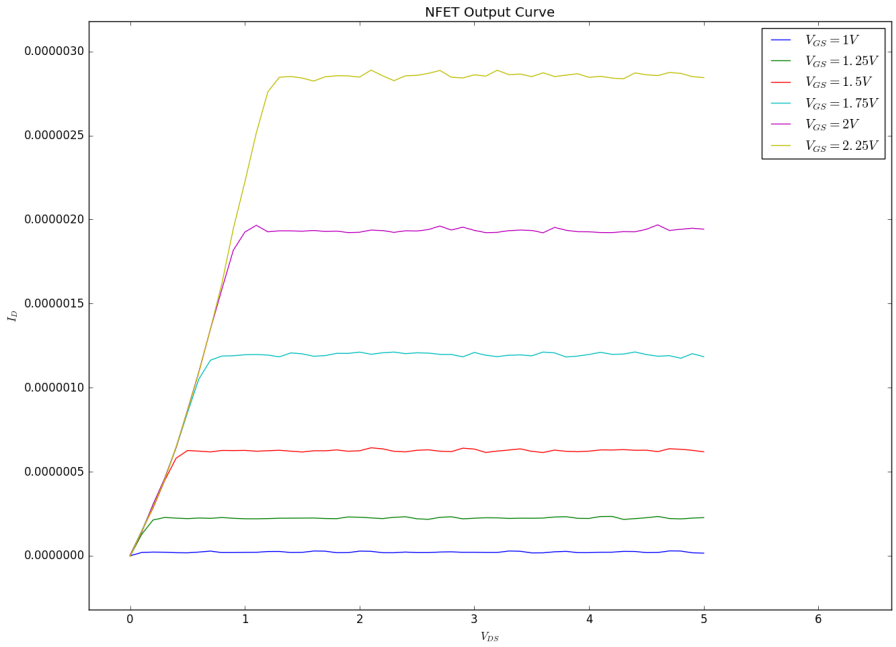
The NFET and PFET were not in agreement. I am not entirly sure why the NFET data is so much different. I think that we may have damaged the NFET at some point by having too large of a bias voltage or messing up the sweep voltage. However with this being said. The shape of the curve is what we want. k_p is the correct value based on the transistor data sheet given to us.

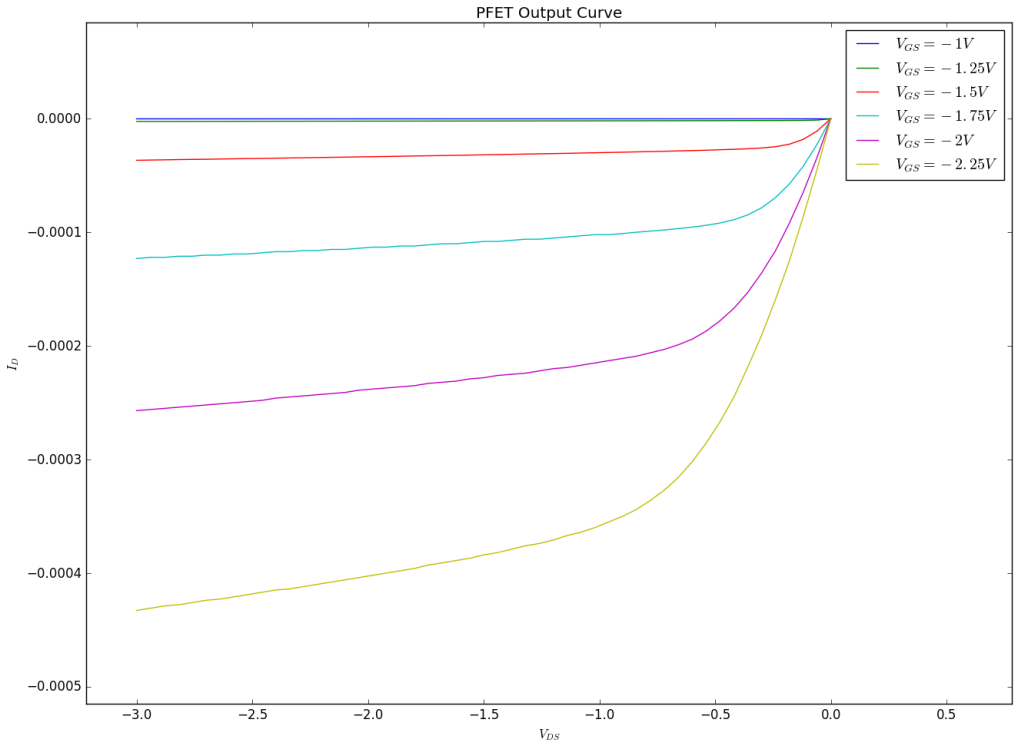
2.2 Subthreshold Condition



The measured inverse slope value was $175\frac{mv}{dec}$

2.3 FET Output Curves

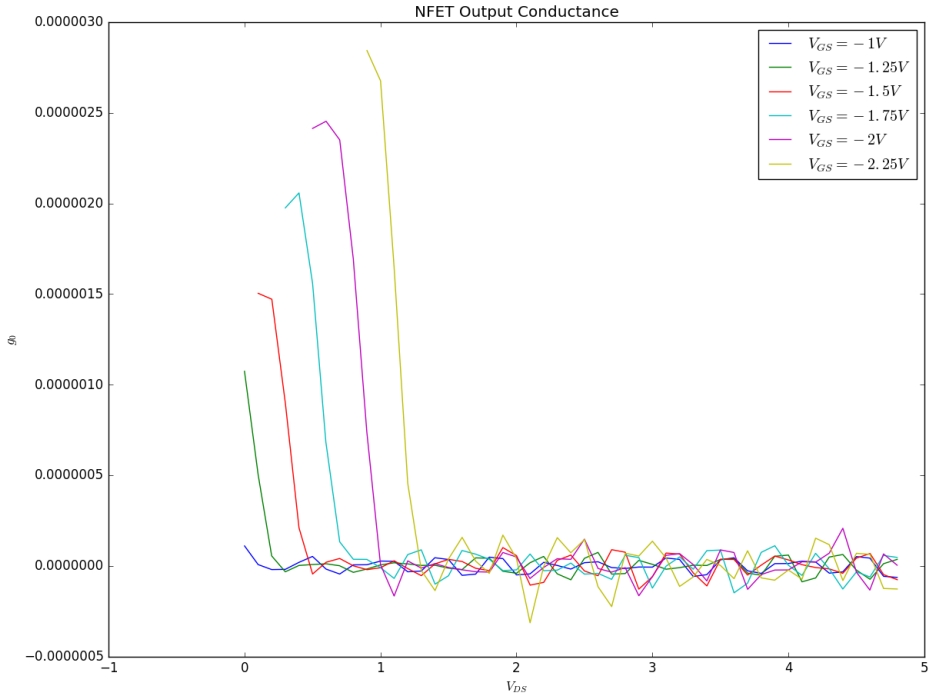




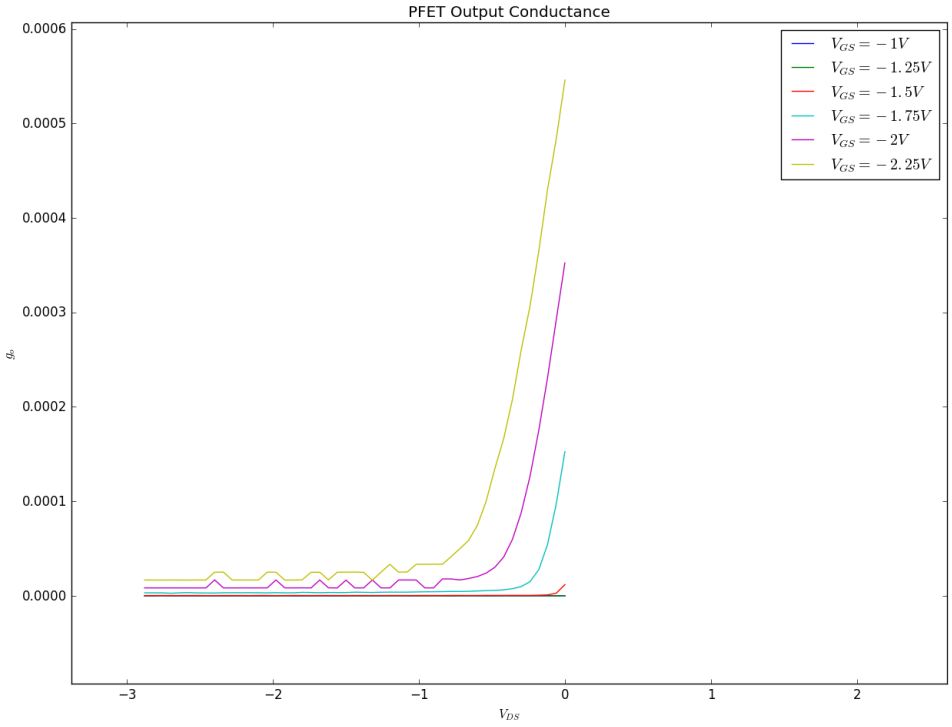
The slope of the PFET output curve above threshold was larger due tue a larger channel

length modulation. The NFET seemingly has a much smaller output current compared to the PFET, but this I believe is due to a damaged NFET. However if you were to scale the NFET data up so it was the same order of magnitude as the PFET it would have larger magnitude output current for a given V_{GS}.

2.4 FET Output Conductance

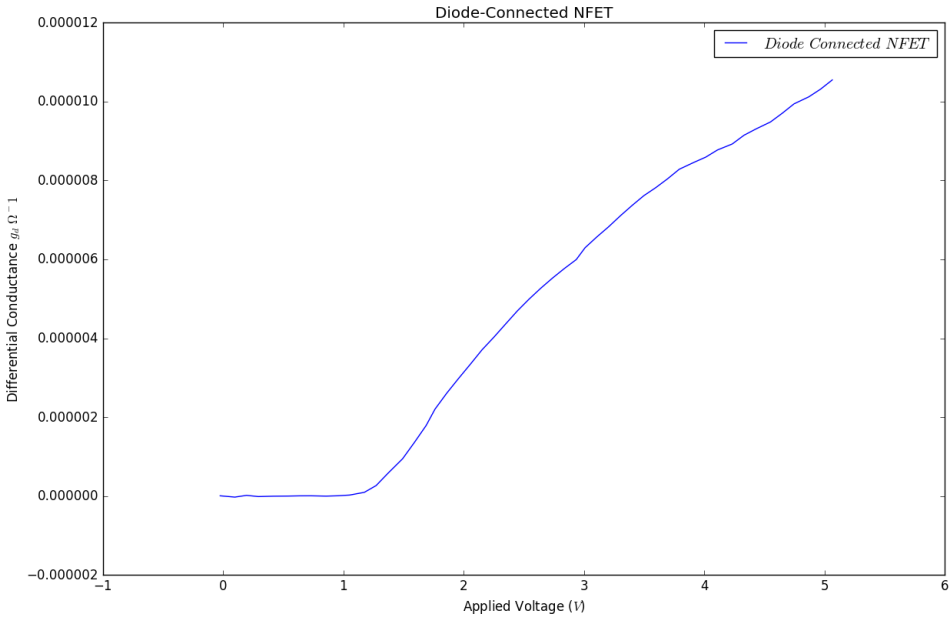


Again the values of g_o we got were quite off when compared to the PFET. We know the PFET is corect because I compared the values we got to the transistor data shet There is also a lot more noise in the NFET data. Both may be due to a damaged NFET. Also I noticed an odd taper down for the NFET.



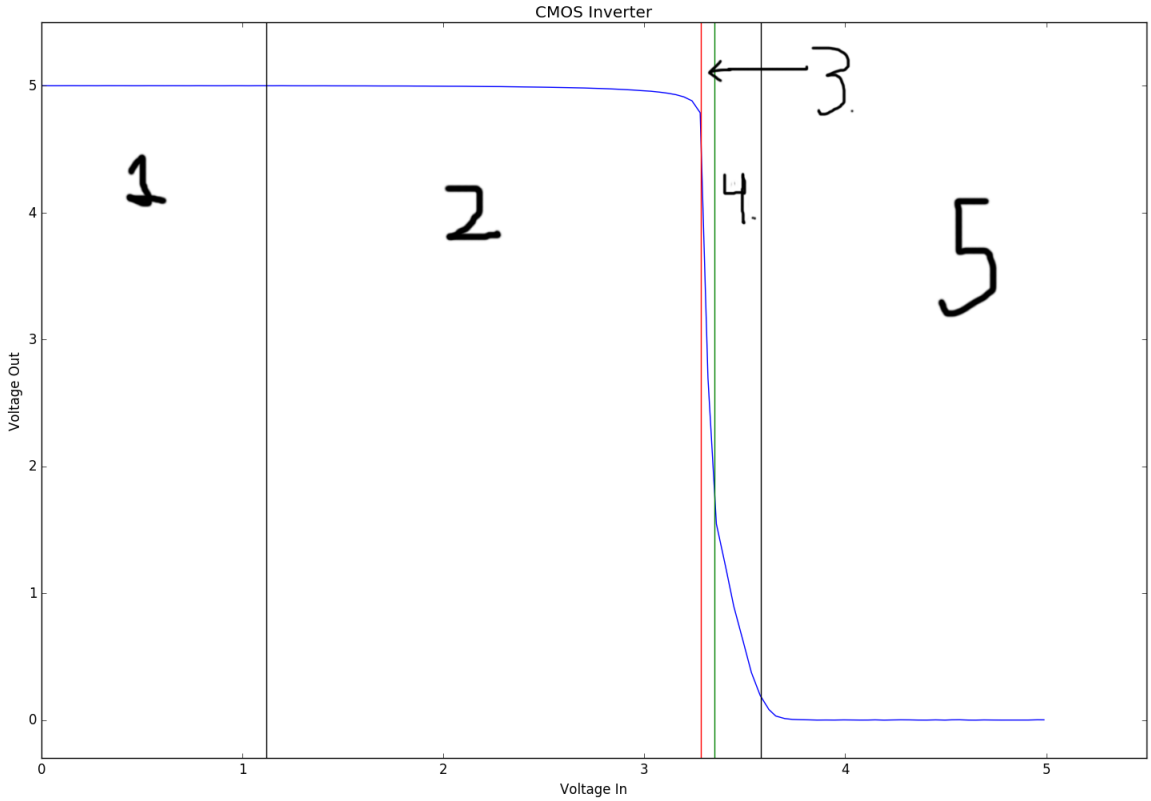
The PFET data shows only up to -3V. However because there will not be much output conductance at voltages less than V_{TP}, it can be extrapolated that from -3 V to -5V the data will be very similar if not exact to the values from -2V to -3 V.
I graphed more plots than the post lab said to do because I found it very interesting that at -1V V_{GS} and -1.25V V_{GS} for the PFET that there was almost no output conductance. A similar thing happened with the NFET for 1V V_{GS}

2.5 Diode-Connected NFET



The differential conductance that we measured follows the same path as the plot of transconductance in 2.1. The differential conductance bows out away from transconductance plot/ data. However the data values of the Diode-Connected This shows that is only an approximation of the transconductance we measured. It makes sense that these plots are similar because it is still an NFET device.

2.6 CMOS Inverter



1. NFET in cutoff region, PFET is in linear region
2. NFET in saturation region, PFET is in linear region
3. Both are in saturation
4. NFET in linear region, PFET is in saturation region
5. NFET in cutoff linear, PFET is in cutoff region

Due to the damaged NFET that we have the the CMOS inverter diagram is also incorrect. It again follows the correct shape but the V_{TN} value is very much off.