Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2016

Lab 2 **Due one week after your lab day in the course "Lab Dropbox"**

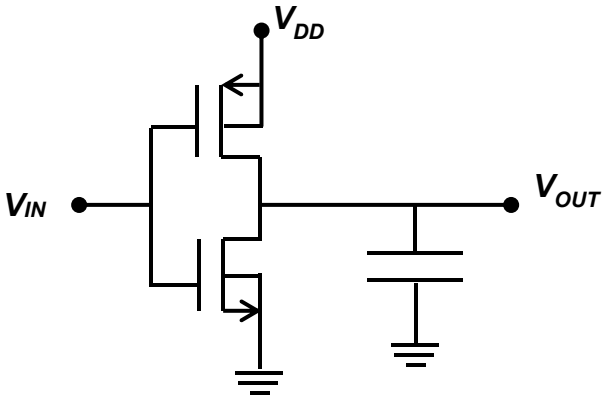
Lab Goals

1) Learn how to measure the terminal characteristics of FETs with the SMUs.
2) Manipulation of measured IV curves to deduce FET parameters including the threshold voltage and the transconductance parameter.
3) Explore both NFET and NFET devices.
4) Introduction to the CMOS inverter.

Pre-Lab Work

2.1 A CMOS (Complimentary MOS) Logic Inverter:

A CMOS logic inverter consists of a NMOS FET and a PMOS FET connected as shown below:



The capacitor at the output is not a part of the inverter- it is just there to help you understand the operation of the inverter better. Qualitatively, the operation of the inverter is easy to understand. When the input voltage V_{IN} is low (close to 0 V), the PFET is turned on but the NFET is turned off (in cut off). The PFET charges the output to a high voltage value – close to V_{DD}. When the input voltage V_{IN} is high (close to V_{DD}), the PFET is turned off (in cut off) but the NFET is turned on. The NFET discharges the output to a low voltage value – close to 0 V. For intermediate values of the input voltage, both the FETs could be turned on.

a) For what values of V_{IN} and V_{OUT} is the NFET in the linear region?
Answer: $V_{OUT} < V_{IN} - V_{TN}$

b) For what values of V_{IN} and V_{OUT} is the NFET in the saturation region?

c) For what values of V_{IN} and V_{OUT} is the NFET cut off?

d) For what values of V_{IN} and V_{OUT} is the PFET in the linear region?

e) For what values of V_{IN} and V_{OUT} is the PFET in the saturation region?

f) For what values of V_{IN} and V_{OUT} is the PFET cut off?

g) Suppose:

$V_{DD} = +5.0\ \text{V}$

$V_{TN} = +1.5\ \text{V}$

$V_{TP} = -1.5\ \text{V}$

$k_n = k_p$ (for the FETs)

Using the above values, sketch the transfer curve $V_{OUT} - \text{vs} - V_{IN}$. When you make the sketch, keep in mind the symmetry between the PFET and the NFET and the qualitative inverter description discussed above. Don't try to compute the $V_{OUT} - \text{vs} - V_{IN}$ curve. The sketch is meant to be qualitative.

Hint: In handout 10 you saw the transfer curve of the inverter in which there was a resistor in place of the PFET on top of the NFET.

h) On the transfer curve of part (g) indicate the regions of operation of the two FETs. For example, there is one region in which the NFET is in the saturation regime and the PFET is in the linear regime. There should be five distinct regions of the transfer curve.

Lab Preparation

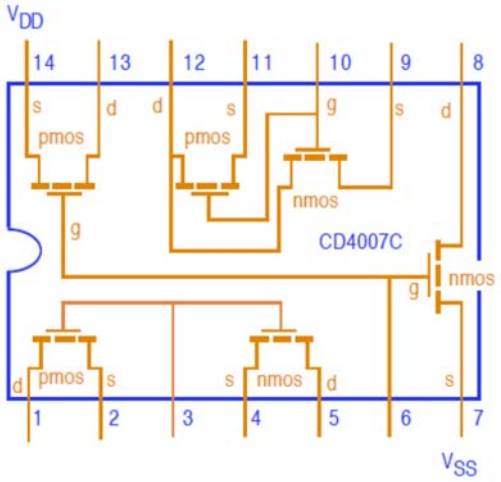
1) Carefully review this document. You need to know all that you will be doing in the lab and all the data that you will need later (after the lab) for the post-lab work.
2) You can use a USB memory stick to get data out of the lab computer (recommended). Or you might also be able to email the data files to yourself (not recommended).
3) Be sure to understand the analysis of the circuit to be built (pre-lab work).
4) Examine the lab bench. There are 2 SMUs per bench. The upper instrument is at address 5 and the lower instrument is at address 7.
5) Go over the transistor's data sheet (CD4007 chip). You should have some idea what the devices threshold voltages are and the range of drains currents expected.
6) Do the pre-lab before coming to the lab.

Lab Work

2.2 Measurement of MOSFET Current-Voltage (I-V) Characteristics

We first connect a single NFET in the CD4007C package to two SMUs. For convenience, the pin out diagram for the CD4007 part is given below in Figure 1. Choose the NFET device whose source is labeled VSS at pin 7. The source is connected to the ground lead of both SMUs, while the gate is connected to the upper SMU (GPIB address=5) and the drain is connected to the lower SMU (GPIB address=7). Place a CD4007C on your bread-board. It needs to straddle the long center pin gap so each

pin is isolated. Wire its source to the ground leads (which, BTW, also connects the device bulk/substrate contact to the ground). Connect the upper and lower SMUs to the gate (pin 6) and drain (pin 8), respectively.



CD4007 Chip: pin assignments

a) **NFET Threshold and $I_D - V_{GS}$ Curves:** Run the Keithley software for controlling the SMUs:

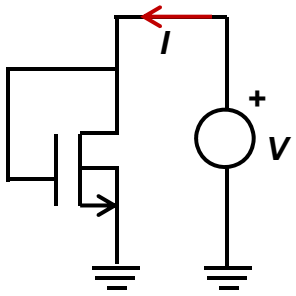
Start→All Programs→Keithley Instruments→Labtracer 2.0

Click the Setup 2400 on each SMU and select parameters for the $I_D - V_{GS}$ curves of the NFET. This means the gate voltage is swept (use Sweep Voltage) in small increments (25 mV) from below threshold (0 volts) to +3 volts with the source grounded and the drain voltage fixed at +5 volts. Perform a sweep with your SMU settings, and examine the drain current vs gate-to-source voltage on the graph frame of the Data Center window. If the data is noisy then increase the integration NPLC. Does your $I_D - V_{GS}$ show current a quadratic function of the gate voltage? If so, continue. If not, look for wiring problems. Save the data. Now input a formula in the software to take the square root of the measured drain current and plot this vs the gate voltage (both on linear scales). You will have to re-run the measurement after the formula is entered. From this graph estimate and record the device's threshold voltage V_{TN}. Vtn = 1.4v

b) **NFET Transconductance:** Here we are performing the same test as above – part (a) - except we want to time average this data to remove as much noise as possible because we will be evaluating derivatives of this data in the post-lab analysis. Go under Setup 2400 windows of each SMU and change the averaging parameter NPLC to 10. Run the measurement. Be patient as it will take a few minutes to run. Examine the $I_D - V_{GS}$ graph (linear scale). If the data looks as expected and is clean (noise free) then store the data to a data file for use in the post-lab work.

c) **NFET Output Curves:** Click the Setup 2400 on each SMU and select parameters for the $I_D - V_{DS}$ **output curves** of the NMOS transistor. This means the drain voltage is swept (use Sweep Voltage) in small increments (0.1 volts) from zero to +5 volts for several different fixed gate-source bias voltages (1 to 2.5 volts in 0.25 volt steps - use Step Voltage). This is the conventional way of displaying MOSFET output curves. Strike the RUN TEST button and the measurement begins. When it is completed the Data Center window appears. If your output curves appear not as expected, the transistor may be oscillating. A 0.1 μF capacitor across the drain-source terminals might stop the oscillation (or might make things even worse). Save your data and make sure information on the gate voltage for each output curve is also recorded and stored for later access.

d) **Diode-Connected NFET:** Short the gate and drain terminals together and remove SMU2 from the circuit leaving SMU1 connected to the diode-connected transistor. Modify the SMU1 Set Up for a 0 to 5 volt sweep on the diode connected NMOS transistor. You can remove SMU2 from the test set up or just ignore the data it produces. Run the test and examine the current-voltage curve. Does it look like a diode? Save the data for the analysis.



e) **PFET Threshold and $I_D - V_{GS}$ Curves:** Now you will repeat part (a) for the PFET device. Wire the PFET device which shares the same gate connection as the NFET device that you have already tested (its source is labelled VDD in the Figure on the previous page). Modify the SMU settings used for the NMOS $I_D - V_{GS}$ curve in part (a) by reversing the voltage polarities. This means the gate voltage is swept (use Sweep Voltage) in small decrements (-25 mV) from above threshold (0 volts) to -3 volts with the source grounded and the drain voltage fixed at -5 volts. Perform a sweep with your SMU settings, and examine the drain current vs gate-to-source voltage on the graph frame of the Data Center window. If the data is noisy then increase the integration NPLC. Does your $I_D - V_{GS}$ show current a quadratic function of the gate voltage? If so, continue. If not, look for wiring problems. Save the data. Now input a formula in the software to take the square root of the absolute value of the measured drain current and plot this vs the gate voltage (both on linear scales). You will have to re-run the measurement after the formula is entered. From this graph estimate and record the device's threshold voltage V_{TP} .

f) **PFET Transconductance:** Here we are performing the same test as above – part (e) - except we wish to time average this data to remove as much noise as possible because we will be evaluating derivatives of this data in the post-lab analysis. Go under Setup 2400 windows of each SMU and change the averaging parameter NPLC to 10. Run the measurement. Be patient as it will take a few minutes to run. Examine the $I_D - V_{GS}$ graph (linear scale). If the data looks as expected and is noise free then store the data to a data file for use in the post-lab work.

g) **PFET Output Curves:** Click the Setup 2400 on each SMU and select parameters for the $I_D - V_{DS}$ output curves of the PMOS transistor. This means the drain voltage is swept (use Sweep Voltage) in small decrements (-0.1 volts) from zero to -5 volts for several different fixed gate-source bias voltages (-1 to -2.5 volts in -0.25 volt steps - use Step Voltage). This is the conventional way of displaying MOSFET output curves. Strike the RUN TEST button and the measurement begins. When it is completed the Data Center window appears. If your output curves appear not as expected, the transistor may be oscillating. A 0.1 µF capacitor across the drain-source terminals might stop the oscillation (or might make things even worse). Save your data and make sure information on the gate voltage for each output curve is also recorded and stored for later access.

h) **A CMOS Inverter:** Now we take the same NFET and PFET devices already tested and short their drains together (their gate are already shorted inside the CD4007C package). The NFET source is the circuit ground, the PFET source is attached to VDD which is a 5 volt DC supply. Configure SMU1 as a

sweeping voltage source (from 0 to 5 volts) with at least 101 steps in between. Connect SMU1 to the circuit's input. Configure SMU2 as a voltage meter with a 6.0 Volt compliance. Connect SMU2 to the circuit's output. Run the measurement and plot the voltage transfer function (V_{OUT} – vs – V_{IN} on linear scales). Does it look like an inverter characteristic? Save the data for the analysis.

i) **Wind down:** Dismantle your circuit(s) and place your bread-board and the devices you tested in the bins that the TAs provided. Transfer all generated files for access outside the lab. Alternatively, if you brought portable media (USB memory stick) then gather up all the files onto your media.

Post-Lab Work

2.3 Analysis

a) **Transconductance**: For the NFET and PFET devices tested in lab works 2.2(b) and 2.2(f), use the measured data to calculate the transconductance g_m of both the FETs and plot it as a function of the gate to source voltage V_{GS} . You need to generate two separate plots; one for the NFET and one for the PFET. Note that,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

so you will need to numerically calculate the transconductance from the $I_D - V_{GS}$ data. Fit a straight line to the data and from the x-axis intercepts find the threshold voltage for each device. And from the slope of the fitted line, find the current constant, k_n or k_p , of each device. How well matched are the NFET and PFET devices (i.e. is $V_{TN} = -V_{TP}$ and is $k_n = k_p$)?

b) **Subthreshold Conduction:** All NFETs conduct a little in cut off when $V_{GS} < V_{TN}$ (and so do the PFETs). This is called subthreshold conduction and is considered a big problem in the industry. We will discuss the mechanism for this conduction later in the course. Using the data collected for the NFET device in lab work 2.2(b) plot the drain current (log10 scale) vs. the gate-source voltage (linear scale). The curve should have a near-linear appearance below the threshold voltage. Fit this portion of the curve with a straight line and find the inverse slope of this line. The inverse slope is usually expressed in units of mV/decade (i.e. how many mV of gate-to-source voltage is required to change the current by one order of magnitude). This number is often referred to as the sub-threshold slope and its value is around 59 to 60 mV/decade but in practice its value can vary a lot.
NOTE: if you can figure out a way to make the sub-threshold slope for FETs much smaller than 59 to 60 mV/decade, you will become one of the richest persons in the world.

c) **FET Output Curves:** For the NFET and PFET devices tested in lab work 2.2(c) and 2.2(g), plot the measured output curves (for each FET on a separate graph). Label the gate-source bias voltage values for the curves in each graph. What features of these output curves are markedly different between the NFET and PFET?

d) **FET Output Conductance:** For the NFET and PFET devices tested in lab work 2.2(c) and 2.2(g), you need to find (numerically) and plot the output conductance,

$$g_o = \frac{1}{r_o} = \frac{\partial I_D}{\partial V_{DS}}$$

using your measured data. Calculate and plot the output conductance g_o as a function of V_{DS} for different values of V_{GS}. For NFET, use a range of 0 to 5 Volts for V_{DS} and a range of $V_{TN} + 0.5$ to 2.5 Volts (with 0.5 Volts steps) for V_{GS}. For PFET, use a range of 0 to -5 Volts for V_{DS} and a range of $V_{TP} - 0.5$ to -2.5 Volts (with -0.5 Volts steps) for V_{GS}.

e) **Diode-Connected NFET:** From the measured current-vs-voltage data of the diode connected NFET in lab work 2.2(d), compute (numerically) and plot the measured differential conductance (resistance),

$$g_d = \frac{1}{r_d} = \frac{\partial I}{\partial V}$$

versus the applied voltage. In lab work 2.2(a) you found the transconductance of the NFET. How does the measured differential conductance above compare to the measured transconductance in 2.2(a). Are they the same? Should they be the same and why, or why not?

f) **CMOS Inverter:** In lab work 2.2(h) you measured the transfer curve of the CMOS inverter. In pre-lab work, you had analyzed the transfer curve of the CMOS inverter. Plot the measured transfer curve obtained in lab work 2.2(h) and using the measured values of the NFET and the PFET threshold voltages (see post-lab work 2.3(a)), indicate on your plots regions where the PFET is in cut off, linear and saturation regions and also indicate regions where the NFET is in cut off, linear and saturation regions.