Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2015

Homework 4 **Due on Feb. 26, 2015 at 5:00 PM**

Suggested Readings:

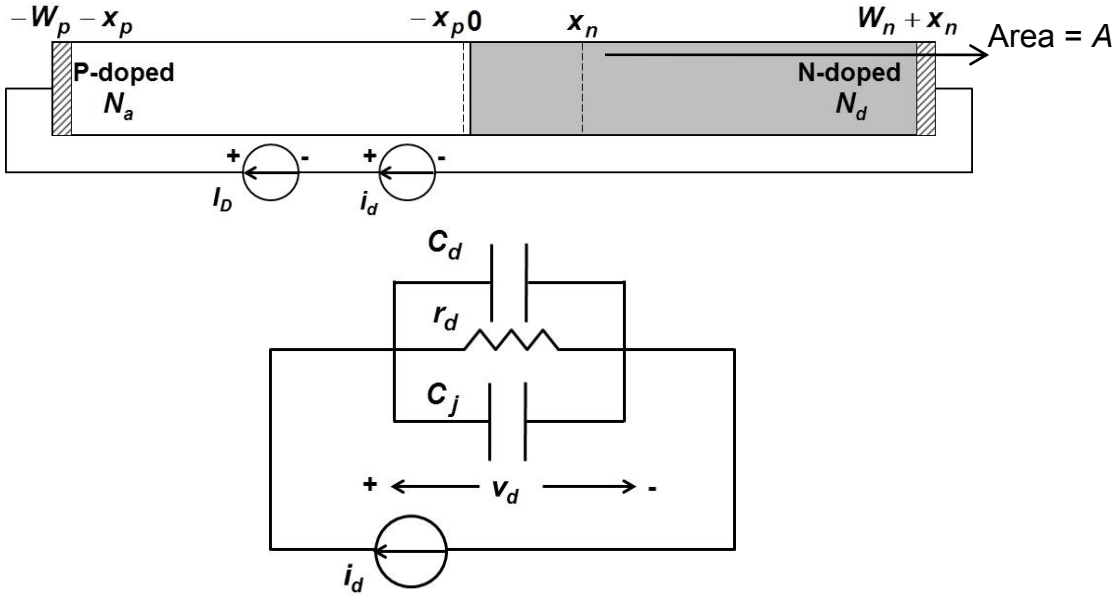
a) Lecture notes

Important Note:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Lab 2 is scheduled for the week of March 02
3) Unless noted otherwise, always assume room temperature.

Problem 4.1: (Response time of PN diodes)

Consider the following PN diode structure and its small signal circuit model:



Assume that the PN diode is strongly forward biased by the DC current source such that the junction depletion capacitance C_j is much smaller than the junction diffusion capacitance C_d. So you can ignore C_j. Also assume that the junction is asymmetrically doped such that $N_a >> N_d$ and therefore current contribution is entirely from hole injection into the N-side and the diffusion capacitance is also entirely due to the excess charge on the N-side. Assume the short-base limit ($L_p >> W_n$). The goal of this problem is to figure out the response time of PN diodes and answer the following questions; can one operate the PN diodes at infinitely fast frequencies? If not, then why not?

a) Derive (or rather write down) analytical expressions for the junction diffusion capacitance C_d and the junction differential resistance r_d consistent with the assumptions outlined above.

b) Suppose the small signal currente source is sinusoidal,

$$i_d(t) = \mathrm{Re}\left\{ i_d(\omega) e^{j\omega t} \right\}$$

Therefore,

$$v_d(t) = \mathrm{Re}\left\{ v_d(\omega) e^{j\omega t} \right\}$$

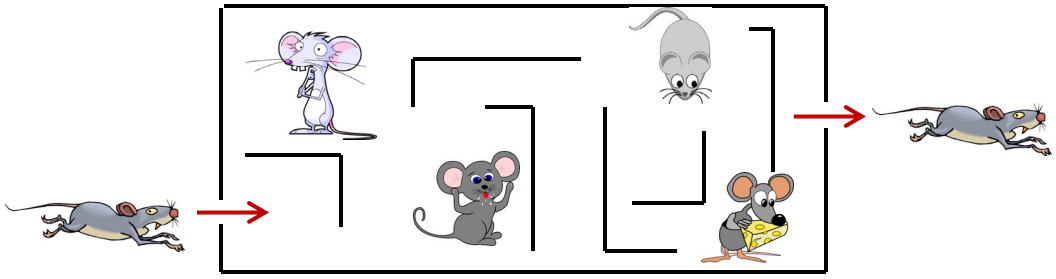
Find an expression that relates the voltage phasor $v_d(\omega)$ to the current phasor $i_d(\omega)$.

c) At high enough frequencies most devices appear like shorts because capacitances decrease the impedance of the devices. The PN diode is no exception. From the answer in part (b), you will notice that the voltage across the device goes to zero (and the device behaves like a short) in the limit $\omega \to \infty$. Find the frequency ω at which the square-magnitude of the voltage phasor is one-half of its value at zero frequency. This frequency, called the 3dB frequency or $\omega_{3\mathrm{dB}}$, determines the upper limit at which the PN diode behaves reasonably well and does not appear like a short.

d) Using your results in part (a), derive an expression for $\omega_{3\mathrm{dB}}$ in terms of the given device dimensions, dopings, diffusion coefficients, etc.

Now we approach the question of the fastest speed at which PN diodes can operate from a very different perspective.

e) Consider a box-maze shown below. Mice enter from one side (left), spend some time roaming around in the maze until they find the exit on the other side (right), and then they exit the box.



If one mouse enters the box from the left per second, and on the average each mouse spends 4 seconds in the box trying to find the exit, how many mice are in the box at any given time in steady state?

f) Now generalize: if the rate at which the mice enter the box is R, and each mouse spends time T in the box, and the number of mice in the box at any time in steady state is N, then how are these quantities related?

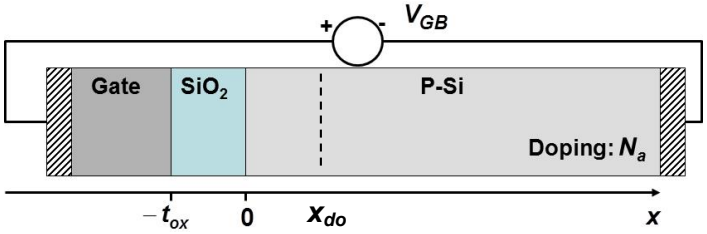
g) Now consider the holes which are injected into the N-side in the PN diode at $x = x_n$. The holes diffuse through the N-side, randomly move around, until finally they reach the right metal contact. We need to find the average time τ_{p-diff} that a hole takes to diffuse through the N-side. This diffusion time, as you might imagine, determines the maximum speed at which the PN diode can operate. Now compare the problem at hand with the mice problem above. We know the diffusion current due to excess holes at $x = x_n$ in steady state. We also know the total excess hole charge in the N-side in steady state. All that

remains to be found is the hole diffusion time τ_{p-diff}. Find an expression for τ_{p-diff} in terms of the given device dimensions, dopings, etc.

h) Compare the hole diffusion time τ_{p-diff} found in part (g) to the 3dB frequency ω_{3dB} found in part (c) and compare them and explain your results.

Problem 4.2: (NMOS Capacitor with a charged oxide)

Consider the MOS capacitor structure shown below.



Unfortunately, as is often the case, during the microfabrication process the oxide got charged. This means that fixed charged impurity atoms got incorporated into the oxide. The result is that the oxide now has a fixed **positive** volume charge density ρ_o (C/m^3). The gate is N+ silicon with doping $N_d = 10^{19}$ 1/cm^3. The substrate doping is $N_a = 10^{16}$ 1/cm^3.

a) Find the value of the built-in potential ϕ_B.

Next step is to find the depletion region thickness x_{do} in equilibrium ($V_{GB} = 0$). The electric field in the semiconductor can be obtained just as in the handouts:

$$\frac{dE_x}{dx} = \frac{\rho}{\varepsilon_s} = -\frac{qN_a}{\varepsilon_s} \qquad \{E_x(x = x_{do}) = 0$$

$$\Rightarrow E_x(x) = \frac{qN_a}{\varepsilon_s}(x_{do} - x)$$

The potential in the semiconductor follows from the field:

$$\frac{d\phi(x)}{dx} = -E_x(x) = -\frac{qN_a}{\varepsilon_s}(x_{do} - x) \qquad \{\phi(x = x_{do}) = \phi_p$$

$$\phi(x) = \phi_p + \frac{qN_a}{2\varepsilon_s}(x_{do} - x)^2$$

Things begin to change (from what is in the handouts) when we consider the field and the potential in the oxide.

b) Find the field everywhere in the oxide.

c) Sketch the field in the semiconductor and the oxide paying due attention to the boundary conditions.

d) Using your result in part (b), find the potential everywhere in the oxide.

e) Sketch the potential in the semiconductor and the oxide paying due attention to the boundary values of the potential in the bulk and in the gate, and indicate the numerical values of these boundary values on your sketch.

f) Find an expression for the depletion region thickness x_{do} in equilibrium.

For the following parts assume $V_{GB} \neq 0$.

g) Find an expression for the flatband voltage V_{FB}. Flatband voltage is defined as the value of V_{GB} for which there is no charge (of any sort) in the semiconductor. Notice how the flatband voltage depends on the oxide charge density ρ_o.

h) Find an expression for the gate charge surface charge density Q_G under flatband condition. Is it zero?

i) Sketch the field everywhere under flatband condition.

j) Sketch the potential everywhere under flatband condition.

k) Find an expression for the gate charge surface charge density Q_G for $V_{GB} < V_{FB}$.

l) Find an expression for the depletion region thickness x_d in the depletion regime; $V_{TN} > V_{GB} > V_{FB}$.

m) Find an expression for the gate charge surface charge density Q_G in the depletion regime; $V_{TN} > V_{GB} > V_{FB}$.

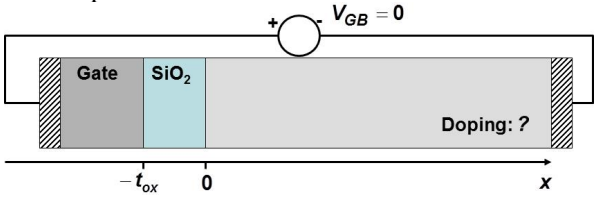
n) Find an expression for the threshold voltage V_{TN} in terms of the flatband voltage V_{FB}. If you did everything correctly, you will observe that the effect of the oxide charge density ρ_o have been absorbed in the definition of the flatband voltage and ρ_o does not explicitly appear in the expression for the threshold voltage.

o) How much has the threshold voltage V_{TN} shifted as a result of the oxide charge density?

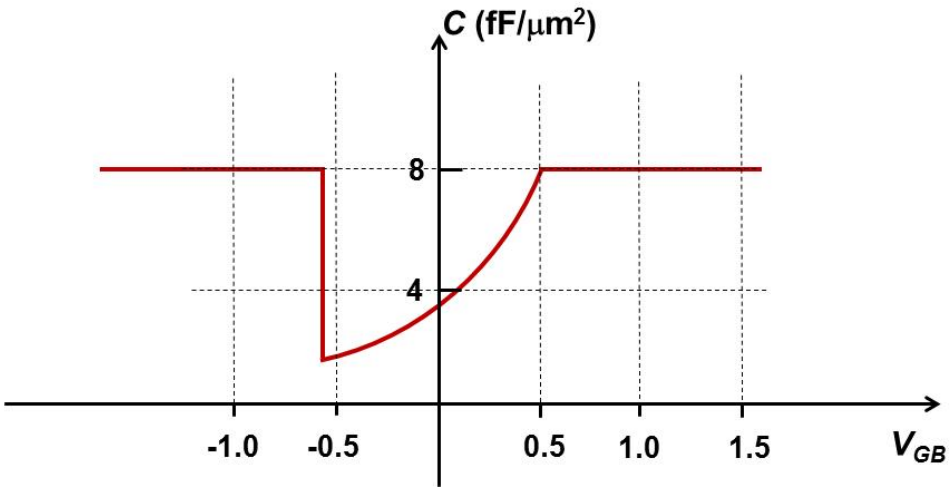
p) Find an expression for the gate charge surface charge density Q_G in the inversion regime; $V_{GB} > V_{TN}$.

Problem 4.3: (Mystery MOS Capacitor)

Consider the following MOS capacitor structure:



The type of the MOS structure is unknown (whether NMOS of PMOS). A graduate student decides to measure its capacitance vs gate-to-bulk voltage and obtains the following results:



a) What is the flatband voltage?

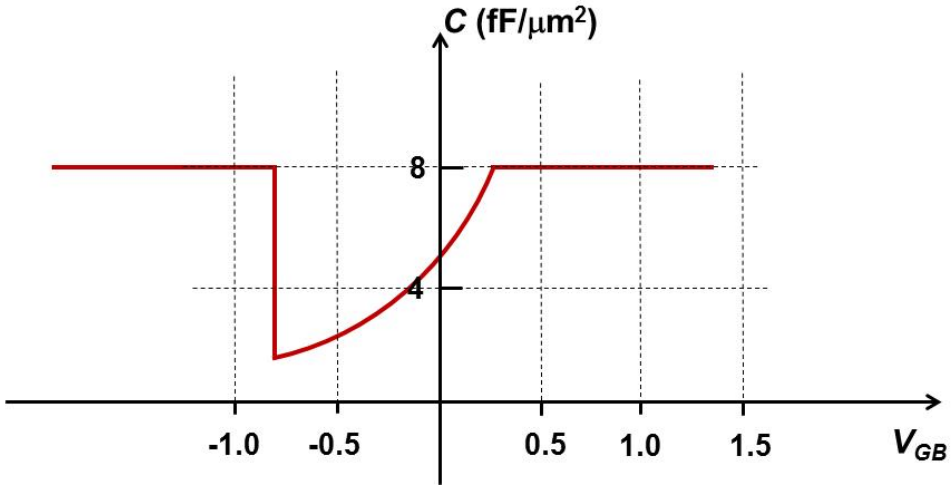
b) What is the threshold voltage?

c) What is the oxide thickness?

d) What is the substrate type (N or P)?

e) What is the substrate doping (in $1/cm^3$)?

f) The student accidentally leaves his MOS device uncovered at night and exposed to moisture and impurities. When he comes back in the morning and measures the device again he obtains, to his horror, the following curve:



The student concludes that the oxide got contaminated with charged impurities. If one models the charged impurities as a uniform charge density ρ_o, find the sign and magnitude of the charge density ρ_o.

Problem 4.4: (NMOS FET)

Suppose one is interested in obtaining and plotting the channel potential $V_{CS}(y)$ as a function of position y inside the channel from the source end ($y = 0$) to the drain end ($y = L$). Suppose that one is operating in the linear (or the triode) regime: $V_{DS} < V_{GS} - V_{TN}$ in which the current is:

$$I_D = \frac{W}{L}\,\mu_n\,C_{ox}\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$

a) Start from the current equation:

$$I_D = W\,\mu_n\,C_{ox}\left(V_{GS} - V_{TN} - V_{CS}(y)\right)\frac{dV_{CS}(y)}{dy}$$

and integrate the above equation from $y = 0$ to $y = y$. Solve the resulting equation for $V_{CS}(y)$ as a function of y and plot your answer for $0 \le y \le L$. Note that $V_{CS}(y = 0) = 0$ and $V_{CS}(y = L) = V_{DS}$.

b) The electric field is the derivative of the potential:

$$E_y(y) = -\frac{dV_{CS}(y)}{dy}$$

Find and plot the electric field from $y = 0$ to $y = L$. Is the field constant/uniform? If not, explain why not (using physical rather than mathematical arguments).

c) From your answer in part (b), find the magnitude of the field at the Drain end ($y = L$) when V_{DS} approaches $V_{GS} - V_{TN}$ from below and the current approaches:

$$I_D = \frac{W}{2L}\,\mu_n\,C_{ox}\left(V_{GS} - V_{TN}\right)^2$$

Explain your answer (using physical rather than mathematical arguments).