Department of Electrical and Computer Engineering, Cornell University

ECE 3150: Microelectronics

Spring 2015

Homework 7 **Due on March. 19, 2015 at 5:00 PM**

Suggested Readings:

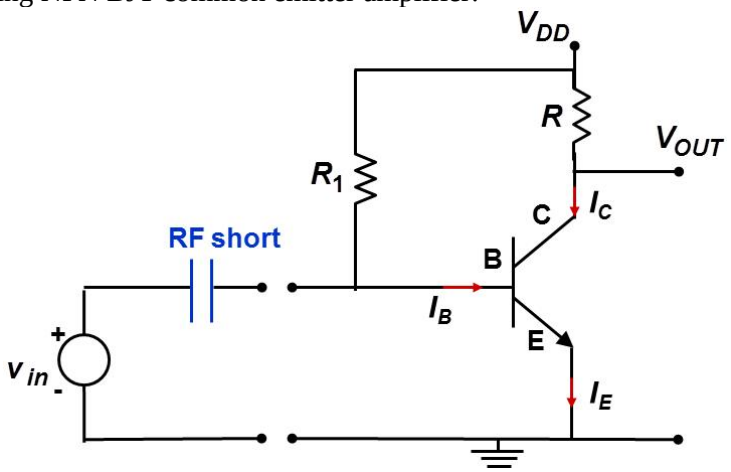
a) Lecture notes

Important Notes:

1) MAKE SURE THAT YOU INDICATE THE UNITS ASSOCIATED WITH YOUR NUMERICAL ANSWERS. OTHERWISE NO POINTS WILL BE AWARDED.
2) Unless noted otherwise, always assume room temperature.

Problem 7.1: (A NPN Common Emitter Amplifier)

Consider the following NPN BJT common emitter amplifier:



For the BJT assume:

$\beta_{FO} = 100$
$V_{BE-ON} = 0.6\,V$
$V_{CE-SAT} = 0.2\,V$
$V_{DD} = 5.0\,V$
$V_A = 50\,V$

For BJTs, the collector current in the forward active region is often written as,

$I_C = \beta_F I_B$

The current gain factor β_F depends on the width of the base region, which in turn depends on the collector voltage because of base-width modulation as discussed in the lecture handouts (the depletion region of the reversed biased base-collector junction expands into the base region when the collector

voltage is increased thereby reducing the width of the base region). Therefore, the current gain factor β_F depends on the collector voltage as well. One can model this dependence using a convenient analytical expression,

$$\beta_F = \beta_{FO} e^{\frac{V_{CE}}{V_A}} \approx \beta_F \left(1 + \frac{V_{CE}}{V_A}\right) \qquad \{ I_B > 0, V_{CE} > V_{CE-SAT}$$

This implies that,

$$g_o = \frac{\partial I_C}{\partial V_{CE}} = \frac{\partial \beta_F}{\partial V_{CE}} I_B = \frac{\beta_F}{V_A} I_B = \frac{I_C}{V_A}$$

which is the expression given in the lecture handout for the output conductance of BJTs. **Whenever the early voltage is specified, as in this problem, you should use the V_{CE} -dependent expression for the current gain β_F .**

Compare the above to what we did for FETs. In a FET in saturation,

$$I_D = \frac{k_n}{2}(V_{GS} - V_{TN})^2 (1 + \lambda_n V_{DS})$$

And,

$$g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{k_n}{2}(V_{GS} - V_{TN})^2 \lambda_n \approx \lambda_n I_D$$

The problem below is very similar to problem 6.1 for the NFET. It will be helpful if you compare parts of this problem with what you did in the same part in problem 6.1.

In the following parts, the small signal source at the input is not connected.

a) Generally one would like to keep the resistor R large in order to get a large voltage gain. But if it is too large, the BJT could go into the saturation region. Suppose you are at liberty to choose any value of the DC base current I_B. For every value of $I_B > 0$ the value of the resistor R has to be within a range in order to keep the BJT in the forward active region of operation. For values of I_B between 5 and 50 μA, find the maximum ($R_{\max}$) and the minimum ($R_{\min}$) values of the resistance R needed to keep the BJT operating in the forward active region. Plot $R_{\max}$ and $R_{\min}$ on the same plot as a function of I_B.

b) Suppose you need to the keep the DC voltage at the output V_{OUT} equal to $2.5\,V$. And you also need to keep the small signal gain, and therefore g_m, reasonably high, so you choose $I_C = 1\,mA$. What should be the values of the resistor R and the base current I_B needed to meet these objectives?

c) With the numerical value of the resistor as in part (b), and a varying base current I_B, what are the maximum and the minimum values of the ouput voltage V_{OUT} such that the BJT remains in the forward active region?

d) With the value of the resistor as in part (b), what are the maximum and the minimum values of the base current I_B such that the BJT remains in the forward active region?

e) The DC biasing of a BJT requires some care. In the circuit shown, the base-emitter junction of the BJT is effectively current biased using the resistor R_1. And R_1 should be much larger than the small signal resistance r_π of the base-emitter junction otherwise the small signal gain gets spoiled, as you will see below. For the value of the base current I_B found in part (b), what should be the value of the biasing resistor R_1?

In the following parts, the small signal source at the input is connected via a DC-blocking capacitor that is effectively a short at the RF frequencies of interest.

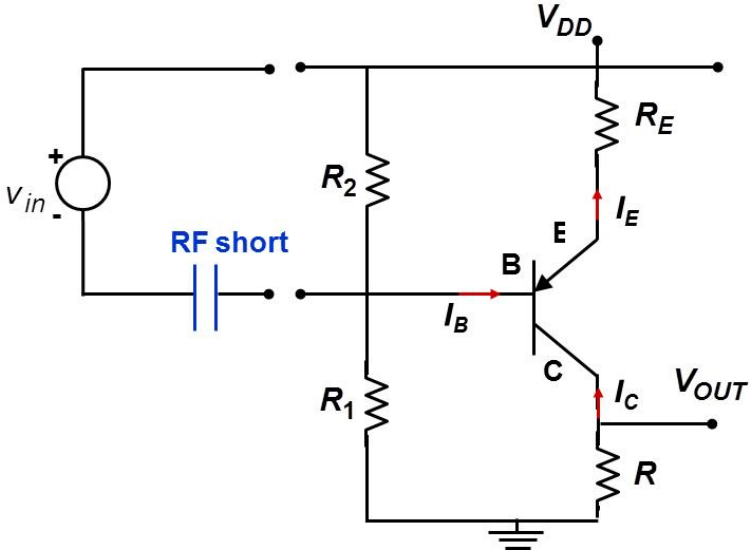
f) Draw a small signal model of the circuit, and find an expression for the open circuit small signal voltage gain $A_V = v_{out}/v_{in}$. Now explain what will happen if $R_1 << r_\pi$.

g) With the values of the resistors, R and R_1, as in part (b) and part (e), what is the open circuit small signal voltage gain $A_V = v_{out}/v_{in}$. Need a numerical number as an answer.

h) Under the constrain that the DC output voltage V_{OUT} must equal $2.5\,V$, you perhaps wonder if the voltage gain A_V could have been made significantly larger by choosing a different DC value of I_C than the 1 mA value picked in part (b). Of course, then the resistors R and R_1 would also need to change accordingly. Can you pick values for I_C, R and R_1 that let you obtain a much larger value for the voltage gain A_V than that obtained in part (g)?

Problem 7.2: (PNP Common Emitter Amplifier with a Degenerate Emitter: A Design Problem)

Consider the PNP common emitter amplifier circuit with emitter degeneration:



Assume the following for the PNP BJT:

$$\beta_{FO} = 100$$
$$V_{BE-ON} = -0.6\,V$$
$$V_{CE-SAT} = -0.2\,V$$
$$V_{DD} = 5.0\,V$$
$$V_A = \infty\,V$$
$$\beta_F = \beta_{FO} e^{\frac{|V_{CE}|}{V_A}} \qquad \{ I_B < 0, V_{CE} < V_{CE-SAT}$$

Suppose we have the following design constrains:

$$R_E = 100\ \Omega$$
$$V_{OUT} = 2.5\,V$$
$$I_C = -1.0\,mA$$

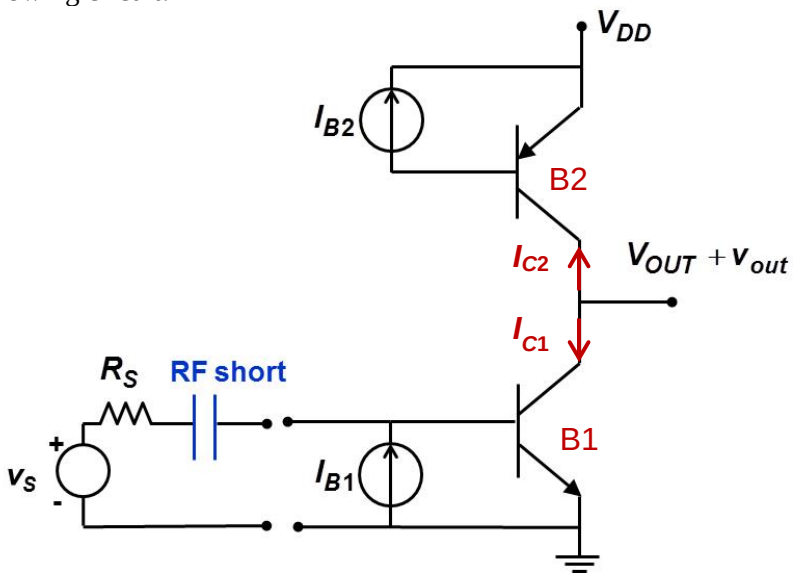
a) Find values of the three resistors R, R_1, and R_2 that meet the design constrains given above and get you the desired values of the output voltage and the collector current. Explain your reasoning. There might not be a unique set of values.

b) Draw a small signal model of the circuit, and find an expression for the open circuit small signal voltage gain $A_v = v_{out}/v_{in}$. Note the polarity of the small signal input voltage.

c) What are the maximum and minimum values the output voltage V_{OUT} can take while keeping the BJT in the forward active region of operation.

Problem 7.3: (PNP Loaded NPN Common Emitter Amplifier)

Consider the following circuit:



Assume that for the NPN:

$\beta_{FO} = 100$

$V_{BE-ON} = 0.6\,V$

$V_{CE-SAT} = 0.2\,V$

$V_A = 50\,V$

And for the PNP:

$\beta_{FO} = 100$

$V_{BE-ON} = -0.6\,V$

$V_{CE-SAT} = -0.2\,V$

$V_A = 50\,V$

And:

$V_D = 5.0\,V$

$\beta_F = \beta_{FO} e^{\frac{|V_{CE}|}{V_A}}$ in forward active operation

a) Choose values for the DC biasing base currents, I_{B1} and I_{B2}, such that:

$I_{C1} = -I_{C2} = 1\,mA$

$V_{OUT} = 2.5\,V$

b) What is the highest voltage V_{OUT} can take if both the BJTs are to remain in the forward active region?

c) What is the lowest voltage V_{OUT} can take if both the BJTs are to remain in the forward active region?

d) Is the output voltage swing (the difference between the maximum and the minimum allowed output voltages) of this amplifier better than that of the ones in problems 7.1 and 7.2?

e) Draw a small signal circuit for the amplifier and find an expression for the open circuit voltage gain, $A_v = v_{out}/v_s$.

f) Do you think the open circuit voltage gain of this amplifier (assuming $R_S = 0$ for a fair comparison) would be better than the open circuit voltage gains of the amplifiers in problems 7.1 and 7.2? Why or why not?

g) For the bias currents calculated in part (b), find A_v assuming $R_S = 0$. Need a numerical value as an answer.

h) Find an expression for the small signal output resistance R_{out} of the amplifier. As in the lecture handout 13, you will need to apply a small signal test voltage v_{test} at the output and calculate the small signal current that flows in as a result. Does the output resistance depend on the source resistor R_S?

i) For the bias currents calculated in part (b), find R_{out} assuming $R_S = 0$. Need a numerical value as an answer.

j) Find an expression for the small signal input resistance R_{in} of the amplifier looking in from the input terminals. As in the lecture handout 13, you will need to apply a small signal test voltage v_{test} at the input and calculate the small signal current that flows in as a result. When you apply v_{test} make sure you remove both the source voltage v_s and the source resistor R_S and replace these by v_{test}.

k) For the bias currents calculated in part (b), find R_{in}. Need a numerical value as an answer.