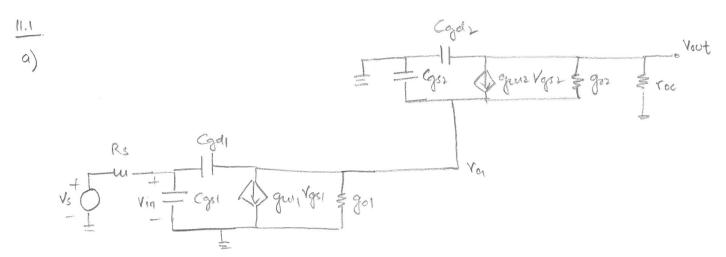
ECE Homework #11 Solutions (Farhan Rang)



d) see altached plot.

=>
$$\frac{V_0}{V_{uv}} = \frac{-g_{uv} + j_{uv} (g_{dv})}{g_{01} + g_{02} + j_{uv} (g_{dv} + g_{02}) - g_{02} + h_2(u)} = H_1(u)$$

f) See affactived plot.

i)
$$|H_2(\omega)|^2$$
 has a 3dB freq of ~ 2.5 GHz. $|H_1(\omega)|^2$ has a 3dB freq of ~ 1.58 GHz. $|H_0(\omega)|^2$ has a 3dB freq of ~ 1.29 GHz. So the first and the second stages limit the

freq. bandwidth of the amplified

See the attached plot. The 3dB frequency for
$$|H_T(\omega)|^2$$
 is ~ 0.80 GHz.

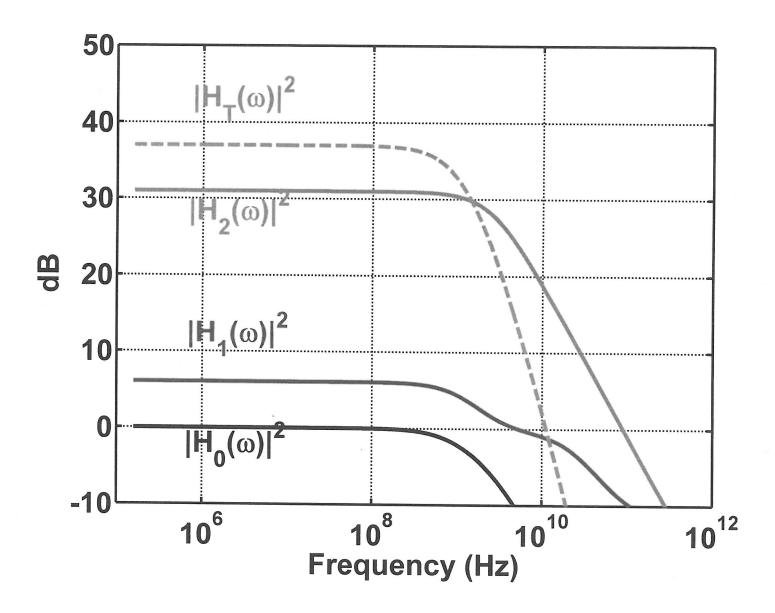
The 3de freq. of the Common Source comp is ~ 0.18 GHz.

The conscide has ~ 4.4 times larger 3dB frequency.

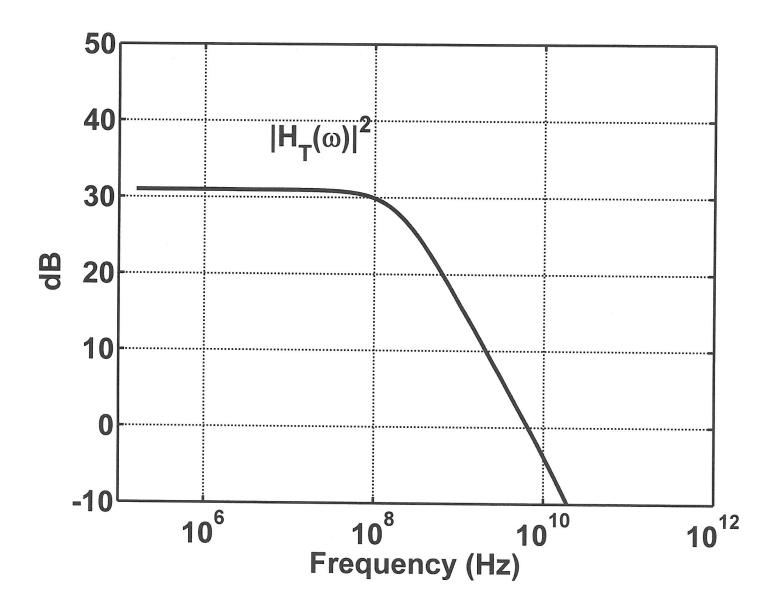
compared to the Common Source.

e) Common deain does not suffer from the Milles effect of there is no gain provided by this stage.

{ Cascode }



see (i)(j) for the 3dB frequencial of each curve



a). As long or Vos > VC15-VTN for the NFET, or Voot > VAD-VTN, the NFET will be in Saturation. In Saturation.

$$\frac{C_{1} dV_{00}T}{dt} = -\frac{T_{0}}{2} = -\frac{F_{11}}{2} \left(V_{00} - V_{7M}\right)^{2}$$

$$\Rightarrow V_{00}T(t) = V_{00}T(t=0) - \frac{F_{11}}{2} \left(V_{00} - V_{7M}\right)^{2} t$$

$$= V_{00} - \frac{F_{11}}{2} \left(V_{00} - V_{7M}\right)^{2} t$$

The time it takes for the output to reach VOO-VTN

For t>t, NFET will be in the linear region. where,

VOO-VIN (2(VDB-VIN) - VN) Vout = - Kn t ZCL.

- b) The expression for fall time will be the source as in part (a) if we replace kn in there by kn because two NFETS in series with the Same gate Voltage is like one longer NFET that is twice as long.
- then the bottom FET never operates in saturation. It always operates in the linear region.
- d) Yes. The top FET goes four calination into the linear region when Vour < VAD-VTN.

11.3

ABHAB. So the pull-up network (ould be;

AHE AHE
BYONT

The pull-down network

is just the duel of

it.

We will need to generale A and B using invertors. So we will need total of 12 FETs.