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A D-Band Power Amplifier with 15 dBm P_{sat} in 0.13 μm SiGe BiCMOS Technology

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***Abstract* — This paper presents a two-stage D-band power amplifier (PA) realized in 0.13 µm silicon-germanium (SiGe) BiCMOS technology. The amplifier employs the cascode topology at both stages and achieves a saturated output power (P_{sat}) of 15 dBm while output referred 1-dB compression point (OP1dB) is 11 dBm. The maximum power-added-efficiency ($\mathrm{PAE_{max.}}$) is 7.8% and the small signal gain peaks at 18.2 dB. The presented amplifier occupies an area of 0.83 × 0.52 $\mathrm{mm^2}$ including the pads.**

***Keywords* — power amplifier (PA), SiGe, millimeter wave (mm-wave), efficiency, D band, 140 GHz.**

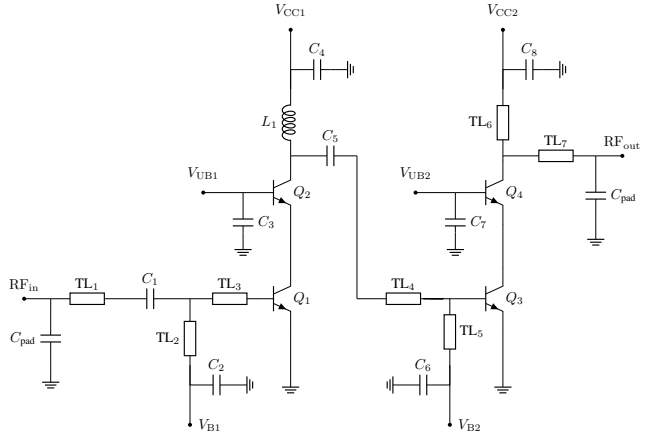
I. Introduction

The ever increasing demand for the high-data-rate applications and communication systems requires larger bandwidths, thus, necessitates higher frequency of operation. Power amplifier is one of the most critical components in such systems since it becomes more challenging to achieve a high output power with decent efficiency, as the frequency of operation increases. Numerous works with compound semiconductor technologies have been demonstrated at D-band frequencies [1], [2]. However, the silicon-based processes are also very attractive due to high-integration capabilities and competitive performance metrics. Availability of advanced silicon-based technologies with high cutoff frequency (f_{t}) and maximum frequency of oscillation (f_{max}) devices facilitates fast speed operations and allows higher integration levels while offering a cost-effective solution.

The rising impact of the parasitics and increased interconnection losses due to the skin effect make the PA design a challenging task at mm-wave frequencies. Besides, scaling down to the lower transistor nodes to improve f_{t} and f_{max} results in reduced breakdown voltages, putting another limit on attainable power levels.

The proposed studies in the literature that reported larger P_{sat} values often rely on power combining techniques [3], [4] to achieve a high saturated output power, at the expense of larger required chip area. Besides, they also suffer from the losses incurred in the combining networks which lead to reduced efficiencies. Other demonstrated works that do not rely on power combining techniques and achieve a similar or larger P_{sat} values as this work [5] exhibit lower PAEs.

The PA achieves a P_{sat} of 15 dBm and has a peak PAE of 7.8% at 140 GHz. It is realized in IHP's 0.13 μm SiGe BiCMOS technology SG13G2 which features an f_{t} / f_{max} of 300/500 GHz. The process includes heterojuction bipolar transistors (HBTs) with collector-emitter breakdown voltage ($\mathrm{BV_{CEO}}$) of 1.7 V and collector-base breakdown voltage ($\mathrm{BV_{CBO}}$) of 4.5 V. The back-end-of-line (BEOL) process offers seven aluminum (Al) based metal layers where the two top-most ones are thicker and provide lower losses.



$\mathrm{TL_1}$	72 µm @ 50 Ω	$\mathrm{TL_6}$	35 µm @ 50 Ω	$\mathrm{C_2}$	9 pF	$\mathrm{C_7}$	9.4 pF
$\mathrm{TL_2}$	44 µm @ 50 Ω	$\mathrm{TL_7}$	70 µm @ 50 Ω	$\mathrm{C_3}$	9.4 pF	$\mathrm{C_8}$	10.4 pF
$\mathrm{TL_3}$	40 µm @ 50 Ω	$\mathrm{L_1}$	250 pH	$\mathrm{C_4}$	9 pF	$\mathrm{V_{CC1}}$ & $\mathrm{I_{CC1}}$	3.5 V & 16.8 mA
$\mathrm{TL_4}$	40 µm @ 50 Ω	$\mathrm{C_{pad}}$	17 fF	$\mathrm{C_5}$	350 fF	$\mathrm{V_{CC2}}$ & $\mathrm{I_{CC2}}$	4.2 V & 35.6 mA
$\mathrm{TL_5}$	60 µm @ 50 Ω	$\mathrm{C_1}$	120 fF	$\mathrm{C_6}$	9 pF	$\mathrm{Q_{1,2,3,4}}$	20 × 70 nm × 900 nm

Fig. 1. Simplified circuit schematic of the two-stage PA

II. Circuit Design

A. PA Topology

The major investigation in mm-wave PA design includes the analysis of P_{sat}, PAE and gain. First of all, the common-emitter (CE) and cascode topologies are compared in terms of their achievable P_{sat}. Since the output voltage headroom in CE topology is limited by $\mathrm{BV_{CEO}}$, increasing the power level relies mostly on the increased transistor size to boost up the current flow. As the transistor size increases, the optimum load impedance ($Z_{\mathrm{opt,load}}$) drops substantially, requiring a larger impedance transformation and a more complicated matching network. As a result, the losses introduced by the more complex matching network overcome the increase in the performance due to the larger device size,

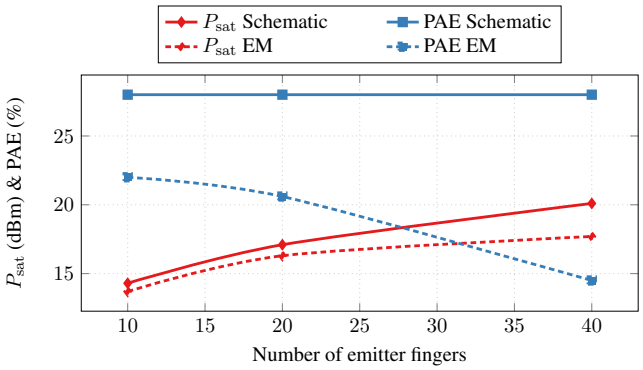


Fig. 2. Simulated P_{sat} & PAE vs. device size

and lead to a significant performance drop. On the other hand, the cascode topology has an increased voltage headroom which is beyond $\mathrm{BV_{CEO}}$, since it benefits from the low impedance (AC ground) at the base of the common-base (CB) device that prevents the voltage built-up. In this way, SiGe HBT cascode PAs can handle larger collector voltage swings without going into long-term reliability issues [6]. The proposed PA employs the cascode topology, as shown in Fig. 1.

B. PA Core Design

The design of PA cores includes the device layout and interconnects from the lower metal layer device terminals to the higher metal layers to connect to the matching network elements. A proper EM modeling of the core is crucial in mm-wave PAs since it involves considerations on device size, optimum load & source impedances, layout complexity and stability. Investigation on device sizes concludes that increasing the core size indefinitely results in diminishing increase in P_{sat} and a reduction in PAE. Fig. 2 shows the change in P_{sat} and PAE based on different device sizes. In ideal schematic simulations, doubling the device size results in additional 3-dB of P_{sat} while maintaining a similar PAE. However, after the devices are laid out and an EM simulation is performed on the core, the benefit of doubling the device size reduces due to interconnect losses.

The schematic level comparisons provide important insights on the power generation capability of cores with

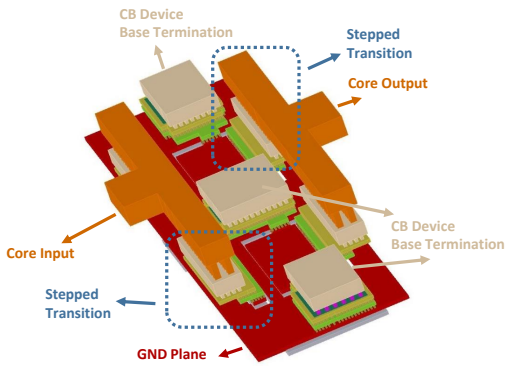


Fig. 3. 3-D view of the PA core

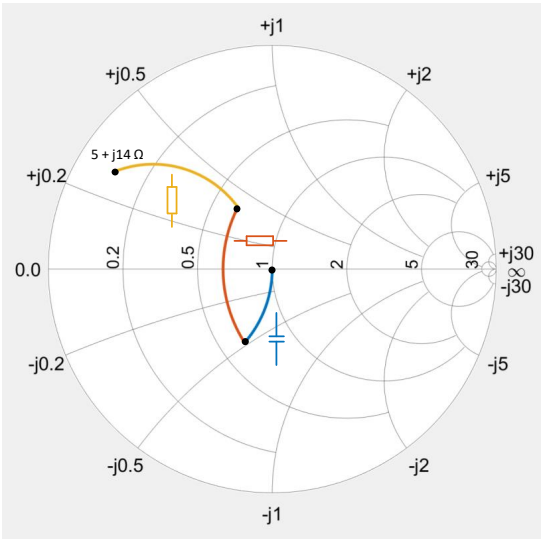


Fig. 4. Output impedance transformation on Smith chart

different device sizes. On the other hand, it is essential to make layout level comparisons to account for the layout parasitics from the interconnects to the device terminals. In this work, a P_{sat} of 15 dBm is targeted, meaning that the PA core needs to generate well above 15 dBm to compensate for the losses incurred by the output matching network. Device sizes and bias points are optimized through load-pull simulations towards that purpose. A device size of $20 \times 900\ \mathrm{nm} \times 70\ \mathrm{nm}$ (number of emitter fingers, effective emitter length & width) has been chosen, and the output stage devices have the current density of $1.78\ \mathrm{mA}$ per finger.

From the layout point of view, the primary aim is to minimize the contact losses of the metals and vias, in addition to avoiding parasitic coupling between the device terminals, mainly between the input and the output. Clear interfaces at the top-most metal layer have been created to connect to the matching networks. All the interconnections between the device terminals and the matching network interfaces are simulated in Keysight's Momentum electromagnetic (EM) simulator.

First of all, a stairway based layout method has been chosen to minimize parasitic coupling between the I/O terminals of each device and to reduce the shunt parasitic capacitances. In cascode topology, the base node of the cascode transistor (Q_2 & Q_4) is susceptible to oscillation at mm-wave frequencies. Therefore, the capacitive base termination of the CB device is carefully analyzed, and performed by large AC ground capacitors at the closest possible proximity to the base terminal to avoid unstability. The 3-D view of the PA core is displayed in Fig. 3.

Afterwards, load-pull simulations have been performed on the EM simulated core to obtain the $Z_{\mathrm{opt,load}}$ and the attainable P_{sat}. The simulated P_{sat} of around 16.3 dBm is observed when a load impedance of (5 + j14) Ω is presented to the PA output core. This impedance value indicates a parallel

equivalent resistance (R_{p}) of around 45 Ω, which requires only a small impedance transformation and correspondingly a lower loss. The output matching network, shown in Fig. 1, provides the desired impedance matching as illustrated in Fig. 4. Although a simple single element matching network, formed by a shunt line, would be sufficient to perform the matching, the pad capacitance (around 17 fF) is taken into account and incorporated into the matching network together with a series line.

III. Measurement Results

The small-signal characterization has been performed using OML's D-band frequency extension modules attached to a PNA-X network analyzer from Keysight. The measured and simulated S-parameters are in good agreement and shown in Fig. 5. The small-signal gain (S_{21}) peaks at 18.2 dB around 135 GHz and has a 3-dB bandwidth of 21 GHz (16%).

WR6.5SGX-M signal generator frequency extension module is used as the input source. A variable attenuator is attached to the source module to broaden the dynamic range of the input power for the large-signal characterization. The power levels of the input source are then determined through Erickson PM4 power-meter and used as reference levels. Afterwards, the insertion loss of the probes and the S-bend wave-guides are extracted through a thru measurement. A scalar loss calibration has been performed and the measured data are corrected accordingly. This setup is illustrated in Fig. 6.

The measured PAE peaks at the frequency of 140 GHz. The measured and simulated P_{sat}, PAE and gain results at this frequency are shown in Fig. 7. The large signal measurement is performed for the input power range from -19.5 dBm to 6.5 dBm. As P_{in} increases, the amplifier gain starts to compress and the compression reaches to 1-dB at the output power (OP1dB) of 11 dBm. Furthermore, PAE is maximized when an input power of 2.5 dBm is applied to the amplifier. The corresponding P_{out} for this input power level is around 14.5 dBm.

A detailed comparison with state-of-the-art D-band PAs is given in Table. 1. At similar operating frequencies, the proposed PA outperforms the others, except for [9], in terms of PAE. On the other hand, [3] and [7] report much higher

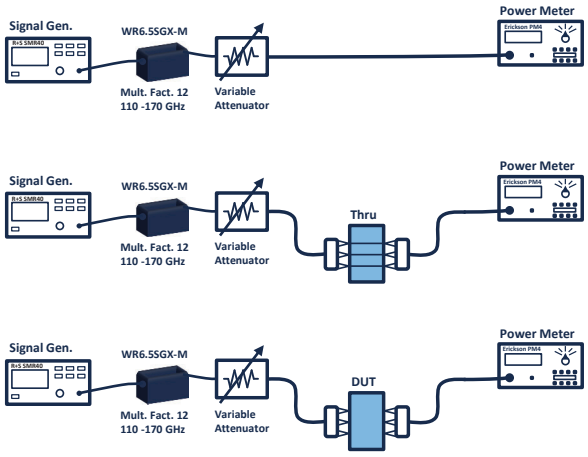


Fig. 6. Measurement setup

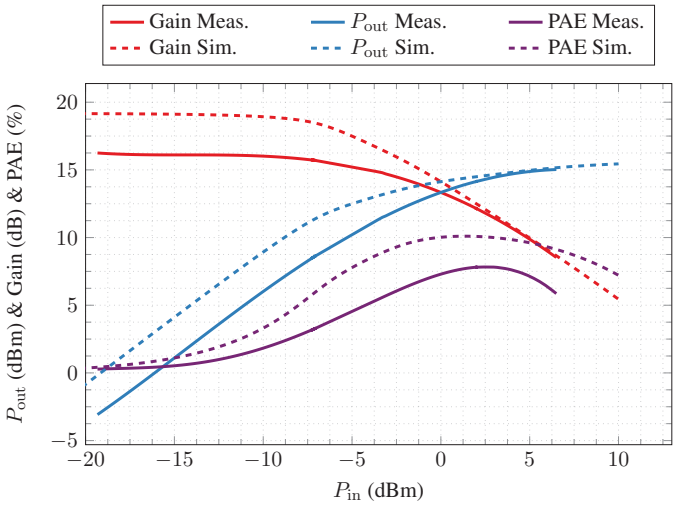


Fig. 7. Measured and simulated large signal parameters at 140 GHz

P_{sat}, since they employ 4-way and 8-way power combining techniques. OP1dB has been used to evaluate the linearity performance of the PA and the PA exhibits an OP1dB of 11 dBm. The total chip area is 0.463 mm^2 including the pads, and the dimensions of the PA core itself are 0.365 $\mathrm{mm} \times 0.3$ mm. The chip micrograph of the fabricated PA is shown in Fig. 8.

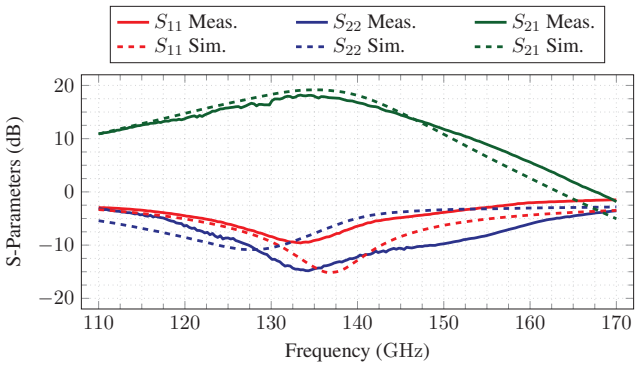


Fig. 5. Measured and simulated small signal S-parameters

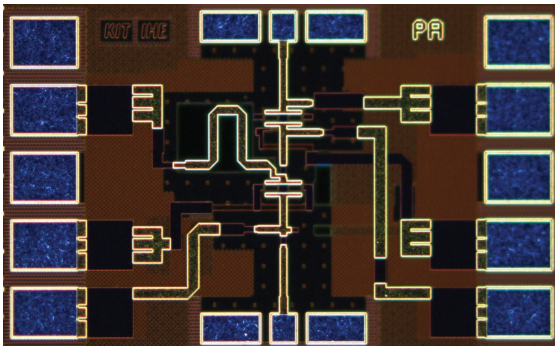


Fig. 8. Chip micrograph of the PA with dimensions of 0.83 $\mathrm{mm} \times 0.52$ mm

Table 1. Performance comparison of state-of-the-art PAs at D-Band

	[1]	[7]	[5]	[3]	[8]	[9]	[10]	**This Work**
Frequency (GHz)	135	124	160	165	140	135	140	140
3-dB BW (GHz)	35	20	49	25	60	17	27	21
Gain (dB)	27.8	15	27	30.2	21	20.3	21	16.7
P_{sat} (dBm)	24	20.8	14	18	12	14.8	7	15
OP1dB (dBm)	20	17	n.a	15.6	10	10.7	n.a	11
$\mathrm{PAE}_{\mathrm{max.}}$ (%)	7	7.6	5.7	4	5.1	8.9	7	7.8
Area (mm^2)	1.9	4.95	0.48	0.85	0.3	0.34	n.a	0.44
Technology	250 nm InP	90 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	40 nm CMOS	28 nm CMOS	130 nm SiGe

IV. Conclusion

A high-power, high-efficiency D-band PA in IHP's 0.13 μm SiGe technology has been realized and characterized. The proposed PA is based on two-stage cascode topology and employs LC based matching networks. It achieves a P_{sat} of 15 dBm, a peak PAE of 7.8% with a compact chip area and no power combining techniques.

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