A V-Band Vector Modulator Based Phase Shifter in BiCMOS 0.13 µm SiGe Technology

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***Abstract* — This paper presents a vector modulator based phase shifter circuit for the 57-66 GHz Band in IHP 0.13 µm SiGe BiCMOS technology. The input balun is avoided and the single to differential conversion is performed using the input transistors of the variable gain amplifier to achieve small area occupation and power consumption for a scalable design. The full phase range of 0-360° can be reached for a gain higher than −3 dB. The 1 dB compression point is reached at −12 dBm input power. The power consumption is measured at 45 mW, while the active area is only about 0.15 mm². The vector modulator characteristics are set by two pairs of control voltages which are applied directly through pins. The paper covers design, simulation and measurement of a prototype chip.**

***Keywords* — millimeter wave integrated circuits, BiCMOS integrated circuits, phased arrays, phase shifters**

I. Introduction

In modern communication technology the aim to higher data rates generates a growing demand for high coherent bandwidth. This demand can only be fulfilled in increasingly high frequency regions. Therefore a trend towards applications in the unlicensed 60 GHz band is noticeable. Due to high path loss in these frequency regions, the deployment of phased array transceivers with beamforming capabilities is necessary to achieve an adequate range. An essential part of these beamformers is the phase shifter. For adequate small bandwidths, a phase shift is equivalent to a time delay, which is used to influence the overall characteristics of the array by adding up differently phase shifted antenna signals. The changeable characteristics can be used to steer the main beam of the antenna array in the direction of the incoming wave or to suppress unwanted signals by steering minimums in their direction of arrival (null steering) [1].

The phase shift can be accomplished at different stages of the transceiver [2]. Furthermore various methods can be used to generate controllable phase shifts, e.g. switched reactance [3], varactor [4] or reflection based [5] circuits. Another common way to achieve a phase shift is by using a vector modulator (VM) circuit [6]–[8]. An overview of the general structure is shown in Fig. 1(a). The basic principle of the VM is to first separate the orthogonal IQ-components of the radio frequency (RF) signal, by splitting it and applying a 90°-phase shift to one of the signal parts. Then the amplitude of the individual components is changed by means of a variable gain amplifier (VGA). After this the two branches must be vectorially combined again to one RF signal, which can then be further processed. Changing the amplitudes of the IQ component will influence the amplitude and phase of the overall signal. This phase shifter architecture is known as vector sum phase shifter (VSPS) [9]. This paper presents a VSPS circuit for 60 GHz phased array systems. This paper is organized as follows: in Section II, the proposed phase shifter design details are discussed. Section III provides the measurement results and Section IV concludes the paper.

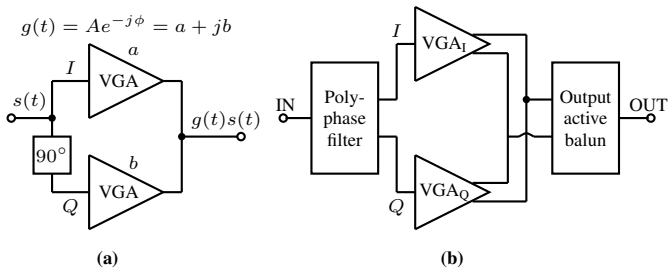

Fig. 1. Principle of vector modulator based phase shift with (a) basic mathematical background and (b) presented implementation

II. Circuit Design

The proposed phase shifter was designed and realized using SiGe:C BiCMOS technology provided by IHP. This process features HBTs with f_t of 240 GHz and f_{max} of 340 GHz . This technology has seven metalization layers, including two top metal layers. Metal 3 was used as ground plane and Metal 2 for V_{CC}. The VM is a single ended input and output circuit which consists of three stages as shown in Fig. 1(b). The first stage is a RLC 90° polyphase filter, followed by a variable gain amplifier (VGA) and the third stage is an active balun.

A. Input Stage

The RLC 90° polyphase filter at the input is acting as a power divider with 90° phase shift between its outputs to generate the IQ-signals needed for VM functionality. Careful design was necessary to guarantee a reasonable good phase accuracy and amplitude balance between the outputs, as well as a good input matching to 50 Ω for the whole bandwidth. A symmetric approach for value determination was chosen ($R_1 = R_2$, $L_1 = L_2$, $C_1 = C_2$) to design the polyphase filter with its target frequency in the middle of the band at 61.5 GHz. Later the theoretical values were slightly adjusted to compensate for parasitic influences.

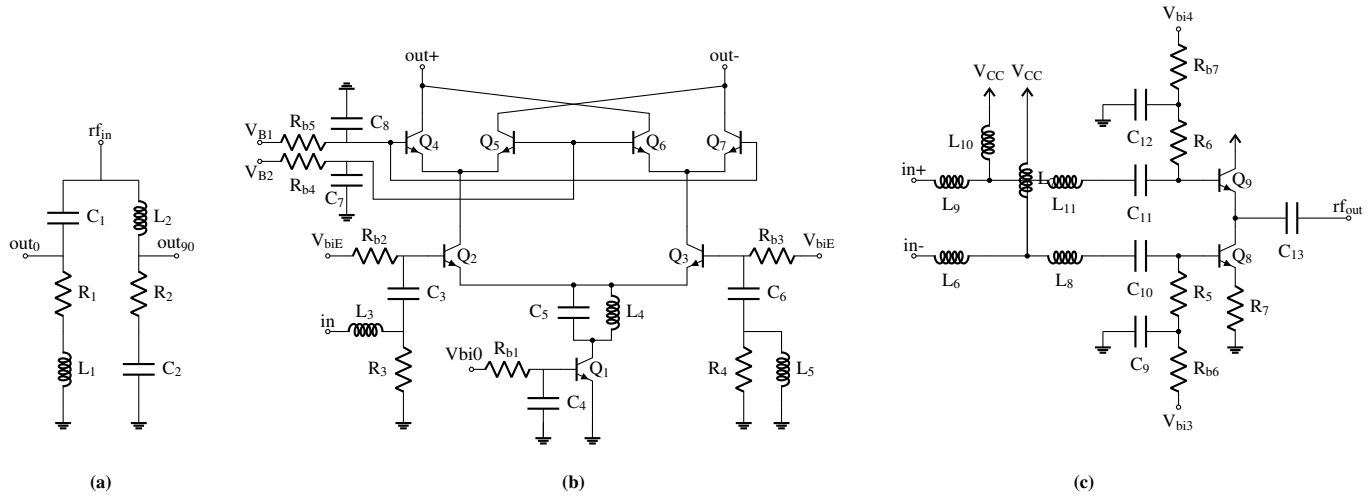

Fig. 2. Schematic of polyphase filter (a), current steering VGA (b) and active output balun (c) of the phase shifter without biasing networks

B. Variable Gain Amplifier

Both signals created by the polyphase filter are separately fed into the second stage, which is a VGA using a current steering topology as illustrated in Fig. 2(b). Its upper stage consists of two differential transistor pairs Q_4/Q_5 and Q_6/Q_7, biased with V_{B1} and V_{B2} in order to steer the current and therefore the signal through different branches.

For allowing negative gain (signal inversion), the circuit uses a differential input signal and therefore usually needs a separated balun upstream to deal with single-ended input signals. This would require additional chip area and power consumption. Active baluns can be built using differential pairs similar to the ones utilized in the lower stage of the VGA. This led to the idea of combining both steps and use Q_2/Q_3 simultaneously as the lower stage of the VGA and the differential pair for the balun (see Fig. 2(b)). A special challenge for this combined design is the current source on the emitter (Q_1), which has a major influence on the performance of the balun. Ideally it provides a constant DC current and a ground for the RF-signal, while a signal flow from the emitter of Q_2 to the emitter of Q_3 is needed for the balun functionality. Therefore, a parallel resonant cicuit consisting of C_5 and L_4 is used as a band stop for signals in the target bandwidth. This leads to a better RF isolation, which means less signal loss through Q_1, and increases the performance significantly. The large shunt capacitor C_4 combined with the resistor R_{b1} at the base contact of Q_1 ensures further RF-DC separation to prevent RF leaking to the biasing network.

The input matching network at the base of Q_2 consists of L_3 and R_3 together with the coupling capacitor C_3. L_5, R_4 and C_6 at the base of Q_3 are added to guarantee symmetric conditions for Q_2 and Q_3, which is needed for the best possible balun performance.

The upper stage is biased with standard current mirrors separated from the RF part of the circuit by means of resistors (R_{bx}) and shunt capacitors (C_7, C_8). The output matching and the supply feed is performed after recombination of I and Q signals at the output stage (see Fig. 2(c)).

As mentioned before, managing the gain of the VGAs is done by controlling the base voltages of the upper transistors ($Q_{4\text{-}7}$), V_{B1} and V_{B2}. These are connected to four pads (two for each VGA) on the chip through voltage dividers. In later applications digital control circuits could be used instead. The different settings for one VGA can be seen in table 1, where V_{Cx1} and V_{Cx2} are the control voltages at the pads and $V_{Sx} = V_{Cx1} - V_{Cx2}$ is a helping variable to describe the offset from the neutral point ($V_{Cx1} = V_{Cx2} = 3.25\,\mathrm{V}$).

Table 1. Control voltages extreme values

V_{Sx} (mV)	V_{Cx1} (V)	V_{Cx2} (V)	Gain
−155	3.095	3.405	$-G_{MAX}$
0	3.25	3.25	0
155	3.405	3.095	G_{MAX}

C. Output Stage

After the VGAs, the I and Q branches are combined by connecting them in current. The DC-feeding of the VGAs and the matching to the output stage is done by two T-joints consisting of three inductors each ($L_{6\text{-}11}$) and a pair of capacitors (C_{10}, C_{11}), as shown in Fig. 2(c).

The further signal processing requires a single ended signal. Therefore, an active balun, consisting of two transistors (Q_8, Q_9), is deployed at the output. To get amplitude balance between the two transistors, a degeneration resistor R_7 is placed on the emitter of Q_8. Interstage matching between stage 2 and stage 3 has been done in part by the previously mentioned T-joint, but also by the two resistors R_5 and R_6, combined with the two shunt capacitors C_9 and C_{12}. Similar to the input of the VM, the output is matched to $50\,\Omega$. Due to carefully adjustment of Q_8/Q_9 biasing via V_{bi2} and V_{bi3}, no further matching network is needed and the coupling capacitor C_{13} is sufficient.

III. Measurement

The chip micrograph of the proposed design is depicted in Fig. 3. The core area of this circuit occupies $0.15\,\mathrm{mm}^2$ ($0.43\,\mathrm{mm} \times 0.36\,\mathrm{mm}$). At nominal bias conditions and middle

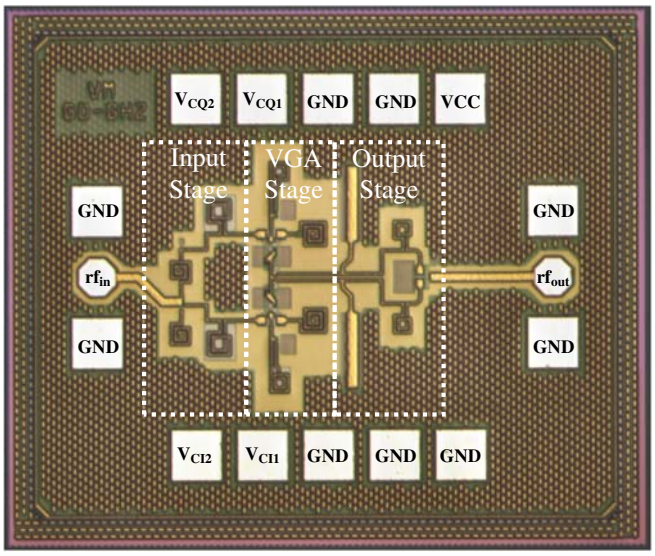

Fig. 3. Chip layout with marked stages and pads

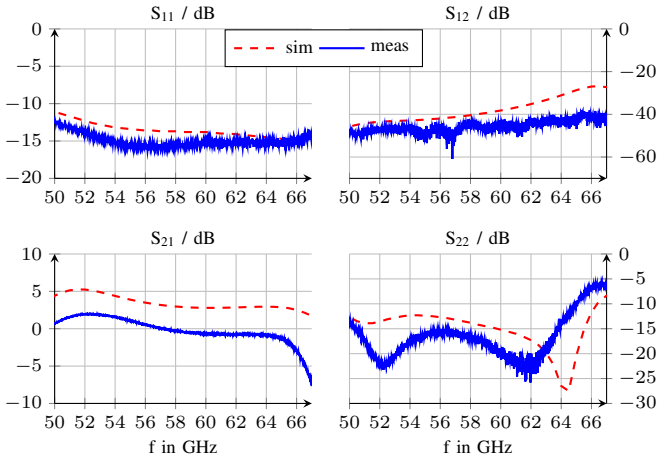

Fig. 4. Simulated and measured S-Parameters for $V_{BI} = 65\,\mathrm{mV}$ and $V_{BQ} = 25\,\mathrm{mV}$

gain the designed phase shifter consumes 45 mW with 3.3 V supply. All measurements were done on wafer. Small signal measurements were done using Rohde&Schwarz ZVA67 Vector Network Analyser (VNA). MPI DC-67 GSG Titanprobes with 100 µm pitch have been utilized for RF probing. The large-signal measurements are evaluated using a R&S NRP-257 power sensor.

A. *Small Signal Measurements*

Fig. 4 shows the s-parameters results of the designed phase shifter at middle gain stage where $V_{SI} = 65\,\mathrm{mV}$ and $V_{SQ} = 25\,\mathrm{mV}$. Within the target band a small signal gain between 0 dB and −2.8 dB along with input and output return losses less than 10 dB have been measured. The overall performance shows the expected behavior. The main differences between simulation and measurement can be seen in an overall lower gain and a slight shift to lower frequencies. Such differences can be due both to input and output pads

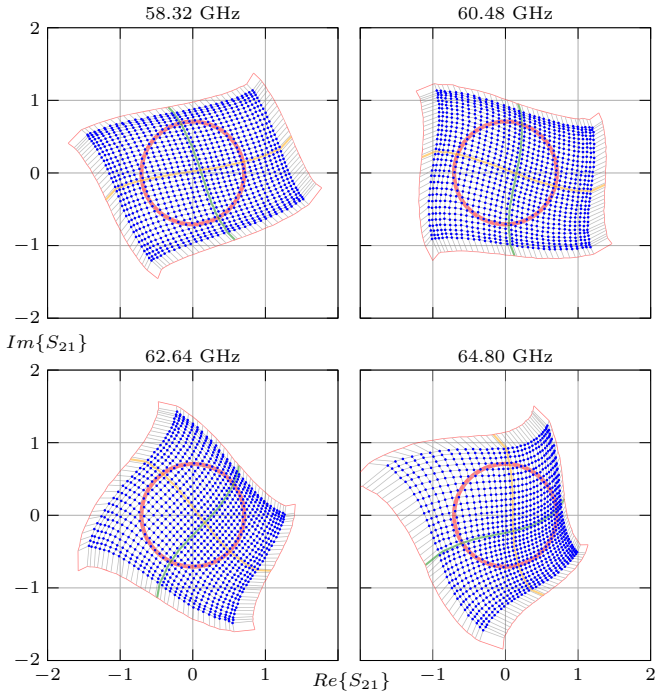

Fig. 5. Measured transmission characteristics (S_{21}) at the four middle frequencies swept over the full control range with steps of 5 mV ($\widehat{=}$ 10 bit) shown in the complex plain. The −3 dB gain circle is shown in red.

losses and to the way the control voltages are set (via on-chip resistive divider), rather error prone and easily improvable by a digital control not here included for lack of silicon area.

In order to analyze the full reachable phase and amplitude shift capabilities of the VM, S_{21} is best shown at a specific frequency point. Therefore, the four middle frequencies of IEEE802.11ad (58.32, 60.48, 62.64, 64.80 GHz) standard are used. The results are converted to the complex plane and reported in Fig. 5. Ideally, the figure would show a square. At the higher gain stages some compression can be observed, which leads to denser distribution to the edges. On top of that, the edges themselves show a slightly curved behavior. The figure shows the worst behavior at the highest middle frequency. Still, it is possible to match a circle (shown in red) of −3 dB at all frequencies. The gain settings close to this circle can be used to set a certain phase with only a small amplitude change over the different phase settings. For the lower frequencies this circle can be brought up to about −1 dB.

Fig. 6 illustrates the phase response for a subset of states from Fig. 5, as well as phase and amplitude RMS errors. The target states were the phase shifts of 0°, 90°, 180° and 270°, with a gain of −3 dB. For every middle frequency the best performing available points were chosen. The RMS phase error inside all channels is below 6°, while being below 3° for the lower three channels. The RMS amplitude error is lower than 1.3 dB for the whole bandwidth and 0.5 dB for the lower frequencies.

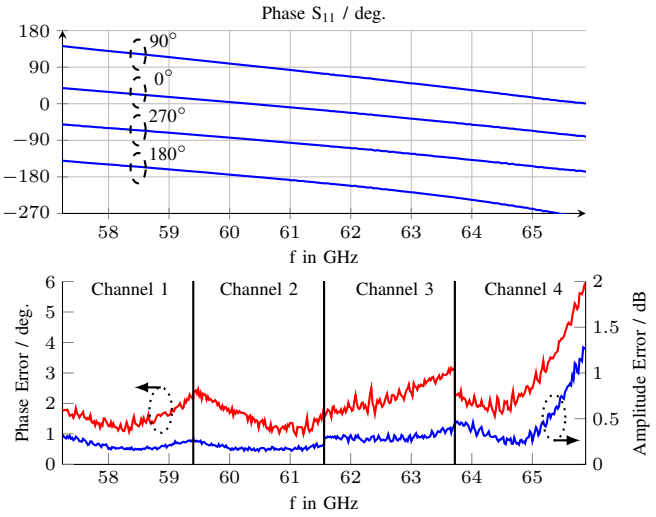

Fig. 6. Top: Phase response for 4 example states (0°,90°,180°,270°) at 60.48 GHz; Bottom: Phase and amplitude errors of the 4 example states, selected at each middle frequency.

B. Large Signal Measurements

The large signal behavior has been tested by sweeping the input power given by the VNA to obtain the 1 dB compression point (P_{1dB}) of the phase shifter. As shown in Fig. 7 the measured input 1dB compression point (IP_{1dB}) is −12 dBm at a frequency of 60.48 GHz and middle gain state $V_{SI} = 65\,\mathrm{mV}$ and $V_{SQ} = 25\,\mathrm{mV}$.

IV. Conclusion

In this paper, a 57-66 GHz band VM IC was designed, manufactured and characterized. Table 2 summarizes and compares the achived performance with the state of the art. A unique approach to the input balun saving space and lowering power consumption for the deployment in scalable multi-antenna systems was used. It was shown that phase shifts between 0° and 360° with gains higher than −3 dB are possible. The control is done by two pairs of control voltages, which can easily be replaced by digital control units for future applications. The circuit shows good linearity up to −12 dBm input power. The overall performance of the prototype is consistent with the simulation and a proof of concept for the novel combined balun/variable gain amplifier (VGA) circuit was provided. This concept showed to be a feasible alternative to the usage of separated input baluns for the current steering VGA. The presented circuit shows to be especially good in regards to its small active chip area and relatively low power consumption, which is advantageous for its usage in scalable antenna array systems.

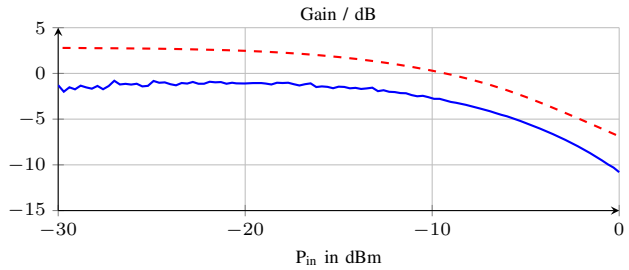

Fig. 7. Simulated and measured gain and phase over input power for $V_{BI} = 65\,\mathrm{mV}$ and $V_{BQ} = 25\,\mathrm{mV}$

Table 2. Performance comparison between this work and the state of the art

Design	**This Work**	[7]	[10]	[8][i]
Technology	**0.13 µm SiGe**	0.25 µm SiGe	90 nm CMOS	55 nm CMOS
Architecture	**VSPS**	VSPS	VSPS	VSPS
Area (mm^2)	**0.48**	0.8	0.66	1.69
P_{DC} (mW)	**45**	105	34	16
f (GHz)	**57-66**	40-50	57-64	55-67
Phase Range (°)	**360**	360	360	360
Phase Steps[ii] (°)	**inf.**	inf.	22.5	6.4
$Gain_{MAX}$ (dB)	**-3**	7.6	-5.5	-4.2
ICP_{1dB} (dBm)	**-12**	N/A	-12	-16
Phase Error (°)	**(<6)**[iii]	N/A	<10.5	<2.5
Amp. Error (dB)	**(<1.3)**[iii]	N/A	<1.2	<0.5

[i] full transeiver [ii] inf.: Infinite / Controlled by continuous voltage
[iii] Dependent on digital controller; here under 10-Bit controlling condition also used for Fig. 5

References

[1] J. S. Herd and M. D. Conway, "The evolution to modern phased array architectures," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 519–529, 2016.

[2] G. D'Amato, G. Avitabile, G. Coviello, and C. Talarico, "DDS-PLL phase shifter architectures for phased arrays: theory and techniques," *IEEE Access*, vol. 7, pp. 19 461–19 470, 2019.

[3] J. Bae and C. Nguyen, "A small-insertion-loss-variation phase shifter with optimized body-floating transistors," in *2015 10th European Microwave Integrated Circuits Conference*. IEEE, 2015, pp. 128–131.

[4] A. S. Nagra and R. A. York, "Distributed analog phase shifters with low insertion loss," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 9, pp. 1705–1711, 1999.

[5] Z. Iskandar, J. Lugo-Alvarez, A. Bautista, E. Pistono, F. Podevin, V. Puyal, A. Siligaris, and P. Ferrari, "A 30–50 GHz reflection-type phase shifter based on slow-wave coupled lines in BiCMOS 55 nm technology," in *2016 11th European Microwave Integrated Circuits Conference*. IEEE, 2016, pp. 484–487.

[6] Y. Itoh, N. Mizuo, and A. Ohta, "An L-band SiGe HBT active vector modulator using lookup tables of the control voltage for high stability and small amplitude/phase errors," in *2015 45th European Microwave Conference*. IEEE, 2015, pp. 1096–1099.

[7] Y. Sun and C. J. Scheytt, "A 360 degree phase shifter for 60 GHz application in SiGe BiCMOS technology," in *IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems, 2009*. IEEE, 2009, pp. 1–4.

[8] F. Hameau, C. Jany, B. Martineau, A. Larie, and E. Mercier, "A highly linear bidirectional phase shifter based on vector modulator for 60GHz applications," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2017, pp. 1707–1710.

[9] Y. Ye, L.-Y. Li, R. Tong, and X.-W. Sun, "A full-360° vector-sum phase shifter with low RMS phase and gain errors for 60 GHz 5-bit application," in *2014 9th European Microwave Integrated Circuits Conference*. IEEE, 2014, pp. 305–308.

[10] J.-C. Wu, J.-C. Kao, J.-J. Kuo, K.-Y. Kao, and K.-Y. Lin, "A 60-GHz single-ended-to-differential vector sum phase shifter in CMOS for phased-array receiver," in *IEEE MTT-S International Microwave Symposium digest (MTT), 2011*. IEEE, 2011, pp. 1–4.