A 220GHz Subharmonic Receiver Front End in a SiGe HBT Technology

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***Abstract*— A monolithic 220-GHz receiver front-end manufactured in an engineering version of an f_T/f_{max} = 280/435-GHz SiGe technology is presented. The front-end consists of a three-stage differential LNA and a subharmonic mixer. A breakout of the 220-GHz LNA provides 15 dB gain and a bandwidth of 28 GHz. The integrated downconverter yields a conversion gain of 16 dB, a 15-dB DSB NF, and a 30-GHz bandwidth when pumped with a 0-dBm, 110-GHz LO signal.**

***Index Terms*— Millimeter wave receivers, MMIC frequency converters, heterojunction bipolar transistors, silicon.**

I. Introduction

Millimeter-wave receivers are used in an increasing number of applications, such as communication, security scanning and imaging, as well as remote sensing. The use of frequencies beyond 200 GHz can improve the resolution of imaging systems, while communication systems can benefit from the larger available bandwidth at higher carrier frequencies. A fully monolithically integrated receiver front-end has been demonstrated at 220 GHz in a III-V technology [1]. Silicon is, however, a viable alternative for circuits operating above 200 GHz. An engineering version of SiGe HBT technology has recently reached an f_{max} of 500 GHz [2] and a similar near-time target is set for commercial SiGe BiCMOS process technologies [3]. In comparison to III-V MMICs, SiGe HBT/BiCMOS-based chips can offer a higher degree of integration, smaller die size, and lower cost in large quantities.

Receivers based on SiGe HBTs have previously been demonstrated up to a frequency of 170 GHz. Examples include a low-noise 160-GHz downconverter [4], as well as completely integrated receivers with LO chains based on VCOs [5] and frequency multipliers [6]. These circuits use downconversion mixers pumped by a fundamental LO signal. On-chip generation of a sufficiently strong LO signal does, however, become increasingly difficult with higher operating frequencies. An alternative is offered by a subharmonic downconversion architecture, where the LO can be generated at half the RF frequency.

A modified Gilbert cell with two stacked mixer cores driven with quadrature LO signals is commonly used as a subharmonic down-converter in bipolar technologies. This combination of two cascaded fundamental-frequency mixers for a two-stage downconversion process does not suffer from the same conversion-gain and noise limitations as harmonic mixers based on higher-order non-linearities. The required quadrature LO signals can be generated by a conventional RC poly-phase network, as demonstrated with the 94-GHz and 122-GHz subharmonic mixers in [7] and [8], respectively. The high insertion loss of the poly-phase network is, however, disadvantageous at higher frequencies where LO power becomes increasingly difficult to generate. The branch-line coupler used for the quadrature LO-generation in a similar 122-GHz subharmonic mixer [9] offers lower insertion loss but at the cost of narrow bandwidth and large area requirements.

In this paper, a 220-GHz three-stage differential LNA is integrated with a subharmonic mixer to form a receiver front-end. A compact -3dB transmission-line coupler, implemented in the back-end metallization, is used to drive the cascaded mixer cores with the required quadrature LO signals. The downconverter is manufactured in an engineering version of a 0.25-μm SiGe BiCMOS technology, which features HBTs with cut-off frequencies of f_T/f_{max} = 280/435 GHz.

II. Subharmonic Down-Conversion Front-End

The downconversion front-end consists of a three-stage LNA and a subharmonic mixer, as shown in Fig. 1. A fully differential architecture is used in both the LNA and the mixer. Hence, the front-end is well suited for on-chip integration with balanced antennas such as folded dipoles.

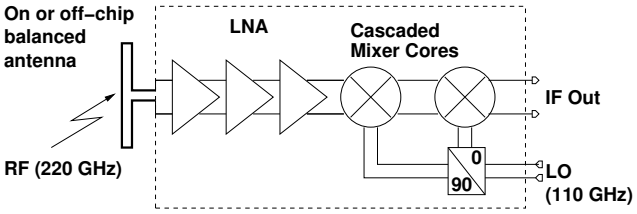

Fig. 1. Block diagram of the monolithically integrated subharmonic receiver front-end. The three-stage 220-GHz LNA is followed by two cascaded mixer cores pumped by quadrature LO signals in order to obtain subharmonic mixing.

A. A 220-GHz Low-Noise Amplifier

The LNA is designed with three cascaded differential cascode stages as shown in Fig. 2. Identical device sizes, bias points and tuning elements are used in all three stages. Each cascode is equipped with four $A_E = 3 \times (0.12 \times 0.96)$-$\mu$m^2 large devices Q1-Q4. This device size was chosen to obtain an optimum noise match to a 2×50-Ω differential source impedance. The HBTs are biased at the maximum-f_t current

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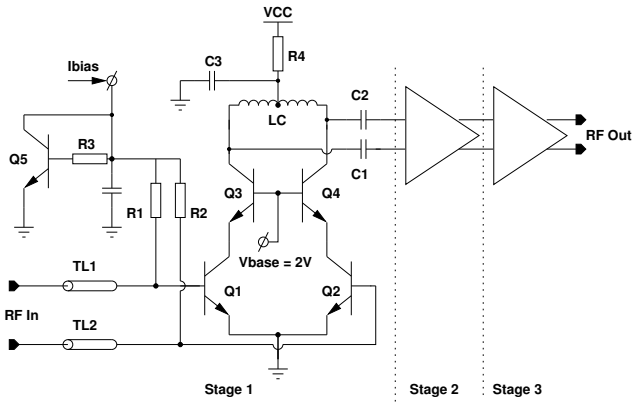

Fig. 2. Circuit schematic showing the first stage of the 220-GHz differential three-stage LNA. The second and third stages are of similar design and tuning.

of 5.4 mA. An LC tank equipped with a single-turn differential inductor and a 14-fF series MIM capacitors is used as the output tuning and biasing network of each stage.

The supply voltage VCC is provided to each amplifier stage through the filter network R4/C3 in order to minimize the risk of instability due to coupling between the stages. Due to the voltage drop in these filters, the VCC is selected to 3.6 V, which yields a total current consumption of 42 mA for the three-stage amplifier.

Preliminary device models of the optimized HBTs available in an engineering version of the SiGe HBT technology were used to simulate the LNA. The simulated gain and noise figure of the LNA at 220 GHz is 14 dB and 13 dB, respectively.

B. Subharmonic Mixer

Figure 3 presents the schematic diagram of the subharmonic mixer. The RF signal from the LNA is applied to the input

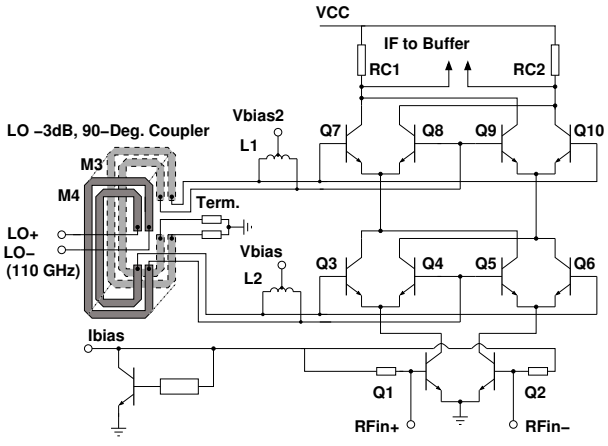

Fig. 3. Simplified schematic diagram of the subharmonic Gilbert-cell mixer. Two stacked mixer quads driven with quadrature LO signals provide subharmonic mixing.

stage Q1/Q2, which drives a differential signal current through the cascaded mixer quads Q3-Q6 and Q7-Q10 to the collector loads RC1/RC2. The two mixer quads are pumped 90-degrees out of phase by a quadrature LO signal in order to obtain subharmonic mixing. Minimum-size transistors ($A_E = 0.12 \times 0.96$-μm^2) are used in the mixer quads in order to minimize the required LO-drive power. The differential IF signal available at the collectors is provided to an emitter-follower output buffer, thus yielding a wide-band IF output capable of dc to 10-GHz operation.

A -3-dB differential 90-deg. coupler is used to generate the quadrature LO signals required for the subharmonic mixing. The coupler is implemented as two coupled quarter-wave long coplanar striplines (CPS) in the adjacent M3/M4 layers of the back-end metallization. In order to reduce the required silicon area, the coupler has been folded into a C-shape. Two differential inductances L1/L2 provide shunt compensation of the LO input capacitance of the mixer devices, as well as a dc-bias path for the base terminals.

The mixer is powered from a 3.6-V supply in order to provide sufficient voltage headroom for three stacked transistors. At this bias level, the current consumption of the mixer is 18 mA, which is dominated by the IF-output emitter followers. The simulated conversion gain of the mixer is 0 dB for a 0-dBm 110-GHz LO signal.

C. Test Benches and Circuit Break-Outs

Although the receiver front-end is intended to be interfaced to a differential antenna, such as a folded dipole, wafer probing at sub-millimeterwave frequencies can only be performed using single-ended probes. For this reason, the breakouts of the differential LNA and the full downconverter have been integrated with on-chip test benches as shown in Fig. 4. Marchand baluns and capacitance-compensated GSG probe

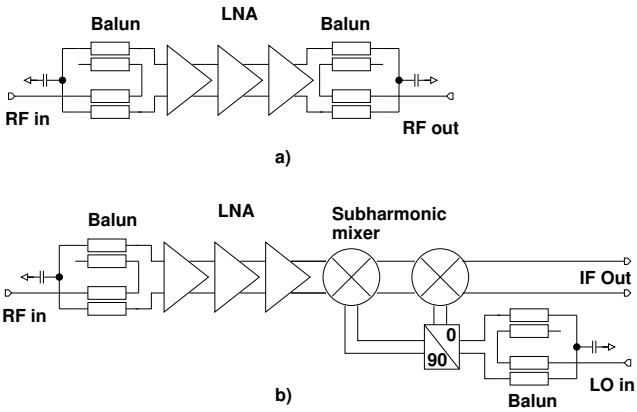

Fig. 4. Breakout of the differential 220-GHz LNA with input and output baluns for wafer probing (a) and the integrated downconverter with compensated pads and Marchand baluns for the 220-GHz RF and 110-GHz LO inputs.

pads [10] are used at the 220-GHz RF terminals, as well as the 110-GHz LO input. The simulated insertion loss of the pad and balun combination is 2 dB at 220 GHz.

III. Technology and Manufacturing

The down-conversion front-end has been manufactured in an engineering version of a 0.25-μm SiGe-BiCMOS process technology provided with an upgraded SiGe HBT module. Compared to the standard technology (SG25H1), the HBTs have been laterally scaled to a minimum emitter area of 0.12x0.96 μm^2. The collector and emitter formation has also been improved. These changes yielded f_T/f_{max} values of 280GHz/435GHz with an open-base emitter-collector breakdown voltage of 1.7V. A further optimized version of this technology with a peak f_T/f_{max} = 300GHz / 500GHz is presented in [2].

The micrograph of the manufactured 1.1×0.6-mm^2 large front-end chip is shown in Fig. 5. The largest part of the die is

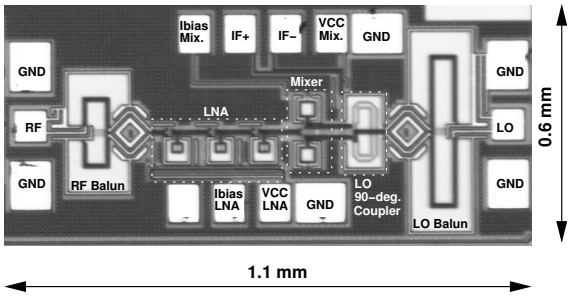

Fig. 5. Micrograph of the 0.7-mm^2 large integrated downconverter die.

occupied by the pad frame and the RF/LO input baluns, while the downconverter core only requires an area of 0.5×0.2-mm^2.

IV. Characterization Setup

The LNA S-parameters were measured with a network analyzer equipped with WR-03 frequency-extender modules and waveguide wafer probes. SOLT calibration was performed using a millimeter-wave calibration substrate.

Figure 6 presents the measurement setup used for the characterization of the conversion gain and noise of the integrated receiver front-end. The RF input power from a sub-

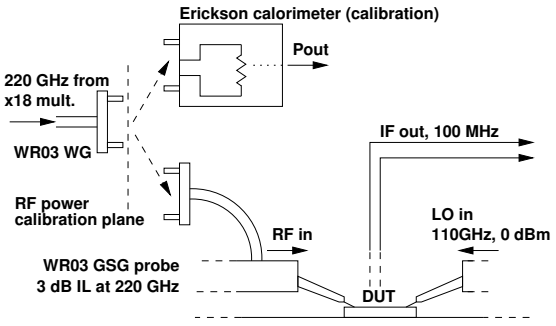

Fig. 6. Integrated downconverter conversion-gain measurement setup.

millimeterwave multiplier chain was calibrated at the wafer-probe wave-guide interface using an Erickson calorimeter. This calibration was performed over the 190 to 240-GHz frequency range, and yielded a measured input power of -28 dBm at 220 GHz. The insertion loss of the 220-GHz wafer probe was calculated from return-loss measurements of impedance standards and found to be 3 dB.

The 110-GHz LO drive to the mixer is provided by a synthesizer-driven x6 frequency multiplier feeding the integrated mixer through a coaxial W-band probe. An LO drive power of 0 dBm is obtained at the pads of the DUT.

An external balun was used to combine the 100-MHz differential IF outputs to a single ended signal. The 100-MHz IF frequency and surrounding noise floor was monitored with a spectrum analyzer. Due to the lack of a 220-GHz noise source, the noise figure of the receiver front-end is calculated from the measured conversion gain and output noise floor.

V. Results

The measured and simulated gain of the three-stage LNA breakout is shown in Fig. 7. Relatively good agreement

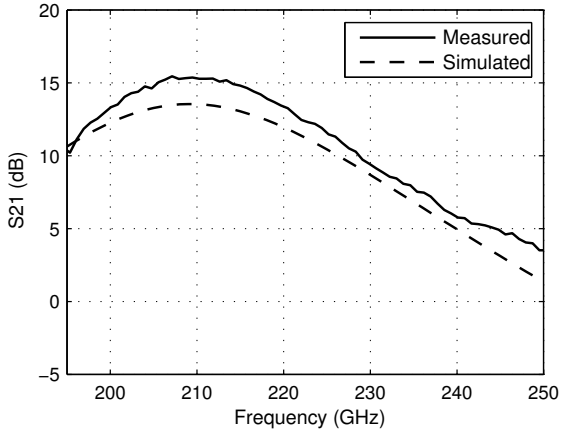

Fig. 7. Measured (solid line) and simulated (dashed line) gain of the three-stage differential LNA including pads and input and output baluns.

between measured and simulated gain is obtained over the complete 195 to 250-GHz frequency range. The 2-dB higher gain in the measurement compared to the simulation at the 210-GHz peak gain frequency can be explained by the use of preliminary device models in the simulations, as well as minor shifts in the biasing conditions.

Figure 8 presents the measured conversion gain and noise floor of the integrated receiver front-end. At the 220-GHz operating frequency, a 16-dB conversion gain and a -140-dBm/Hz output noise floor is obtained. This corresponds to a 18-dB single-side-band (SSB) NF or a 15-dB DSB NF, since both side bands lie within the LNA bandwidth. The measured NF is in good agreement with the simulated 13-dB NF of the LNA and the estimated 2-dB losses of the auxiliary on-chip RF balun and impedance-compensated pad.

The measured current consumption is 20 mA for the mixer and 40 mA for the LNA from a 3.6-V supply.

TABLE I
COMPARISON OF MONOLITHICALLY INTEGRATED RECEIVERS ABOVE 150 GHZ

Technology [μm]	Integration Level [circuit blocks]	BW[1]/Freq. [GHz]	LO Input [GHz]	Conv. Gain [dB]	NF [dB]	Reference
III/V-based						
0.1-μm mHEMT	Ant., LNA, Mixer	208-224	109	2	8.4	[1]
0.1-μm mHEMT	Ant., LNA, Mixer, LO-Chain	212-224	55	3.5	7.4	[11]
Silicon-based						
0.13-μm SiGe HBT	LNA, Mixer, VCO	160-175	Int. VCO	-5	21	[5]
0.13-μm SiGe HBT	LNA, IQ-Mixer, LO-Chain	158-165	18	25 / 27[2]	11 / 9[2]	[6]
0.13-μm SiGe HBT	LNA, Mixer	155-161	160	27 / 29[2]	9.5 / 7.5[2]	[4]
0.13-μm SiGe HBT	LNA, Mixer	202-230	110	16 / 18[2]	15[3] / 13[2,3]	This Work

[1]3-dB bandwidth.
[2]Excluding the 2-dB auxiliary input balun losses.
[3]Estimated from conv. gain and output noise.

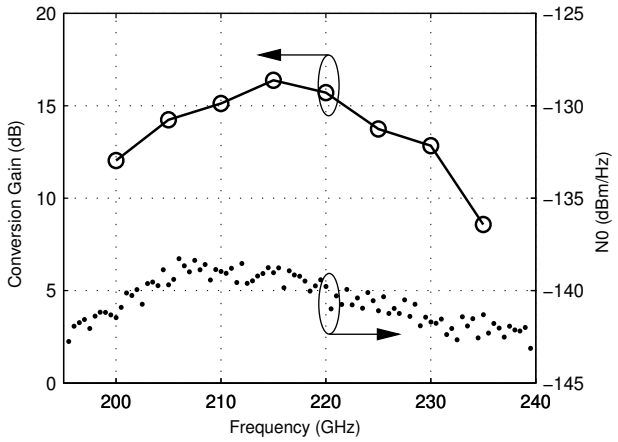

Fig. 8. Measured conversion gain and output noise floor including the 2-dB losses of the on-chip auxiliary balun in front of the LNA.

VI. CONCLUSION

A 220-GHz integrated receiver front-end has been demonstrated in a SiGe HBT technology. The use of subharmonic downconversion facilitates the generation of the LO-drive signal and can also help simplify the LO distribution in a multi-channel array configuration. As shown in Table I, the demonstrated 16-dB conversion gain is higher than the gain obtained with a similar circuits in a III-V technology. The comparatively high noise figure of 15 dB is partly caused by the use of an integrated RF balun at the receiver input. An 18-dB conversion gain and 13-dB NF should be obtainable in the intended configuration with a differential input signal from an on-chip antenna. The use of a further optimized device technology and circuit design is also expected to yield a reduced NF and improved conversion gain.

VII. ACKNOWLEDGMENT

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