A High Linearity 6 GHz LNA in 130 nm SiGe Technology

A. Bahadir Ozdol[#], Hamza Kandis[#], Abdurrahman Burak[#], T. Alper Ozkan[#], Mehmet Kaynak[*], Yasar Gurbuz[#]

[#]Faculty of Engineering and Natural Sciences, Sabanci University, Orhanli, Tuzla, 34956, Istanbul, Turkey

[*]IHP Microelectronics, Im Technologiepark, 25, 15236, Frankfurt (Oder), Germany

yasar@sabanciuniv.edu

***Abstract* — In this work, a high linearity LNA at 6 GHz with 1.15 dB NF, 27.7 dB gain is reported with IHP 130nm SiGe BiCMOS technology. The reported LNA achieves a highly linear performance and has -12.2 dBm IP1dB and 4.2 dBm IIP3. A two-stage cascode amplifier with inductive degeneration topology is used to obtain high gain. Optimum transistor biasing and sizing achieves an input matching without using any inductor which allowed low NF and high linearity. Additionally, custom, not PDK defined, transistor layouts have been created to decrease the core's parasitics to enhance the LNA's performance. LNA uses 3.3V as supply and consumes 98 mW DC power while occupying a 0.75 mm^2 die area without pads. The reported LNA achieved one of the highest figures-of-merit among silicon-based LNAs and has comparable performance to SOI CMOS LNAs.**

***Keywords* — Cascode, HBT, high linearity, IIP3, IP1dB, low noise amplifier, NF, WLAN.**

I. Introduction

Sub-6 GHz WLAN applications have pushed for higher data rate requirements with each new generation. The demand for increased data rates has not only increased expectations on the noise performance of low noise amplifiers but also created a demand for increased communication distances which have attracted attention to massive multiple-input-multiple-output (MIMO) systems [1]. MIMO systems have introduced a new challenge for modern receiver chains, an increased linearity requirement since a stronger interferer resistance is required with each new channel in the sub-6 GHz region.

In receiver systems, a low noise figure (NF) is one of the most determinative specifications for a high data rate and maximizing the range of communication. Since the LNA mainly dominates the noise figure of a receiver system, many modern receiver systems require an LNA with very low NF and high gain. Moreover, high gain increases the maximum communication distance, which is valuable for MIMO systems. Also, LNAs with high linearity are crucial if the signal detection range is significantly large and interferers are present.

The high gain of an LNA is a vital parameter to allow the LNA to dominate the NF of the receiver chain. For this purpose, 130nm SiGe BiCMOS technology was used in this work due to higher trans-conductance at the same DC current and higher f_T of HBTs [2].

Recently, several silicon-based sub-6 GHz LNAs have been published [3], [4], [5], [6], [7], [8], [9]. Narrow-band SOI LNAs [4], [6], [7] demonstrated very good NF performances and reported the state-of-the-art NF value of 0.6 dB. Moreover, CMOS LNAs [8] with low NF have also been reported, but these LNAs' OIP3 and OP1dB can be limiting factors in receiver front-ends with high dynamic range requirements. Additionally, reported SiGe LNAs [5] and [9] have lacked low noise figure performance and have been unable to achieve NF values lower than 2 dB. Previous works have shown that there is a lack of very highly linear, low NF LNA in the literature.

A very highly linear 6 GHz 2-stage cascode LNA with 1.15 dB NF, 27.7 dB gain, 4.2 dBm IIP3, and -12.2 dBm IP1dB is presented in this work. LNA was matched between 5.8 GHz and 9.8 GHz. LNA draws 29.7 mA from a 3.3V supply.

In Section II of this paper, the design steps of the reported LNA are described, and in the later section, measurement results of the LNA are shown. Finally, Section IV concludes this work.

II. The Design Of The LNA

A. Input Matching

Instead of using the conventional simultaneous power and noise matching method, the number of transistors of the common-emitter device of the first cascode stage is selected to enable input matching without using an inductor in the input matching network. For inductively degenerated cascode amplifiers, the input impedance can be matched to 50 ohms by carefully selecting the L_e and the number of transistors of the common-emitter device at the first stage of the amplifier. The main reason for this approach is eliminating the inductors in the input matching network because of their lossy and noisy behavior that arises from their parasitic resistances. Since simultaneous power and noise matching is not achieved in this approach, the difference between the NF and the NF_{min} is significantly higher with respect to the conventional technique. However, this method improves NF and obtains a lower NF than the conventional noise matching method. The NF difference between these two approaches is around 0.1 dB at 6 GHz and this gap widens as operating frequency increases. The comparison between the conventional and the modified method can be seen in Fig. 1. In both matching methods, inductors with the same Q-factors are used on the schematic level simulation.

B. Cascode Amplifier

The schematic of the LNA is shown in Fig. 2. Both stages of the LNA are designed in cascode topology and cascode

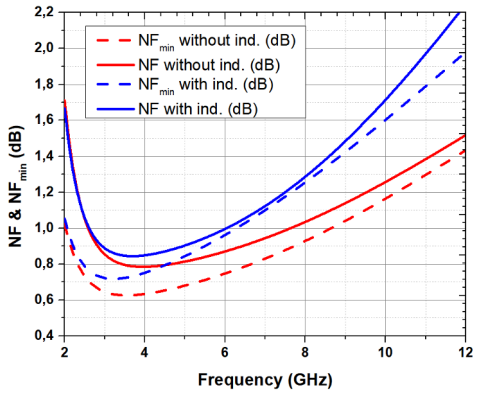


Fig. 1. NF & NF_{min} for different input matching methods.

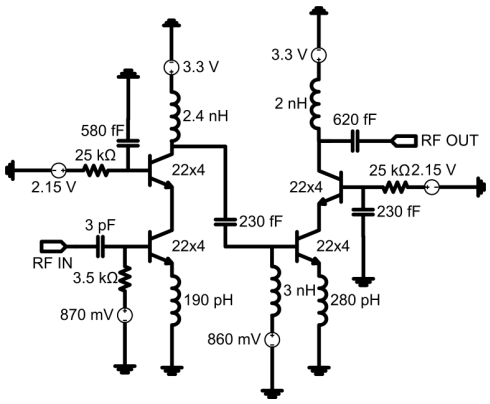


Fig. 2. Schematic of the reported LNA.

amplifier topology introduces high isolation between its output and input, which enables input matching with negligible effects from the output. For the second cascode stage, a higher inductively degeneration is used to increase its linearity since the overall amplifier's linearity is mainly dominated by the second stage.

At the base node of both common-base transistors, relatively low shunt capacitors are used, and base bias is applied over a highly resistive resistor. This method is applied to see significant impedance from the base node of these transistors instead of creating RF shorts at those nodes. The main aim of the method is to create a voltage swing at the base of these transistors to increase linearity [10]. The effect of the selected capacitance on IIP3 performance of the amplifier can be seen in Fig. 3. Decreasing the capacitance at the base node increases IIP3 monotonously, but as the capacitance decrease, S_{21} also decreases, making the base node's capacitance selection a trade-off between S_{21} and IIP3. Therefore, for an optimum and balanced design, a maximum S_{21} and IIP3 product (OIP3) should be considered during capacitance selection. For the second-stage, OIP3 is maximized when the mentioned capacitance is selected as 230 fF.

Inter-stage and output matching is done by using conventional methods by using shunt inductors and series capacitors which are also used for DC feeding and blocking

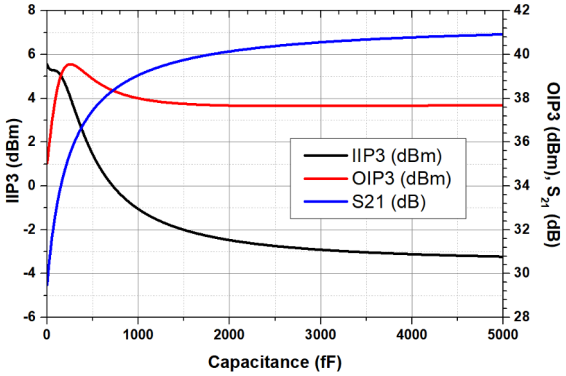
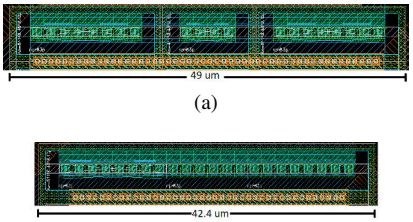


Fig. 3. IIP3 vs. capacitance characteristic.



(a)

(b)

Fig. 4. (a) Pre-layout optimization, (b) Post-layout optimization without an LVS and DRC violation.

purposes.

C. *Layout Optimization*

HBTs in the IHP 130 nm SiGe BiCMOS technology have a restriction for a maximum number of transistors of eight in a single active region. If more than eight transistors were used in a single device, there should be spacing between these groups of transistors seen in Fig. 4. Since restriction of the number of the transistors would lead to a bigger active area and longer metal lines, NF would have increased due to increased parasitic capacitance and resistance. The mentioned restriction is avoided by redrawing active areas to create transistor groups larger than eight transistors to prevent this NF increase. In this work, all devices have 88 transistors, and 22 transistors are used per active region row for each device for an optimal layout. Core layout optimization can be seen in Fig. 4. Since the base signal is applied from the left side, transistors at the right side see more resistance with respect to closer transistors in the pre-optimization case. In the post-optimization case, these transistors see less parasitic resistance and capacitance due to decreased distance, which decreases the NF. Change in the NF is shown in Fig. 5. At 6 GHz, simulated NF is decreased by 0.05 dB. Although the NF difference may not be significant, there is no cost for the core layout optimization, and the optimization also decreases the core area, and it is applicable to other works with the same technology.

III. Measurement Results

This work is sent for tape-out and fabricated in IHP 130 nm SiGe BiCMOS technology. The chip photograph of the reported LNA is shown in Fig. 6. The chip area without pads

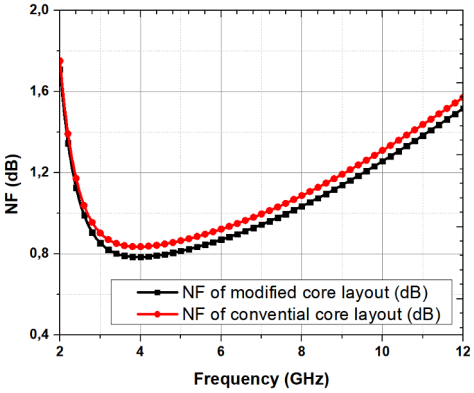


Fig. 5. NF of conventional and modified transistor of the used technology.

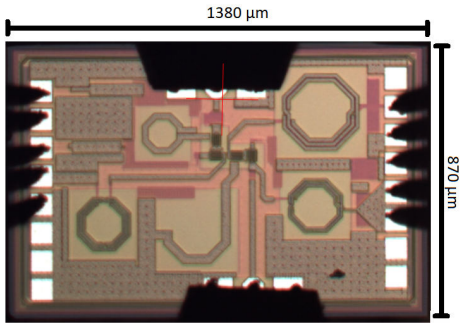


Fig. 6. Chip photo of the two-stage cascode LNA. Total die area is 1.2 mm^2 with pads. The area without pads is 0.75 mm^2.

is 0.75 mm^2. The S-parameters are measured from 3 GHz to 10 GHz with Cascade Microtech 40 GHz GSG probes by using Keysight N5224A PNA. Noise figure measurement is conducted for the 4-10 GHz region by using Keysight E4448A PSA and 346A noise source. OIP3 and OP1dB performances of the LNA are measured from 4 GHz to 7 GHz by using Keysight E8257D PSG and E4448A PSA.

S_{11} and S_{22} measurement results are shown in Fig. 7, and input and output matchings are better than -10 dB between 5.8-9.8 GHz. The measurement result of the output matching was similar to its simulation result. On the other hand, a frequency shift has been observed at the input side. Input matching's lower frequency limit had been shifted from 5 GHz to 5.8 GHz, which is addressed to the input pad's parasitic capacitance. The measured small-signal gain (S_{21}) has reached 34 dB at 4 GHz and was recorded as 27.7 dB at 6 GHz, as shown in Fig. 8.

The noise figure reached its lowest value, 1.05 dB at 4 GHz, and measured as 1.15 dB at 6 GHz. NF is smaller than 2 dB for the matched frequency region. However, an NF increase has been observed at the low-frequency region due to the input matching shift between 4-6 GHz. The NF measurement result can be seen in Fig. 9.

OIP3 measurement is done by applying two tones centered around the center frequency and the frequency spacing between the tones was selected as 10 MHz. OIP3 was measured as 31.9 dBm at 6 GHz and reached its highest value of 33 dBm at 5

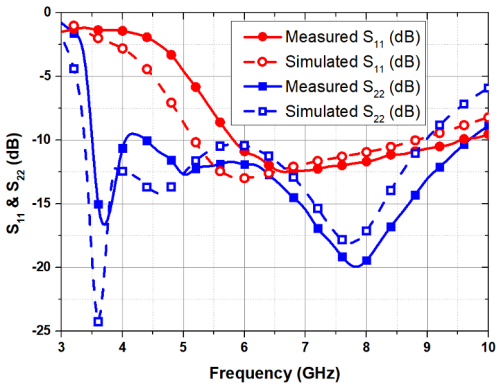


Fig. 7. Measured S_{11} & S_{22} of the LNA.

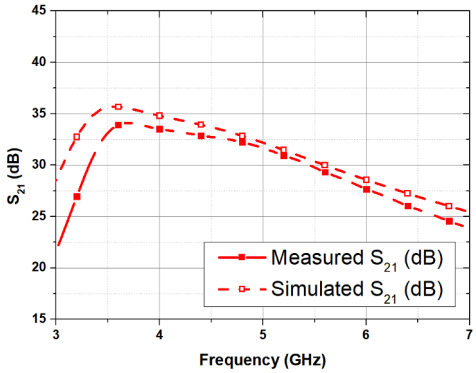


Fig. 8. Measured S_{21} of the LNA.

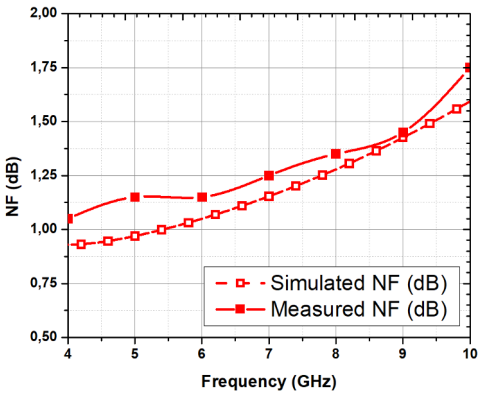


Fig. 9. Noise figure result of the LNA.

GHz. Thus, the measurement result ensures a highly linear operation. Finally, the OP1dB was measured as 14.5 dBm at 6 GHz, which is a very high OP1dB value for LNAs, and it is characterized with the SiGe BiCMOS cascode amplifiers. Linearity measurement results are shown in Fig. 10.

Moreover, the reported LNA performed stable operation and no oscillation was observed when the LNA's output is analyzed with the spectrum analyzer.

Measurement results of this work are summarized in Table 1 and compared with the other state-of-the-art silicon-based LNAs. Two different figures-of-merits are used for comparison. FoM_1 compares gain IIP3, f_c, NF, and DC

Table 1. Comparison of State-of-the-art LNAs.

Reference	**This Work**	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Technology	**130nm SiGe**	65nm CMOS	130nm SOI	250nm SiGe	180nm SOI	130nm SOI	180nm CMOS	180nm SiGe
Freq (GHz)	**6**	5.8	5.2	5	5	5.8	5.2	5.8
NF (dB)	**1.15**	1.9	0.6	2.2	0.95	1.34	1.1	2
Gain (dB)	**27.7**	30	10.4	12.8	11	9	16.5	18.8
IIP3 (dBm)	**4.2**	-10.3	12	11.6	5	12.7	-4	-6
IP1dB (dBm)	**-12.2**	-21.6	N/A	-6.2	-7	-2	-19.9	-14.5
Area (mm^2)	**0.75**	0.03	0.6	N/A	0.29	0.85	0.22	0.72
P_{DC} (mW)	**98**	16	10	23.8	12	9.6	12.4	32.4
FoM_1 (GHz)	**312.78**	61.64	609.95	87.84	67.84	251.5	25.87	5.83
FoM_2 (GHz)	**7.17**	4.57	-	1.46	4.28	8.52	0.66	0.82

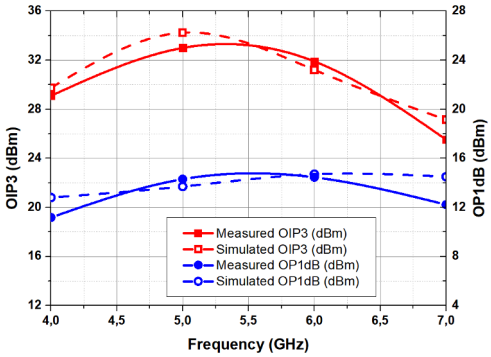


Fig. 10. OIP3 and OP1dB measurement results of the LNA.

power consumption [3].

$$FoM_1 = \frac{Gain[abs] \times IIP3[mW] \times f_c[GHz]}{(F-1)[abs] \times P_{DC}[mW]}. \quad (1)$$

while FoM_2 compares gain, IP1dB, f_c, NF, and DC power consumption [11].

$$FoM_2 = \frac{Gain[abs] \times IP1dB[mW] \times f_c[GHz]}{(F-1)[abs] \times P_{DC}[mW]}. \quad (2)$$

This work achieves one of the highest figures-of-merit, and lowest NF with respect to state-of-the-art SiGe BiCMOS LNAs and has one of the highest figure-of-merits compared to state-of-the-art Si-based LNAs.

IV. Conclusion

In this work, a 6 GHz two-stage cascode LNA is reported that is fabricated in IHP 130nm SiGe BiCMOS technology. This work shows that the SiGe BiCMOS technology offers very high gain LNAs without significantly sacrificing the noise performance due to the high trans-conductance, and high f_T values of the HBTs of this technology. Additionally, custom-drawn transistors and inductorless input matching technique are used to improve the NF performance furthermore. Moreover, common-base devices' base node capacitances are selected to enhance the OIP3 and OP1dB performances of the reported LNA. HBTs in this technology achieve a very highly linear performance in both OP1dB and OIP3 parameters. The reported LNA has an NF value of 1.15 dB at 6 GHz with a small-signal gain (S_{21}) of 27.7 dB. The measured OP1dB is 14.5 dBm, and OIP3 is recorded as 31.9 dBm.

Acknowledgments

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