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Ultra-Wideband Frequency Doubler with Differential Outputs in SiGe BiCMOS

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***Abstract*—We present an ultra wideband push-push based frequency doubler with differential outputs and a 3 dB-bandwidth from 4.8 to 80 GHz. The maximum conversion gain is 1.7 dB at 25 GHz and -13 dBm input signal. An on-chip active balun provides the differential drive signal enabling a good fundamental rejection over a wide bandwidth. Measurements up to 100 GHz verify the circuits functionality. The output bandwidth of 75 GHz combined with less than 3 dB output power variation exceeds the results of previous publications with differential outputs.**

***Index Terms*—Silicon Germanium, BiCMOS integrated circuits, Multiplying Circuits**

I. Introduction

For test and measurement applications or emerging millimeter wave systems like software defined radio, frequency sources and multipliers covering a wide frequency range are required [1]. VCOs as frequency sources for millimeter wave applications suffer from high phase noise and low tunability. A commonly used solution is generating signals at lower frequencies and multiplying their outputs, for example by one or multiple frequency multipliers [2]–[4]. There are multiple solutions like using a single transistor, self mixing with Gilbert cell-based multipliers [5] or a push-push transistor pair [6]. For millimeter wave systems, differential signal sources are important due to many building blocks operating as differential circuits. Therefore, we present a modified push-push frequency doubler to generate differential outputs without the use of a post-doubler balun, the doubler is operational across a very wide bandwidth from 4.8 to 80 GHz output frequency. With synthesizers this enables flexible and ultra wideband signal generation [7].

II. Circuit Design

A. Active Balun

To drive the frequency doubler and provide a well balanced wideband differential signal, an active balun was integrated on chip. Passive baluns require a large area and offer only limited bandwidth [3]. Fig. 2 on the left side shows a simplified schematic of the used active balun topology. The circuit itself is a classical single transistor balun with $R_{\mathrm{E,B}} = R_{\mathrm{C,B}}$. Special care has to be taken to keep amplitude and phase balance with increasing frequency, since any error in the differential signal will translate into fundamental leakage at the doubler's output. Single transistor baluns introduce quite large errors at frequencies higher than 10 GHz. Therefore, C_{E} is used to tune the phase and amplitude response in a first step, as can be seen in Fig. 1. Increasing this capacitance helps to keep the phase difference between the collector and emitter tap close to 180°. However, this acts as a peaking capacitor for the signal tapped at the collector, while being a low pass filter for the signal at the emitter. As a result the amplitude balance degrades drastically. As a trade-off with the focus on a better phase response C_{E} was chosen to be 15 fF. However, the response still shows a deviation from the desired differential signal. A second correction step is introduced with a fully differential amplifier following the balun stage. This stage uses a degenerated current mirror for common mode suppression.

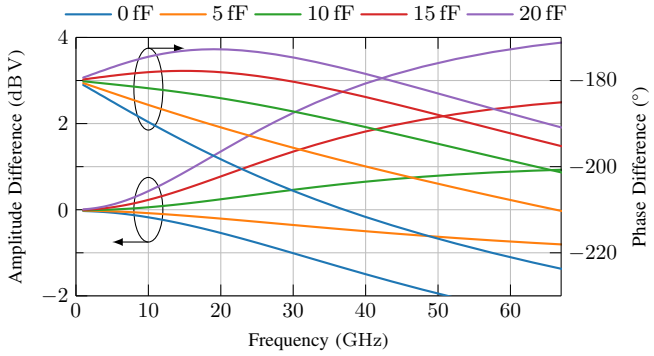


Fig. 1: Phase difference at collector and emitter of the balun's input transistor for different values for C_{E}.

B. Push-Push Doubler

As a frequency doubler a push-push configuration of two npn HBTs is used. In Fig. 2 the simplified circuit diagram of the push-push doubler stage is shown. The transistors are biased close to Class-B and so the circuit is operating as a rectifier. A differential signal at its input then generates a total current through the transistor pair with the main frequency component of $2f_{\mathrm{in}}$. Usually a single ended signal with $2f_{\mathrm{in}}$ is then taken from the collector [6], [8], [9]. The fundamental frequency is suppressed by the subtraction if the inputs are differential. However, depending on the balance of the input signal, it's power, circuit parasitics and non-idealities a certain amount of the fundamental frequency is still present at the output. Filtering of the fundamental frequency can be achieved by optimizing the output matching network for $2f_{\mathrm{in}}$ or high-

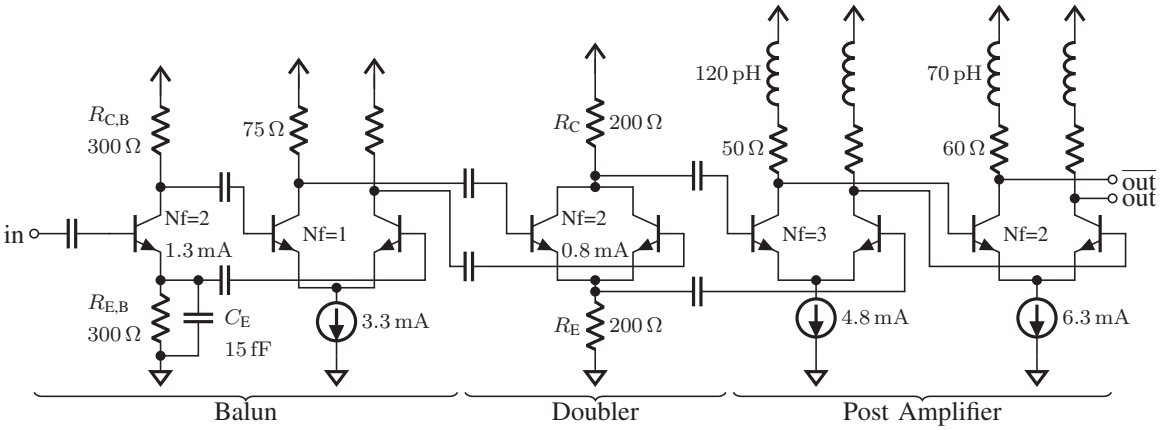


Fig. 2: Simplified circuit diagram of proposed doubler with balun and post amplifier. The emitter area is defined as the number of fingers (Nf) with 900 nm x 70 nm each. The supply voltage for all stages is 1.8 V.

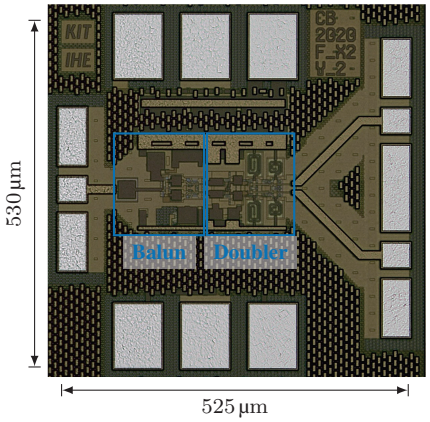
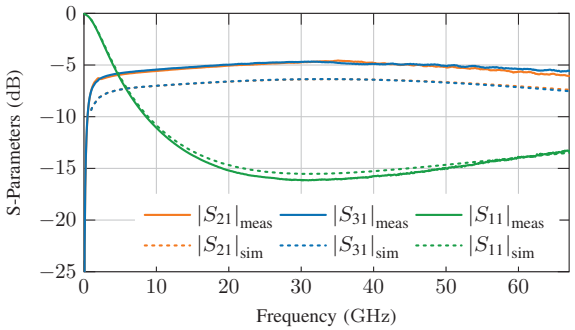
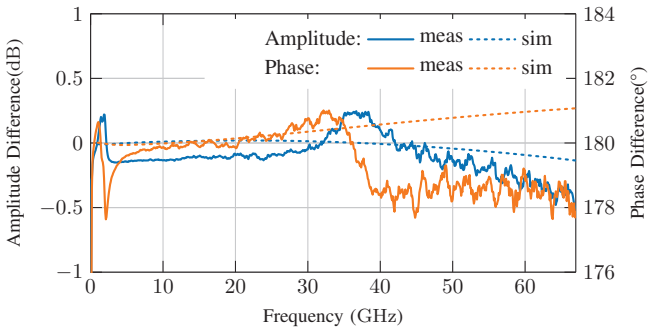


Fig. 3: Photograph of the Chip. Total area: $0.278\,\mathrm{mm}^2$. Core area (balun and doubler): 280 µm x 125 µm = $0.035\,\mathrm{mm}^2$.



(a) S-parameters for active balun alone.



(b) Phase and Amplitude Imbalance.

Fig. 4: Balun small signal measurement response.

pass filters. Since we target a broadband operation this is not an option for this design, hence the integrated balun is optimized for the best possible differential symmetry. Here we use load resistors on both sides of the coupled npn pair to generate a differential voltage. Due to a lack of 2nd harmonic reflectors because of their limited bandwidth and other techniques (e.g. cascode [10]) to increase conversion gain the doubling stage itself has a low conversion gain. Therefore, a two stage fully differential amplification chain is used to boost the output signal. The amplifiers are optimized for a wide bandwidth and therefore only boost the conversion gain to around 1 dB. Fig. 3 shows a photograph of the chip with balun and doubler. The total area is $0.278\,\mathrm{mm}^2$, while the active circuit core only accounts for $0.035\,\mathrm{mm}^2$. It was fabricated in IHP's SG13G2 BiCMOS technology including npn HBTs with $f_T = 350\,\mathrm{GHz}$ and $f_{max} = 450\,\mathrm{GHz}$.

III. Measurement Results

A breakout circuit of the balun is measured independently. It is tested with an on-wafer measurement system and 3-port S-parameter setup. Fig.4 shows the results for this balun. Since the input is DC-Blocked S_{11} is greater than $-10\,\mathrm{dB}$ below 8 GHz but for higher frequencies S_{11} shows a good match. The amplitude and phase balance is very good with an amplitude mismatch below 0.5 dB and a phase mismatch below ±2° in the frequency range from 2.4 to 67 GHz. The balun itself consumes 11.3 mW DC-power. The gain of the balun is low, since it is not designed for a 50 Ω load at the output, as it was the case during this measurement. Apart from having a

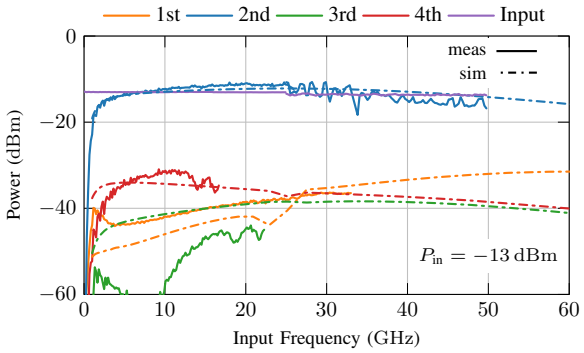


Fig. 5: Output harmonics at $P_{in} = -13\,\mathrm{dBm}$.

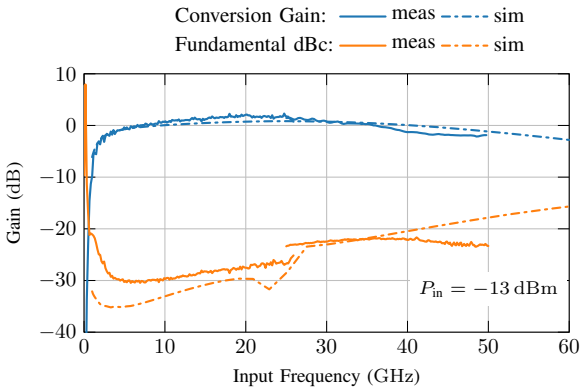
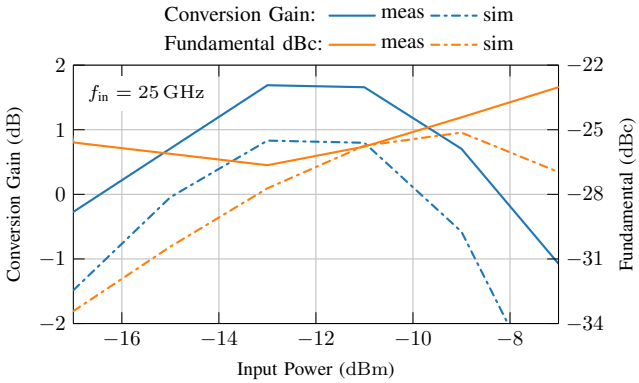
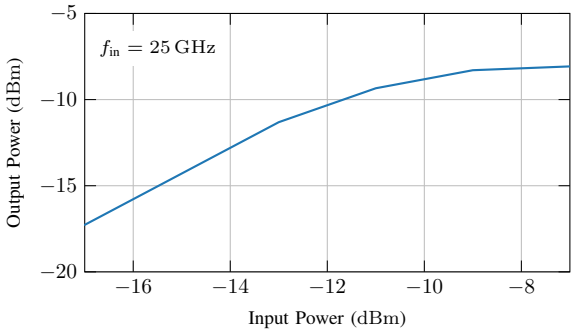


Fig. 6: Conversion gain and fundamental leakage at $P_{in} = -13\,\mathrm{dBm}$.



(a)



(b)

Fig. 7: (a) Conversion gain and fundamental power with respect to the 2nd harmonic versus input power and (b) 2nd harmonic output power versus input power at $f_{in} = 25\,\mathrm{GHz}$.

slightly higher gain, the measurement and simulation fit very well and show the capability of this simple balun structure. The doubler with integrated balun is also measured with an on-wafer measurement setup. For measurements up to 50 GHz output frequency a Keysight N5247B VNA is used to measure the harmonics up to the 4th harmonic and to generate the input signal. Two ports are used as a differential receiver with calibration up to the measurement probe tips. Therefore, there is no need for external baluns to measure a differential response, which in turn would introduce measurement uncertainties. For output frequencies above 50 GHz a broadband frequency extender was used to measure the output power single ended. 3 dB was added to the measured power to account for the differential result. Fig. 5 shows the measured and simulated harmonic power with respect to the input frequency. There is a strong ripple on the measured power on the output above 50 GHz which is due to calibration difficulties for absolute power measurements in our system. Fig. 6 shows conversion gain and fundamental rejection. The results agree with simulated values. The simulated conversion gain 3 dB-bandwidth is from 2.4 GHz to 56.4 GHz with respect to the input frequency. While in measurement the upper limit is at 40 GHz input frequency. However, due to probe losses not being accounted for in the power calibration this value is slightly underestimated. Fig. 7 presents conversion gain and fundamental rejection at $f_{in} = 25\,\mathrm{GHz}$ as a function of input power. These results also match the simulated response. The total DC power consumption is 39.6 mW from a 1.8 V supply including 11.3 mW for the balun and 25.1 mW for the differential post amplifiers.

IV. Conclusion

We present a broadband frequency doubler based on the push-push topology with differential outputs. To drive the doubler and to establish a well defined phase relation between the doubler's input signal, an active balun was integrated on chip. It has a measured peak conversion gain of 1.7 dB with an input power of $-13\,\mathrm{dBm}$ at $f_{in} = 25\,\mathrm{GHz}$ while providing over 20 dB of fundamental rejection. The balun and doubler use a compact design without large passive structures and hence require only $0.035\,\mathrm{mm}^2$ for the active circuit area. The doubler has a measured 3 dB-bandwidth of at least 75 GHz, with a good match between simulation and measurement. Tab. I presents an overview of similar publications for broadband doublers and doublers with differential outputs. Our frequency doubler shows the highest conversion gain 3 dB bandwidth for differential output circuits.

TABLE I: Comparison of wideband frequency doubler circuits.

	Technology	Topology	Output	BW[a] (GHz)	peak CG (dB)	Fundamental rejection (dB)	P_{DC} (mW)
[11]	InP DHBT	Gilbert cell	single ended	$\mathrm{DC}-86$	-0.25		730
[3]	$0.18\,\mu\mathrm{m}$ CMOS	push-push	single ended	$15-36$	-10	33	$4-11$
[5]	$0.18\,\mu\mathrm{m}$ SiGe	Gilbert cell	differential	$36-80$	10.2	20	137
[12]	$0.18\,\mu\mathrm{m}$ SiGe	Gilbert cell	differential	37 @120 GHz	3	21	69
[8]	130 nm SiGe	push-push	differential[b]	$55.6-66.5$	-15	42	23.5
This work	130 nm SiGe	push-push	differential	$5-80$	1.7	18.5	39.6

[a] Conversion Gain 3 dB bandwidth, [b] two doublers with polyphase filter

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