A Ku-band Low Noise Amplifier Design in 0.13-um SiGe BiCMOS Technology

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***Abstract*—a Ku-band monolithic low noise amplifier (LNA) is presented in this paper, which is fabricated in commercial 0.13-um SiGe BiCMOS technology. An inductively degenerated cascode topology combined with small resistance in series at base of HBT transistor are used to improve the noise figure and stability. The results show that this single-stage LNA achieves 3.2 dB minimum noise figure at 16.4 GHz and a highest power gain of 15 dB at 16 GHz with a 3-dB bandwidth from 14 to 18.3 GHz. The total area of this LNA is 720×580 um^2 including pads.**

I. Introduction

With the rapid development of the wireless communication and radar, the operating frequency is moving toward higher frequency range for high data rate communication system. It has attracted some research on Ku-band applications such as satellite communications and phased array systems. Due to the inherent radio frequency advantages of III/V semiconductor ,traditional radio frequency integrated circuit design is usually produced by processes such as GaAs and InP. However, because of the restriction of high cost and incompatibility with traditional silicon-based integrated circuit technology, people began to seek for BiCMOS/CMOS technology which is cheaper and compatible[1].

As the first stage of the wireless communication front-end , LNA with lower noise is crucial to the performance of the receive system. Most previous Ku-band LNAs were implemented in GaAs process. In recent years, as the scale of transistors has decreased, transistors have been able to operate higher f_t and f_{max} of 200-300 GHz, as well as improve noise performance. So it is possible to realize the implementation of Ku-band LNA based on BiCMOS/CMOS technology[2]-[4].

A single-stage cascode Ku-band LNA using standard commercial 0.13-um SiGe BiCMOS technology (f_t/f_{max}=200/250 GHz) is demonstrated in this paper. In order to achieve the optimal noise and the conjugate match of input impedance simultaneously, an inductively degenerated cascode topology is adopted. The potential instability of cascode structure is analyzed , and the small resistance is in series at the base of the cascode transistor to maintain the stability. Besides, the layout of the transistor is symmetrical, minimizing contact resistance and introduced parasites.

II. LNA Design

A. 0.13-um SiGe BiCMOS Technology

0.13-um SiGe BiCMOS technology is adopted. The technology mainly consists of seven layers of metal (M1-M7), and the top two thick layers are 4-um M7 layer and 1.42-um M6 layer, which is illustrated in Fig.1. In addition to the above seven layers of metal, the technology also provides the QY layer, which is only used to form the Metal-Insulator-Metal (MIM) capacitance with the M6 layer. Inductance and metal interconnect wires are realized through top metal for reducing routing loss and parasitism. To achieve sufficient power and ground contact, M7-M6-M5-M4 is applied to VDD-GND-VDD-GND.

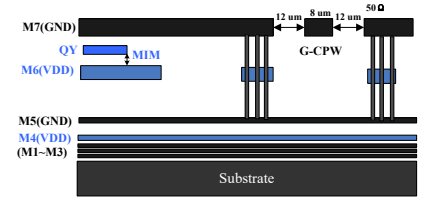

Fig.1. 0.13-um SiGe BiCMOS technology

B. LNA Circuit

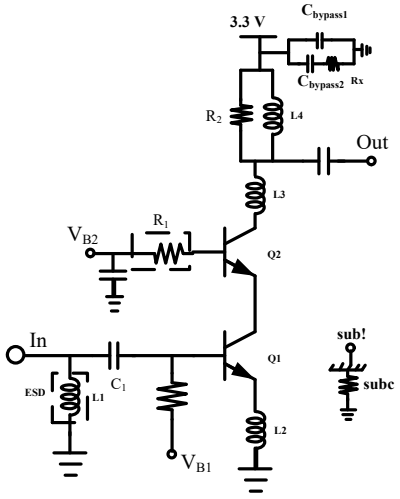

Fig.2. Topology of The LNA

The typical topology of the HBT LNA, which is cascode with the emitter inductor degeneration, is shown in Fig.2.The topology is used to simultaneously optimize the input matching and noise performance. In addition, the inductance L_2 increases linearity, but the gain decreases. So choosing the proper inductance needs to be taken into account.

With proper degenerated inductance, Fig.3 shows the position relationship between the circle of noise figure and the input reflection coefficient (S_{11}) on the Smith circle diagram at 17 GHz. When the input source impedance Rs is 50 Ω, the noise figure is about 2.8 dB, and the S_{11} is close to the center of Smith circle.

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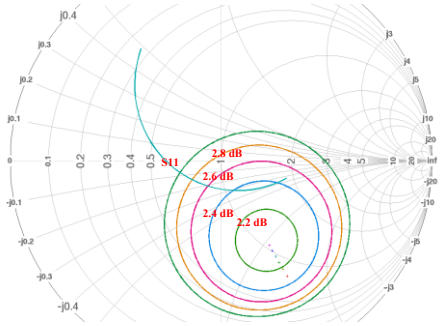


Fig.3. the circle of noise figure and the input reflection coefficient(S_{11}) at 17 GHz

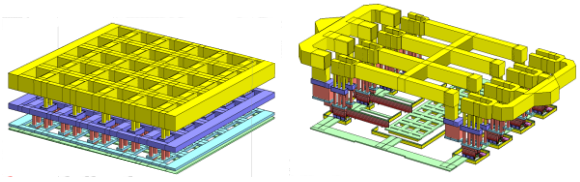
The input matching network consists of inductance L_1 and capacitance C_1. The inductance L_1 is parallel to ground also has the function of electrostatic protection. The output is matched by inductance L_4 and resistance R_2 in parallel for the gain flatness and the broadband matching .

The bias current of the topology is fed through the bypass network, consists $C_{bypass1}$, $C_{bypass2}$ and Rx. The $C_{bypass1}$ is designed for in-band bypass, and $C_{bypass2}$ for low-frequency band bypass. The Rx is designed to depress the low-frequency gain and prevent resonance of bypass capacitor and effective inductance.

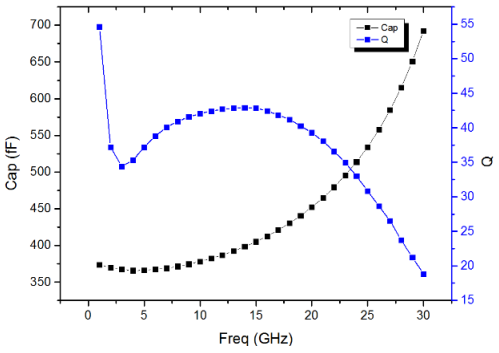
III. LAYOUT AND STABILITY ISSUES

A. Layout

The contribution of routing and ground/supply inductance must be considered at radio frequency. Therefore, the passive part of the layout should be emulated to be closer to the reality. A larger amount of ground and power is spread in the chip to minimize the parasitic inductance and increase the equivalent coupling capacitance between power supply and ground with the effect of decoupling, as shown in Fig.4(a). Fig.4(c) shows the equivalent coupling capacitance between power supply and ground in 100 x 100 um^2 .The active layout adopts multiple transistors in parallel to reduce the base parasitic resistance. By optimizing the transistor layout, better performance of noise and gain at high frequency can be achieved, as shown in Fig.4(b).



(a) (b)



(c)

Fig.4.(a) The power supply and ground layout structure (b) Transistor layout (c) The equivalent coupling capacitance between power supply and ground in 100 x 100 um^2

B. Stability

It has been proved that cascode topology may be unstable at higher frequency[5]. The real part of the base input impedance of the cascode transistor can be expressed as equation (1):

$$R_{bin} = \frac{g_m r_\pi R_1 (1-\omega^2 C_\pi r_\pi C_1 R_1)}{(1+\omega^2 C_\pi^2 r_\pi^2)(1+\omega^2 C_1^2 R_1^2)} + \ldots \quad (1)$$
$$\ldots + \frac{r_\pi}{1+\omega^2 C_\pi^2 r_\pi^2} + \frac{R_1}{1+\omega^2 C_1^2 R_1^2}$$

The above (1) indicates that with the increase of frequency, $(1-\omega^2 C_\pi r_\pi C_1 R_1)$ may be less than zero, thus resulting in instability. The stability of the whole circuit can be achieved by reducing the transconductance g_m , while the gain is reduced. Small resistor R_1 (as in Fig.1) in series at the base of the cascode transistor enhances the stability is used in this paper. In this way, the real part of the reflection coefficient product at the left and right ends of the base node is less than 1 to achieve stability. However, the resistance should not be too large, otherwise the DC operating state will be offset and large noise will be introduced.

IV. RESULTS

Fig.5 presents the microphotographs of the fabricated Ku-band low noise amplifier, which is implemented with commercial 0.13-um SiGe BiCMOS technology. The Ku-band LNA occupies an area of 720×580 um^2 including RF and DC pads and the power consumption is 28.5 mW under the supply of 3.3 V. As plotted in Fig.6 and Fig.7, the results show that : input and output matching within 14.3 to18.3 GHz is less than -10 dB. The measured Ku-band LNA result in a minimum noise figure (NF) of 3.2 dB at 16.4 GHz (within 4 dB from 14 to 19.2 GHz) and a highest power gain of 15 dB at 16 GHz with a 3-dB bandwidth from 14 to 18.3 GHz.

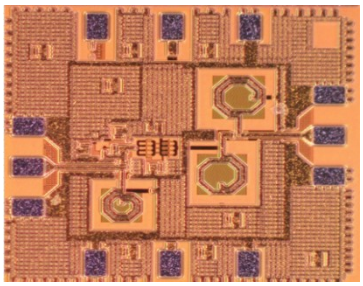


Fig.5. Chip microphotograph of Ku-band LNA

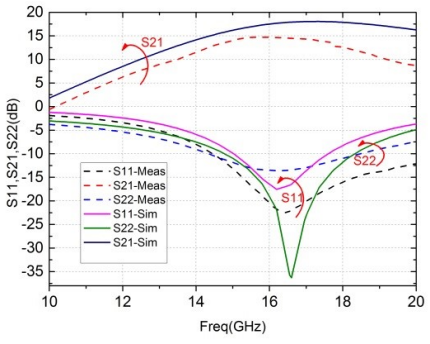


Figure.6. Measured S-parameters

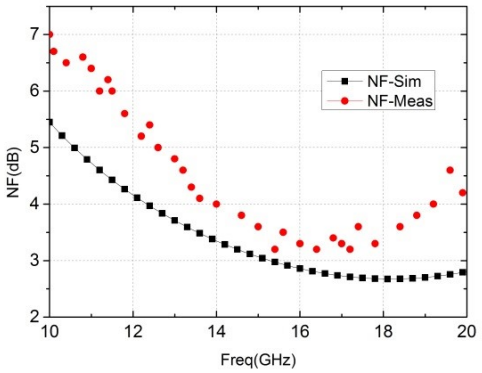


Figure.7. Measured NF

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