# Full D-Band Transmit–Receive Module for Phased Array Systems in 130-nm SiGe BiCMOS

Alper Karakuzulu, *Member, IEEE*, Mohamed Hussein Eissa, *Member, IEEE*, Dietmar Kissinger, *Senior Member, IEEE*, and Andrea Malignaggi

***Abstract*—This letter presents a D-band (110 to 170 GHz) transmit–receive module in 0.13-$\mu$m silicon–germanium (SiGe) BiCMOS for phased-array applications. The module includes single-pole double throw (SPDT) switches, a low noise amplifier (LNA), a power amplifier (PA), and two variable gain amplifiers (VGAs). A broadband quarter-wave SPDT is designed with power handling capacity of 17 dBm and a state-of-the-art insertion loss of 2 dB at 140 GHz. The three-stage cascode LNA and PA and the two-stage phase-compensated VGA cover the entire D-band. In the receive mode, the module has a measured peak gain of 28.3 dB with a 3-dB bandwidth (BW) of 110–170 GHz, along with a minimum noise figure (NF) of 9 dB (at 120 GHz) and an $IP_{1dB}$ of $-21$ dBm. In the transmit mode, the peak gain is 22.4 dB within a 3-dB BW of 113–170 GHz, while the $OP_{1dB}$ is 7 dBm and the $P_{sat}$ 9.5 dBm at 140 GHz.**

***Index Terms*—5G, 6G, broadband, D-band, integrated circuits (IC), millimeter-wave (mm-wave), silicon–germanium (SiGe) BiCMOS.**

## I. Introduction

Next-generation 5G system, called "Beyond 5G" or 6G, has been becoming popular nowadays. The data rate of 6G is expected to be more than 100 Gbit/s [1]. Due to large bandwidth (BW) availability, the D-band is considered as a potential candidate for high capacity backhaul links for beyond 5G and 6G [2]. At millimeter-wave frequencies, the free-space path loss is high and limits the communication distance. Phased-arrays with beam forming and beam steering capabilities improve signal-to-noise ratio (SNR) and compensate path loss. Therefore, broad BW mm-wave phased array is a key solution for high-data rate wireless communication. Up to now, there are very few wireless transceivers (TRx) reported with data rates around 100 Gbit/s [3]–[7]. 80 Gbit/s is reported using a 16-QAM modulation scheme and 35 GHz 3-dB RF BW [3]. In [4] and [5], 100 Gbit/s are achieved, both using a 16 QAM with 28 GHz 3-dB and 35 GHz 6-dB RF BW, respectively. Hamada *et al.* [6] presented 120 Gbit/s using 64 QAM and 24 GHz 3-dB RF BW. Lastly, using a 16-QAM modulation and 35 GHz 3-dB BW, 120 Gbit/s are shown in CMOS technology [7]. In silicon amplifiers, due to the low output power and high noise figure achievable at high frequencies, the SNR is usually not enough to use high-order modulation schemes. Due to these constraints, achieving data rates beyond 100 Gbit/s is only possible through very broad TRx BWs. In this letter, a broadband transmit–receive module covering the entire D-band is described. As can be seen in Fig. 1, the module consists of two single-pole double throw (SPDTs) [8], low noise amplifier (LNA), power amplifier (PA) [9], and variable gain amplifiers (VGAs) for both receive (Rx) and transmit (Tx) operating modes. The module can be included in a phased array system using, for example, the true time delay (TTD) circuit presented in[10]. Despite the fact that single-ended designs are, especially at mm-wave, more prone to instability than their differential counterpart, all circuits are designed as single-ended in order to save power and area.

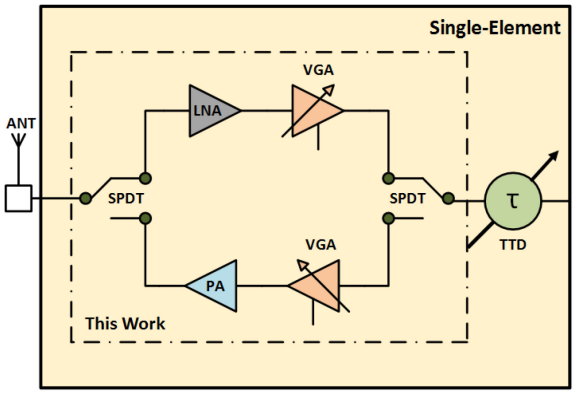


Fig. 1. Phased-array single element block diagram.

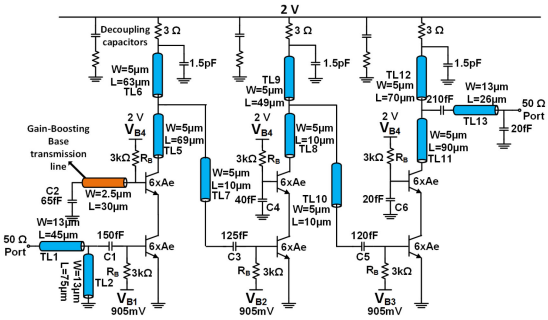


Fig. 2. Schematic of the D-band three-stage cascode LNA.

## II. Circuit Design

### A. LNA Design

The schematic of the designed LNA is shown in Fig. 2. The LNA consists of three-stage cascode amplifiers. A cascode topology is chosen owing to its high gain and good port isolation. In addition to that, gain boosting and low-Q wideband matching techniques are utilized. Optimal sizing and biasing of the transistors are important as they affect noise figure, available gain, and input and output impedances. To determine the transistor size and biasing, as a first step, a sweep on the number of emitter fingers and on the collector current has been done. Then, the current density per finger which yields a good compromise between NF and gain is defined. The

Manuscript received November 12, 2020; revised December 23, 2020 and January 13, 2021; accepted January 19, 2021. Date of publication January 26, 2021; date of current version February 17, 2021. This work was supported in part by the European Commission (ECSEL TARANTO) under Contract 737454, and in part by the German Federal Ministry of Education and Research within the research project ForMikro-6GKom under Grant 16ES1107. This article was approved by Associate Editor Long Kong. *(Corresponding author: Alper Karakuzulu.)*

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Digital Object Identifier 10.1109/LSSC.2021.3054512

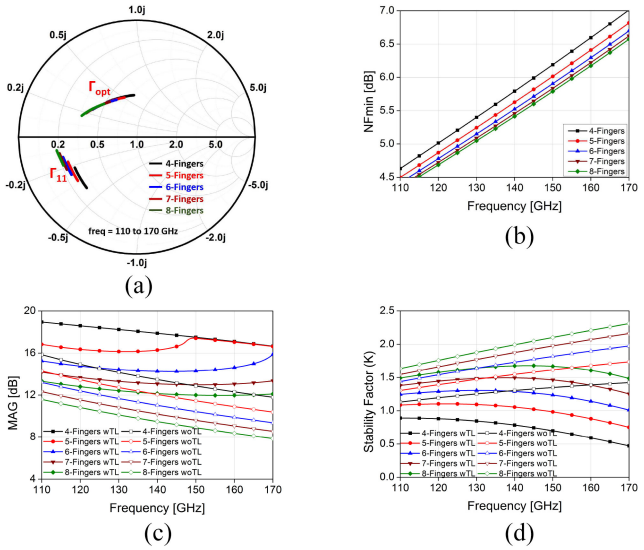


Fig. 3. Simulated (a) optimum source and input impedance, (b) NFmin, (c) MAG, and (d) stability factor versus frequency of a cascode topology with and without gain boosting base transmission line for 4 to 8 emitter fingers.

transistors are biased at a quiescent current of 1.67 mA/finger. As the next step, the most suitable device size for optimum noise matching is found by sweeping the number of fingers from 4 to 8. As visible in Fig. 3(a), transistors with four fingers have a higher optimum source impedance when compared to eight fingers HBTs. At the same time, the higher the number of fingers, the lower the NF [Fig. 3(b)]. Also, the maximum available gain (MAG) increases lowering the number of fingers [Fig. 3(c)]. Utilizing the gain-boosting base transmission line (TL), the MAG of the 6 finger device increases by 3.2 dB at 140 GHz, showing an increase which is for high frequencies more evident than it is for lower ones. This contributes to a broadband frequency response flattening the MAG curve. The risk of using a gain boosting technique can be seen in Fig. 3(d), since the stability factor becomes lower than 1 for devices having less than 5 fingers. According to these analyses, 6 finger devices with a bias current of 9.8 mA have been employed, providing 5.4 dB NF and 14 dB MAG at 140 GHz.

The main design goal lays in achieving a wide BW of 60 GHz centered at 140 GHz. In order to maintain a wideband response, the interstage matching network of each stage is designed employing the staggering method using low-Q matching networks [9]. After defining the optimum $Q_1$ input impedance ($Z_{in}$) using noise and gain circles, an input matching consisting of $TL_1$, $TL_2$, and $C_1$ is realized. This input impedance point lays on the circle where $Q = 1$. Therefore, broadband matching can be achieved using low-Q matching networks. Fig. 3(a) and (b) shows the impedance transformation performed in input and between first and second stage, respectively. In order to match the optimum input impedance to 50 Ω, the $\Gamma_{opt}$ (at 110–170 GHz) is transformed to 50 Ω using $C_1$,$TL_1$ and $TL_2$ [see Fig. 4(a)]. In the same way, conjugate matching is performed using $TL_5$, $TL_6$, $TL_7$, and $C_3$ to transform the first stage output impedance to the second stage input impedance [Fig. 4(b)]. Second interstage and output matching have been realized in a similar way. In order to reduce the size of all matching networks, high characteristic impedance microstrip lines (70 Ω) are employed.

### B. VGA Design

Within a phased array system, VGAs are used to shape the antenna beam for reducing gain error and sidelobes (tapering). However,

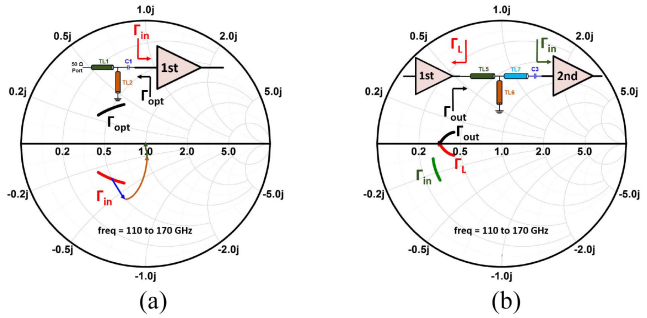


Fig. 4. LNA matching: (a) $\Gamma_{in}$, $\Gamma_{opt}$, and input matching network and (b) $\Gamma_{in}$, $\Gamma_{out}$, and $\Gamma_L$ for the first interstage matching network.

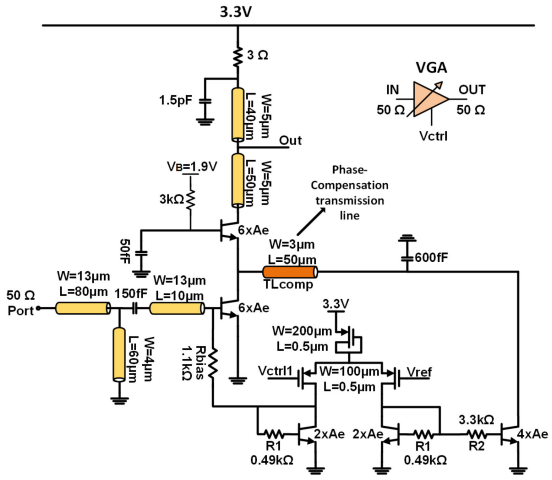


Fig. 5. Schematic of the VGA first stage.

VGAs can cause phase distortion when tuning the gain, triggering unwanted beam nonidealities. In order to prevent such phase variations, the designed module employs two phase compensated wideband VGAs. The VGA consists of two similar stages, the first being shown in Fig. 5. The second stage is omitted for simplicity. The phase imbalance is compensated by the current injection performed through the shunt inductor $TL_{comp}$ [11]. Through this mechanism, the transconductance $g_m$ of the common-base transistor $Q_2$ is kept constant preventing the phase variation introduced by $Q_2$ and minimizing the overall one. Also, an optimum $TL_{comp}$ value is chosen to minimize the phase variation of the common-emitter device $Q_1$. The phase compensation circuit works as follows: when the control voltage ($V_{ctrl}$) is increased, the $V_{be}$ of $Q_1$ will decrease so that its $g_m$ and its current will decrease; at the same time, the $V_{be}$ voltage of $Q_5$ will increase and an additional current will be injected to $Q_2$ to keep its $g_m$ constant. In this way, the gain will be changed with minimum phase variation.

## III. Measurement

Two-port s-parameters, noise and large signal power measurements have been performed on-wafer.

### A. LNA and VGA

Fig. 6(a) and (b) presents the chip micrographs of the single-ended LNA and VGA, respectively. The measured D-band LNA has a broadband response with a peak gain of 24 dB at 130 GHz and a 3-dB BW of 110–170 GHz [Fig. 6(c)]. Noise measurements are performed using a D-band Elva noise source and an external D-band high gain amplifier at the output. A WR-6.5 external sub-harmonic mixer is

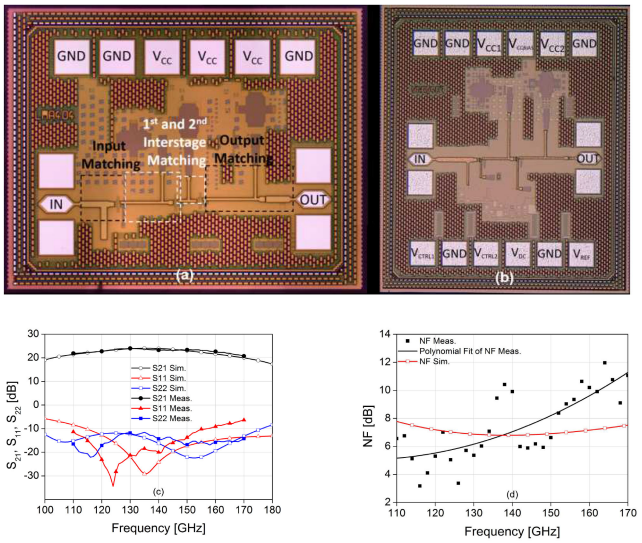


Fig. 6. Chip photograph of (a) LNA and (b) VGA. Simulated and measured LNA. (c) S-parameters and (d) NF.

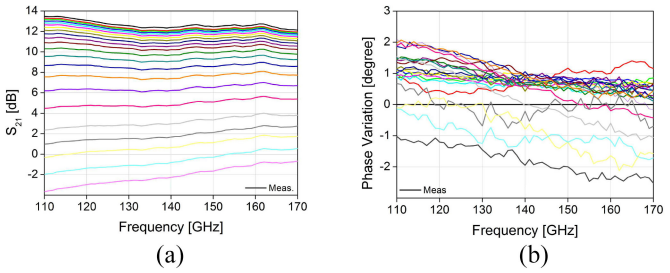


Fig. 7. Measured VGA: (a) small signal gain and (b) phase variation for different gain states.

used to convert the LNA output down to an IF of 1330 MHz. As shown in Fig. 6(d), the measured NF is showing results close to the simulated ones at around 140 GHz. There is a discrepancy especially above 150 GHz between measured and simulated NF due to the excess loss of the external mixer, reducing the accuracy of the NF measurements. The input referred 1-dB compression point ($IP_{1dB}$) is measured as $-21$ dBm at the center frequency.

The designed VGA occupies an area of $0.61\times$ 0.75 mm$^2$. Fig. 7(a) presents the measured small signal gain response of the VGA at different gain states. At the maximum gain state, where the control voltage is 0 V, the peak gain is 13.5 dB. The gain fluctuation in band is only 1.5 dB. Fig .7(b) shows the measured VGA phase variation within the different gain states. It can be seen that the worst case phase variation is 2° along the whole D-band. The VGA $IP_{1dB}$ is measured as $-8$ dBm, leading to a corresponding $OP_{1dB}$ of 3.5 dBm.

### B. Transmit–Receive Module

Fig. 8(a) shows the chip photograph of the transmit–receive module, which has a size of 1.7 × 1.2 mm$^2$ including pads. In the Rx mode, the measured peak gain is 28.3 dB with a 3-dB BW of 110–170 GHz at maximum gain state [Fig. 8(b)]. The small signal gain is plotted for all gain states in Fig. 8(c). The good input and output matching can be seen looking at the input and output return losses of Fig. 8(d). A min NF of 9 dB was measured at 120 GHz, while an average NF of 10.7 dB was measured across the whole band, as shown in Fig. 8(e). The $IP_{1dB}$ in the Rx mode is measured being $-30$ dBm at the center frequency [Fig. 8(f)]. In the Tx mode, as

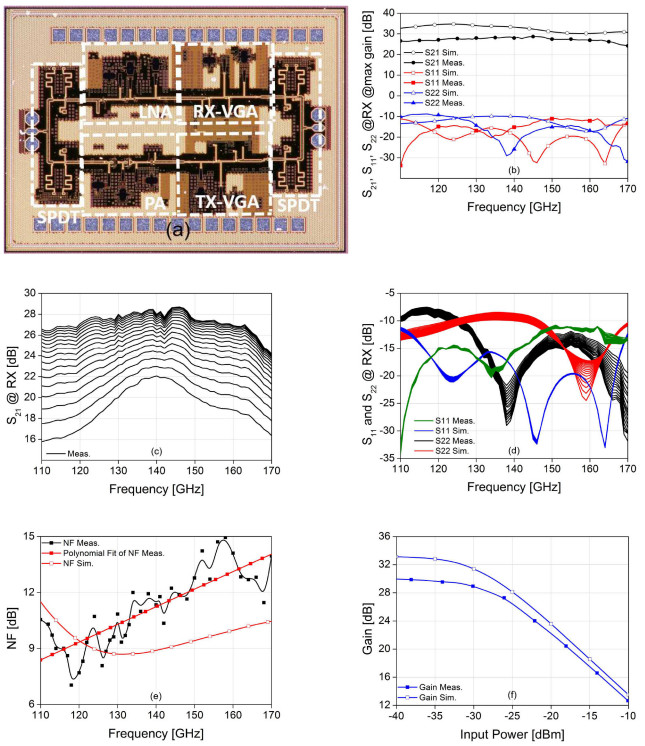


Fig. 8. (a) Transmit–receive module chip photograph. Simulated and measured Rx mode. (b) S-parameters at maximum gain state, (c) small signal gain, and (d) input and output return losses for all gain states. Simulated and measured Rx mode. (e) NF and (f) Gain versus $P_{in}$ at 140 GHz at the maximum gain state.

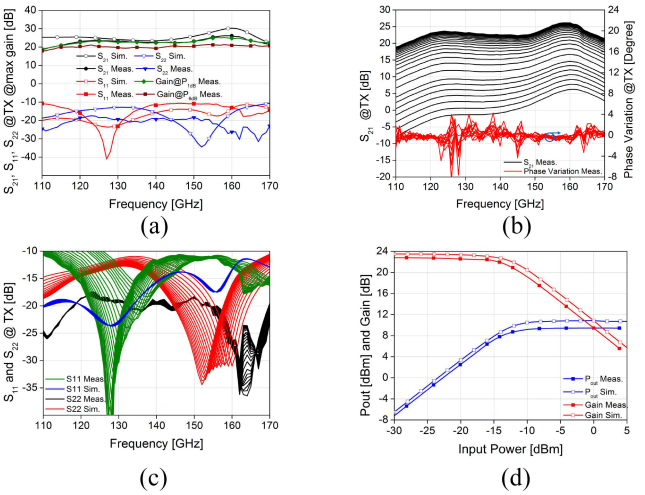


Fig. 9. Simulated and measured Tx mode. (a) S-parameters and large signal gain at maximum gain state, (b) small signal gain and phase variation, and (c) input and output return losses for gain states. (d) Gain and $P_{out}$ versus $P_{in}$ for the maximum gain state at 140 GHz.

reported in Fig. 9(a), the peak small signal gain reaches 22.4 dB at maximum gain state, along with a 3-dB BW which spans from 113 to 170 GHz. Both measured input and output return losses are below 10 dB along the D-band. Measured gain, phase variation, and input and output return losses at the various gain states are given in Fig. 9(b) and (c). As shown in Fig. 9(d), the $IP_{1dB}$ in Tx mode is measured to be $-13.5$ dBm at 140 GHz, corresponding to an $OP_{1dB}$ of 7 dBm. The $P_{sat}$ in the Tx mode is 9.5 dBm at 140 GHz.

Table I shows the performance comparison between the presented D-band transmit–receive module and other D-band modules. From

TABLE I
COMPARISON TABLE OF PUBLISHED D-BAND TRANSMIT–RECEIVE MODULES FOR PHASED ARRAYS

| Reference | Rx/Tx or TRx 3-dB-BW (GHz) | Technology | Architecture | Rx/Tx $P_{DC}$ (W) | Rx Gain (dB) | Rx NF (dB) | Tx Gain (dB) | Tx Psat (dBm) |
|---|---|---|---|---|---|---|---|---|
| **This Work** | 110-170 | 0.13-$\mu$m SiGe BiCMOS | TRx | 0.43/0.56 | 28.3 | 9-14 | 22.4 | 9.5 |
| [12] | 110-170/120-160 | 0.25-$\mu$m InP | Tx/Rx | 0.19/0.16 | 26 | 9.5* | 25 | 9 |
| [13] | 130-170/130-170 | 0.13-$\mu$m SiGe BiCMOS | Tx/Rx | 0.16/0.33 | 22 | 10 | 16 | 10 |
| [14] | 115-155 | 0.13-$\mu$m SiGe BiCMOS | TRx | 1.0/1.35 | 65 | 7.5-10 | 17 | 13 |
| [14] | 135-170 | 0.13-$\mu$m SiGe BiCMOS | TRx | 1.3/2.1 | 65 | 8-11 | 18 | 13 |
| [15] | -/170-200 | 0.13-$\mu$m SiGe BiCMOS | Tx | -/0.66 | - | - | 18.5 | -13 |

*simulated

Table I, it can be observed that this letter presents the broadest BW when compared to the literature, only nearly similar to [12] which uses an InP technology.

## IV. CONCLUSION

This letter presented a broadband D-band SiGe transmit–receive module. SPDT switches, LNA, PA, and VGA have been designed and optimized for broadband operation. All designed circuits show a 3-dB BW of 60 GHz from 110 GHz to 170 GHz. Thanks to the phase compensated VGAs, within the gain variation range the maximum phase variation is 2°, which makes the presented work suitable for an use within the phased array systems.

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