DC-Coupled Ultra Broadband Differential to Single-Ended Active Balun in 130-nm SiGe BiCMOS Technology

Festim Iseini, Andrea Malignaggi, Falk Korndörfer, and Gerhard Kahmen, *Senior Member, IEEE*

***Abstract*— The dc-coupled (DCC) broadband operation is a fundamental requirement in many applications, especially in optical communication systems. However, circuits allowing differential to single-ended conversion in a DCC fashion are very rare to be found in the literature. In this letter, a novel differential to single-ended ultrabroadband DCC balun in a 130-nm SiGe BiCMOS technology featuring f_t/f_{max} of 300/500 GHz is presented. A circuit analysis and a performance comparison between the proposed balun and two other configurations which are commonly used to convert a differential signal to a single-ended one is carried out. The design of the mentioned balun is described focusing on the trade-offs between gain, bandwidth (BW) and linearity. Measurement results show how the presented topology can achieve a low-frequency power gain of −7 dB and a 1 dB BW of 80 GHz, along with a total harmonic distortion (THD) of 7%.**

***Index Terms*— Active balun, BiCMOS, dc coupled (DCC), optical communication systems, SiGe, ultrabroadband.**

I. Introduction

With the constant growth of the data traffic demand in wireless and optical communication systems, the need for fast circuits supporting high data rates is gaining relevance and a particular interest in the scientific community [1]. In terms of integrated circuit (IC) design this translates into complex systems which have to satisfy strict technical requirements, especially when dealing with very high frequencies. The choice of using fully differential designs, instead of single-ended ones, can be justified by their better grounding and their property to reject part of the noise. On the other hand, in case of complex and long interconnections on printed circuit boards (PCBs) between two or more ICs, the use of differential signaling can lead not only to a hardly manageable routing complexity but also to phase impairments, which are very detrimental especially at high frequencies [2]. These are the main reasons why typically differential ICs preferably offer single-ended RF interfaces for single-ended OFF-chip signal routing, making the circuit block that allows such conversion, called balun, of fundamental importance. The standard differential to single-ended active balun topology, consisting of a common collector (CC) stage stacked on top of a common emitter (CE) one, which can be resistively degenerated for improving its linearity [Fig. 1(a)], is suitable for microwave applications, but not in cases where dc-coupling is required, such as optical communication systems where bandwidths (BWs) starting from dc up to several GHz are required [3]. In this context, passive baluns are not of interest since they are by nature ac-coupled. This letter is organized as follows. Section II describes in detail the three topologies, which have been analyzed in depth, finally focusing on all design considerations and trade-offs adopted while designing the proposed topology. The measured results, compared with the simulated ones, are described in Section III, while Section IV concludes the letter.

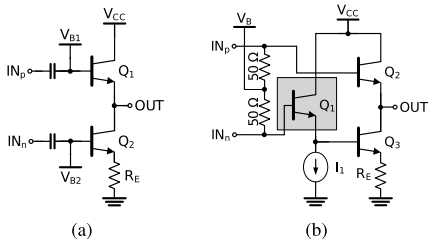


Fig. 1. (a) Standard ac-coupled resistively degenerated differential to single-ended balun. (b) Proposed DCC topology.

II. Circuit Analysis and Design

Typically, dc-coupled (DCC) differential to single-ended conversion is performed considering only one branch of a differential CC or CE stage, as shown in Fig. 2, leading to the loss of half of the power and decreased linearity performances [4]. This letter addresses these issues by introducing an additional CC stage preceding the CE stage into the standard configuration of Fig. 1(a), which results in a DCC balun allowing for a true dc to RF operation [Fig. 1(b)]. A similar topology has been used in [5] and [6] as a fully differential driver. In this work, a comparison between the proposed design and the other two commonly used topologies is presented. In particular, it is shown how the DCC balun represents the best compromise between BW, gain and linearity. In this section, a detailed analysis of the three considered configurations is carried out by the analytical calculation of both low-frequency voltage gain and 3 dB BW. Finally, the design process followed for the development of the DCC balun is reported.

A. Common Emitter Active Balun

The CE active balun (CEB), shown in Fig. 2(a), is based on a standard differential pair amplifier where the output is taken

Manuscript received 20 June 2022; revised 23 August 2022; accepted 15 October 2022. Date of publication 7 November 2022; date of current version 13 March 2023. *(Corresponding author: Festim Iseini.)*

Festim Iseini, Andrea Malignaggi, and Falk Korndörfer are with IHP Microelectronics GmbH, 15236 Frankfurt, Germany (e-mail: iseini@ihp-microelectronics.com).

Gerhard Kahmen is with IHP Microelectronics GmbH, 15236 Frankfurt, Germany, and also with the Institute of Electrical Engineering and Information Science, Brandenburg Technical University, 03046 Cottbus, Germany.

Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2022.3216347.

Digital Object Identifier 10.1109/LMWC.2022.3216347

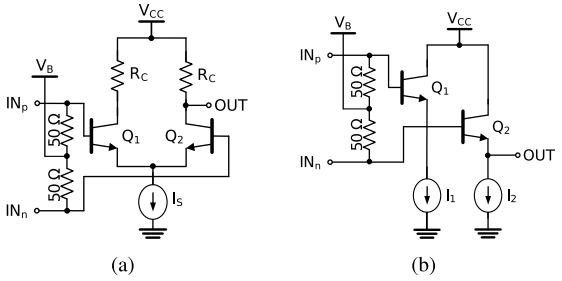


Fig. 2. Two widely used DCC differential to single-ended converters. (a) CE based. (b) CC based.

only from one arm of the circuit. Its low-frequency voltage gain, obtained from a small signal analysis, is given by the well-known equation to be seen in the following [4]:

$$A_{v,\mathrm{CEB}} \simeq -\frac{g_m}{2} R_C \tag{1}$$

where the two transistors have been considered equally sized and biased ($g_{m1} = g_{m2} = g_m$), and R_C is the collector resistance. The factor 1/2 in the equation results from the fact that in the active balun case only one side contributes to the output signal. The 3 dB frequency cut-off (f_c) is derived in [7], resulting in the expression to be seen in the following:

$$f_{c,\mathrm{CEB}} = \frac{1}{2\pi \{r_{\pi 0}\left[C_\pi + C_\mu(1 + g_m R_L)\right] + R_L C_\mu\}} \tag{2}$$

where C_π is the base–emitter capacitance, C_μ the base–collector capacitance, R_L the load resistance, $r_{\pi 0} = r_\pi \| r_b \| R_S$ with r_π the base–emitter resistance, r_b the base resistance, and R_S the internal source resistance.

B. Common Collector Active Balun

The CC active balun (CCB), shown in Fig. 2(b), consists of a differential CC stage, whose output is taken only from one side. Ideally, the CC stage has a unitary low-frequency voltage gain [8], which in the considered case results in the following:

$$A_{v,\mathrm{CCB}} = \frac{1}{2}. \tag{3}$$

Equation (3) means that this topology inherently offers 6 dB loss. The 3 dB cut-off frequency $f_{c,\mathrm{CCB}}$, considering transistors of equal size and bias, can be described as in the following [4]:

$$f_{c,\mathrm{CCB}} = \frac{g_m}{2\pi C_\pi}. \tag{4}$$

C. DCC Active Balun

As already mentioned, the proposed topology is based on a standard balun topology shown in Fig. 1(b), mainly composed of a CE and a CC stage, including a degeneration resistance for linearity purposes, complemented by an additional CC stage used for dc-coupling. For the calculation of the DCCB gain, it is necessary to consider separately the bottom and the upper halves of the circuit before combining them (Fig. 3). The bottom half is composed of a CC and a degenerated CE, loaded by a CC with output resistance equal to the inverse of its transconductance. This means that the output voltage of this branch can be expressed as in the following [9]:

$$v_{\mathrm{out}}^D = -\frac{1}{1 + \left(g_m + \frac{1}{r_\pi}\right) R_E} v_{\mathrm{in}}^D. \tag{5}$$

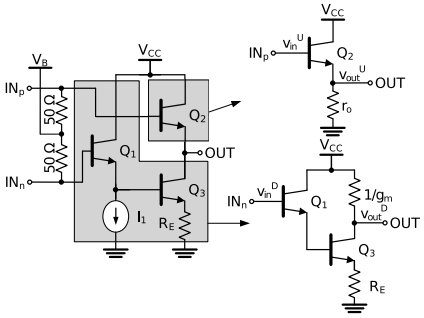


Fig. 3. Upper half and bottom half of the DCCB used for the voltage gain evaluation. r_o is the output resistance of Q_3.

Being the upper half simply a unity gain CC, one can easily obtain the expression reported in the following [9]:

$$v_{\mathrm{out}}^U = v_{\mathrm{in}}^U. \tag{6}$$

The sum of the two voltages leads to an overall voltage gain given as follows:

$$A_{v,\mathrm{DCCB}} = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{1}{2}\left(1 + \frac{1}{1 + \left(g_m + \frac{1}{r_\pi}\right) R_E}\right). \tag{7}$$

For the calculation of the BW it is possible to consider the standard equation used for a degenerated CE stage with output resistance $1/g_m$ and source resistance equal to the output resistance of the previous stage [8] (in this case a CC), thus $1/g_m$. The cut-off frequency of this configuration is then given as follows [8]:

$$f_{c,\mathrm{DCCB}} \simeq \frac{g_m}{2\pi\left[\frac{C_\pi}{1 + g_m R_E} + C_\mu\left(1 + \frac{1}{2 + g_m R_E}\right)\right]}. \tag{8}$$

In order to directly compare the three topologies, typical values for the transistors' parameters have been used to calculate both f_c and gain. Furthermore, for a straightforward performance comparison the gain-BW product (GBP), a very often used figure of merit for comparing circuits having low pass characteristics, has been employed. The obtained results are shown in Table I. It can be noticed that the DCCB performance depends on the value of the degeneration resistor R_E, giving an additional degree of freedom in the design process since its value can be chosen for optimizing the balun's performance. Low frequency gain, 3 dB BW, total harmonic distortion (THD) and GBP for different values of R_E (from 150 Ω to 310 Ω) are shown in Fig. 4. It can be noticed how a small degeneration leads to a high gain, while a higher value of R_E improves both BW and linearity as expected. An optimum R_E value of 230 Ω has been chosen for the realized design with the aim of reaching a good trade-off between the above performance. In Table I, gain, BW, and GBP of the three analyzed topologies are numerically calculated as in (1)–(8) by using typical values for the small signal parameters of a single finger transistor of the employed technology. In the calculation, the resistors have been considered to be $R_L = 100\ \Omega$, $R_S = 50\ \Omega$, and $R_E = 230\ \Omega$. From the presented values, it is clear that the DCCB shows the best compromise in terms of small signal gain and 3 dB BW, expressed by the GBP. Within the circuit analysis, an open load method has been considered to extract both gain and BW. In order to

TABLE I

CALCULATED LOW-FREQUENCY VOLTAGE GAIN, 3 dB BW AND GBP OF THE CONSIDERED CONFIGURATIONS

Topology	Voltage gain [dB]	f_c [GHz]	GBP [GHz]
CEB	1.6	120	142.8
CCB	-6	340	170
DCCB	-4.7	380	216.6
Considered values: $r_\pi = 3\,k\Omega$, $C_\mu = 4\,fF$, $C_\pi = 9\,fF$, $g_m = 24\,mS$, $r_b = 30\,\Omega$			

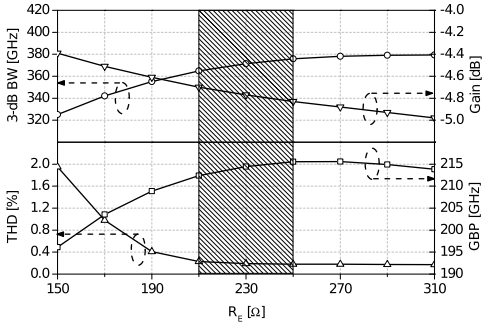
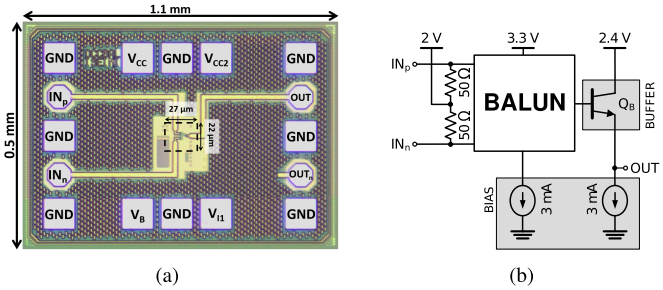


Fig. 4. Simulated performance with varying the degeneration resistor R_E: (bottom) THD with a −5 dBm input tone at 5 GHz, (top) 3 dB BW and (middle) low-frequency gain. It is noticeable how the performance after $R_E = 230\ \Omega$ saturate, justifying the design choice for this parameter.



(a) (b)

Fig. 5. (a) Chip micrograph of the manufactured chip. (b) Generic circuit scheme used for evaluating the balun performance. The pad OUT_n is terminated to an ON-chip 50 Ω resistor.

measure the DCCB in a 50 Ω environment, and for enabling a fair comparison between the three topologies, all of them have been biased and buffered at the output as shown in Fig. 5(b). In particular, all the transistors, including the one employed within the output buffer, are designed to have one finger with an emitter area of 0.07 × 0.9 μm, and biased with 3 mA emitter current in order to operate close to the maximum f_t conditions. Furthermore, the baluns' output dc voltage, which means the input bias voltage of the output buffer, has been kept equal in all three simulated topologies.

III. MEASUREMENT RESULTS

The circuit was fabricated in the IHP 0.13-μm SiGe HBT BiCMOS technology SG13G2, featuring f_t/f_{max} values of 300/500 GHz and offering a full set of passives, namely silicided and unsilicided polysilicon resistors, MIM capacitors (1.5 fF/μm^2), and seven aluminum interconnect layers including two thick top metal layers (2 and 3 μm thick). The chip occupies an area of 0.5 × 1.1 mm, with a core area of 0.022 × 0.027 mm, and its chip micrograph is shown in Fig. 5(a). Small signal measurements have been carried out using 100-μm pitch wafer probes and a four-port Keysight N5291A PNA network analyzer with N5295AX03 120-GHz frequency extenders at each port. In Fig. 6, the DCCB measurement results and the simulated ones of all three configurations, simulated for a fair comparison within the scheme reported in Fig. 5(b), are presented. The measured 3 dB BW exceeds the limits of the test equipment which is 115 GHz, so only the value of the 1 dB BW, which is 80 GHz, has been measured. The 3 dB BW can be obtained by interpolation and it is expected to be around 140 GHz. From Fig. 6 can be seen how the CEB topology presents the highest S_{21} but the lowest BW, and that the proposed DCCB shows the better overall performance when compared to the CCB configuration, in terms of both gain and BW. Linearity measurements have been performed using a Rhode & Schwarz FSW67 spectrum analyzer for evaluating the THD and the output 1-dB compression point (OP1dB) using a 5-GHz input tone. Fig. 6 shows that all three configurations offer similar linearity, both in terms of THD and OP1dB, demonstrating once more that the DCCB shows the best trade-off between gain, BW and linearity. In particular, the measured DCCB balun offers a peak gain of −7 dB, a 1 dB BW of 80 GHz, a THD of 7% at P1dB and an OP1dB of −8.4 dBm. In Table II, the proposed DCC active balun is compared with some passive baluns.

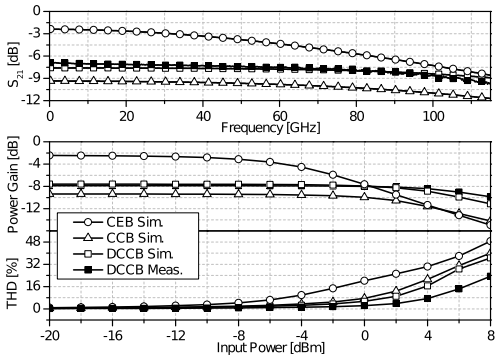


Fig. 6. S_{21} (top), power gain (middle), and THD (bottom) measurements of the DCC chip (full symbols) compared to the simulation results of all three considered configurations (empty symbols).

TABLE II

PERFORMANCE COMPARISON BETWEEN THE PROPOSED DESIGN AND STATE-OF-THE-ART BROADBAND BALUNS

	[10]	[11]	This work
Balun type	Passive	Passive	Active
DC-coupled	No	No	Yes
Losses [dB]	5	10	7
Frequency range [GHz]	28.5-95	15-65	DC-115
Area [mm^2]	0.08	0.2	0.06
Technology	130 nm SiGe	180 nm CMOS	130 nm SiGe

IV. CONCLUSION

In this letter, a DCC ultra wideband differential to single-ended balun has been presented and evaluated. An accurate theoretical analysis of different DCC balun configurations has been carried out. Measurement results showed a low-frequency power gain of −7 dB, a 1 dB BW of 80 GHz, THD at P1dB of 7% and an OP1dB of −8.4 dBm, showing that between the three considered configurations the proposed DCCB reaches the best compromise between gain, BW and linearity, making it suitable for its use in optical communication systems.

REFERENCES

[1] *Cisco Visual Networking Index: Forecast and Trends*, UltraCAD Des., Issaquah, WA, USA, 2022.

[2] D. Brooks, "Differential signals," CMP Media Publication, Cisco Syst., San Jose, CA, USA, Annu. Rep., 2001.

[3] A. Franzese, M. H. Eissa, T. Mausolf, D. Kissinger, R. Negra, and A. Malignaggi, "Ultra broadband low-power 70 GHz active balun in 130-nm SiGe BiCMOS," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2020, pp. 1–4.

[4] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Hoboken, NJ, USA: Wiley, 2009.

[5] K. Abugharbieh, Y. Koh, S. Krishnan, and J. Mohan, "A 33 mW 12.5 Gbps BiCMOS transmitter for high speed backplane applications," *Microelectron. J.*, vol. 45, no. 1, pp. 110–118, Jan. 2014.

[6] A. Manian et al., "A simultaneous bidirectional single-ended coaxial link with 24-Gb/s forward and 312.5-Mb/s back channels," *IEEE JSSC*, vol. 56, no. 3, pp. 972–987, Mar. 2021.

[7] B. Razavi, *RF Microelectronics*, vol. 2. New York, NY, USA: Prentice-Hall, 2012.

[8] M. C. Wu. (2015). *Microelectronic Devices and Circuits*. [Online]. Available: https://inst.eecs.berkeley.edu/∼ee105/fa17/lectures/Lecture00-Logistics.pdf

[9] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. New York, NY, USA: Oxford Univ. Press, 1998.

[10] S. Chakraborty, L. E. Milner, X. Zhu, O. Sevimli, A. E. Parker, and M. C. Heimlich, "An edge-coupled Marchand balun with partial ground for excellent balance in 0.13 μm SiGe technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 1, pp. 226–230, Jan. 2021.

[11] Y.-C. Hsiao, C. Meng, and Y.-H. Peng, "Broadband CMOS Schottky-diode star mixer using coupled-CPW Marchand dual-baluns," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 5, pp. 500–502, May 2017.