A Broadband 110–170-GHz Stagger-Tuned Power Amplifier With 13.5-dBm P_{sat} in 130-nm SiGe

Alper Karakuzulu, *Member, IEEE*, Mohamed Hussein Eissa, *Member, IEEE*, Dietmar Kissinger, *Senior Member, IEEE*, and Andrea Malignaggi

***Abstract*— This letter presents a fully integrated three-stage single-ended *D*-band power amplifier (PA) designed in 0.13-μm silicon–germanium (SiGe) BiCMOS technology. Several bandwidth extension techniques and matching networks are mutually exploited to maximize Bandwidth (BW) performance while assuring unconditional stability. Its measured 3-dB bandwidth covers the entire *D*-band (110–170 GHz). The PA has a small-signal peak gain of 21 dB at 151 GHz. Its saturated output power (P_{sat}) in the *D*-band varies from 11.8 to 13.9 dBm and its output referred 1-dB compression point ($OP_{1\ dB}$) from 9.2 to 12.5 dBm within the *D*-band. The presented amplifier occupies 0.65 × 0.47 mm^2 (including pads) and draws a current of 115 mA from a 3.3-V supply. To the best of our knowledge, these performances represent the state of the art in silicon technology with a minimum (P_{sat}) of 11.8 dBm and ($OP_{1\ dB}$) of 9.2 dBm covering the entire *D*-band.**

***Index Terms*— Broadband, *D*-band, integrated circuits (IC), millimeter-wave (mm-wave), power amplifier (PA).**

I. Introduction

EMERGING millimeter-wave (mm-wave) frequency applications continue to grow due to the recent advancements in silicon-based semiconductor technologies. To meet increased demands for high-data-rate applications, wireless communication systems with high-order modulation schemes, such as quadratic-amplitude modulation (QAM), achieved remarkable data rates of tenths of Gbit/s in mm-wave frequencies [1]. However, larger bandwidths are required for even higher data rates. In order to achieve that, a promising solution is represented by the *D*-band broadband spectrum, which is considered as a potential candidate for high capacity backhaul links for 5G and beyond [2], [3]. By using 16 QAM or high-order modulation schemes with 60-GHz bandwidth, data rates of 100 Gbit/s or more are possible. To realize such high data rates, highly linear, high power, and broadband power amplifiers (PAs) need to be designed.

Advanced integrated technologies provide transistors with high f_t and f_{max}. Due to many effects, such as interconnect parasitics and passives' quality factors, designing an amplifier with both high gain and high bandwidth is still a challenge, especially at high frequencies. Various bandwidth extension techniques are employed to mitigate these drawbacks at the *D*-band. For instance, silicon–germanium (SiGe) PA achieving 3-dB bandwidth of 24 GHz with a gain of 15 dB using a power matching technique was presented in [4]. A 110–155-GHz PA with a 10-dB gain was proposed in [5] using a broadband impedance transformation technique. High-gain PAs were designed for 25-dB gain with 3-dB bandwidth of 20 GHz in [6] and 50 GHz in [7] by using T-matching and gain-boosting techniques, respectively. A 100–180-GHz broadband amplifier is realized in [8]. In [9]– [11], particular inter-stage matching and impedance transformation techniques were used to broaden the bandwidth, achieving a 3-dB bandwidth of 35.6 [9], 66.5 [10], and 25 GHz [11], respectively.

In this letter, the staggered tuning technique [12], [13] for PA bandwidth extension is fully exploited and realized. In addition to that, the low-quality factor (Q) matching networks and gain-boosting techniques are employed. The employed design techniques are implemented in a single-ended three-stage cascode amplifier. Despite the fact that the single-ended design especially at mm-wave is more prone to instability, the single-ended PA is realized to make it more efficient and small size. The PA covers the entire *D*-band with unconditional stability.

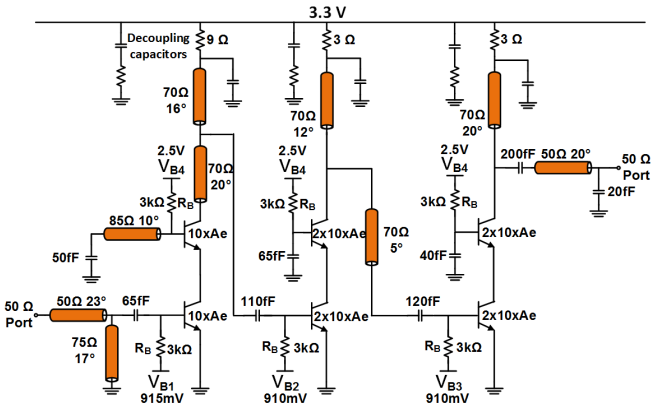

Fig. 1. Schematic of the 110–170-GHz single-ended three-stage cascode PA.

II. Circuit Design

A schematic of the proposed single-ended broadband PA is shown in Fig. 1. It is designed using the IHP 0.13-μm SiGe BiCMOS technology, featuring f_t/f_{max} of 300 GHz/500 GHz. The process offers seven metal layers with two top thick metals. Top thick metal layers, TM1 and TM2, are used

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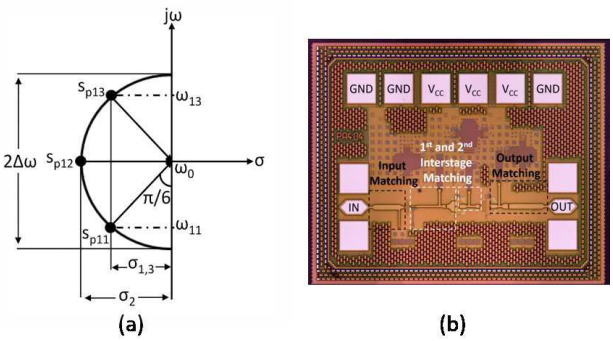

Fig. 2. (a) Pole–zero diagram of the amplifier's gain function. (b) Chip microphotograph of the three-stage PA.

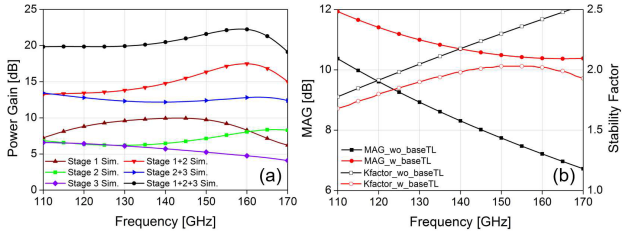

Fig. 3. (a) Power gain of the individual stages. (b) MAG and K-factor versus frequency for the ten fingers' cascode stage with and without base TL.

to implement transmission lines (TLs) with M3 as a ground shield.

A. Staggered Tuning Technique

When broad bandwidth and flat frequency characteristics are targeted, tuning every stage of the multistage amplifier to slightly different frequencies around the center frequency of the band can be a solution. To obtain the desired frequency characteristic of the multistage amplifier, the positions of the poles in the gain transfer function [14] were investigated. Once the number of dominant poles where resonance peaks are formed and their relative positions are known, Q of each dominant pole can be determined defining the overall bandwidth. Since, within an amplifier as the presented one, each state contributes to a dominant pole, our analysis has to consider three dominant poles. The targeted 60-GHz bandwidth can be achieved using more than three stages as well. However, each additional stage will increase the power consumption and degrade the power added efficiency (PAE). In order to get a flat frequency characteristic, the Butterworth pole–zero distribution [14] is used, obtaining a gain function having the pole-zero diagram shown in Fig. 2(a). According to this diagram, the bandwidth of the three-stage amplifier is $2\Delta\omega$, and the appropriate positions of the poles can be expressed as

$$\sigma_2 = -\frac{\omega_0}{2Q_2}, \quad \text{and} \quad \sigma_{1,3} = -\frac{\omega_{11}}{2Q_1} = -\frac{\omega_{13}}{2Q_3}. \tag{1}$$

From the geometry of the pole-zero diagram, ω_{11} and ω_{13} are calculated as

$$\omega_{11} = \omega_0 - \Delta\omega\cos\left(\frac{\pi}{6}\right) \quad \text{and} \quad \omega_{13} = \omega_0 + \Delta\omega\cos\left(\frac{\pi}{6}\right) \tag{2}$$

and the magnitude of the real part of the poles can be calculated

$$|\sigma_2| = \left|\frac{\omega_0}{2Q_2}\right| = \Delta\omega, \quad |\sigma_{1,3}| = \left|\frac{\omega_0}{2Q_{1,3}}\right| = \frac{\Delta\omega}{2}. \tag{3}$$

From (3), the Q values of each dominant pole can be extracted as

$$Q_2 = \frac{\omega_0}{2\Delta\omega} = \frac{f_0}{2\Delta f} \text{ and } Q_{1,(3)} = \frac{\omega_{11,(13)}}{2\Delta\omega} = \frac{f_{11,(13)}}{2\Delta f}. \tag{4}$$

Once ω_{11} and ω_{13} are determined from (2), the Q-factor of each dominant pole can be directly found from (4). The tuning frequencies of the considered amplifier are calculated as $f_{11} = 114.02$ GHz and $f_{13} = 165.98$ GHz, considering a center frequency $f_0 = 140$ GHz. Using these values, knowing that the targeted bandwidth $2\Delta f$ equals 60 GHz, Q of each stage is found to be $Q_1 = 3.8$, $Q_2 = 2.33$, and $Q_3 = 5.53$. Now, the interstage matching between each stage needs to be designed based on the calculated Q values. Both input and output impedances of the interstages are chosen for high-gain (conjugate) matching. Looking at the gain circles, after few iterations, optimum impedances satisfying both gain and bandwidth (Q values) requirements can be determined. Q of the matching network is controlled and defined according to [15] where R_L is the load and R_S is the source resistance of the matching network, and for the case of $R_L > R_S$

$$Q = \sqrt{\frac{R_L}{\sqrt{R_S R_L}} - 1}. \tag{5}$$

After defining tuning frequencies and Q of each stage, the gain of each stage needs to be properly determined. The basic design principle of the staggered tuning technique consists of tuning the gain of all the individual stages at different tuning frequencies in order to broaden the bandwidth of the overall transfer function. Fig. 3(a) shows the simulated power gain for the different stages of the PA. Stage 1 is designed to have peak gain at 140 GHz. Considering the high-frequency gain drop, stage 3, the one having minimum gain, is tuned at the low portion of the band. Besides, stage 2 is tuned around 165 GHz, and a combined peak gain of stages 1 and 2 is designed to compensate for the drop in gain at the higher part of the band. In addition, the maximum available gain (MAG) is increased by utilizing the gain-boosting technique with base TL at the first stage. The MAG has been increased to 2.2 dB at 140 GHz [Fig. 3(b)]. More importantly, the MAG of the device is becoming flattered and showing the broadband response.

B. Broadband PA Design

The broadband PA consists of three cascode stages biased in class A. The cascode topology provides high gain and good isolation between ports. Due to the high isolation, matching the output of a stage will not affect its input impedance. This allows designing interstage matching for predefined Q values without affecting the previous and following stages. Optimal sizing of the transistors is important as it affects available gain, output power, and input and output impedances. A transistor size that has an output impedance close to the Smith chart center is preferable to avoid an output matching network with high loss and narrow bandwidth [7]. For a linear and high-power PA design, an HBT transistor of emitter area $10 \times (0.12 \times 0.9)$ μm^2 is chosen. The HBT transistors are biased near their peak $f_{\max}$ current density at a quiescent current of 2.4 mA/Finger. Two of such transistors connected in parallel are used within the second and third stages. These

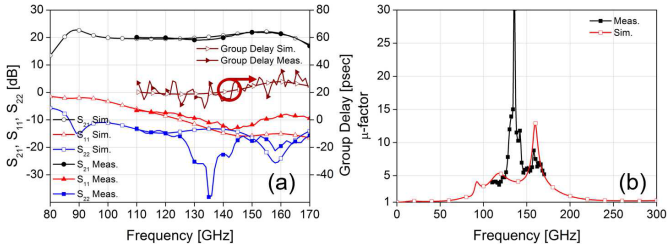

Fig. 4. Measured and simulated. (a) PA S-parameters with group delay response. (b) μ-factor of the PA showing unconditional stability.

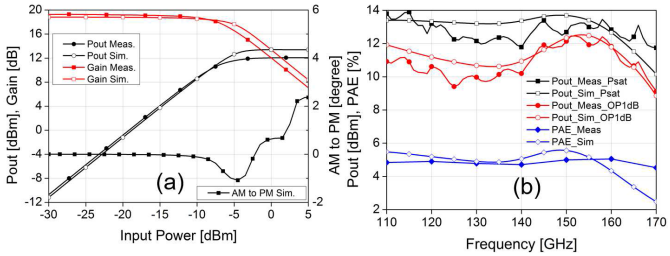

Fig. 5. Measured and simulated. (a) P_{out} and gain versus input power of the three-stage PA at 140 GHz. (b) $\text{OP}_{1\text{ dB}}$, PAE at $P_{1\text{ dB}}$, and P_{sat} over frequency.

transistors are twice as big as the ones used in the first stage to be able to deliver enough power in output. The circuit has been fully electromagnetic (EM) simulated. All the matching networks are implemented using TLs and MIM capacitors. Inductors are implemented using TLs with different characteristic impedances. Input and output are matched to 50 Ω for allowing easier top-level integration. Interstage nodes are matched at higher characteristic impedances to reduce matching losses and make TLs shorter. The gain is boosted using shunt capacitance and inductive positive feedback on the common-base stage. The first two stages are matched for maximum gain, while, on the third one, a load–pull has been performed.

Due to the boosted gain given by the inductive positive feedback on the common-base stage, the PA could be prone to instability. Therefore, the stability check has been done with different techniques. The common "K-factor" analysis may give some indication of possible instabilities; however, it is not sufficient for multiple-stage amplifiers [16]. K-factor analysis should be done separately for each amplifier stage [17]. For this reason, each stage is separated, and both μ- and K-factors are checked. Besides, s-probe analysis [18] has been done for critical nodes, especially common base nodes that could show a negative impedance. At the same time, to ensure unconditional stability at all frequencies, a small stabilization resistance is used between the supply and collector of each stage to prevent any possible cross-coupling across the stages. The value of the stabilization resistor is 9 Ω for the first stage and 3 Ω for the last two stages. Furthermore, supply decoupling capacitors de-Q'ed with small resistors are integrated at the dc supply node. Fig. 4(b) presents both simulated and measured μ-factor of the PA. According to the measurement results, the PA is unconditionally stable along the D-band.

III. Measurement

A. Small-Signal Measurements

The chip microphotograph of the single-ended PA is shown in Fig. 2(b). The overall size of the PA is only 0.48×0.39 mm^2 due to the single-ended design. The measurement and simulation results of the small-signal S-parameters are presented in Fig. 4(a). An excellent agreement for S_{21} can be seen, with a peak gain of 21.6 dB at 155 GHz. The measured 3-dB bandwidth is limited at the lower side by the measurement equipment. The measured output return loss is better than 13 dB along the D-band. Another important parameter for broadband communication applications is the group delay [19], which is measured showing variations of only ±8 ps across the whole band, as plotted in Fig. 4(a).

TABLE I

Comparison Table of Published D-Band PAs

Reference	3-dB-BW (GHz)	Technology	ft/fmax (GHz)	Topology	Peak Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	P_{DC}(W)	Area (mm^2)	PAE (%)
This Work	110-170	0.13-μm SiGe BiCMOS	300/500	3-stage single-ended	21	11.8-13.9	9.2-12.5	0.379	0.3	5.1
[5]	110-155	65-nm CMOS SOI	-	5-stage single-ended	19	-	-	0.109	0.37	-
[7]	131-180	0.13-μm SiGe BiCMOS	250/300	5-stage differential	27	12-14	-	0.44	0.48	5.5
[8]	100-180	0.13-μm SiGe BiCMOS	250/370	4-stage differential	24.8	7.5-11	-	0.262	0.42	4.8
[9]	110-150	0.25-μm InP HBT	350/600	4-way combining	29.4	24	22.3	2.9	1.88	7
[10]	120.7-187.2	0.25-μm InP HBT	350/600	2-way combining	25.3	20.6	18.9	1.18	1.19	5.6
[11]	155-180	0.13-μm SiGe BiCMOS	300/500	4-way combining	30.2	18	15.6	-	0.85	4
[20]	140-220	0.13-μm SiGe BiCMOS	350/450	4-way combining	19	15	13	0.83	0.92	2.3
[21]	168-195	0.13-μm SiGe BiCMOS	300/500	4-way combining	23.6	18.7	-	1.6	1.35	4.4
[22]	145-205	GaN HEMT	100/300	10-stage single-ended	30	16.9	-	0.76	1.24	1.7
[23]	96.5-135	65-nm CMOS	-	3-stage differential	15.8	14.6	9.3	-	3.3	9.4

B. Large-Signal Measurements

The output power (P_{out}) and gain versus input power (P_{in}) at 140 GHz are shown in Fig. 5(a). Regarding the gain measurement, the input-referred 1-dB compression point ($\text{IP}_{1\text{ dB}}$) is −8 dBm, and the corresponding $\text{OP}_{1\text{ dB}}$ is 10.26 dBm at 140 GHz. To the best of our knowledge, the PA shows state-of-the-art $\text{OP}_{1\text{ dB}}$ having a minimum of 9.2 dBm across the whole D-band for Si-based PAs, with a maximum of 12.5 dBm at 151 GHz. As can be seen from the P_{out}-versus-P_{in} plot, the saturated output power at 140 GHz is 12.1 dBm. The measured and simulated $\text{OP}_{1\text{ dB}}$ and P_{sat} over the frequency are given in Fig. 5(b). The PA achieves state-of-the-art performance showing a minimum saturated power of 11.8 dBm across the entire D-band for Si-based PAs, with a maximum of 13.9 dBm at 114 GHz. The measured PAE over frequency is reported to be around 5% within the D-band. The stages show a current consumption of 23, 46, and 46 mA, respectively, with 3.3-V supply voltage. The AM–phase modulation (PM) distortion of the PA has been simulated, reaching a value of less than 1° in the linear region and 3° at P_{sat} at 140 GHz.

IV. Conclusion

Table I shows the performance comparison of the designed PA with other D-band amplifiers. The designed PA shows high output power performance over an outstanding broad frequency band. Compared with the state-of-the-art Si-based PAs, this work shows broader bandwidth, comparable with the one showed by Ahmed *et al.* [8] that, on the other hand, presents 3 dB lower P_{sat} and lower efficiency. This letter presents a broadband high-power D-band SiGe PA. The designed three-stage PA shows a 3-dB bandwidth from 110 to 170 GHz (limited by the measurement setup). The PA achieves state-of-the-art $\text{OP}_{1\text{ dB}}$ and P_{sat} of at least 11.8 and 9.2 dBm within the entire D-band, respectively.

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