A 60 GHz Wideband High Output P1dB Up-conversion Image Rejection Mixer in 0.25 μm SiGe Technology

Mohamed Elkhouly, Srdjan Glisic and Christoph Scheytt

IHP-microelectronics, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

Abstract — **A high output 1dB compression point 60-GHz up-conversion mixer fabricated on 0.25 μm SiGe:C technology is presented. It is based on the Gilbert cell and integrated with LO passive stacked Marchand balun to convert the LO single ended signal into differential. It employs tuned load consisting of spiral inductor and MIM capacitor to match the differential output to 100 ohm and to attenuate the image signal by 15 dB in the middle of the band. The conversion gain is 2.2-dB in 61 GHz and varies within 2 dB over 9 GHz band We achieve output 1-dB compression point of -3.4 dBm. To the best of our knowledge it is the highest output 1-dB compression point in silicon-based 60-GHz mixers. It consumes 10 mA from 3.3 V supply**

Index Terms — **up-conversion mixer, linearity, 60 GHz, OP 1dB point.**

I. INTRODUCTION

Recent advances in silicon technologies both SiGe and CMOS have made it possible to build high performance millimeter-wave circuits and transceivers with low cost and high integration [1]. 60-GHz-bands have become a center of such transceiver developments because of its capability to transmit multi-gigabit data with unlicensed 7-GHz spectrum. For long-range application such as wireless LAN and uncompressed video distributions, orthogonal frequency division multiplexing (OFDM) is preferred due to its robustness to multi-path interference. However, it imposes high peak-to-average power ratio (PAPR) which requires high linearity in RF building blocks. In general, a power amplifier is known as a major source of transmitter nonlinearity, however, a frequency up-conversion mixer is also important when a power amplifier operates in linear region (e.g. by applying high output backoff) In addition, image rejection is required in order to eliminate the use of an image-rejection filter which would occupy large size on chip integration.

There are several papers on silicon-based 60 GHz up-conversion mixers [3], [4], [5]. They suffer from high conversion loss or low output power. Moreover, they do not consider image signal attenuation.

In this paper we present a high linearity up-conversion mixer based on Gilbert cell. It includes LO balun and tuned load for image signal rejection as shown in Fig. 1. The mixer was fabricated on the 0.25 um SiGe HBT technology of IHP. This mixer is designed to be integrated in a 60 GHz transmitter which consists of an up-conversion mixer, 48 GHz phase-locked loop (PLL) and high power amplifier. The schematic of the transmitter is shown in Fig. 2. To achieve the required system performance, a frequency up-conversion mixer should provide high output 1 dB compression point to eliminate the use of an additional drive amplifier before a power amplifier. It should also- provide image signal attenuation to avoid the use of an image rejection filter.

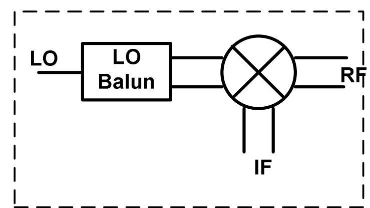

Fig.1. Block diagram of the mixer.

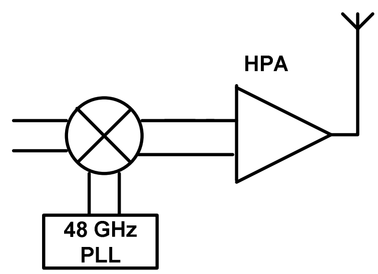

Fig.2. Transmitter block diagram

II. CIRCUIT DESIGN

A. Mixer Design

The simplified schematic of the proposed up-conversion mixer is shown in Fig. 3. As the target for this mixer is higher linearity, therefore emitter degeneration resistors are used. For wideband operation some mixers employ resistive loads but for 60 GHz the resistive load and the output node parasitic capacitance will form low pass filter. This causes that the upper side band of the spectrum will be lower in amplitude than the lower sideband. Also the resistive load will limit the headroom in the mixer. To overcome this problem a tuned load is used. This tuned load consists of spiral inductor with tap points at which output can be taken, the tap location and the coupling capacitors are optimized to match the outputs of the mixer to 100 ohm differential impedance, so each branch can be directly loaded by 50 ohm. By selecting the value of the emitter resistor and the inductance value of the load, both conversion gain and linearity can be optimized. The admittance of the inductive load at 60 GHz it gives around 80 ohms which is good enough to get conversion gain and moderate linearity. The current in the main differential pair is 3.5 mA per branch. The 1 dB compression point voltage can be calculated by [7]:

$$v_{1dB} = \frac{2\sqrt{2}v_t}{5.25}\left(g_m R_E + 1\right)^{\frac{3}{2}} \quad (1)$$

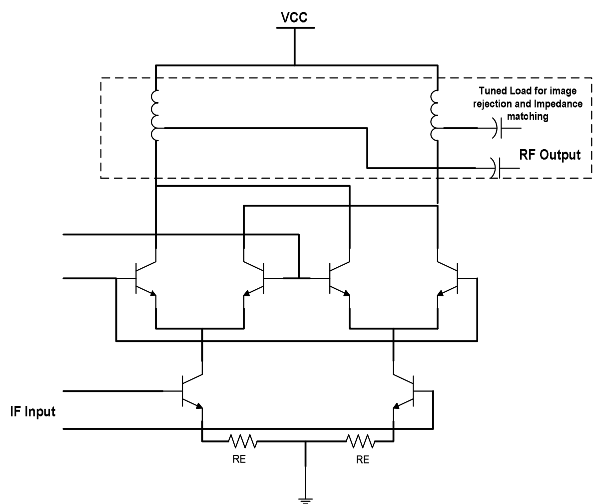

Fig.3. Up-conversion mixer schematic.

Where g_m is the transconductance of the IF differential pair, R_e is the emitter degeneration resistor and v_t is the thermal voltage. From equation (1) the 1 dB compression point increases with the increase of degeneration resistance but the gain decreases. For 70 ohm degeneration resistor, the simulated conversion gain is 2.2 dB and the input 1dB compression point is -4.5 dBm at 61 GHz.

Fig. 4. shows the load network and the tape points at which the capacitors are connected. As a result of this configuration, the lower side band is attenuated by 15 dB thus eliminating the need for an image rejection filter.

B. Passive Balun

In order to test the Gilbert cell mixer, a differential LO signal is needed. So a passive balun based on Marchand type is designed as in [2]. This balun has wideband response with low insertion loss. It converts the single ended signal to differential signals by the coupling across a half-wave transmission line. The Balun is built with the two upper thick metals stack. The length and width of the balun are optimized for 48 GHz operation. In order to make the line shorter and to enhance amplitude and phase balance between the differential ports a capacitor is added at the end of the single ended line as shown in Fig.5. The balun should work from 45 GHz to 55 GHz to cover all LO frequency band. By EM simulation and optimization, the width and length are determined to be 15µm and 430 µm respectively. The balun has 2 dB insertion loss, 4 degrees phase imbalance and 0.5 dB amplitude imbalance. The output of the balun is placed very close to the LO input of the Gilbert cell. The required LO signal to drive the Mixer is 4 dBm.

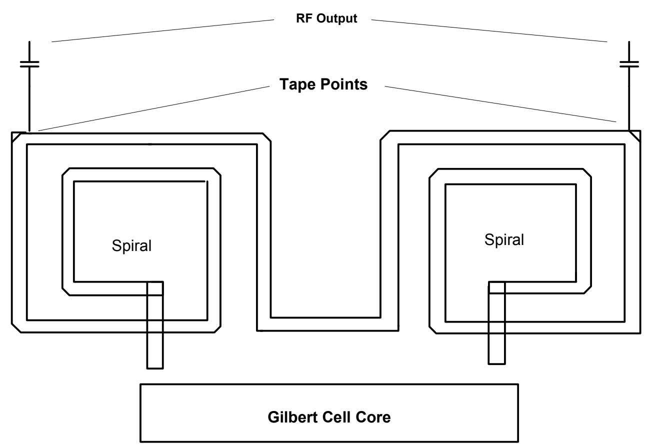

Fig.4. Tuned load for the mixer.

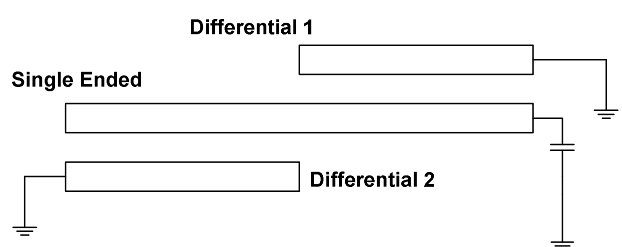

Fig.5. Marchand balun schematic.

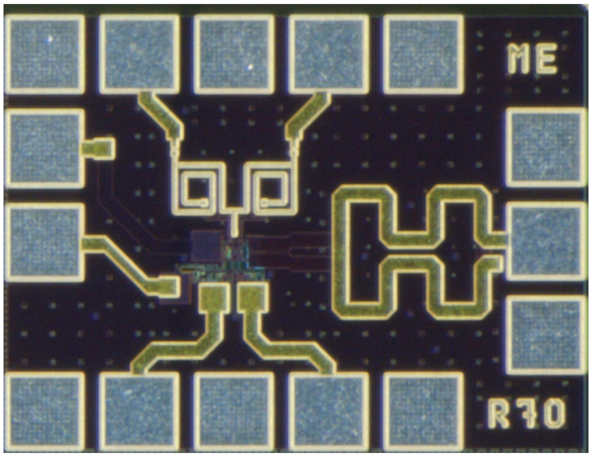

Fig.6. Chip micrograph of the mixer.

III. Measurements Results

The proposed up-conversion mixer was fabricated using 0.25 µm SiGe:C technology. The chip micrograph is shown in Fig. 6. The chip area including all test pads and passive balun is 0.615 mm x 0.46 mm^2. On wafer test setup is used to characterize the mixer. The mixer circuit core consumes 7.7 mA from 3.3 V supply and on chip bias circuit consumes 2.2 mA from the same supply. For LO input ground-signal ground (GSG) probe was used. For differential RF output one terminal is terminated with 50 ohm resistor and the output is measured with V band GSG probe. The IF input is fed though GSGSG probe. Fig. 7 shows mixer conversion gain vs. the LO power sweep. The conversion gain of the mixer increases as LO power increases and it saturates around 2.2 dB at 4 dBm LO power.

Fig. 8. shows the mixer measured gain with frequency sweep. From the figure it is clear that the mixer is working from 57 GHz to 65 GHz. where the IF and LO changes from 11 GHz to 13.2 GHz and 44 GHz to 52.8 GHz respectively. The conversion gain is 2.2 dB at 61GHz. The image signal frequency is from 33 GHz to 40 GHz. The image signal attenuation is -15 dB at the center of the band as shown in Fig.9. The output 1 dB compression point is shown in Fig.10. The mixer has -3.4 dBm output 1 dB compression point. By terminating the IF input with 50 ohms and injecting the LO signal. The LO to RF isolation could be measured and it was found to be -30 dB. This proves that the mixer is double balanced and the LO balun has very good phase and amplitude balance.

Table 1 shows the performance of the proposed up-conversion mixer and the published up-conversion SiGe mixers [2], [5] and CMOS [2, 3, 4, and 6].

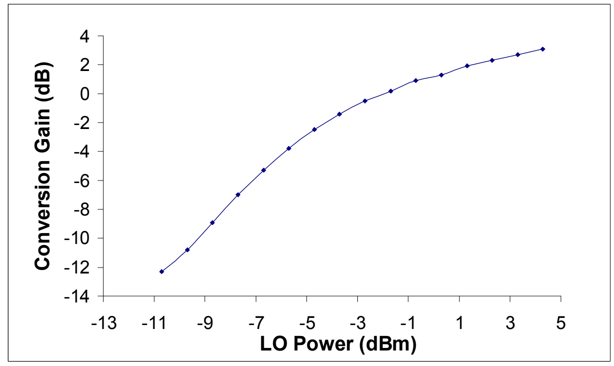

Fig.7. Conversion gain of the mixer vs. LO power.

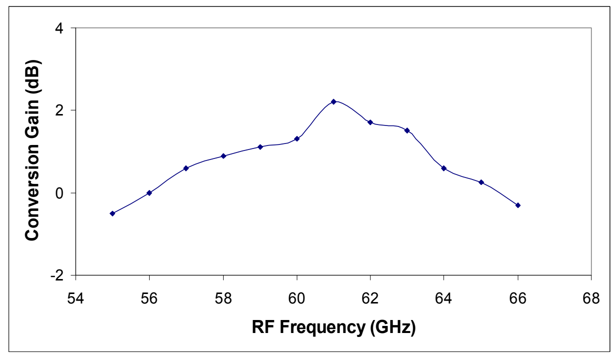

Fig.8. Conversion gain vs. output frequency.

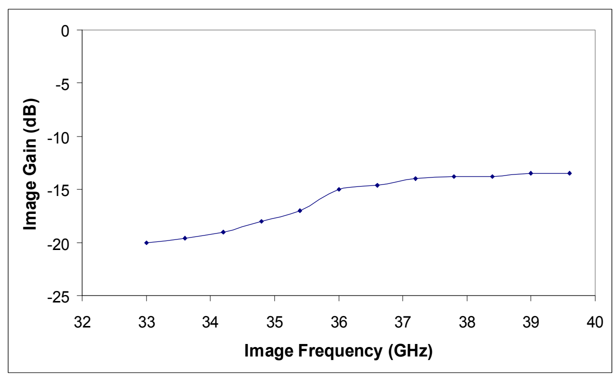

Fig.9. Image signal gain vs. image frequency.

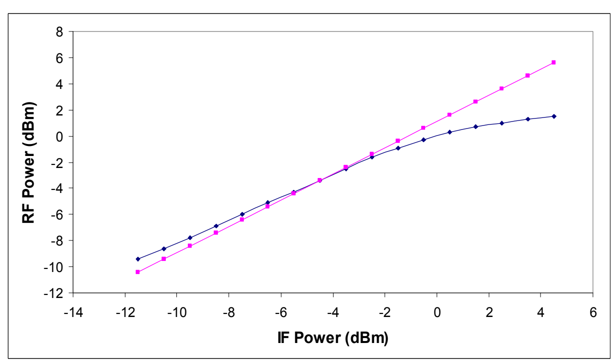

Fig.10. Measured 1dB compression point of the mixer.

Table 1.
Comparison with published up-conversion mixers

Ref.	Tech.	Freq	Gain (dB)	Output 1 dB (dBm)	Power (mW)
[2]	0.25 BiCMOS	60	-6.5	-6	82.5
[3]	90 nm CMOS	51	-11	-10	13.2
[4]	130 nm CMOS	59-65	-0.7 to 4	-5.6	24
[5]	0.25 BiCMOS	60	-3	-15	35
[6]	130 nm CMOS	58.3-62.5	-5.6	-20	2.7
This* work	0.25 BiCMOS	57 - 66	-0.5 to 2.2	-3.4	33

IV. Conclusion

A 60 GHz up-conversion mixer based on Gilbert cell with emitter degeneration resistors has been designed and fabricated using 0.25µm SiGe technology. The tuned load is designed for upper sideband selection and image signal attenuation. The mixer is driven by 4 dBm LO signal due to balun insertion loss. It has conversion gain of 2.2 dB at 61 GHz and OP 1dB of -3.4 dBm. To the best of our knowledge it is the highest output power among the published up-conversion mixers. The mixer demonstrates a high potential to be integrated in the high performance sliding IF transmitter.

Acknowledgement

The authors acknowledge the excellent cooperation with all project partners within the EASY-A project and the support by the German Federal Ministry of Education and Science (BMBF).

References

[1] B. Floyd et al., "A Silicon 60GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE J. Solid State Circuit*, Vol. 41 no. 12 pp.2820-2831, Dec. 2006.

[2] Van-Hoang Dol., et al., "A 60 GHz Monolithic Up-conversion Mixer in SiGe HBT Technology." In *Proc. Of IEEE International workshop on Radio Frequency Integration Technology*, Singapore, Dec. 2007.

[3] I. C. H. Lai, et al., "50GHz double-balanced up-conversion Mixer using CMOS 90-nm process," *in Proc. of IEEE Int. Circuits and Systems Symp*, May 2007, pp. 2542–2545.

[4] F. Zhang, et al., "60 GHz double-balanced up-conversion Mixer on 130 nm CMOS technology," *Electronic Letters,* vol. 44, issue 10, pp. 633–634, May 2008.

[5] Y. Sun, S, et al. "An Integrated 60 GHz Transceiver Front-End for OFDM in SiGe: BiCMOS," in *Proc .of the 16th. Wireless World Research Forum,,* 2006, pp. 121–127

[6] Min –Chiao, et *al*., "A CMOS Up-Conversion Mixer with Wide IF Bandwidth for 60-GHz Applications" *SiRF2009.*

[7] John Rogers, Calvin Plett, Radio Frequency Integrated Circuit Design, Boston: Artechouse, 2003