Lab 4 Report
Anya Agidi & Angel Amaya
11/3/2024

Top Level (toplevel.v and toplevel_tb.v)

In the top-level module, we instantiated all the key components. We made sure to control the data flow between the ALU and the registers based on the opcodes and inputs from our simulations. The corresponding testbench that was made was used to ensure the functionality and interactions of the ALU and registers.

ALU (alu_32bit.v and alu_1bit_slice.v)

We built the 32-bit ALU by connecting multiple instances of the 1-bit ALU slices. Each slice was designed to perform basic operations and handle the carry or borrow to the next bit. This was the foundation to our computational logic. The 1-bit ALU slice was another important part of our design. We used it to ensure that each bit of our larger ALU performed exactly what was expected, which was essential for operations like addition, subtraction, and bitwise functions.

Full Adder (FA_str.v)

The full adder was a critical component within each 1-bit ALU slice. We used it to perform single-bit additions with carry-in and carry-out. This component was needed for our structural Verilog modeling since it allowed us to effectively handle arithmetic operations.

Register mods (nbitreg.v and register_32bit.v)

We designed the nbitreg.v to allow us to store a variable number of bits, which allowed us to use this module across different parts of our design. The register_32bit.v was specifically instantiated from nbitreg.v to manage 32-bit data. This was aligned with our ALU's architecture and was key in storing results efficiently after each operation. Our testbenches included a wide range of input conditions to test all ALU operations extensively, from simple bitwise NOT to complex arithmetic operations like addition and subtraction with edge cases such as overflows.

Testbenches

To ensure our design was ready to work with all the modules, we developed specific testbenches for each module. The top-level testbench (toplevel_tb.v) was important in making sure that the entire system functioned well together under various conditions. This helped us confirm the accuracy of our design through different simulations.

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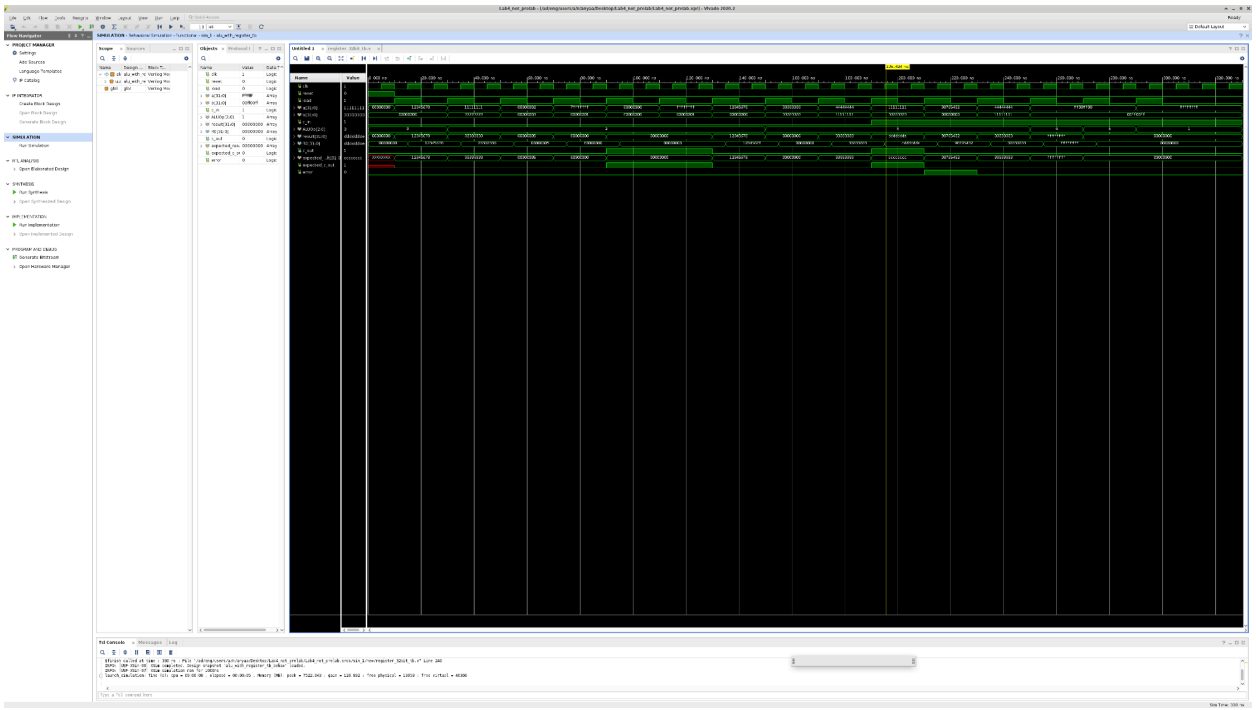
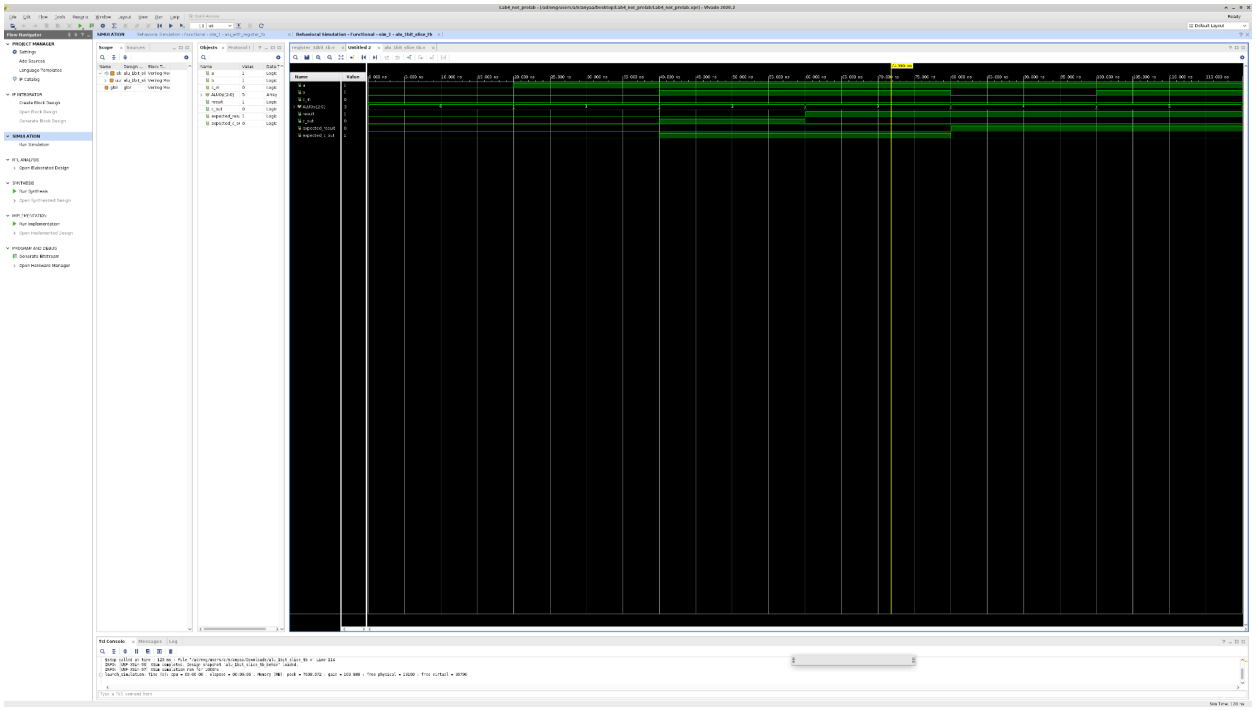


Waveform for alu_with_reg tb



Waveform for alu bit slice tb

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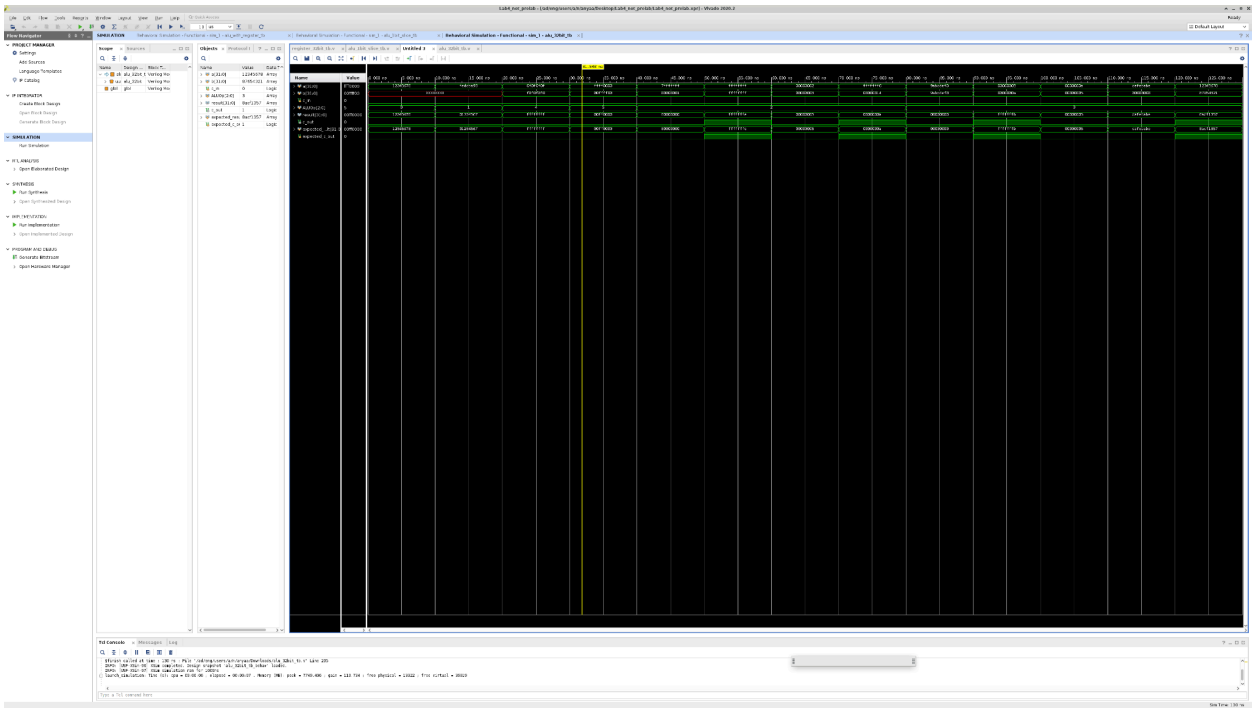

Waveform for alu 32 bit tb