Project-Compressed Extension of RISC-V Core

Compressed Instructions

Compressed instructions are a set of instructions which has length 16 bit with respect to RISC-V architechture. The Compressed instruction are represented by the character "C" in RISC-V specifications.

Team Members

- Nadeem Asghar
- Areeba Zahid
- Soban Ahmed

Project Details and Task Distribution

In this project, the team needs to add compressed instruction extension ("C" extension) to the core (aqlrv32). Originally the core supports "I" and "M" extensions.

If team members accomplish these segments ahead of schedule, this task distribution is adjusted accordingly. They can begin working on the following section regardless of the time frame outlined below.

Concisely divide the tasks to be done by every member in team. Team work is valued.

3-days

- Understand the RTL & infrastructure
- Get a concise plan ready aided with Block Diagrams for the blocks that needs to be included in the RTL

1-day

- Detailed verification plan
- Discussion of the Issues (If any) and design verification plan

6-days

- Get the RTL & updated infrastructure
- Write tests and verify the implementation
- Complete the coverage of core

Takeaways

- Every team member should have the understanding of the project and other team member's work

Project Timeframe

- Time frame of the project is two weeks

Meetings Times

- Meetings can be called anytime by project owners/members. If project owners are not available at that time then meeting can be delayed

Resources

- Resources for the project can be cloned from the following links.

```
https://github.com/aamir-sultan/aqlrv32-setup.git
```

```
https://github.com/aamir-sultan/aqlrv32.git
```

- Clone the repos. One repo contains the setup process and the other repo contains the core
- Compressed instructions reference

Project Owners

- Aamir Sultan
- Haseeb Ahmed