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Carrier transport through the ultrathin silicon-oxide layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells

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ABSTRACT

The carrier transport through the silicon-oxide (SiO_x) layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells has been studied experimentally and by simulation. The current intensity versus voltage (J-V) characteristics of GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al structures shows a linear Ohmic characteristic, while a non-Ohmic behavior is observed in the samples without the n^+-poly-Si contact layer. Conductive Atomic Force Microscopy (c-AFM) images reveal some current spikes on the surface of the samples, which could be related to the transport through pinholes. The simulation results show that 1) a rectification characteristic is obtained when only the tunneling mechanism is included, 2) both the reverse saturation current and the forward current increase when a small amount of transport through pinholes is introduced, and 3) finally a linear Ohmic behavior is observed when the pinhole transport component reaches a certain level. Furthermore, the simulation for whole TOPCon solar cells provides some useful results. For very thin SiO_x (< 1.2 nm), the tunneling provides sufficient high tunneling probability and high efficiency TOPCon solar cells can be obtained without transport through pinholes if the passivation is ensured; while for a relatively thick SiO_x (> 1.2 nm) without the transport through pinholes, the TOPCon solar cell shows a poor fill factor (*FF*) with a high series resistance (*Rs*) because the tunneling does not provide a sufficient high transport channel for carrier transport, and the introduction of a small number of transports through pinholes improves the *FF* and reduces the *Rs*, hence improves the PCE. However, a high possibility for carrier going through pinholes reduces all of the performance parameters and degrades PCE for all the cases simulated. Therefore, an optimized pinhole density and size distribution is critical engineering for solar cell performance optimization. However, the establishment of an optimized method to precisely control the pinhole formation and characterization is still on the way.

1. Introduction

Crystalline silicon (c-Si) solar panels have been dominating the photovoltaic (PV) market since the PV technology become a viable renewable energy source because of the well-developed manufacturing technology with low manufacturing cost, abundant environmentally friendly raw materials, and high-level market acceptance. With the manufacturing technology improvements, the solar cell efficiency has been increased steadily in recent years, especially with some new cell structures introduced to replace the conventional p-type polycrystalline silicon (poly-Si) solar cells with an aluminum back surface field (ABF). Among them, the passivated emitter rear contact (PERC) solar cells have been developed and established a 25.0% world record efficiency in the 90's [1,2]. The PERC technology has been widely incorporated into large volume PV module productions in the PV manufacturing mainstream. Silicon Heterojunction solar cell with Intrinsic amorphous silicon (α-Si:H) Thin-layers (HIT) was also introduced in the 90's and has been proven to be a high efficiency (25.1%) solar cell structure with high open-circuit voltage (V_{oc}) up to 750 mV [3–5]. The combination of the HIT with the Inter-digitized Back Contact (IBC) has resulted in a new world record efficiency of 26.7% [6,7]. In recent years, the HIT technology has been transferred from laboratory to manufacturing in

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several companies. Because of the effective α-Si:H passivation, HIT solar cells have shown several advantages over PERC solar cells such as high V_{oc}, low temperature coefficient, and low manufacturing temperature. However, the manufacturing cost of HIT solar modules is still higher than that of PERC modules because of the low compatibility with the traditional silicon PV manufacturing process and the requirement for unique materials such as low temperature silver paste. To take the HIT advantages in the surface passivation and overcome the manufacturing non-compatibility issue at the same time, a new cell structure with a thin silicon oxide (SiO_x) surface-passivating layer and a doped poly-Si carrier collection contact was proposed. This new structure is named as TOPCon solar cell by taking the abbreviation of Tunnel Oxide Passivating Contact with the assumption of carrier transport through the ultrathin SiO_x (< 2.0 nm) by quantum tunneling [8–10]. The efficiency of TOPCon solar cell has been improved rapidly, and a 25.8% efficiency has been obtained without the IBC contact [11], which is higher than the 25.1% achieved by the HIT structure without the IBC contact [5].

Although the TOPCon cell efficiency has been improved quickly, some fundamental device physics has not been fully understood yet. An example is the carrier transport in the TOPCon structure. It is well known that SiO_2 is a perfect insulator and has been widely used as the insulating dielectric layer in Thin Film Transistors (TFT) in displays [12,13]. It is also an excellent surface passivation layer on c-Si for solar cell application. However, in TOPCon solar cells, photo-generated carriers have to transport through the insulating SiO_x layer, and the transport mechanism is logically assumed to be tunneling. On the other hand, because the SiO_x is very thin and pinholes could easily form during the SiO_x fabrication and/or thermal treatment. Therefore, one has proposed that the carrier transport could be through the pinholes in the SiO_x layer [14–18]. Experimentally, pinholes or weak SiO_x areas are indeed observed by cross-sectional transmission electron microscopy (TEM) [15] and scanning electron microscopy (SEM) on the surface of TOPCon structure with etching back of the doped poly-Si layer [16,17]. Also, current spikes were observed by conductive atomic force microscopy (c-AFM) [14], which could be considered as the evidence of carrier transport through pinholes. These experimental results confirmed the existence of pinholes in the SiO_x passivation layer and carriers could pass through the pinholes in principle. Recently, a temperature dependence dark current density versus voltage (J-V) study by Feldmann et al. [18] suggested that although transport through pinholes exists, the dominant transport is still going through tunneling. Then, the remaining question is how the carrier transport through pinholes affects the cell performance. In a simple word, are pinholes beneficial or harmful for TOPCon solar cell performance?

The objective of this paper is to experimentally identify the existence of pinholes in the SiO_x layer used in high-efficiency TOPCon solar cells and to study the carrier transport mechanisms in the SiO_x layer. In addition, we use a simulation to study the property of transport through pinholes and its effect on the cell performance. The dark J-V and c-AFM measurements confirmed that a portion of carrier transports is through pinholes; the simulation results showed that a proper amount of carrier transport through the pinhole benefits for the TOPCon solar cell performance for the SiO_x of and thicker than 1.0 nm, while too much carrier transport through pinholes degrades the cell performance by a noticeable reduction in all of the performance parameters.

2. Experimental details and simulation

The samples for the dark current-voltage (I-V) measurements were made on commercially available 0.2–2 Ω cm 170-μm n-type Cz c-Si wafers. The sample preparation involved surface damage removal with 25% tetramethylammonium hydroxide (TMAH) solution at 85 °C, followed by RCA chemical cleaning and SiO_x tunnel silicon oxide (SiO_x) growth in 68 wt% HNO_3 acid at 110 °C for 15 min. The resulting tunnel SiO_x thickness was ~1.4 nm, determined by spectral ellipsometry.

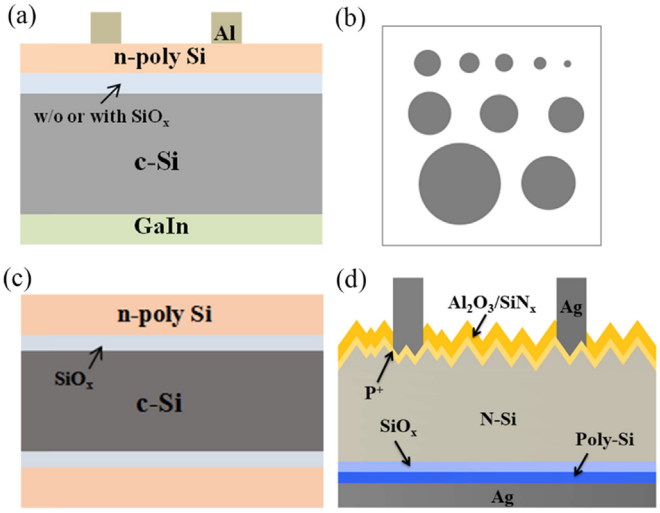

Fig. 1. Schematic drawings of (a) the layer structure of the sample for transport measurements, (b) electrode distribution for the I-V measurements, (c) layer structure of the samples for the passivation measurements, and (d) the TOPCon solar cell structure.

Next, a 40 nm thick phosphorus-doped hydrogenated amorphous silicon (n^+-α-Si:H) layer was deposited on one side using a plasma enhanced chemical vapor deposited (PECVD), followed by an 820 °C annealing for 30 min in an inert atmosphere to facilitate crystallization and dopant activation to turn the n^+-α-Si:H into n^+-poly-Si. After annealing, the front side metal contacts was realized by thermally evaporated Al dots through a shadow mask with various circular openings for different electrode areas and the back electrode was covered by GaIn to form an Ohmic contact with the n-type c-Si wafer. The sample structures were GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al and GaIn/n^+-c-Si/SiO_x/Al, as described in Fig. 1(a), (b). Similarly, the samples for the minority carrier lifetime (τ) measurements were made with the same SiO_x and n^+-poly-Si fabrication process on both sides of the wafers but without the metal contact as shown in Fig. 1(c). The dark I-V characteristics were measured by a Keithley-4200 multi-function meter at the room temperature. The lifetime of the samples with different passivation layers were measured using a Sinton (WCT-120) system and the single-side reverse saturated recombination current density (J_0) and implied open-circuit voltage (iV_{oc}) were extracted from the measured photoconductive decays. The crystalline structure of the n + -poly-Si layer was measured using a Raman spectroscopy (Renishaw inVia-reflex) with 325 nm excitation laser to ensure the laser only probes the coating layer and the influence from the substrate c-Si wafer is minimized. The active phosphorus profile in the TOPCon structure was determined using an electrochemical capacitance-voltage (ECV) system (Buchanan, CVP21).

The TOPCon solar cells fabricated within this study have a designated area of 2 cm × 2 cm and are made of 0.2–2 Ω cm 170-μm n-type Cz c-Si wafers. The solar cell structure is shown in Fig. 1(d). The front side of the solar cells features an alkaline textured (random-pyramids) surface with a boron-doped p^+ emitter (80 Ω/□). Next, the ~1.4 nm tunnel oxide and the 40 nm n^+ poly-Si layers were grown on the rear side according to the process described above. Then a thin Al_2O_3 was deposited by atomic layer deposition (ALD) and a capped SiN_x:H film was deposited by PECVD for front surface passivation and anti-reflection coating. The rear-side full-area electrode was fabricated by thermally evaporated Ag; the front-side grids were realized by lithography technology cooperating with an e-beam evaporated Cr/Pd/Ag seed layer and then thickened by electroplating. The solar cell performance was characterized by one-sun light J-V measurements under a Class AAA solar simulator (Oriel, Sol3A) under AM 1.5 illumination (100 mW/cm^2) at 25 °C.

C-AFM imaging [19–21] was based on the contact mode of AFM

Table 1
(a) Parameters of the transportation structure. (b). Parameters of the TOPCon solar cells.

Layers	Default parameters
(a)	
Front contact boundary	Planar structure, Fix metal work function (4.28 eV, Al electrode)
Front contact	MS Schottky contact model, SRV = 1×10^7 cm/s
n^+ Si layer (with or w/o)	t = 30 nm, $N_d = 4 \times 10^{20}$ cm^{-3}, $\tau = 1 \times 10^5$ μs (default bulk-defect density)
Interface: SiO_x	*Chi* = 1.0 eV, *Eg* = 8.9 eV, *dk* = 3.9, m_e = 0.98, m_h = 0.49
	$D_{ph} = 0, 1 \times 10^{-8}, 1 \times 10^{-6}, 1 \times 10^{-5}, 1 \times 10^{-4}, 1 \times 10^{-3}, 1 \times 10^{-2}$
n-type c-Si layer	t = 200 μm, $N_d = 5 \times 10^{15}$ cm^{-3}, default bulk-defect density
Rear contact	MS Schottky contact model, SRV = 1×10^7 cm/s
Rear contact boundary	Planar surface, Flat band
(b)	
SiNx dielectric	t = 70 nm
Front contact boundary	Standard texture surface (54.74°), w/o absorption loss, flat band
Front contact	MS Schottky contact model, SRV = 100 cm/s (assuming good passivation)
p^+-type Si layer	t = 0.3 μm, *Na* = 2.6×10^{19} cm^{-3}, τ = 1 μs, default bulk-defect density
n-type c-Si layer	t = 200 μm, $N_d = 5 \times 10^{15}$ cm^{-3}, $\tau = 1 \times 10^5$ μs (default bulk-defect density)
Interface: SiO_x	*Chi* = 1.0 eV, *Eg* = 8.9 eV, *dk* = 3.9, m_e = 0.6, m_h = 0.2 (Ue WKB approximation)
	$D_{ph} = 0, 1 \times 10^{-12}, 1 \times 10^{-8}, 1 \times 10^{-6}, 1 \times 10^{-4}, 1 \times 10^{-3}, 1 \times 10^{-2}, 1 \times 10^{-1}, 1$
n^+ Si layer	t = 30 nm, $N_d = 4 \times 10^{20}$ cm^{-3}, τ = 0.1 μs, default bulk-defect density
Rear contact	MS Schottky contact model, SRV = 1×10^7 cm/s
Rear contact boundary	Plane surface, Fix metal work function (4.26 eV, Ag electrode)
Ag electrode	t = 1 μm

(Veeco D5000 and NSV controller) setup in an Ar glove box to prevent oxidation of the Si samples under a bias voltage during the imaging. The Si probe coated with Ti/Pt (Asylum Research AC240TM) was pressed onto the sample surface in a moderate force (~ 50 nN), and the current was measured using a low noise sensor in a current range of 1 pA–100 nA. The sample was biased in Vs = 0.5 V, and the probe was virtually grounded. The contact mode AFM and current images were simultaneously obtained.

We used the AFORS-HET V2.5 simulation program to perform the numerical simulation [22,23] of the transport properties of the designed devices as shown in Fig. 1(a) and the light J-V curve of the TOPCon solar cells as shown in Fig. 1(d). The structures and the parameters of the transport model and the TOPCon solar cell are presented in Table 1(a) and (b), respectively. The optical absorption is described by the multiple reflections and coherence model. The carrier transport through the SiO_x layer is described by the thermionic-emission/thermionic-field model and the quantum tunneling model. The default parameters of the electrical and optical layers are generally referred to the published work [8,9]. The definition of the pinhole is demonstrated as follows. The pinhole of SiO_x is the micro hole through the ultrathin SiO_x in essence, which is caused by the impurity diffusion or by the high-temperature annealing [14,15]. A proportion of bulk carriers will leak through the oxide because of pinholes. Mathematically, the pinhole density can be considered as the proportion of the carriers that leak through the oxide layer, which turns the 2D physics issue into the 1D mathematics manipulation.

where t is the thickness, SRV the surface recombination velocity, N_a and N_d the acceptor concentration and donor concentration, τ the lifetime, *Chi* the electron affinity energy, E_g the band gap, *dk* the relative dielectric constant, m_e and m_h the relative effective mass of electron and hole, D_{ph} pinhole density through the insulator layer (dimensionless unit) as described above, and w/o means without.

3. Results and discussion

We first checked the passivation quality of our TOPCon structure. Fig. 2(a), (b) plot an example of photoconductive decay and lifetime distribution as a function of injection intensity of our optimized double-side TOPCon passivated sample, from which τ = 1.24 μs (at n = 1×10^{15} cm^{-3}), J_0 = 6 fA/cm^2 and iV_{oc} = 731 mV were obtained, indicating a high quality of surface passivation. Fig. 2(c) and (d) show the Raman spectra and the P doping profile, respectively. The Raman spectra show that the n-a-Si:H is in a pure amorphous phase without detectable crystalline features, it is fully crystallized with very little amorphous component remaining after the high temperature (820 °C) annealing. The ECV profile reveals that the P doping concentration in the n^+-poly-Si is about 4×10^{20} cm^{-3} and a tail extends into the n-c-Si wafer as normally observed in TOPCon structures [24]. From the analyses, we conclude that the TOPCon structure studied here could be a good rear side contact for high efficiency solar cell. Because the passivation is of high quality, the characterization results from this structure are meaningful for device analysis and optimization.

We have systematically optimized our TOPCon solar cell design and fabrication processes and improved the cell efficiency to over 21%. Fig. 3 shows the light J-V and EQE curves of our best solar cell with an efficiency of 21.12%. The details of the solar cell optimization will be reported elsewhere. The primary purpose of showing the cell performance here is to demonstrate that the SiO_x/n^+-ploy-Si/Al TOPCon structure is indeed a device grade carrier-selective passivation junction and a reasonable good structure to study the carrier transport.

We first take a simple approach to examine the carrier transport through the ultrathin SiO_x layer in the TOPCon structure by dark J-V measurements. The two kinds of samples as described in the previous section were measured, where the GaIn layer forms a low resistance Ohmic contact with the n-type c-Si wafer. Thus, the J-V characteristics are dominated by the transport mechanism through the top contact formed by the n-c-Si/SiO_x/n^+-poly-Si/Al or n-Si/SiO_x/Al, as shown in Fig. 1(a). The carrier transport through such structures has been very well studied theoretically and experimentally because of the application of tunneling metal oxide semiconductor diodes (MOS or MIS) [25–30]. It has been shown that the J-V characteristic should have a diode behavior when the tunneling process through the SiO_x layer can provide a high enough transport path and the current is limited by the junction in the semiconductor layer; but when the tunneling process current is smaller than the diode current at a higher positive bias and comes the limiting factor for the transport, the J-V curve would level off from the diode characteristic and become linear. However, if the carrier transport through pinholes is the main path, one would expect a linear behavior as if the pinholes are considered as micro-resistors. Therefore, by measuring the dark J-V characteristics of the structures mentioned above, one could find out if the tunneling is the only transport mechanism or additional transport paths exist.

Accurately measuring the dark J-V is very tricky on the samples with high conductivity substrate and a special attention must be paid on

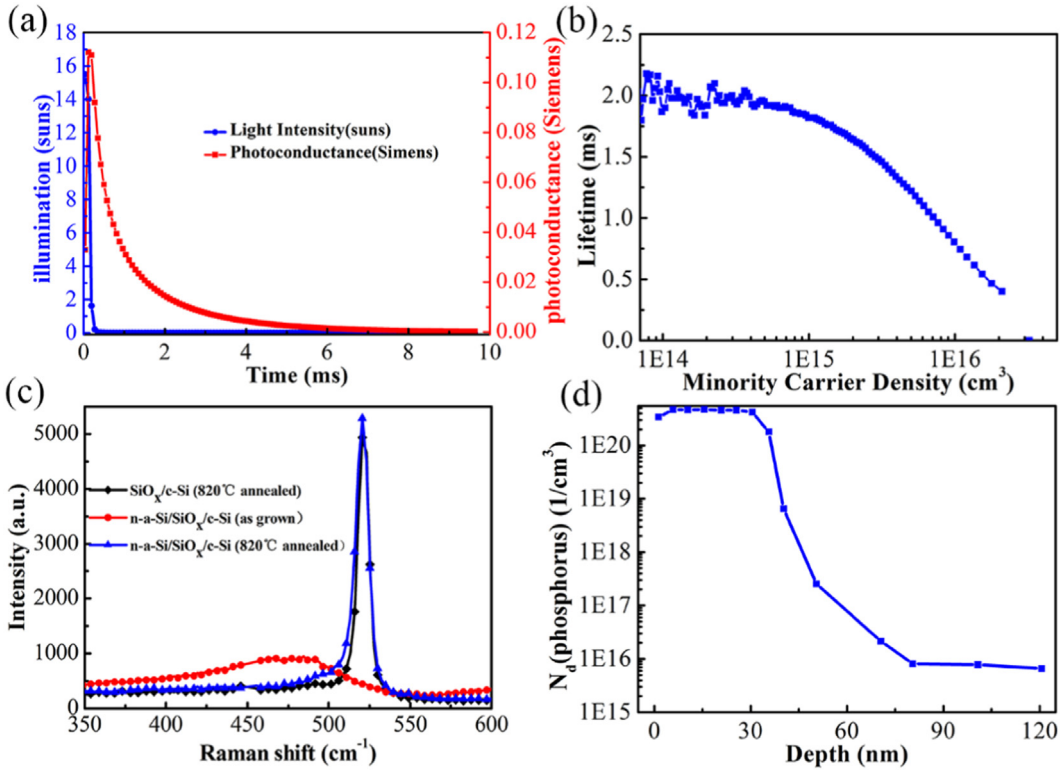

Fig. 2. (a) Conductivity decay, (b) Raman spectra, and (c) doping profile in a TOPCon structure.

the spreading of current outside of the electrode if the carrier diffusion length is comparable to or longer than the thickness of the sample, especially when small area electrode is used. Cox and Strack [31] developed a method to take care of the current spreading effect by measuring the I-V curves with different electrode areas. Fig. 4(a), (b) plots the measured dark I-V characteristics on the GaIn/n-c-Si/SiO$_x$/n$^+$-poly-Si/Al and GaIn/n-c-Si/SiO$_x$/Al structures with various electrode areas. We normalized the measured J-V with the electrode areas and obtained J-V curves and found that the curves do not coincide and large separations still exist even between the relatively large area electrodes, which indicates the current spreading has a large influence on the J-V characteristics. By comparing the slope of the I-V curves as shown in Fig. 4(a), one can obtain the specific contact resistance or called contact resistivity from the plot of measured resistance versus the inverse of electrode area (1/S) as shown in Fig. 4(c). For the sample used in Fig. 4(a), the contact resistivity is 7.7 mΩ.cm^2 from the GaIn/n-c-Si/SiOx/n$^+$-poly-Si/Al sample, which is reasonably small and good enough for high efficiency TOPCon solar cells. Similarly the contact resistivity could be also obtained even if the I-V curves are not linear by taking the derivatives of the I-V curves at the low bias near zero. For the GaIn/n-c-Si/SiOx/Al sample, the contact resistivity is 771 mΩ cm^2, which is larger than the sample with the n$^+$-poly-Si contact layer.

The most important observation is that a perfect linear Ohmic behavior is observed from the GaIn/n-c-Si/SiO$_x$/n$^+$-poly-Si/Al sample, but non-linear curves from the GaIn/n-c-Si/SiO$_x$/Al sample. The results indicate that the carrier transport in the GaIn/n-c-Si/SiO$_x$/n$^+$-poly-Si/Al structure is not a pure tunneling transport, while the J-V curve of the GaIn/n-c-Si/SiO$_x$/Al looks like a mixture of a linear curve with a diode characteristic. The difference between the two samples is one with the n$^+$-poly-Si contact layer and the other without the n$^+$-poly-Si layer. We speculate that the nonlinear behavior from the GaIn/n-c-Si/SiO$_x$/Al is caused by the band bending in the n-c-Si induced by the Al contact because of the different work functions, which normally forms a MOS diode. The imperfect of the diode characteristic in the sample without the n$^+$-poly-Si layer is an indication of a second carrier path exists, and it could be through pinholes even without the n$^+$-ploy-Si contact layer.

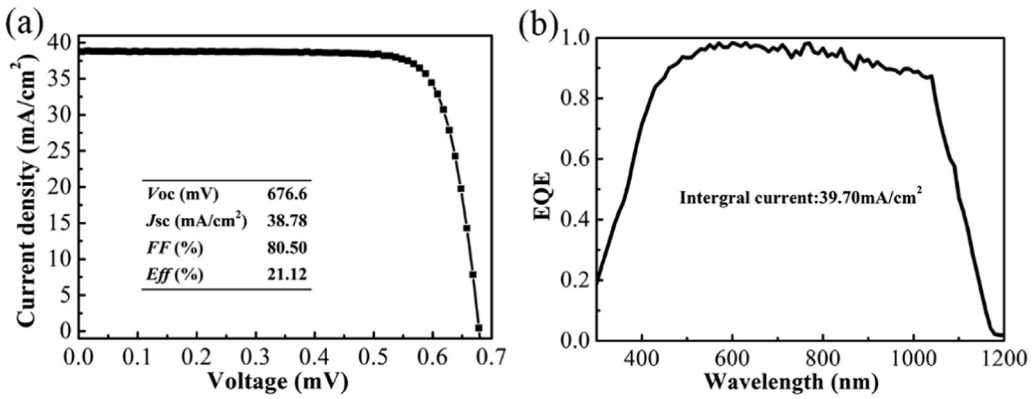

Fig. 3. (a) The J-V characteristics and (b) EQE spectrum of a TOPCon solar cell with an efficiency of 21.2%.

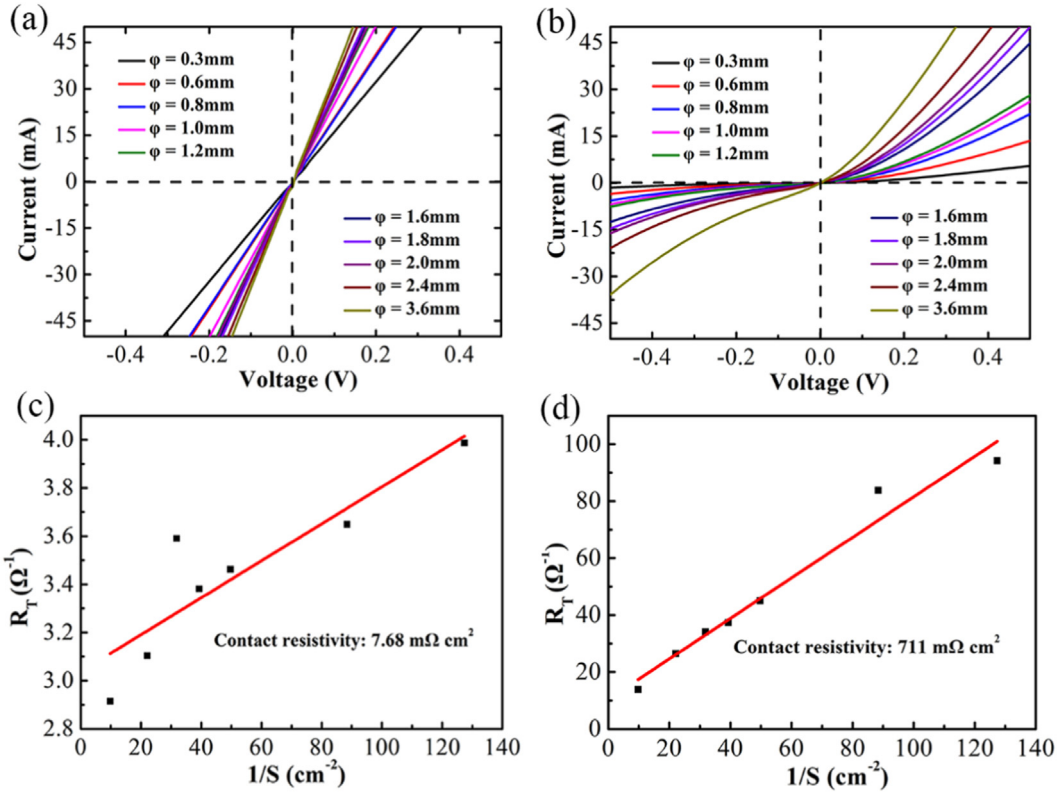

Fig. 4. Dark I-V curves of the (a) GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al and (b) GaIn/n-c-Si/SiO_x/Al samples, (c) and (d) the Cox and Strack plots for the two samples in (a) and (b), respectively.

While the band bending occurs in the n^+-poly-Si/Al interface in the sample with the n^+-poly-Si layer, where Ohmic contact forms because the doping concentration in the n^+-poly-Si is much higher than in the n-Si wafer. In addition, the diffusion of P through the SiO_x into the c-Si wafer might also promote to form an Ohmic contact, which contributes to the difference between the samples with and without the n^+-poly-Si layer. The key point is that the carrier transport through the ultrathin SiO_x layer exhibits an Ohmic behavior, which confirms that the carrier transport through the ultrathin SiO_x is not a simple tunneling process and additional paths such as through pinholes should be involved.

To find out the additional transport channels through the insulating ultrathin SiO_x layer, we did c-AFM measurements on the sample surface of c-Si/SiO_x/n^+-poly-Si without the Al contact. Fig. 5 shows an example of the c-AFM images. First, some current spikes are observed on the surface, which we believe the high current areas are the transport through the pinholes, or weak-insulating oxide areas where charge carriers can transport by hopping through defect state in the ultrathin SiO_x layer, however, the weak-insulating areas are also referred "pinhole" through the paper. Second, the sizes of the pinholes are highly non-uniform, generally 2–10 nm in diameter. These measured pinhole sizes should be larger than the actual pinhole sizes because current routes through the pinholes spread out with a distance away from the pinholes in the n^+-poly-Si layer. The measurements were taken with a small scan size of 120 nm by 120 nm to have a high resolution on the pinholes. Third, there are some non-uniformities from locations to locations on a sample, and therefore the statistics for estimation of the pinhole density is not very reliable, but a rough estimation gives the pinhole density in the order of 10^{10}/cm^2. Nevertheless, we may conclude that there are indeed some pinholes in the ultrathin SiO_x in our TOPCon structure, which was used in real high-efficiency solar cells. We note that the surface morphology in this small scan area is relatively flat, with the roughness less than 2 nm and overall corrugation about 5 nm. This flat surface does not generate artifact of the current spikes as shown in the images that no correlation of the current and topography was observed.

Although we have confirmed that quantum tunneling is not the only mechanism for carrier transport in the TOPCon solar cells and the transport through pinholes indeed exists, a remaining question is whether the transport through pinholes benefits for solar cell performance. If the pinholes are good for the solar cell performance, it needs to understand how much carrier transport through pinholes is the optimum for solar cell efficiency; but if the transport through pinholes is harmful to the cell performance, it is desired to figure out the tolerance level for the transport through pinholes. For this purpose, we did a systematic simulation study on the carrier transport in the TOPCon structure and the solar cell performance as a function of pinhole transport.

Actually many simulation works have been reported in the literature [23,32,33]. Steinkemper et al. [32] did a systematic simulation study of TOPCon solar performance as a function of various material and structure parameters such as the surface recombination speed and SiO_2 thickness with the assumption of the transport through tunneling only without considering the transport through pinholes. The contribution from Peibst et al. [33] considered the transport through pinholes, and studied the correlation between recombination saturation current J_0 and contact resistivity without the correlation to TOPCon solar cell performance. Here we are aiming the effluence of carrier transport through both tunneling and pinholes and study the correlation of TOPCon cell performance as a function of the degree of pinhole transport.

First, we examine the case without any pinholes with the assumption of the pure tunneling transport. From the experimental results, we learned that TOPCon solar cell performance is affected by the SiO_x properties such as fabrication process and layer thickness significantly, which agrees with the reported ones in the literature [34]. Fig. 6 presents a set of simulation results for the carrier transport in the TOPCon

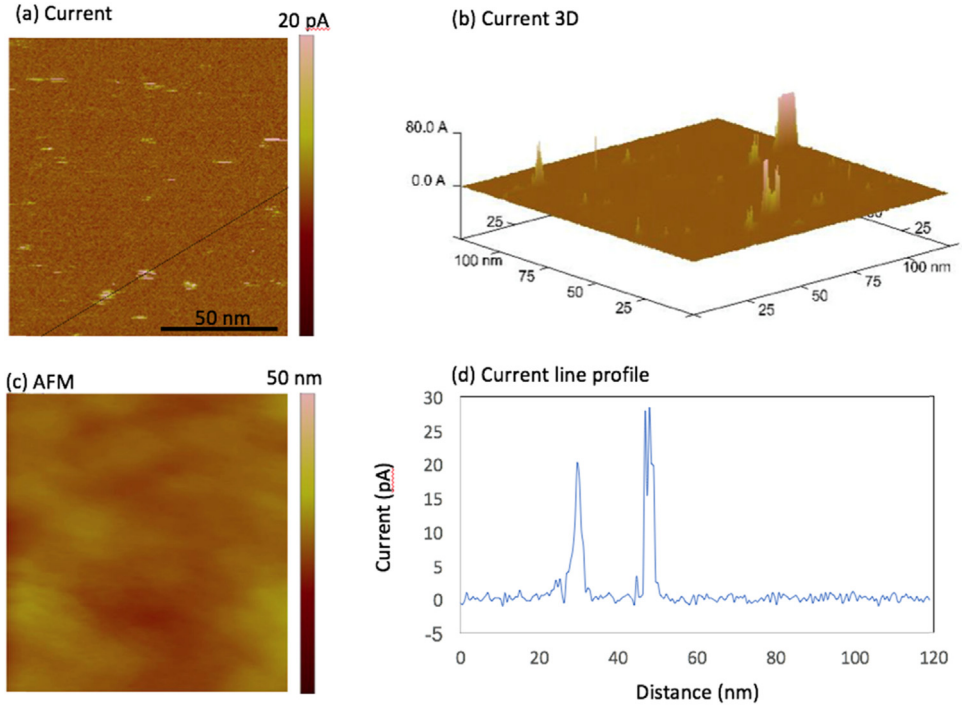

Fig. 5. c-AFM and AFM images from a c-Si/SiO_x/n^+-poly-Si structure. (a) a planar view of the c-AFM image, (b) a 3-D image, (c) the corresponding AFM image, and (d) a line plot along the line in (a).

structures as used for the J-V measurement in Fig. 4(a), (b), where (a) and (b) are for the sample without the n^+-poly-Si contact layer in the linear and semi-logarithmic, respectively; (c) and (d) are the same plots for the sample with the n^+-ploy-Si contact layer. Noted that the simulation is one dimensional calculation and does not consider the lateral transport, and therefore no current spreading effect is included. For the sample without the n^+-poly-Si layer, a set of diode characteristics is obtained for different SiO_x thicknesses with the turn-on voltage increasing with the increase of the SiO_x layer thickness. A perfect linear behavior in the low positive voltage in the semi-logarithmic plot indicates a perfect diode characteristic, and it levels off at high positive biases, indicating the tunneling cannot provide a high enough transport path and becomes the limiting factor for the current flow. This result agrees well with the analysis from Shewshun et al. [26]; the reverse saturated current density decreases significantly with the increase of the SiO_x thickness; finally, for the case of no SiO_x layer, an Ohmic

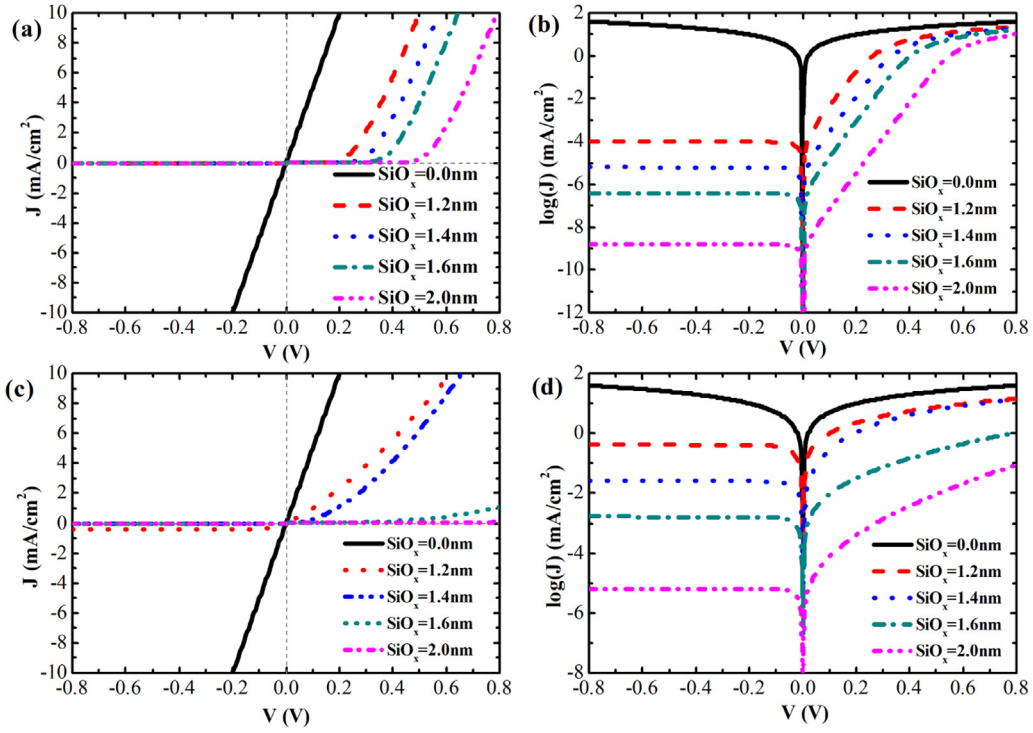

Fig. 6. Simulated J-V characteristics of (a, b) GaIn/n-c-Si/SiO_x/Al and (c, d) GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al.

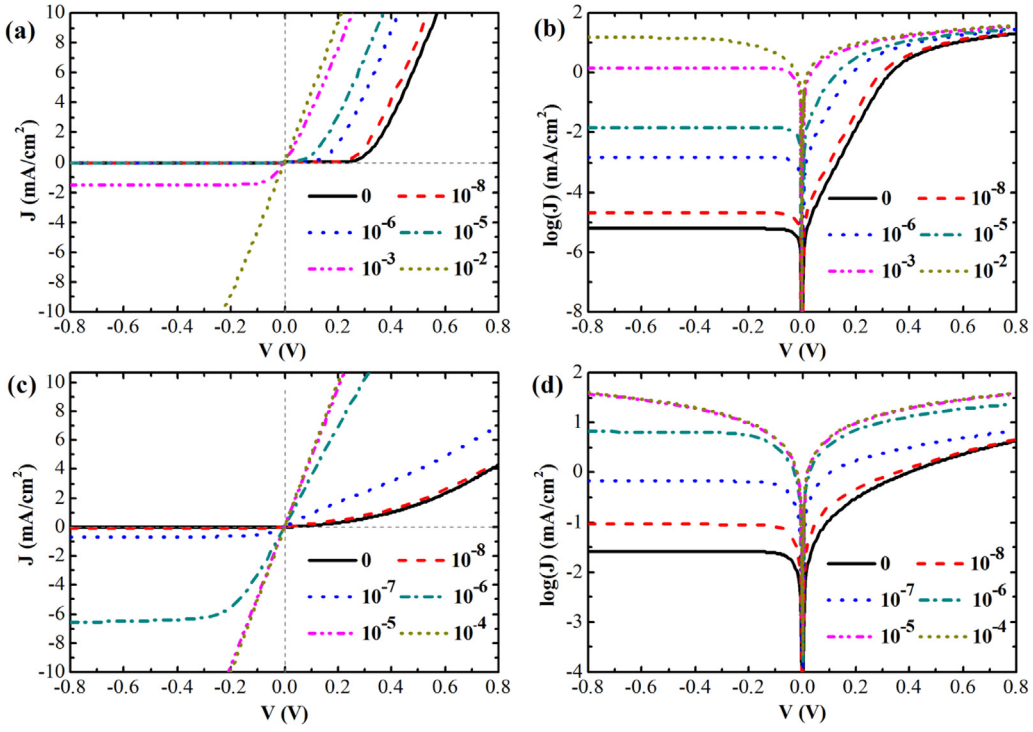

Fig. 7. Simulated J-V characteristics of (a, b) the GaIn/n-c-Si/SiO_x/Al, and (c, d) GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al structures with different magnitudes of transport possibility through pinholes, where the SiO_x thickness is 1.4 nm, similar to what used in the real TOPCon solar cells.

straight line is obtained. The situation for the sample with the n^+-poly-Si contact layer shows three major differences from the results of no n^+-poly-Si contact layer sample. First, the forward current turns on at a much smaller voltage; second, the forward curves are no longer in a linear form in the semi-logarithmic plot, indicating an imperfect diode characteristic; third, the magnitude of the reverse saturated current density is significantly higher than from the sample without the n^+-poly-Si contact layer. The key points that we learned from the simulation results are that a non-linear rectification behavior is obtained when an ultrathin SiO_x is inserted between the c-Si wafer and the back metal contact, and the transport property is sensitive to the thickness of the SiO_x layer.

As observed experimentally, a linear behavior forms in the TOPCon contact with the SiOx layer that produces a good solar cell performance (Fig. 4), and the transport through pinholes exists from the c-AFM measurements (Fig. 5), we simulated the transport properties in the TOPCon structure including the transport through pinholes. Fig. 7 plots the simulated dark J-V curves of two sample structures as shown in Fig. 6 with various possibilities of transport through pinholes, where the SiO_x thickness is fixed at 1.4 nm which is consistent with the value used in our real TOPCon solar cells. The plots of Fig. 7(a), (b) are for the sample without the n^+-poly-Si contact layer, where the introduction of the transport through pinholes shifts the turn-on voltage to small values, increases the reverse saturated current, and keeps the similar shape of the curves as if the SiO_x layer is reduced by the pinholes. In addition, a linear part in the negative bias appears as the pinhole current increase, and it extends to large voltage range to form a linear Ohmic characteristic when the transport possibility through pinholes reaches to 10^{-2}. Similar to the case of different SiO_x thicknesses, the J-V curves of the GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al sample do not show the perfect diode characteristics; a small magnitude of pinhole transport increases both the forward and reverse currently noticeably (10^{-7}); the linear behavior appears with a much smaller possibility of transport through pinholes than in the GaIn/n-c-Si/SiO_x/Al sample, as shown in Fig. 7(c), (d). When the possibility of pinhole transport is larger than 10^{-4}, all of the simulated curves come together, implying the transport is limited by the bulk of the c-Si instead of the junction. From the simulation results, we find that although the transport through pinholes is one of the transport channels, and a small amount of pinhole transport already affects the dark J-V characteristics significantly, the major transport is still through the quantum tunneling, which is consistent with the recent dark J-V measurements at different temperatures [18]. We also simulated the double-side passivated sample structure with 1.4 nm SiOx. The J_0 and iVoc values with different transport probabilities through pinholes are listed in Table 2, with the comparison of measured values. It shows that the transport through pinholes increases the J_0 and reduces the iVoc, which means it degrades the passivation quality.

From the transport study, we learn that in addition to the tunneling, the transport through pinholes affects the J-V characteristics of the junction significantly. Therefore, it is logical to expect the transport through pinholes could affect the real TOPCon solar cell performance. For this purpose, we simulated the solar cell performance as a function of the possibility of carrier transport through pinholes. Fig. 8 plots the AM1.5 light J-V curves and performance parameters of the TOPCon solar cells with various pinhole transport possibilities, where four sets of SiO_x layer thicknesses of 0.6 nm, 1.0 nm, 1.4 nm, and 1.6 nm are used. Very interesting observations are made. First, Fig. 8(a) plots the

Table 2
J_0 and iV_{oc} of TOPCon structure: n-type c-Si (5×10^{15} cm^{-3}, 200 μm)/SiO_x(1.2 nm, w/o D_{it}, D_{ph} is variable)/n^+-poly-Si film (4×10^{20} cm^{-3}, 50 nm) / contact (S = 1×10^7 cm/s). The measured data are also included as a comparison.

D_{ph}	J_0 (fA/cm^2)	iV_{oc} (mV)
< 1e-6	4.5	743
1e-4	4.6	742
1e-2	10.0	724
0.1	21.5	705
1	26.0	700
Measured	**6.0**	**731**

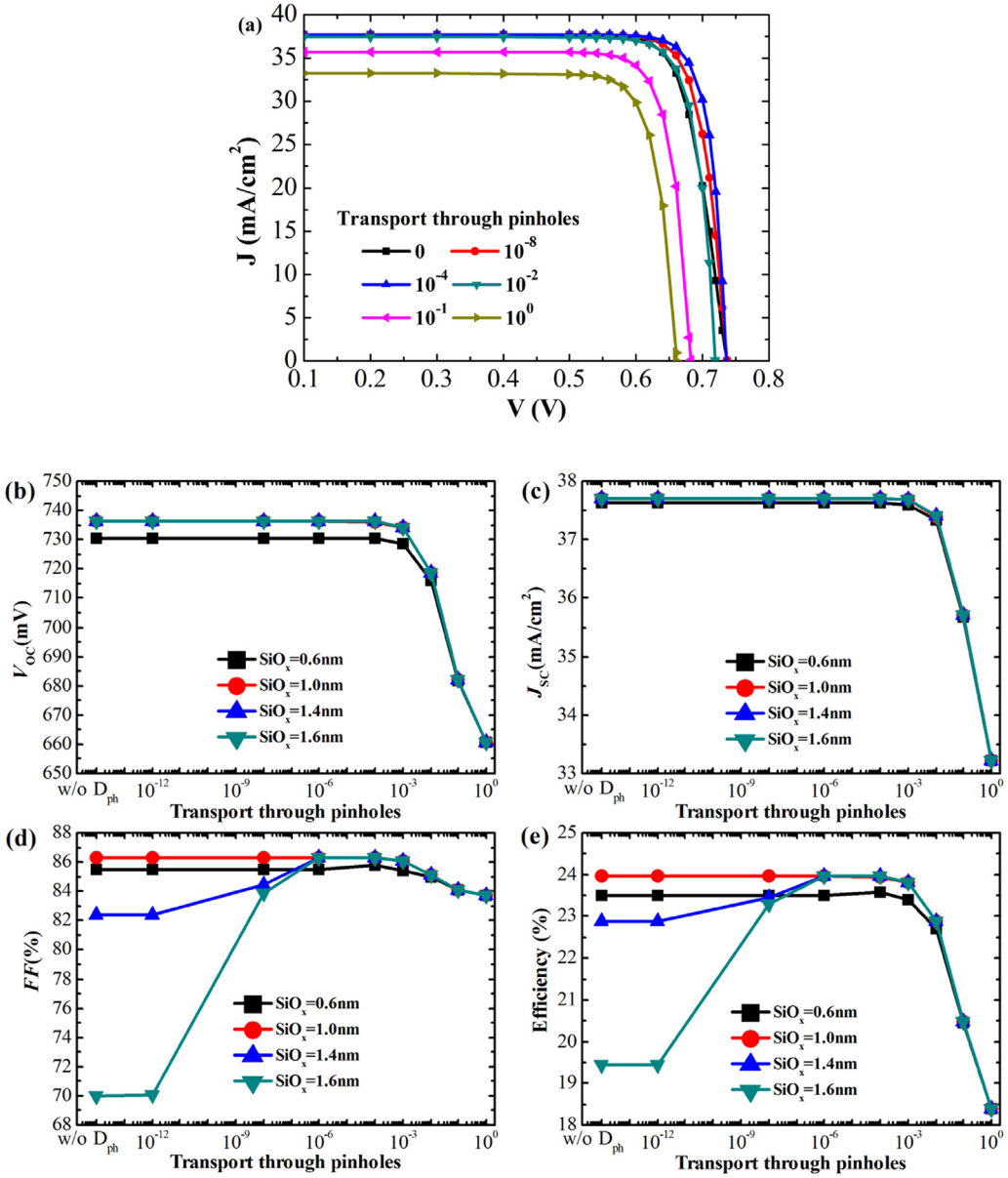

Fig. 8. (a) the J-V curves of the TOPCon solar cell performance as a function of the possibility of transport through pinholes for the SiO_x thickness of 1.4 nm. (b) to (e) the performance parameters of the four sets of solar cells (with the SiO_x thickness of 0.6, 1.0, 1.4, and 1.6 nm) as a function of the possibility of transport through pinholes.

light J-V curves of TOPCon solar cells with 1.4 nm SiO_x and various transport possibilities through pinholes. It shows that without transport through pinholes, a poorer fill factor (*FF*) is observed; a small amount transport through pinholes improves the *FF*; while too much transport through pinholes ($> 10^{-2}$ in this case) degrades the *FF*, V_{oc}, and J_{sc} significantly. Second, Fig. 8(b)-(e) plot the performance parameters as a function of transport probability through pinholes. It shows that in the low pinhole transport region ($< 10^{-3}$), when the solar cells are with a SiO_x layer of equal to or less than 1 nm, the *FF* is not affected by transport through pinhole. In this case, the ultrathin SiO_x layer provides high enough tunneling current to allow most of the photo-carrier passing through the SiO_x layer freely. However, when the solar cells have a SiO_x layer of more than 1.4 nm, the *FF* will be changed significantly by the transport through pinholes. For the solar cells with relatively thick SiOx (1.4 nm and 1.6 nm), the pure tunneling transport cannot provide enough transport channels, limits the current flow, and results in a high series resistance (*Rs*) and a poor *FF*. With the introduction of the transport through pinholes, the *Rs* decreases and *FF* increases, hence efficiency increases as well to reach the maximum at the pinhole transport probability around 10^{-5} to10^{-4}. In the high pinhole transport region ($> 10^{-3}$), increasing the pinhole transport further, all of the three performance parameters (V_{oc}, J_{sc}, *FF*) start to drop for all of the SiO_x thicknesses and leads to a decrease of efficiency. The observations can be explained by the simulation results of the transport through the TOPCon contact as an example shown in Fig. 7 with 1.4 nm SiOx. With the pure tunneling transport, the non-linear J-V characteristic shows a high derivative resistance, corresponding to a high series resistance, therefore results in a poor *FF*. When pinholes are included, in addition to the transport through tunneling, the carriers can also pass the ultrathin SiO_x in TOPCon junction through pinholes, which reduces the *Rs*, and therefore, improves the *FF* and efficiency until reaching the maximum. However, increasing the pinhole transport further equivalently adds a shunt path and reduces the carrier built up at the junction under the open circuit condition, therefore reduces the V_{oc}. Furthermore, the exceeding pinholes could also reduce the passivation quality, increase the interface recombination, and degrade the cell performance

in reality. From the simulation study, we learn that a proper amount pinholes in the ultrathin SiO_x passivation layer are needed for high-efficiency TOPCon solar cells with a thick enough SiO_x such as 1.4 nm, which is essential for improving the *FF*, however, a low V_{oc} in real solar cells could indicate too much transport through pinholes in addition to other causes such as a poor passivation. Experimentally, how to select a proper SiO_x thickness and control the pinhole density with the compromising the effective passivation, which needs a minimum SiO_x thickness, to reduce the interface defect state and control the P diffusion through the SiO_x layer into the c-Si bulk is a kind of technical art, and a significant effort is needed for the optimization of the material properties and device structure.

4. Summary

In summary, the dark J-V measurements show a linear Ohmic behavior of carrier transport in the high-quality TOPCon junction used in our high-efficiency solar cells, implies that a separated transport path exists in addition to the quantum tunneling. The c-AFM measurements reveal some high current spikes over the area of the TOPCon junction, which are reasonable to be assigned to the transport through pinholes. Therefore, we conclude that the transport through pinholes is one of the transport mechanisms in TOPCon solar cells. From the dark J-V simulation studies, we learn that 1) as expected, the pure tunneling transport in the TOPCon structure without pinhole results in a diode characteristic in the low bias, indicating the tunneling can provide enough transport in this low bias condition, and levels off from the diode characteristics due to the limited tunneling possibility, which is in consistent with the theoretical analysis [26]; 2) the SiO_x thickness affects the transport significantly; 3) the introduction of transport through pinholes increases both the forward and reverse current largely and essentially changes the transport into a linear Ohmic behavior; 4) the insertion of the n^+-poly-Si contact layer increases both the tunneling current and the current through pinholes, which leads to the transition from rectification to linear at a much lower possibility through pinholes than the case without the n^+-poly-Si contact layer. Furthermore, from the simulation of TOPCon solar cell performance as a function of pinhole transport, we observed that for the solar cells with a relatively thin SiO_x ($\leq$ 1.0 nm), the cell performance is not affected by the transport through pinholes in the low pinhole transport probability ($< 10^{-3}$) regime, but declines at the high hole transport probability ($< 10^{-3}$) regime. With a relatively thick SiO_x ($\geq$ 1.0 nm), the TOPCon solar cell without pinhole transport shows a poor *FF* with a high *Rs*. The introduction of pinholes improves the *FF* by reducing the *Rs*, and hence improves the efficiency. In our case, the possibility of transport through pinholes in 10^{-4} results in the highest efficiency. Increasing the transport through pinholes further leads to a reduction of all performance parameters and efficiency. In the real experiments, how to select the SiOx thickness and control the pinhole density and the amount of transport through pinholes is a great challenge for high-efficiency TOPCon solar cells.

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