Solar Energy Materials & Solar Cells 208 (2020) 110423

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: http://www.elsevier.com/locate/solmat

Influence of SiO_x film thickness on electrical performance and efficiency of TOPCon solar cells

Qinqin Wang [a,c,1], Wangping Wu [a,b,d,*,1], Ningyi Yuan [a,c,**], Yali Li [c,***], Yi Zhang [b,d,****], Jianning Ding [a,e]

[a] Jiangsu Collaborative Innovation Center of Photovoltaic Science and Engineering, Changzhou University, Changzhou, 213164, PR China
[b] Electrochemistry and Corrosion Laboratory, School of Mechanical Engineering, Changzhou University, Changzhou, 213164, PR China
[c] School of Materials Science and Engineering, Changzhou University, Changzhou, 213164, PR China
[d] Changzhou High Technology Research Key Laboratory of Mould Advanced Manufacturing, Changzhou University, Changzhou, 213164, PR China
[e] Institute of Intelligent Flexible Mechatronics, Jiangsu University, Zhenjiang, 212013, PR China

ARTICLE INFO

Keywords:
TOPCon solar cell
Tunnel oxide
P diffusion
Efficiency
Simulation

ABSTRACT

The tunnel oxide passivated contact solar cells (TOPCon) on n-type Cz Si wafers instead of passivated emitter and rear solar cells are currently migrated to mainstream production, with ongoing improvements in recent years. In this study, we investigated and characterized one recent batch of TOPCon cells fabricated on 156.75 × 156.75 × 0.18mm^3 wafers with fully screen-printed technology by an industrial-type process. TOPCon cells with an efficiency as high as 22.43%, a Voc value as high as 689.4 mV, and a fill factor as high as 81.35% were obtained. The P dopant diffusion in the poly Si layer as well as the thickness of the SiO_x layer were optimized in order to obtain good electrical contact between screen-printed Ag and Si. The thickness of the SiO_x layer should be over 1.5 nm, which is beneficial for obtaining a good passivation for the cells. The surface P dopant concentration in the polycrystalline Si was higher than 1×10^{20} atom/cm^3, resulted in a low series resistance and a high fill factor. The characterization and simulation results show that both metal shading loss and rear surface recombination were dominant among all of the losses. Application to solar cells with a Voc of 697 mV and a fill factor of 82.45% could lead to an independently confirmed cell efficiency of over 23% for n-type cells with poly Si the herein developed passivated rear contacts, and the front metal contacts by addressing the issue of reducing metal recombination and implementing a selective emitter.

1. Introduction

Currently, passivated emitter and rear solar cell (PERC) is the mainstream production with a median efficiency of 22%. However, it is hard to increase cell efficiency by the present technologies and processes. There are two key factors limiting the efficiency of crystalline silicon solar cells. One is recombination at the metal contacts and the other is loss caused by two- or three-dimensional current transport paths. In order to overcome the two issues, a tunnel oxide passivated contact (TOPCon) cell structure has been proposed and developed, which could achieve an ultra-high efficiency of 25.8% without an interdigitated back contact [1]. TOPCon consists of an ultra-thin tunnel oxide and a P-doped Si layer [2–4]. It offers a simple processing scheme, which is compatible with high-temperature process, such as diffusion. For this solar cell structure, a rear-side full-area metal contact passivated by tunnel oxide provides one-dimensional current transport and significantly reduces metal contact recombination. The fabrication of TOPCon requires three-step process. Firstly, the growth of an interfacial oxide layer, then the deposition of an amorphous (or polycrystalline) Si-based layer, lastly a high-temperature anneal process. The purpose of the interfacial oxide layer is to reduce dangling bonds and thus interface trapped charge density [5–9]. In TOPCon solar cells, photogenerated

* Corresponding authors. Jiangsu Collaborative Innovation Center of Photovoltaic Science and Engineering, Changzhou University, Changzhou, 213164, PR China.
** Corresponding author. Jiangsu Collaborative Innovation Center of Photovoltaic Science and Engineering, Changzhou University, Changzhou, 213164, PR China.
*** Corresponding authors. School of Materials Science and Engineering, Changzhou University, Changzhou, 213164, PR China.
**** Corresponding author. Electrochemistry and Corrosion Laboratory, School of Mechanical Engineering, Changzhou University, Changzhou, 213164, PR China.
E-mail addresses: wwp3.14@163.com (W. Wu), nyyuan660211@163.com (N. Yuan), liyali@cczu.edu.cn (Y. Li), zy@cczu.edu.cn (Y. Zhang).
[1] These authors contributed equally to this work.

https://doi.org/10.1016/j.solmat.2020.110423
Received 12 July 2019; Received in revised form 14 January 2020; Accepted 16 January 2020
Available online 23 January 2020

carrier transport through the tunnel oxide layer is important. The transport mechanism is assumed to be tunneling or transport through pinholes which easily form during the SiO_x fabrication and/or thermal treatment. The appropriate oxide's thickness is also important for passivation.

A thin passivating interlayer is introduced between the high recombination regions at the metal-semiconductor interface to reduce the total recombination/emitter saturation current density (J_0), resulting in a high open-circuit voltage (Voc) [10–13]. However, the interlayer must passivate the Si surface without interfering with the majority carrier transport to ensure a good fill factor (FF) and efficiency (Eff). For example, the heterojunction Si cell with intrinsic thin amorphous layer (HIT) could produce the cell Voc of 750mV with Eff over 25% [10,11]. However, this passivation scheme could not withstand temperature above 250 °C for the metallization process. To obtain highly efficient passivated contacts for solar cells, three prerequisites have to be met [14]: (i) excellent interface passivation, (ii) efficiently doped layers to maintain the quasi-Fermi level separation in c-Si (high Voc), and (iii) an efficient majority carrier transport (high FF).

In this study, TOPCon solar cells featuring screen-printed metal contacts on both sides were fabricated from 156.75 × 156.75 × 0.18 mm^3 n-typeCz Si wafers by an industrial-type process. The tunnel oxide layers with three different thicknesses were obtained by annealing process at temperature 550–650 °C. The influence of the SiO_x layer thickness and the P concentration in the poly Si layer on the efficiency, Voc, FF, series resistance of TOPCon solar cells is investigated. The increase in cell efficiency of TOPCon cells in mass production is analyzed and discussed.

2. Experimental

2.1. TOPCon cell process

TOPCon cells with round chamfer were manufactured from commercially available 156.75 × 156.75 mm^2 n-type Cz Si wafers with resistivity of 0.5–2 Ω cm. The thickness of the Si wafers was 180 ± 10 μm. The industrial-type processes of TOPCon solar cells were: texture → BCl_3 diffusion → rear side etching → tunnel oxide layers → LPCVD → $POCl_3$ diffusion → BSG/PSG removal → front side passivation film → rear side passivation film → screen printing and firing. All wafers were textured in alkaline solution and then cleaned with a mix of HCl and HF. The front emitter was formed in a quartz tube furnace containing BCl_3 gas. Subsequently, the rear side was etched in a mix of HF and HNO_3. A thin interfacial oxide layer was grown in a tube furnace. In this study, there are three different thicknesses of the SiO_x layers. Table 1 shows the process conditions for growing SiO_x layer with different thicknesses. The amorphous Si (a-Si) layer was deposited by LPCVD process with a mean layer thickness of 220 ± 20 nm on both sides. The thickness of the SiO_x and a-Si layers was measured by spectroscopic ellipsometry using software SpectraRay/3 (SE800 PV). A high-temperature annealing and P diffusion were performed at 850 °C for 1 h in a mix of $POCl_3$, O_2 and N_2. In this step the a-Si is converted to poly Si and the initial surface passivation quality is enhanced slightly. In next cleaning BSG/PSG removal step, the front wrap around side was etched using 5 wt% tetramethylammonium hydroxide (TMAH) solution in order to obtain only one side with P-doped poly-Si layer. Then, the front and rear passivations of the cells were fabricated by ALD-4.7nm thick AlO_x and PECVD-80nm thick SiN_x dielectric stacks, respectively. The metallization was applied by screen printing and firing of a metal paste using a H-pattern grid design on both sides of the wafers. The metal area fraction on the front side is about 2.74%. The fast firing in a conveyer belt furnace was set at a peak temperature of 865 °C. Dupont Ag–Al paste and Dupont Ag paste were used for the front and rear sides, respectively. The schematic of a n-type TOPCon solar cell featuring a boron-diffused emitter and a passivating rear contact is displayed in Fig. 1.

Table 1
Parameters for the preparation of SiO_x layer with different thicknesses.

Item	Temperature (°C)	Time (min)	O_2 (sccm)	Thickness (nm)
Condition 1	550	20	2000	1.55
Condition 2	600	15	2000	1.25
Condition 3	650	12	2000	1.43

2.2. Characterization

The current-voltage (I–V) parameters and curves of the TOPCon cell were measured in-house with DENKEN tester after calibration using a standard cell by Fraunhofer ISE. The dopant profiles of monitor wafers were measured by ECV device (WEP CVP21). The ECV-profiling technique is employed to measure the dopant distribution and the concentration of free carriers. The implied Voc (*i*Voc) values were measured on control wafers by WCT-120 Sinton lifetime tester (Boulder, CO, USA) [15]. The saturation current density J_0 of the poly layers was tested by a contactless flash-based photoconductance decay tester (WCT-120 Sinton, Boulder, CO, USA) in the transient mode in the range from 1×10^{15} to 2×10^{16} cm^{-3}, and the internal quantum efficiency (IQE) was measured by PVE300-IVT. The contact resistivity (R_c) of screen-printed metallization on solar cells featuring tunnel oxides with different thicknesses was measured by transfer-length-method (TLM, GP-4 TEST). Fig. 2 shows the principle diagram of transfer-length-method. The resistance that was measured between two fingers consists of diverse parts as following equation (see Fig. 2a):

$$R_{measured} = 2R_{tip} + 2R_c + d \times R_{sheet} \quad (1)$$

where R_{sheet} is the sheet resistance of poly Si layers, R_{tip} is identical to the resistance between the two tips on the same finger and therefore can be eliminated. The Eq. (1) can be reduced as following equation (2):

$$R_{measured} = 2R_c + d \times R_{sheet} \quad (2)$$

In the SiO_x/poly Si layer, the gap model was obtained using laser isolation between two fingers, as shown in Fig. 2b. Then, The values of contact resistivity R_c could be calculated by several measurements in order to remove R_{sheet} value. At the same time, the contact resistivity can estimate the quality of tunnel oxide layer.

In each batch, a set of Si wafers was only partially processed to serve as monitor wafers for saturation current density J_0. In this study, high

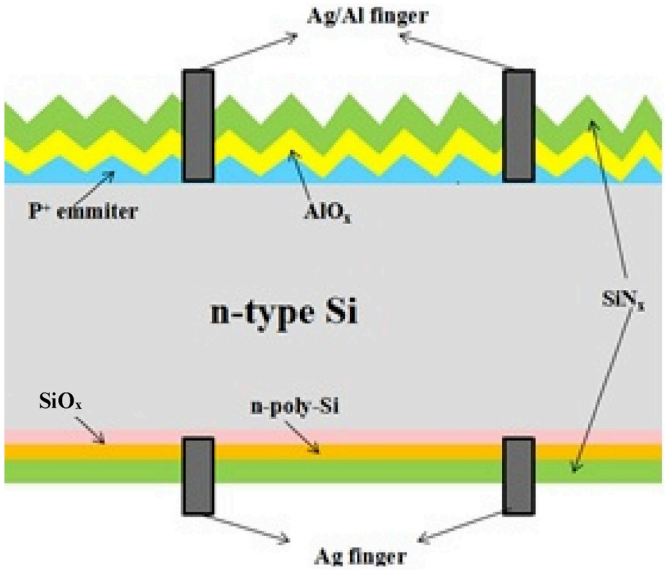

Fig. 1. Schematic of a n-type TOPCon solar cell featuring a boron-diffused emitter and a passivating rear contact.

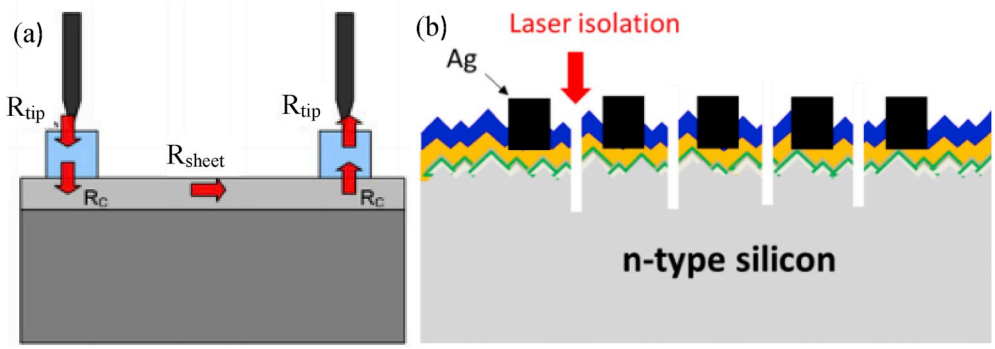

Fig. 2. Principle diagram of transfer-length-method (a) the resistance between two fingers (b) laser isolation between two fingers.

resistivity n-type Cz silicon wafers (10 Ω cm) were used. The texturing, LPCVD, P diffusion and SiN_x processes were the same as for all the solar cells because all monitoring wafers were processed simultaneously with the cells. Fig. 3 shows the schematic diagram of cross-sectional monitoring wafers, which was composed of thin SiO_x, n-type polycrystalline Si and SiN_x layers on both sides of n-Si wafers.

The optical reflection of the solar cells was measured with PVE300-IVT from pv-tools. Simultaneously, an optical loss analysis by above results was carried out by Current Loss Analysis Calculator V1.4 provided by Solar Energy Research Institute of Singapore.

The silicon wafers with as-fabricated oxide layers, without growth of amorphous Si and P doping processes, were directly annealed at 850 °C for 1h under a nitrogen atmosphere, and then etched with 15 wt% TMAH solution at 80 °C for 1min and 2min, in order to observe the surface quality of the oxide layer. The surface morphology of the as-fabricated and as-annealed, and as-etched oxide layers was observed at five locations to confirm defects distribution by an optical microscopy (Olympus, DSX100/DSX500/DSX500i).

3. Results and discussion

3.1. I–V parameters

Table 2 shows the I–V parameters of TOPCon cells. The best solar cell with Eff as high as 22.43% and a Voc value as high as 689.4 mV with tunnel oxide prepared at 550 °C for 20 min (condition 1, 1.55 nm SiO_x) was obtained. The difference among the three conditions is the temperature and duration, resulting in the difference in the thickness of the tunnel SiO_x layer (see Table 1). Fig. 4 shows the plots of Voc, short-circuit current density (J_{sc}), FF and Eff values of TOPCon cells fabricated by three different conditions, where the plot heights have median values. The same low Voc value of about 680 mV was obtained for the cells with 1.25 nm and 1.43 nm thick SiO_x layers. The lowest FF and highest series resistance were obtained for cells with 1.25 nm thick SiO_x. The best TOPCon cells with the highest Voc, J_{sc}, FF and Eff were obtained from the cells with 1.55 nm thick SiO_x (Fig. 4 and Table 2). During annealing at 800–900 °C for 1h in an oxygen-free atmosphere, the following reaction takes place:

$$SiO_2 + Si \rightarrow 2SiO(g) \quad (3)$$

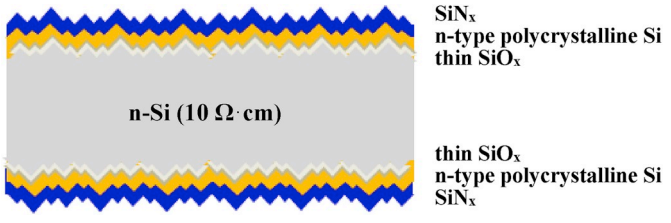

Fig. 3. Schematic diagram of cross-sectional monitoring wafers.

Table 2
I–V parameters of TOPCon cells.

Item		Voc (mV)	J_{sc} (mA/cm^2)	R_{ser} mΩ	FF (%)	Eff (%)	Cell area (cm^2)
Condition 1	Median	687.1	39.92	4.64	81.09	22.25	244.32
	Best cell	689.4	40	4.34	81.35	22.43	
Condition 2	Median	679	39.82	6.18	78.5	21.23	244.32
	Best cell	682.2	39.91	5.97	78.71	21.43	
Condition 3	Median	680.1	39.8	5.23	79.94	21.7	244.32
	Best cell	684	39.94	5.22	79.78	21.79	

Voc: open circuit voltage.
J_{sc}: short circuit current density.
R_{ser}: series resistance.
FF: fill factor.
Eff: efficiency.

This breakup of the thin oxide layer was studied in detail by Wolstenholme et al. [16]. Here, we further summarize and briefly review the study of interfacial oxide layer for solar cells (See Table 3). After reviewing the previous publications, the mechanisms governing carrier conduction through the SiO_x layer are not well understood and based on the thickness of the SiO_x layer. At present, there are two categories of passivated oxide layers [22]. One is SiO_x layer thickness <1.6 nm, the conduction mechanism is tunneling. The other is SiO_x layer thickness >2nm, the conduction mechanism is pinhole. The annealing process, such as temperature and duration is a key technique. On the other hand, the growth processes of oxide layer, such as wet chemically, thermal and plasma-assisted oxidation, could also influence the quality of the tunnel oxide layer. Thermal and plasma-assisted SiO_x provide excellent surface chemical passivation because they are dense, have stoichiometry close to SiO_2, and have few bulk defects. However, wet chemically grown oxide layers are less dense and offstoichiometric, and could result in inferior passivation and blistering [22]. For oxide layer thickness <1.6nm, the oxide's integrity weakens at high-temperature annealing. Some phenomenon, such as broken-up and balling-up, is present [2,16]. Furthermore, when the annealing process keep stable, the thinner oxide layer easily tends to break up or balling up [25]. The effect of annealing on the quality of three different oxide layers is further studied and discussed in the next subsection.

In case, the thickness of the SiO_x layer was less than 1.55 nm, the TOPCon solar cells exhibited poor FF with a high R_{ser} because the tunneling did not provide a sufficient transport channel for carrier transport, and the introduction of a thin layer could not prevent P from diffusing into Si due to the formation of some defects (such as pinhole or balling-up) while increasing the R_{ser} value and reducing FF value. Fig. 5

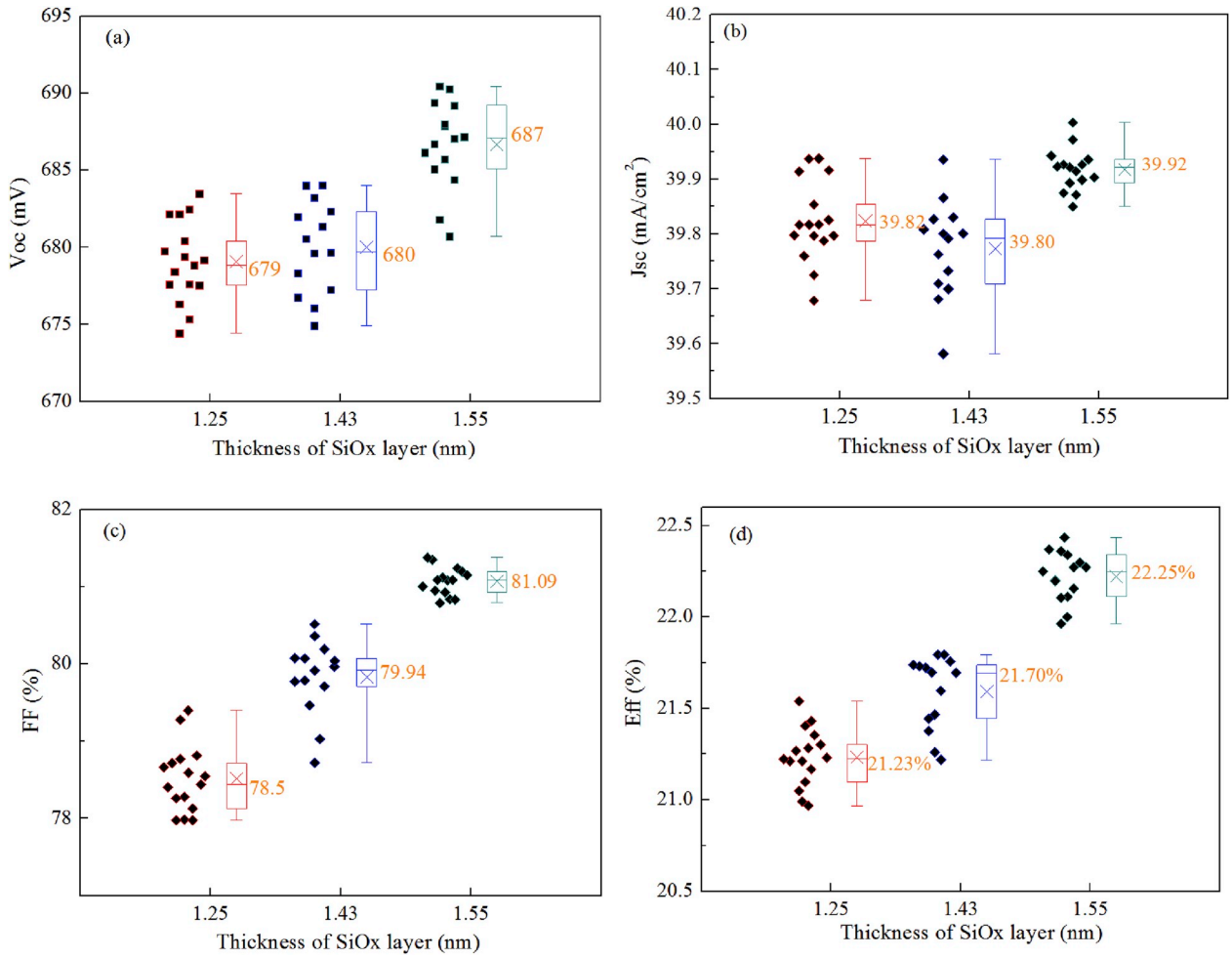

Fig. 4. Plots of (a) Voc, (b) J_{sc}, (c) FF and (d) Eff of TOPCon solar cells fabricated under three different tunneling SiO_x thicknesses.

shows the I–V curves of the cells obtained by different oxide layer thicknesses. These cells have the same pseudo fill factor (pFF), because these cells were from the same wafers and were manufactured in the same processes. The shunt resistance of Si wafer based solar cells with three conditions keeps the same value. However, the R_{ser} value of the wafer with 1.55 nm oxide layer is smaller than the ones with 1.25 nm and 1.43 nm oxide layers. Therefore, the FF loss for the cells with 1.25 nm and 1.43 nm oxide layers is also related to an increase in series resistance.

3.2. Cell performance

Fig. 6 shows the plots of J_0 values against minority carrier density from 1×10^{15} to 2×10^{16} cm^{-3} for the three different SiO_x tunnel layers. Because there are not good fittings at some injection concentrations. The different coloured lines in the figure represents the different injection concentrations. The J_0 results at fit range of 3×10^{15}–5×10^{15} cm^{-3} are chosen here. In this study, the textured poly layers were passivated by SiN_x stacks. The passivation quality of the stacks was quantified by measuring the saturation current density J_0. The J_0 values per side were determined from the slope of the inverse Auger-corrected injection level dependent effective lifetime at high-injection conditions. In Fig. 6, there was the lowest J_0 of about 18 fA/cm^2 for the wafers with 1.55 nm thick SiO_x layer. The J_0 values of the poly layers were 22 fA/cm^2 and 28 fA/cm^2 for the wafers with 1.25 nm and 1.43 nm thick oxide layers, respectively.

The average *i*Voc value of each fabricated cell type is shown in Fig. 7. The solar cell with 1.55 nm SiO_x had a good *i*Voc value of 700 mV. However, the *i*Voc values of the cells with 1.25 nm and 1.43 nm SiO_x were less than that of the cells with 1.55 nm oxide. The oxide layer with a thickness of 1.55 nm exhibited the best passivation effect.

Fig. 8 illustrates the contact resistivity for cells with different tunnel oxide thicknesses after firing at 865 °C. The plot indicates the confidence interval of the median of the contact resistivity. The cells with 1.55 nm thick tunneling layer had a low contact resistivity of 0.67 mΩ cm^2 because of higher surface doping concentration. The cells with 1.25 nm and 1.43 nm oxide layers had high contact resistivity of >1.5 mΩ cm^2. This result explains why the cells from conditions 2 and 3 feature higher R_{ser} compared to condition 1 (see Table 2). The reason for reduced R_c may be an enhanced drive-in of dopants. However, this adversely affects the recombination current at non-metallized sites [29]. Therefore, we should find out a balancing point between R_c and J_0. In this study, the cells with 1.55 nm oxide layer have low J_0 of 18 fA/cm^2 and R_c of 0.67 mΩ cm^2, which is attributed to controlling the thickness of the SiO_x layer and P doping concentration on the surface.

In this study, the cells fabricated with different tunneling SiO_x thicknesses had the same diffusion in the poly Si layers. The only difference was the thickness of oxide layer. Fig. 9 presents the ECV profiles. The cells from three different conditions have different P dopant profiles. The depths of the poly diffused regions, defined here as the depth where carrier concentration equals the bulk doping, were 0.3 μm. The surface concentration of the three carrier concentration profiles is higher than 1×10^{20} atom/cm^2. The monitor wafers with 1.55 nm SiO_x feature a higher surface concentration than the ones with 1.25 nm and 1.43 nm SiO_x. Because the thin oxide layer with thickness of less than 1.5 nm could not prevent P from diffusing into Si, which had a smooth

Table 3
Comparison of the different oxide layer thicknesses for solar cells.

t/nm	Method	T_{anneal}/°C	Cell parameters	Important results	Mechanism	Years	Ref.
1.4	Wet	700-900 × 30min	iVoc = 694mV, FF = 81%	iVoc decreases with increasing T_{anneal}, oxide weakens at 900°C	Tunneling	2014	[2]
–	Thermal*	850	iVoc = 660–730mV, FF = 69–80%	An increase in SiO_x thickness decreases FF	Tunneling	2019	[17]
1.5	Thermal	850 × 30min	Voc = 705mV,FF = 75.1%, R_{ser} = 0.86Ωcm^2	Local non-uniformities in the layer	Tunneling	2019	[18]
2.2		1025 × 30min	Voc = 695mV,FF = 66.3%,R_{ser} = 1.46Ωcm^2	An uniform layer			
1.2	Wet	950 × 30min	The best result: Voc = 714mV, R_{ser} = 0.6Ωcm^2, J_0 = 20fA/cm^2	Regions with broken up interface oxide	Broken up	2014	[19]
2.4	Thermal	900-1000 × 30min		Relative contact resistance remains close to one	Pinhole		
		1050 × 30min		Relative contact resistance drops to zero			
3.1		1050 × 15–90min		Relative contactresistance decreased with increasing duration			
<2	Thermal	900 × 4h	$J_0 = 2.4 \times 10^{-14}$ A/cm^2	Interfacial oxide is broken. An interfacial oxide of good quality is important to obtain low J_0.	Oxide break up	1990	[20]
		1000 × 30–60min	$J_0 = 4.5 \times 10^{-14}$ A/cm^2, $J_0 = 7.9 \times 10^{-14}$ A/cm^2				
		1050 × 30min/2h	With increasing duration, macroscopic junction resistance decreases, but J_0 increases.				
1.7nm	Wet	800 × 30min	J_0 increases with rising T_{anneal} to 1000 °C	A pinhole, uniform oxide layer	Pinhole	2016	[21]
		900 × 30min		Large areas broken up			
		1000 × 30min		Disrupted areas increase further			
2.6	Thermal	1000 × 30min	J_0 decreases with rising T_{anneal} to 1000 °C	No pinholes			
		1050 × 30min		Pronounced oxide disruption			
1.5	Thermal	850/1050 × 30min	iVoc = 724mV, R_c = 2.13 x10 mΩcm^2	No pinhole at 850°C, Oxides broken up at 1050°C	Tunneling	2018	[22]
2.2		850 × 30min	iVoc = 721 mV, $R_c = 3.19 \times 10^9$ mΩcm^2		Pinhole		
		1000 × 30min	iVoc = 735 mV, $R_c = 8.54 \times 10^9$ mΩcm^2	A decrease in contact resistivity due to pinholes			
		1050 × 30min	iVoc = 705 mV, R_c = 1.40 x10 mΩcm^2	Develops pinholes			
2.2	Thermal	1050 × 30min	J_0 = 2.7 fA/cm^2, R_c = 9.1mΩcm^2	Pinhole density of 4.5×10^6 cm^{-2}	Pinholes	2017	[8]
		1050 × 80min	J_0 = 6.2 fA/cm^2, R_c = 0.6mΩcm^2	Pinhole density of 5.8x10^{7}cm^{-2}			
1.5	Wet	850 × 30min		Denser oxide layer	Tunneling	2016	[23]
	Thermal	850 × 30min		Less dense, bubbles or blisters			
<2	Thermal	1050 × 15–120min		Pinholes in the interfacial oxide	Pinhole	2014	[24]
0.5	–	900 × 45min		Oxide balling-up occurred.	Ball-up mechanism is glass transition phenomenon	1987	[25]
1				Continuous oxide layer			
1.5				Continuous oxide layer			
1.4	Wet	900 × 10min		Continuous oxide layer	Pinhole in oxide	1989	[17]
		950–1100		Oxide layer broken up, and then ball up at 1100°C			
1.7	Wet	800 × 60min	J_0 = 50fA/cm^2	Pinhole density = 2.2x10^{7}cm^{-2}	Pinhole	2017	[7]
2.1	Thermal	1035 × 60min	J_0 = 1.5fA/cm^2	Pinhole density = 2.0×10^7 cm^{-2}			
2.4		1050 × 60min	J_0 = 8.7fA/cm^2	Pinhole density = 1.6×10^7 cm^{-2}			
2.5		800 × 60min	J_0 = 3.4fA/cm^2	Pinhole density = 1.3×10^7 cm^{-2}			
3.8	Plasma	800and 950		Pinhole density = 2.5×10^{10} cm^{-2} at 800°C, 7.5×10^{10} cm^{-2} at 950°C	Pinhole	2016	[5]
1.3–1.5	Wet	800 and 900	Voc = 719mV, Eff = 24.9%	Less stoichiometric oxide layer prone to disruption at high T_{anneal}	Tunneling	2015	[26]
2	Plasma	780-920 × 30min	iVoc = 724mV, J0 = 3.0Fa/cm^2, Eff>22.8%	The optimized annealing temperature 850–880°C	Pinhole	2019	[27]
1.8	Wet	850–975		Passivation quality declined at over 900 °C	Tunneling	2017	[28]
1.25	Thermal§	850 × 60min	Voc = 679mV, FF = 78.5%, Eff = 21.23%	Some pinholes	Tunneling	2019	Our work
1.43			Voc = 680mV, FF = 79.94%, Eff = 21.7%	Few pinholes			
1.55			Voc = 687mV, FF = 81.09%, Eff = 22.25%	Continuous oxide layer			

Note: t: thickness, T_{anneal}: anneal temperature *: temperature 700–800 °C, §: low temperature 550–650 °C.

tail ECV profile. On the other hand, the quality of the tunneling oxide layer, such as the size and number of pinholes in the layer could also influence P diffusion. This result would be confirmed by the further experiment. The solar cells with 1.25 nm and 1.43 nm oxide layers have a low surface concentration and are poorly passivated.

In this work, the quality of the oxide layer has been further studied. There are several factors that influence the quality of the oxide tunnel layer, such as the chemical bond structure in the SiO_x, stoichiometry and

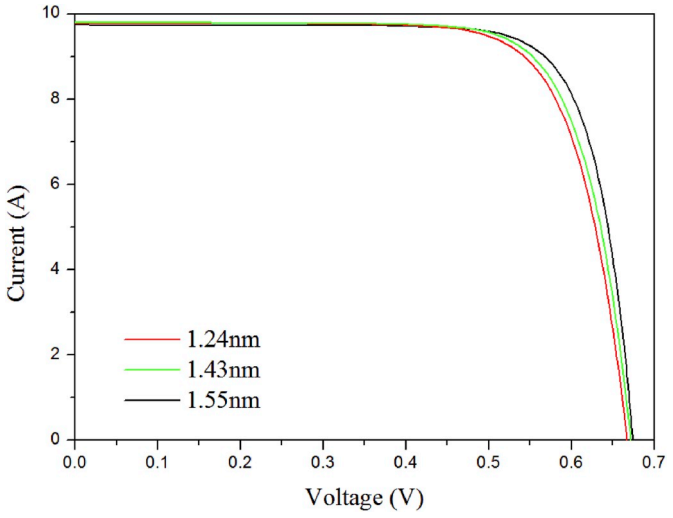

Fig. 5. I–V curves for the cells fabricated under three different tunneling SiO_x thicknesses.

properties of tunnel oxide and the interface-state density at the interface between the SiO_x and c-Si [27,28]. Fig. 10 shows the optical microscopy images of polished silicon wafers with three different thick oxide layers before and after etched in 15 wt% TMAH solution at 80 °C for 1 min and 2 min. The surface of as-deposited and as-annealed oxide layers is continuous, and no defects appear. The high temperature annealing process is the same with high-temperature annealing process for the crystallization and dopant activation at 850 °C for 1h. However, there is no both amorphous Si and P doped processes, the as-annealed oxide layers were etched with 15 wt% TMAH solution at 80 °C for 1 min and 2 min. After a short etching time, the surface of the as-annealed oxide layer is still continuous and dense. However, after 2 min etching time, the surface of thin oxide layers with 1.25 nm thickness presents some defects (dotted circle line), such as etch pits. We could observe some etch pits were present at five different locations. At the same time, the surface of 1.43 nm thick oxide layer also has two etch pits, indicating the defect density in the 1.43 nm thick oxide layer is less than the one in the 1.25 nm thick oxide layer. The resulting etch pits in the underlying silicon are much larger than the original pinholes. Therefore, these etch pits can readily be detected. It could be inferred from these observed defects that the TOPCon solar cells with 1.25 nm and 1.43 nm oxide layer has poor FF and high R_{ser} due to passivation loss, resulting from the quality of thin oxide layer after high-temperature annealing process.

The 1.55 nm thick oxide layer shows perfect surface after etched by TMAH solution, indicating the 1.55 nm thick oxide layer is dense and continuous. However, the reason for the formation of defects in 1.25 nm thin oxide layer might be attributed to the passivation loss at locally thin SiO_x regions after high-temperature annealing process. This result is in agreement with the Ref. [25]. Therefore, it is important to optimize the annealing temperature or duration for the thin SiO_x layer. Zeng et al. [30] also pointed out that it is possible to control the density of pinholes through a well-controlled anneal process. At the same time, the series resistance of the wafer with thin SiO_x layer is larger than the one of the wafer with thick SiO_x layer, due to the existence of locally very thin SiO_x regions in the thin SiO_x layer. Furthermore, according to ECV profiles, the P concentration at the interfacial oxide layer for thin SiO_x layer is higher than that for 1.55 nm thick SiO_x layer. The increase in contact resistivity value in fact matches the amount of series resistance increased and FF loss of the cell (see Figs. 5 and 8). These experimental results confirm that the quality of 1.25 nm thin SiO_x layer is not good, possibly incompletely continuous layer or less stoichiometric oxide. In this study, the low-temperature thermal SiO_x layers were obtained at 550–650 °C for different durations. Therefore, the growth conditions of

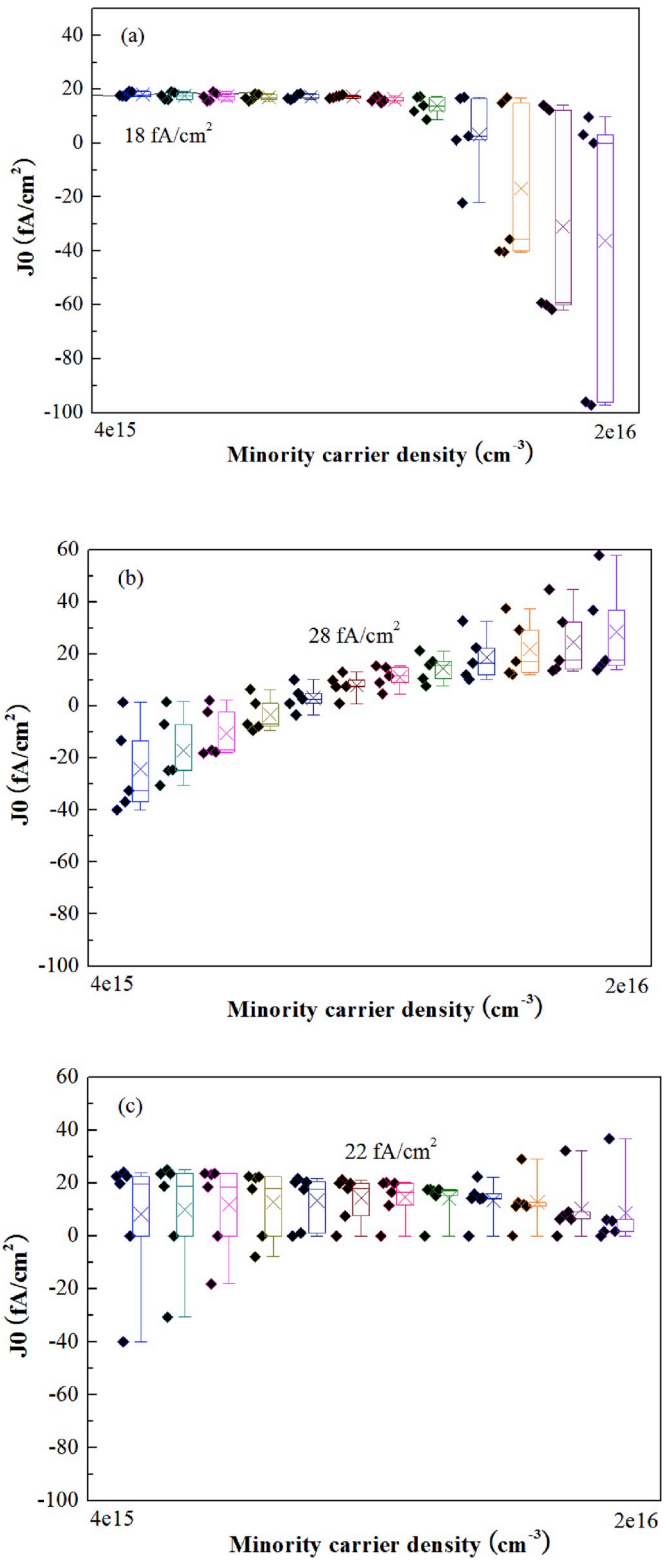

Fig. 6. Plots of J_0 values as a function of minority carrier density from 1×10^{15} to 2×10^{16} $cm^{-3}$for (a) 1.55 nm SiO_x layer, (b) 1.25 nm SiO_x layer, (c) 1.43 nm SiO_x layer.

oxides might result in the difference in the quality of tunnel oxides. The thin oxide layer at locally thin layer regions or less stoichiometric oxide layer is more prone to disruption at high-temperature anneal, which could result in the formation of defects (etch pits). The uniformity and continuity of 1.55 nm thick SiO_x layer is better than the ones of the

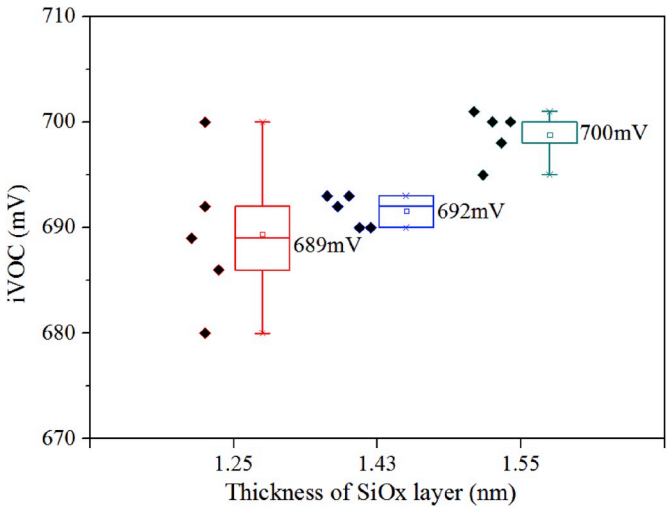

Fig. 7. Average *i*Voc of the cells obtained from three different conditions.

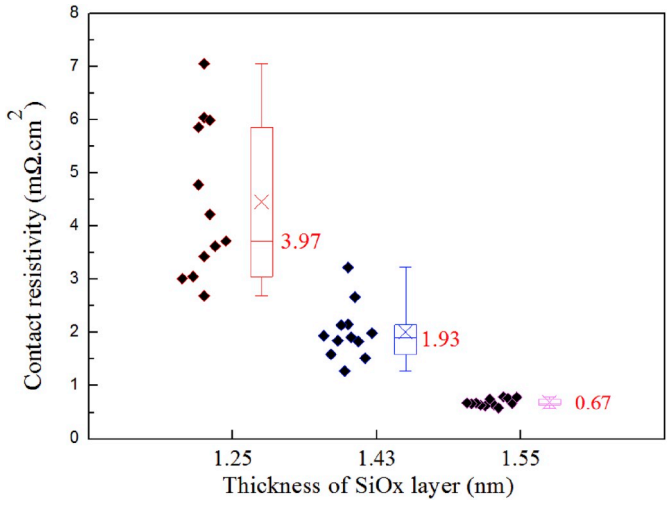

Fig. 8. Contact resistivity of the Si cells obtained from three different conditions.

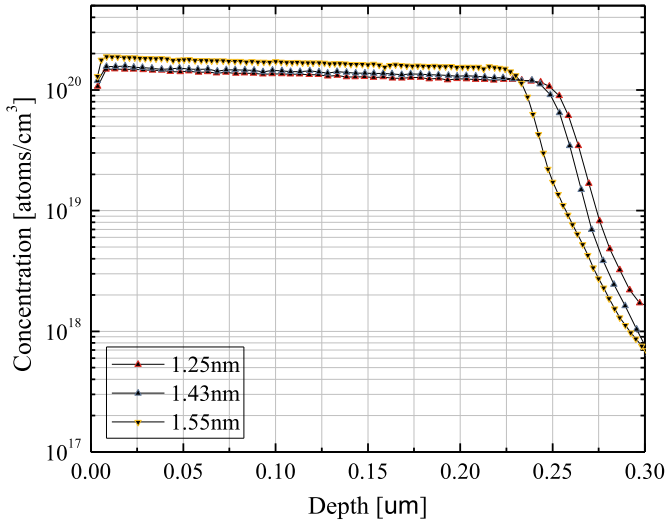

Fig. 9. ECV profiles of poly emitter diffusion.

others. Therefore, the dominant carrier transport mechanism in the 1.55 nm, 1.25 nm and 1.43 nm thick SiO_x contacts is through tunneling.

The simulated optical reflection matches fairly well without any adjustments to a characteristic experimental reflection, as shown in Fig. 11. The experimental reflection was slightly lower than the simulated reflection, as the busbar shading was not included in the measurement. A loss analysis in terms of current density was derived from the simulation, as shown on the right hand side of Fig. 11. Besides the metal shading losses, losses resulted mainly from ARC reflectance and NIR parasitic absorption losses, which partly included the light trapping capability of the TOPCon cells. The light trapping capability may be evaluated looking at the Yablonovitch limit (ideal light trapping) of 46.43 mA/cm^2 [31]. The metal shading loss was due to the front metal grid. In this study, the metal area fraction on the front side is about 2.74% for H pattern grid on both front and back. Therefore, thinning fingers could reduce metal area fraction and then improve the efficiency of the solar cells. While a reduced front metallization fraction could reduce shading loss, hence higher series resistance and lower FF values would be obtained. Optimization of the front side metallization should take all these factors into account. The reflectance loss at the cell front side may be reduced by tuning the ARC optical properties, such as refraction index and thickness, as well as by improved front surface texturing for better light-trapping. An optical loss was due to <100% cell rear surface internal reflectance, and to a certain extend due to free carrier absorption. The optical loss could be decreased by improving the rear internal reflector, e.g. good rear planarization and tuning its optical property. A recombination related current loss was due to finite diffusion length in the wafer and rear surface recombination. The diffusion depth may be increased by good wafer material quality and bulk passivation of electrically active defects in case of multi-crystalline Si. The IR light that escapes from the cells can be reduced by improving the light trapping.

The optimization of thickness of the SiO_x tunnel layer, and annealed temperature could improve the efficiency of solar cells, at the same time the metal paste for rear poly, sintering and boron diffusion processes, and thinning fingers also further need to be optimized, in order to increase the efficiency of solar cells. After optimization of several processes, industrial-type TOPCon cells at the present pilot line with an efficiency as high as 23.03%, a Voc value as high as 697 mV, and a fill factor as high as 82.45% has been obtained.

4. Conclusions

A tunnel oxide passivated contact for the rear side base contact of n-type silicon solar cells has been studied. It has been shown that the TOPCon structure based on a tunnel oxide and P-doped Si layer passivates the surface effectively. A 1.55 nm thick SiO_x layer provides a J_0 value as low as 18fA/cm^2.The solar cells with the TOPCon structure have shown a good performance with Voc as low as 687 mV and FF as high as 81.09%.

After as-annealed oxide layers were etched with 15 wt% TMAH solution at 80 ^{0}C for 2 min, the surface of thin oxide layers with 1.25 nm and 1.43 nm thickness presents etch pits. The 1.55 nm thick oxide layer is dense and continuous. The dominant carrier transport mechanism in the 1.55 nm, 1.25 nm and 1.43 nm thick SiO_x layers is through tunneling.

The best TOPCon cell has an independently confirmed efficiency as high as 22.43%. It has also been demonstrated that the efficiency is limited by recombination at the rear. Hence, by improving poly Si quality and the front metal contacts by addressing the issue of reducing metal recombination and implementing a selective emitter. A further increase of the efficiency well above 24% seems to be possible.

Author contributions

WPW and QQW contributed equally to this work. Profs. YLL and NYY

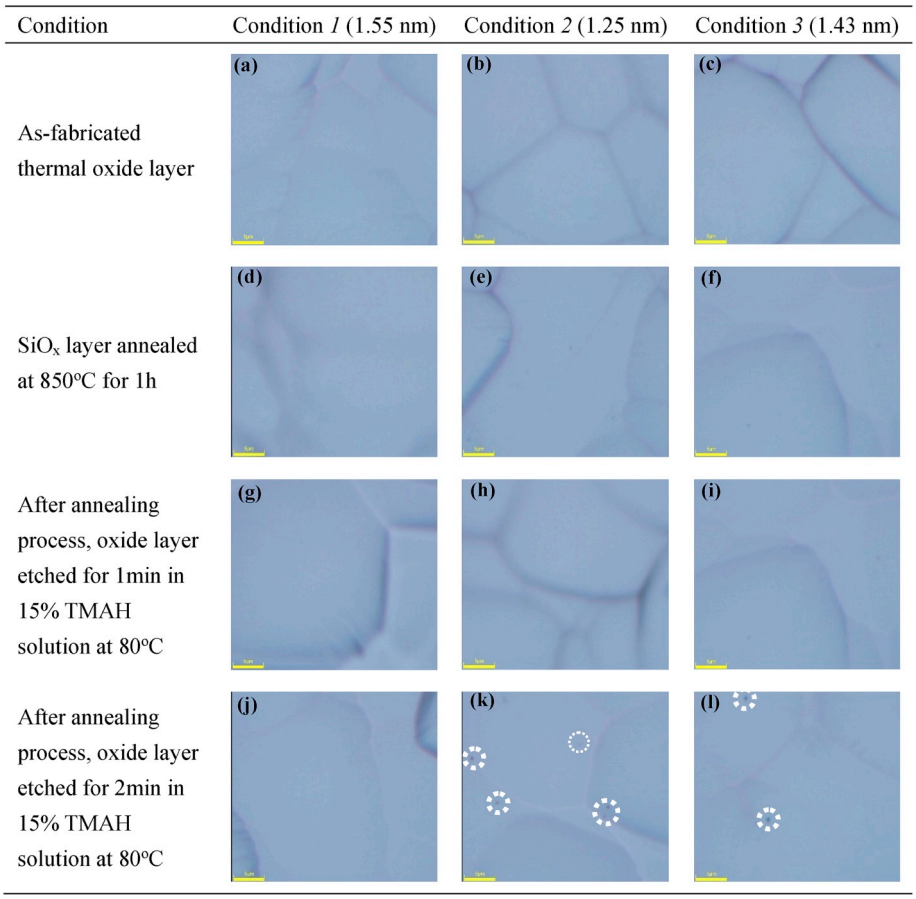

Fig. 10. Optical microscopy images of polished silicon wafers with three different thick oxide layers before and after etched in 15 wt% TMAH solution at 80 °C for 1 min and 2 min. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

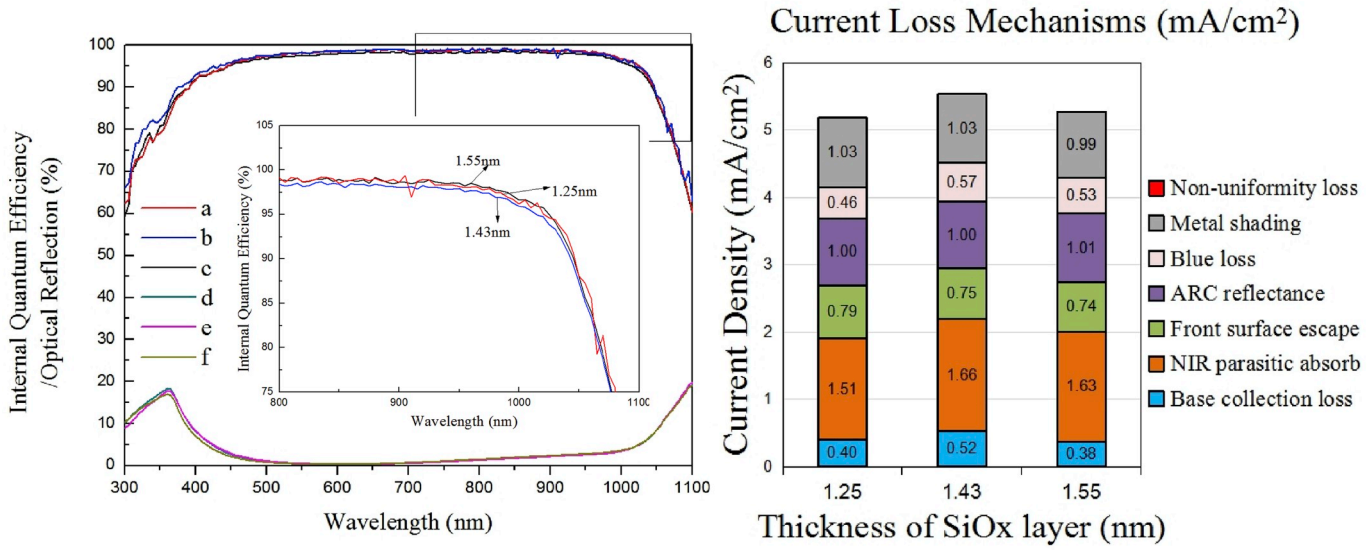

Fig. 11. Internal quantum efficiency (IQE) for (a) 1.55 nm oxide, (b) 1.25 nm oxide, (c) 1.43 nm oxide and optical reflection for (d) 1.55 nm oxide, (e) 1.25 nm oxide, (f) 1.43 nm oxide and current loss mechanisms (right).

supervised Ph.D. candidate QQW. WPW designed the study, wrote and revised the manuscript, QQW performed the experiments, and contributed to the first preparation of this article. WPW, YZ and NYY supervised the preparation and experiments. NYY guided the experiment. All authors discussed the results and approved the submission of the final manuscript.

Declaration of competing interest

We declare that we do not have any commercial or associative

interest that represents a conflict of interest in connection with the work submitted.

CRediT authorship contribution statement

Qinqin Wang: Data curation, Formal analysis, Investigation, Methodology, Resources, Software, Writing - original draft, Writing - review & editing. **Wangping Wu:** Writing - review & editing. **Ningyi Yuan:** Writing - review & editing, Supervision. **Yali Li:** Writing - review & editing, Supervision. **Yi Zhang:** Writing - review & editing. **Jianning Ding:** Writing - review & editing.

Acknowledgements

This work has been partially supported by the National Natural Science Foundation of China (Grant No. 51875053), and Changzhou Sci & Tech Program (Grant No. CJ20190041) and the Funding of Changzhou High Technology Research Key Laboratory of Mould Advanced Manufacturing (Grant No. CM20173001). We thank Dr. Lei Zhang from Changshu Institute of Technology for the discussion. Dr. Wangping Wu thanks the China Scholarship Council (CSC) an "Agreement for Study Abroad for CSC Sponsored Chinese Citizens" awarded a scholarship under the State Scholarship Fund to pursue study in Germany as a Visiting Scholar for July–September 2019.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.solmat.2020.110423.

References

[1] A. Richter, J. Benick, F. Feldmann, et al., n-Type Si solar cells with passivating electron contact: identifying sources for efficiency limitations by wafer thickness and resistivity variation, Sol. Energy Mater. Sol. Cells 173 (2017) 93–105, https://doi.org/10.1016/j.solmat.2017.05.042.

[2] F. Feldmann, M. Bivour, C. Reichel, et al., Tunnel oxide passivated contacts as an alternative to partial rear contacts, Sol. Energy Mater. Sol. Cells 131 (2014) 46–50, https://doi.org/10.1016/j.solmat.2014.06.015.

[3] F. Feldmann, M. Simon, M. Bivour, et al., Efficient carrier-selective p- and n-contacts for Si solar cells, Sol. Energy Mater. Sol. Cells 131 (2014) 100–104, https://doi.org/10.1016/j.solmat.2014.05.039.

[4] Y. Tao, K. Madani, E. Cho, et al., High-efficiency selective boron emitter formed by wet chemical etch-back for *n*-type screen-printed Si solar cells, Appl. Phys. Lett. 110 (2017), https://doi.org/10.1063/1.4973626, 021101-1-5.

[5] K. Lancaster, S. Großer, F. Feldmann, et al., Study of pinhole conductivity at passivated carrier-selected contacts of silicon solar cells, Energy Procedia 92 (2016) 116–121, https://doi.org/10.1016/j.egypro.2016.07.040.

[6] R. Peibst, U. Römer, Y. Larionova, et al., Working principle of carrier selective poly-Si/c-Si junctions: is tunneling the whole story? Sol. Energy Mater. Sol. Cells 158 (2016) 60–67, https://doi.org/10.1016/j.solmat.2016.05.045.

[7] D. Tetzlaff, J. Krügener, Y. Larionova, et al., A simple method for pinhole detection in carrier selective POLO-junctions for high efficiency silicon solar cells, Sol. Energy Mater. Sol. Cells 173 (2017) 106–110, https://doi.org/10.1016/j.solmat.2017.05.041.

[8] T.F. Wietler, D. Tetzlaff, J. Krügener, et al., Pinhole density and contact resistivity of carrier selective junctions with polycrystalline silicon on oxide, Appl. Phys. Lett. 110 (2017), https://doi.org/10.1063/1.4986924, 253902.

[9] F. Feldmann, G. Nogay, P. Löper, et al., Charge carrier transport mechanisms of passivating contacts studied by temperature-dependent J-V measurements, Sol. Energy Mater. Sol. Cells 178 (2018) 15–19, https://doi.org/10.1016/j.solmat.2018.01.008.

[10] M. Taguchi, A. Yano, S. Tohoda, et al., 24.7% record efficiency HIT solar cell on thin silicon wafer, IEEE J. Photovoltaics 4 (2013) 96–99, https://doi.org/10.1109/JPHOTOV.2013.2282737.

[11] K. Masuko, M. Shigematsu, T. Hashiguchi, et al., Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell, IEEE J. Photovoltaics 4 (2014) 1433–1435, https://doi.org/10.1109/JPHOTOV.2014.2352151.

[12] F. Feldmann, M. Bivour, C. Reichel, et al., Passivated rear contacts for high-efficiency n-type Si solar cells providing high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics, Sol. Energy Mater. Sol. Cells 120 (2014) 270–274, https://doi.org/10.1016/j.solmat.2013.09.017.

[13] J.B. Heng, J. Fu, B. Kong, et al., 23% high-efficiency tunnel oxide junction bifacial solar cell with electroplated Cu gridlines, IEEE J. Photovoltaics 5 (2015) 82–86, https://doi.org/10.1109/JPHOTOV.2014.2360565.

[14] F. Feldmann, M. Bivour, C. Reichel, et al., A Passivated Rear Contact for High-Efficiency N-type Silicon Solar Cells Enabling High VocS and FF>82%, in: 28th European PV Solar Energy Conference and Exhibition, 2013, pp. 988–992, https://doi.org/10.4229/28thEUPVSEC2013-2CO.4.4. Paris, France.

[15] R.A. Sinton, A. Cuevas, A quasi-steady-state open circuit voltage method for solar cell characterization, in: Proceedings of the 16th European Photovoltaic Solar Energy Conference and Exhibition, 2000, pp. 1152–1155. Glasgow, UK, http://hdl.handle.net/1885/71035.

[16] G.R. Wolstenholme, N. Jorgensen, P. Ashburn, et al., An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations, J. Appl. Phys. 61 (1987) 225–233, https://doi.org/10.1063/1.338861.

[17] B. Nemeth, S.P. Harvey, D.L. Young, et al., Critical interface: poly-silicon to tunneling SiO_2 for passivated contact performance, silicon PV 2019, the 9th international conference on crystalline silicon photovoltaics, AIP Conf. Proc. 2147 (2019), 050008, https://doi.org/10.1063/1.5123857.

[18] A.S. Kale, W. Nemeth, H. Guthrey, et al., Understanding the charge transport mechanisms through ultrathin SiO_x layers in passivated contacts for high-efficiency silicon solar cells, Appl, Phys. Lett. 114 (2019), 083902, https://doi.org/10.1063/1.5081832.

[19] U. Römer, R. Peibst, T. Ohrdes, et al., Recombination behavior and contact resistance of n^+ and p^+ poly-crystalline Si/mono-crystalline Si junctions, Sol. Energy Mater. Sol. Cells 131 (2014) 85–91, https://doi.org/10.1016/j.solmat.2014.06.003.

[20] J.Y. Gan, R.M. Swanson, Poly silicon emitters for silicon concentrator solar cells, Proceedings of 21st IEEE-PVSC, Kissimmee, FL, USA, 1990, pp. 245–250, https://doi.org/10.1109/PVSC.1990.111625.

[21] D. Tetzlaff, J. Krügener, Y. Larionova, et al., Evolution of oxide disruptions: the (W) hole story about poly-Si/c-Si passivating contacts, in: IEEE 43rd Photovoltaic Specialists Conference (PVSC), 2016, https://doi.org/10.1109/pvsc.2016.7749582. Portland, OR, USA, 0221-0224.

[22] A.S. Kale, W. Nemeth, S.U. Nanayakkara, et al., Tunneling or pinholes: understanding the transport mechanisms in SiO_x based passivated contacts for high-efficiency silicon solar cells, in: IEEE 7th World Conference on Photovoltaic Energy Conversion, Waikoloa Village, HI, USA, 2018, pp. 3473–3476, https://doi.org/10.1109/PVSC.2018.8547211.

[23] B. Nemeth, D.L. Young, M.R. Page, et al., Polycrystalline silicon passivated tunneling contacts for high efficiency silicon solar cells, J. Mater. Res. 31 (2016) 671–681, https://doi.org/10.1557/jmr.2016.77.

[24] R. Peibst, U. Römer, K.R. Hofmann, et al., A simple model describing the symmetric I-V characteristics of p polycrystalline Si/n monocrystalline Si, and n polycrystalline Si/p monocrystalline Si junctions, IEEE J.Photovoltaics 4 (2014) 841–850, https://doi.org/10.1109/JPHOTOV.2014.2310740.

[25] T. Maeda, M. Higashizono, H. Mornose, J. Matsunaga, Poly Si-Si interfacial oxide ball-up mechanism and its for 0.8μm BiCMOS VLSI's, in: Proceedings of the Bipolar Circuits and Technology Meeting, 1989, pp. 102–105, https://doi.org/10.1109/BIPOL.1989.69468. Minneapolis, MN, USA.

[26] A. Moldovan, F. Feldmann, M. Zimmer, et al., Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO_2 layers, Sol. Energy Mater. Sol. Cells142 (2015) 123–127, https://doi.org/10.1016/j.solmat.2015.06.048.

[27] T. Gao, Q. Yang, X.Q. Guo, et al., An industrially viable TOPCon structure with both ultra-thin SiO_x and n^+-poly-Si processed by PECVD for p-type c-Si solar cells, Sol. Energy Mater. Sol. Cells 200 (2019), https://doi.org/10.1016/j.solmat.2019.109926, 109926.

[28] H. Kim, S. Bae, K.-S. Ji, et al., Passivation properties of tunnel oxide layer in passivated contact silicon solar cells, Appl. Surf. Sci. 409 (2017) 140–148, https://doi.org/10.1016/j.apsusc.2017.02.195.

[29] M.K. Stodolny, J. Anker, B.L.J. Geerligs, et al., Material properties of LPCVD processed n-type polysilicon passivating contacts and its application in PERPoly industrial bifacial solar cells, Energy Procedia 124 (2017) 635–642, https://doi.org/10.1016/j.egypro.2017.09.250.

[30] Y.H. Zeng, H. Tong, C. Quan, et al., Theoretical exploration towards high-efficiency tunnel oxide passivated carrier-selective contacts (TOPCon) solar cells, Sol. Energy 155 (2017) 654–660, https://doi.org/10.1016/j.solener.2017.07.014.

[31] E. Yablonovitch, Statistical ray optics, J. Opt. Soc. Am. 72 (1987) 899–907, https://doi.org/10.1364/JOSA.72.000899.