Solar Energy Materials & Solar Cells 150 (2016) 32–38

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Silicon heterojunction solar cells with electron selective TiO_x contact

Xinbo Yang*, Peiting Zheng, Qunyu Bi, Klaus Weber

Research School of Engineering, The Australian National University, Canberra, ACT 2601, Australia

ARTICLE INFO

Article history:
Received 21 July 2015
Received in revised form
28 December 2015
Accepted 15 January 2016
Available online 17 February 2016

Keywords:
Solar cells
Titanium dioxide
Carrier selective contact
Heterojunctions

ABSTRACT

Silicon solar cells featuring carrier selective contacts have been demonstrated to reach ultra-high conversion efficiency. In this work, the electron-selective contact characteristics of ultrathin TiO_x films deposited by atomic layer deposition on silicon are investigated via simultaneous consideration of the surface passivation quality and the contact resistivity. Thin TiO_x films are demonstrated to provide not only good passivation to silicon surfaces, but also allow a relative low contact resistivity at the TiO_x/Si heterojunction. A maximum implied open-circuit voltage (iV_{oc}) of ~703 mV is achieved with the passivation of a 4.5 nm TiO_x film, and a relatively low contact resistivity of (~0.25 Ω cm^2 is obtained at the TiO_x/n-Si heterojunction simultaneously. N-type silicon solar cell with the champion efficiency of 20.5% is achieved by the implementation of a full-area electron-selective TiO_x contacts. A simulated efficiency of up to 23.7% is achieved on the n-type solar cell with a full-area TiO_x contact. The efficient, low cost electron-transporting/hole-blocking TiO_x layer enables the fabrication of high efficiency silicon solar cells with a simplified process flow.

1. Introduction

The main challenge in today's photovoltaics industry is to increase the conversion efficiency and to lower the production cost of solar cells. The passivated-emitter rear locally diffused (PERL) silicon solar cell structure, which features local doping under the front and rear contacts, offers an ultra-high efficiency potential. P- and n-type PERL cells with efficiencies of 25.0% and 23.2%, respectively, have been achieved so far [1,2]. To further improve the conversion efficiency, minimizing carrier recombination at contacts becomes increasingly important for silicon solar cells. When directly in contact with silicon wafer, metals introduce very large densities of electronic states near the interface energetically within the bandgap of silicon, resulting in >50% recombination losses in high efficiency cells [3]. Heavily doped regions immediately beneath the metal contact and small contact areas can be implemented to address this issue, which leads to the concept of the PERL cell. However, producing cells with small contact fractions within the industrial environment has proven to be a significant technological challenge, particularly when applied in conjunction with localized heavily doped regions.

An alternative approach is to introduce a passivated contact or carrier selective contact. In principle, the reduction of carrier recombination at the contact interface can be achieved by the insertion of an ultrathin dielectric interlayer between the silicon surface and the contacting metal, which is now known as a "*passivated contact*". The ultra thin dielectric must simultaneously separate metal from silicon wafer, passivate the silicon surface, and still serve as a conductive contact to the solar cell. Up till now, ultra thin SiO_2, Al_2O_3 and a-Si: H dielectrics have been investigated as passivated contact layers for silicon solar cells [4–9]. Unfortunately, the passivation quality and thermal stability of these ultra thin dielectrics are too poor to be implemented into high efficiency silicon solar cells. Alternatively, carrier selective contacts (CSC), which extract one-type of carrier (electron or hole) from the absorber, have been proposed and developed for high efficiency silicon solar cells [10,11]. A high quality CSC can not only extract one-type of carrier without the need for a p–n junction, but also provide excellent surface passivation and lateral carrier transport. Usually, carrier selectivity at the contacts is achieved by depositing a conductive transport layer (e.g. doped a-Si: H) over the ultra thin dielectrics (e. g. SiO_2 or a-Si: H). For example, an electron/hole-selective contact can be formed by a stack of ultra thin SiO_2 (<2 nm) and phosphorus/boron-doped a-Si: H layer [11]. As-developed CSCs provide not only excellent surface passivation (due to a combination of chemical passivation of dielectrics and field induced passivation induced by a doped a-Si: H layer), but also serve as current-carrying contacts: the dielectric layer is thin to allow carrier collection into the transport layer and from there into the metal contact. The main advantages of a CSC for silicon solar cells include: 1) excellent surface passivation at both contact

* Corresponding author. Tel.: +61 02 6197 0112; fax: +61 02 6125 0506.
E-mail addresses: xinbo.yang@anu.edu.au, louis.xbyang@gmail.com (X. Yang).

http://dx.doi.org/10.1016/j.solmat.2016.01.020
0927-0248/

and non-contact areas; 2) extraction of carriers at the energy of quasi-Fermi level resulting in a high open circuit voltage V_{oc}; 3) no costly thermal diffusion processes; 4) no complicated contact patterning; 5) a simple process flow with low cost. Up till now, two types of CSCs, namely i) intrinsic a-Si: H (*i*-a-Si: H)/n^+ or p^+ a-Si: H and ii) SiO_2/n^+ or p^+ polycrystalline silicon (*pc*-Si), have been successfully developed and implemented into high efficiency silicon solar cells. In 2014, a-Si: H-based CSCs demonstrated spectacular performance in Panasonic's current world-record 25.6% heterojunction interdigitated back-contact (IBC) cell [10]. Recently, n-type silicon solar cells featuring an electron-selective SiO_2/n^+ *pc*-Si contact at the rear and a diffused front p^+ emitter have been achieved a remarkably high efficiency of 24.9% [12]. Additionally, an organic-based hole-selective contact, poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (PEDOT:PSS), has also been developed and implemented in p-type silicon solar cells with an efficiency of up to 20.6% [13]. Therefore, CSCs have shown great potential in future high- and ultra-high-efficiency silicon solar cells.

Although a-Si: H and SiO_2-based CSCs have achieved great success in high efficiency silicon solar cells, they have some intrinsic disadvantages such as complicated deposition process, high fabrication cost, parasitic photon absorption of a-Si: H layers. Transition metal oxides (TMOs) such as molybdenum oxide (MoO_x) [14,15], nickel oxide (NiO_x) [16,17], Titanium oxide (TiO_x) [18] and vanadium oxide (VO_x) [19] have been extensively studied because of their excellent electronic properties for charge injection and extraction in organic or perovskite solar cells. During the last few years, easy-deposited MoO_x [20,21] and TiO_x [22,23] thin films have also been investigated as CSCs and implemented in silicon solar cells. The TiO_x/Si interface has been demonstrated to have a small conduction band offset, which would allow transport of electrons from silicon to TiO_x and a large valence band offset, which would block the holes from silicon to TiO_x, as illuminated in Fig. 1. A double-heterojunction n-type silicon solar cell with an efficiency of up to 12.9% has been fabricated via the implementation of a hole-blocking TiO_x layer deposited by modified chemical vapor deposited (CVD) at the rear and a Si/PEDOT:PSS heterojunction at the front [24,25]. The cells were fabricated at a temperature of < 250 °C at a low cost, which is very attractive for photovoltaics industry. However, the organic-silicon heterojunction localized on the cell front leads to a significant parasitic light absorption within the PEDOT:PSS layer, resulting in a relatively low shirt circuit current density J_{sc}, and hence a low efficiency.

We have previously investigated atomic layer deposited (ALD) TiO_x films as the capping layer on Al_2O_3 to improve the surface passivation to silicon p^+ regions [26]. Recently, electron-selective TiO_x contacts deposited by ALD have been incorporated into a 19.2% efficient InP heterojunction solar cell [27]. In this work, the carrier selectivity of ALD-TiO_x ultrathin films on silicon surfaces is firstly evaluated via simultaneous consideration of the surface passivation quality and the contact resistivity (ρ_c). It is found that

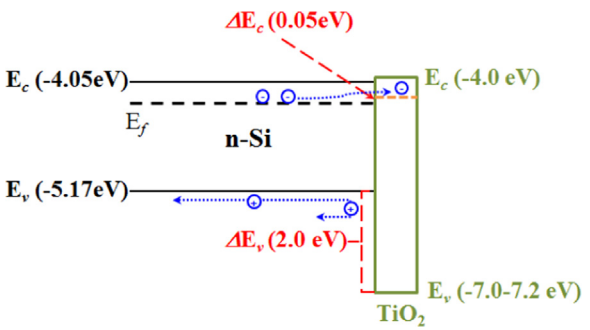

Fig. 1. Conduction and valence band offsets of the TiO_x/n-Si interface.

ultra thin TiO_x film (≤ 5.5 nm) can provide not only good passivation to silicon surface, but also allow a relatively low ρ_c on silicon. N-type silicon heterojunction solar cells featuring an Al_2O_3/SiN_x stack passivated boron diffused emitter at the front and a full-area electron selective TiO_x contacts at the rear are fabricated. The effects of TiO_x film thickness on the cell efficiency are demonstrated and discussed. An efficiency of 20.5% has been achieved on n-type silicon solar cells by the implementation of electron selective TiO_x contacts.

2. Experimental

The surface passivation of ALD-TiO_x film was investigated by means of injection-dependent lifetime measurement utilizing the quasi-steady state photoconductance (QSSPC) technique [28]. Symmetrical lifetime test structures were fabricated on (100)-oriented FZ n-type silicon wafers (1.0 Ω cm, 190 μm). The wafer surface was chemical-polished and RCA cleaned before TiO_x deposition by ALD (TFS 200, BENEQ, FINLAND) at a temperature of 230 °C. Titanium Tetrakis Isopropoxide (TTIP), H_2O and N_2 were used as the titanium precursor, oxidant and purge gas, respectively. The growth rate per cycle was determined to be ~0.035 nm, and the cycle time was ~10 s. TiO_x films with different thickness were deposited on both sides of silicon wafers, and QSSPC measurements were performed before and after annealing with different recipes. Some of the samples were subjected to a short thermal oxidation before TiO_x films deposition. The oxidation was performed in a preheated quartz tube furnace at 700 °C for 3 min in O_2 atmosphere, resulting in a tunnel SiO_2 thickness of 1.2–1.5 nm. The passivation quality was qualified in terms of the implied open circuit voltage (iV_{oc}) at 1 sun, which was calculated according to

$$\mathrm{i}V_{oc} = \frac{kT}{q}\ln\left[\frac{(N_A+\Delta n)\Delta n}{{n_i}^2}\right]$$

where kT/q is the thermal voltage, N_A is the doping concentration, Δn is the excess carrier concentration and n_i is the intrinsic carrier concentration (8.79×10^9 cm^{-3}).

The contact resistance of TiO_x/n-Si heterojunction was measured by the method developed by Cox and Strack [29]. The test structure, as shown in the inset picture of Fig. 6, was prepared by depositing TiO_x on one side of the sample, following which Al/Ag metal stack circles with different diameters were evaporated on top through a shadow mask. To minimize the resistance associated with the rear contact, an ohmic rear contact was prepared using evaporated Al on a phosphorus diffused (60 Ω/□) rear surface. Current–voltage measurements in the dark were performed using a Keithley 2425 source-meter at room temperature. The ρ_c values were obtained by fitting the curve of resistance versus front circle contact diameter [29]. It should be noted that the extracted ρ_c value comprises the resistance of the TiO_x/Si and Al/TiO_x interfaces as well as the TiO_x bulk resistivity.

N-type silicon solar cells featuring an electron selective TiO_x contact at the rear side were fabricated on 1.0 Ω cm FZ-Si wafers with a thickness of ~175 μm. The cell size is 2×2 cm^2. Fig. 2 shows the sketch of the n-type silicon solar cells. The front side was textured with a random pyramid structure in alkaline solution and has a boron diffused p^+ emitter with the sheet resistance of ~120 Ω/□. The p^+ emitter was passivated by Al_2O_3/SiN_x stack (~70 nm), which is formed by plasma ALD (Al_2O_3 ~20 nm) and PECVD (SiN_x, ~50 nm). The front fingers were prepared with photolithography in combination with an evaporated stack of Cr/Pd/Ag that was thickened with Ag electro-plating. TiO_x films with different thickness were deposited at the rear side by ALD. A short annealing in forming gas atmosphere (FGA) was applied after TiO_x

deposition. The rear side was metallized with an evaporated Al/Ag stack (50/2000 nm). Finally, the cells were subjected to a front contact formation annealing at 300 °C for 30 mins in FGA. Light *I–V* tests were performed under standard AM1.5 illumination using an in-house system. The light source intensity of this system was calibrated using a certified reference cell from Franhaufer ISE CalLab. Quantum efficiency measurements were also performed on the solar cells.

3. Results and discussion

3.1. Surface passivation quality of ultrathin TiO_x film on silicon surface

The surface passivation quality of ALD-TiO_x on silicon surfaces has been previously investigated by G. Dingemans et al. [30] and I. Yu et al. [31,32]. Nevertheless, a low level of passivation has been achieved by TiO_x films with the thickness(8 nm compared to that of Al_2O_3 and HfO_2 of similar thickness deposited by ALD [30]. In this work, the passivation performance of ultrathin TiO_x layers ($\leq$8 nm) on n-type silicon wafers was investigated. Six different thickness (2.5, 3.5, 4.5, 5.5, 6.5, and 8 nm) TiO_x layers were selected and deposited on both sides of n-type silicon wafers (1.0 Ω cm). Fig. 3a shows the effects of TiO_x film thickness on the iV_{oc} value measured by the QSSPC technique. It is interesting to observe that ultrathin TiO_x could provide good passivation on n-type silicon surface. As TiO_x film thickness increases from 2.5 to 5.5 nm, the obtained iV_{oc} value increases. With further increasing TiO_x thickness ($>$5.5 nm), the iV_{oc} value decreases again. A maximum iV_{oc} value of 681 mV was achieved with a 5.5 nm TiO_x film. A short FGA anneal at 250 °C for only 3 min improved the surface passivation significantly, as also shown in Fig. 3a. High iV_{oc} values of 698 and 703 mV were achieved with the TiO_x thickness of 4.5 and 5.5 nm, respectively, after extending FGA annealing for 30 min. Fig. 3b shows the injection level dependent effective lifetime (τ_{eff}) of the samples passivated by a 5.5 nm TiO_x film before and after FGA annealing. The τ_{eff} (at the injection level of 1×10^{15} cm^{-3}) was improved from 385 to 715 μs by FGA annealing at 250 °C for only 3 min, and further improved to 865 μs by extending to 30 min. The effective surface recombination velocity (S_{eff}) can be calculated from τ_{eff} measured by QSSPC technique by the expression [28].

$$\frac{1}{\tau_{eff}}=\frac{1}{\tau_{bulk}}+\frac{2S_{eff}}{W}$$

with τ_{bulk} being the *c*-Si bulk lifetime and *W* the wafer thickness. Here the bulk lifetime can be set to infinity due to a high quality FZ c-Si was used. Hence the effective lifetimes of 680 and 865 μs obtained by 4.5 and 5.5 nm TiO_x film after FGA annealing for 30 mins correspond to an upper limit S_{eff} of 13 and 10 cm/s, respectively. The results indicate that ultrathin TiO_x films can provide very good surface passivation to n-type silicon surface.

The change of passivation quality with increasing TiO_x thickness shown in Fig. 3a also demonstrates the fact that a thick TiO_x film ($>$10 nm) does not provide a higher level of surface passivation to the silicon surface, which is consistent with previous reports [30–32]. The mechanism has been investigated by I. Yu et al. [31]. They found that an amorphous TiO_x layer with high tensile stress forms at the beginning of the deposition, which induces the nucleation of anatase phase, and grain growth occurs as the thickness of TiO_x films increases. Therefore, the TiO_x surface passivation degradation with increasing thickness can be attributed to the stress-induced TiO_x phase transformation as well as surface roughening induced interface defects formation.

The thermal stability of TiO_x passivation quality was investigated after FGA annealing under increasing temperatures. Fig. 4 shows the variation of iV_{oc} of TiO_x passivated samples after FGA annealing at different temperatures. Obvious passivation improvement has been observed after FGA annealing at 250 °C for 30 min. However, significant passivation degradation with a rapid iV_{oc} decrease is observed after FGA annealing(300 °C for 30 min. Severe passivation degradation is observed with a thicker TiO_x film (e.g. 5.5 nm). The XRD spectra of the TiO_x film deposited at 300 °C by Liao et al. shown the presence of the anatase phase [33]. It is well known that amorphous TiO_x film is preferred for c-Si surface passivation, as they may introduce fewer interface defects compared to crystalline TiO_x films. Therefore, the TiO_x passivation degradation might be caused by the phase transformation from

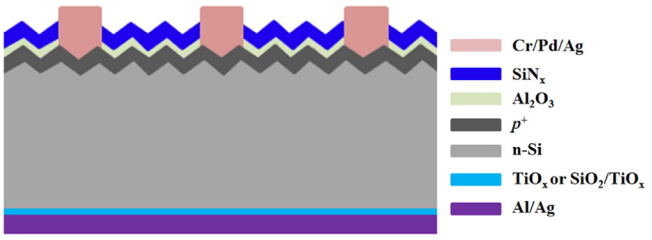

Fig. 2. The structure of n-type silicon heterojunction solar cell fabricated in this work, featuring a full-area TiO_x-based electron-selective contact at the rear side.

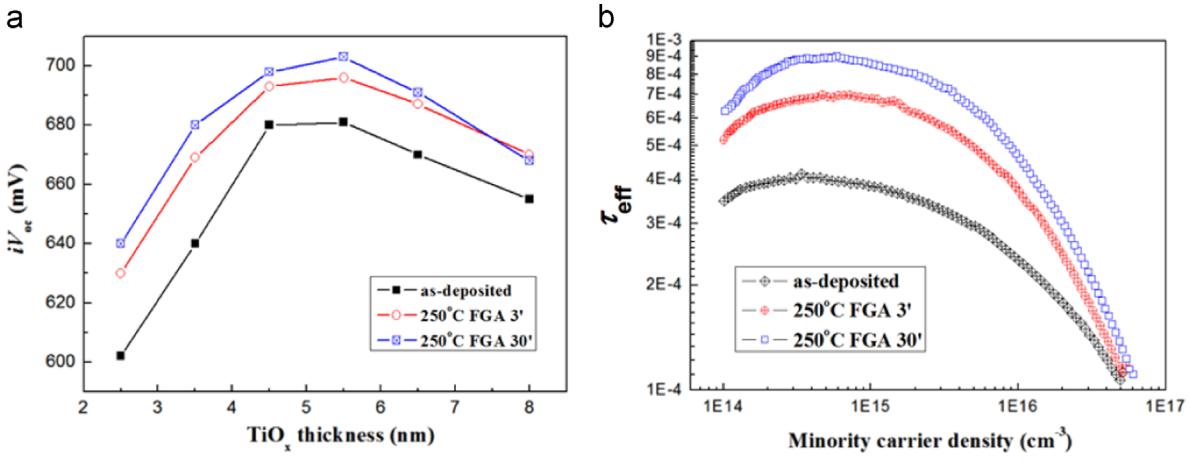

Fig. 3. (a) Effects of TiO_x film thickness on iV_{oc} value measured by the QSSPC technique. The iV_{oc} values after FGA at 250 °C for 3 and 30 min are shown together; and (b) Injection level dependent effective lifetimes of *n*-type silicon passivated by 5.5 nm TiO_x film before and after FGA annealing.

amorphous to the anatase of the as-deposited TiO_x film at a temperature of ≥ 300 °C.

3.2. Surface passivation quality of tunnel-SiO_2/TiO_x stack on silicon surface

It is well known that SiO_2 can provide a high level of passivation to silicon surfaces with a high thermal budget tolerance. SiO_2-based passivated contact or carrier selective contacts have been developed and implemented into high efficiency silicon solar cells [11,34–36]. To overcome the poor thermal stability of ultrathin TiO_x film passivation on silicon surface, a thermally grown tunnel SiO_2 (1.2–1.5 nm) was inserted between silicon and TiO_x film interface. The passivation quality of SiO_2/TiO_x stacks on n-type silicon surfaces (1.0 Ω cm) was investigated. RCA cleaned samples were subjected to a short thermal oxidation at 700 °C for 3 min, and then capped with different thickness TiO_x films on both sides. The iV_{oc} values before and after FGA annealing at different temperatures were obtained by QSSPC measurements. Fig. 5 shows the passivation quality and thermal stability of SiO_2/TiO_x stack on n-type silicon surface. The SiO_2/TiO_x stacks with a TiO_x thickness of 4.5 and 5.5 nm can provide good passivation to the n-type silicon surface, and an iV_{oc} value of(650 mV was achieved before FGA annealing. A low level surface passivation is observed for the SiO_2/TiO_x stack with a TiO_x thickness of 2.5 and 3.5 nm. After FGA annealing at higher temperatures, the passivation quality is improved for SiO_2/TiO_x stacks capped with a thin TiO_x layer (2.5 and 3.5 nm), whereas a gradual passivation degradation was observed for SiO_2/TiO_x stacks capped with a thick TiO_x layer (4.5 and 5.5 nm). Significant passivation degradation was observed in all SiO_2/TiO_x stacks after annealing at 400 °C. A maximum iV_{oc} value of (671 mV has been achieved with a SiO_2/TiO_x stack with a 3.5 nm TiO_x capping layer after FGA annealing at 350 °C for 30 min. The results demonstrate that SiO_2/TiO_x stacks can provide a good surface passivation on n-type silicon surface with an improved thermal stability (up to 350 °C).

The passivation of SiO_2/TiO_x stacks to silicon surfaces is considered to be achieved by a combination of chemical passivation of tunnel SiO_2 and field-effect passivation of the TiO_x film. FGA annealing can improve the chemical passivation of SiO_2 by the diffusion of atomic hydrogen to the SiO_2/n-Si interface where it deactivates recombination centers. However, FGA annealing will degrade the field-effect passivation induced by the TiO_x film. We speculate that the passivation quality of SiO_2/TiO_x stacks with a thin capping TiO_x layer (2.5 and 3.5 nm) is dominated by the chemical passivation of SiO_2, and that FGA annealing at a high temperature improves the passivation quality by the diffusion of atomic hydrogen to the SiO_2/n-Si interface through the thin capping layer. Further, we also speculate that the field-effect passivation of the TiO_x film makes a greater contribution to the passivation quality of SiO_2/TiO_x stacks with a thick capping TiO_x layer (4.5 and 5.5 nm), and that FGA annealing at a high temperature leads to the degradation of the field-effect passivation induced by the TiO_x film. Moreover, a thick TiO_x capping layer may also prevent the atomic hydrogen from diffusing to the SiO_2/n-Si interface, which leads to reduced improvement in SiO_2 chemical passivation. The results shown in Fig. 5 are considered to be caused by the trade-off between the chemical passivation of SiO_2 and field-effect passivation of the TiO_x film during FGA annealing.

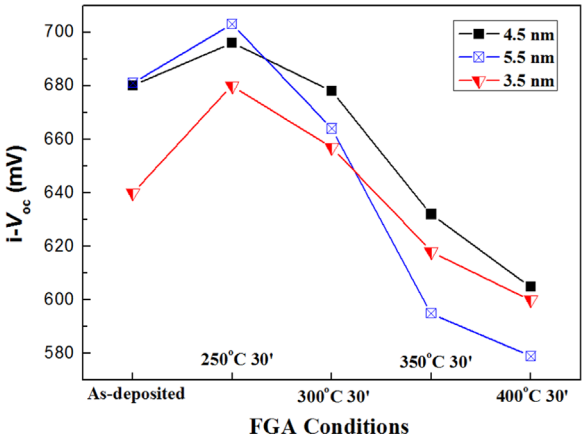

Fig. 4. Dependence of iV_{oc} value of TiO_x passivated samples on FGA annealing conditions.

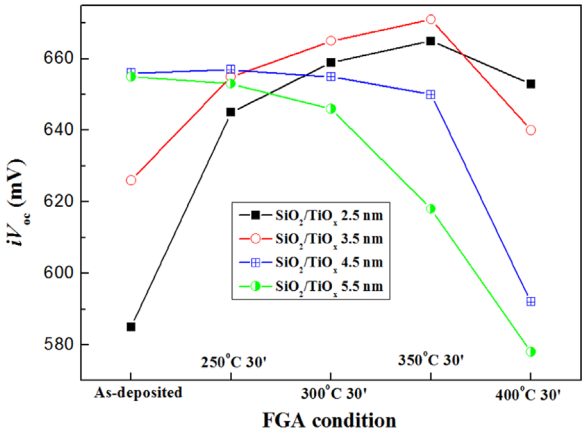

Fig. 5. Dependence of iV_{oc} value of SiO_2/TiO_x stack passivated samples on FGA annealing conditions.

3.3. Contact resistivity of TiO_x/n-Si heterojunction

Although ultrathin TiO_x film could provide good passivation to n-type silicon surface, the contact resistivity of TiO_x/n-Si heterojunction has to be determined before being applied to solar cells. Fig. 6 shows the dependence of contact resistivity on TiO_x film thickness for TiO_x/n-Si heterojunctions, which was extracted from the diode structure (inset in Fig. 6) developed by Cox and Strack [29]. All contacts with circular metal dots of different diameters (0.5–10 mm) at the top exhibit Ohmic *I–V* behavior, which demonstrates that electrons can pass through the ultrathin TiO_x layers. ρ_c values were extracted by fitting the curve of resistance versus top circle contact diameter. The ρ_c value increases as the TiO_x film thickness increases. A relatively low ρ_c value of

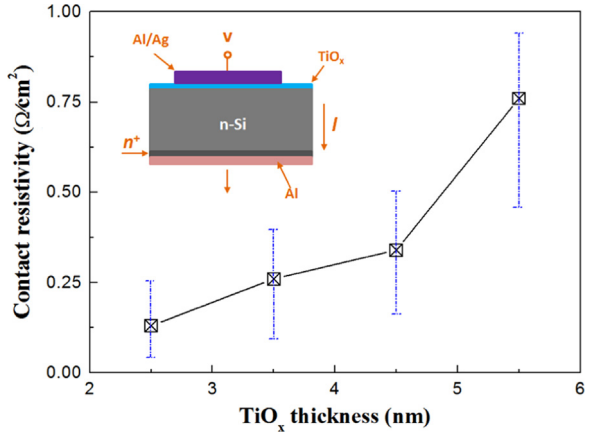

Fig. 6. Dependence of contact resistivity on TiO_x film thickness for TiO_x/n-Si heterojunction. The inset picture is the diode structure used to extract the contact resistivity. The lines are guides to the eyes.

Table 1
Prameters of the champion silicon heterojunction solar cells featuring an electron-selective TiO_x contact with different thickness. The pseudo fill factor (*pFF*) measured by Suns-V_{oc} and the calculated series resistance (R_s) are listed together.

TiO_x Thickness (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	*pFF* (%)	η (%)	R_s (mΩ cm^2)
3.5	603	39.1	80.3	83.3	18.9	0.55
4.5	632	39.3	79.4	82.7	19.7	0.64
5.5	615	39.4	76.6	80.5	18.6	0.76

(0.25 Ω cm^2, which is considered to be dominated by the TiO_x/n-Si interface, has been achieved with a TiO_x film thickness(4.5 nm. For greater TiO_x thicknesses (5.5 nm), ρ_c increases quickly to ~0.75 Ω cm^2. The TiO_x film bulk resistivity may have a higher contribution to the total ρ_c for TiO_x thicknesses ≥5.5 nm. Although these TiO_x/n-Si heterojunctions exhibit much higher contact resistivity than diffused n^+/n-Si homojunctions, they are still acceptable for full-area contacted silicon solar cells. The next section will present solar cells results from the implementation of a full-area electron-selective TiO_x contact.

3.4. N-type heterojunction solar cells with full-area electron-selective TiO_x contact

Based on the passivation performance and contact resistivity results obtained above, n-type silicon solar cells with the structure shown in Fig. 2 were fabricated with three different TiO_x thicknesses (3.5, 4.5 and 5.5 nm) at the rear. Table 1 shows the measured open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (*FF*), pseudo fill factor (*pFF*), conversion efficiency (η) and the series resistance (R_s) of the champion n-type solar cells featuring an electron-selective TiO_x contact with different thickness. The *pFF* was measured by *Suns-*V_{oc} at open circuit [37], which is free from the effects of series resistance. R_s was calculated by the fill factor method [38], which describes the series resistance as

$$R_s = \frac{V_{oc}}{J_{sc}}\left(1-\frac{FF}{pFF}\right)$$

All the light *I–V* curves show well-behaved solar cell characteristic, which confirm that the ultrathin TiO_x film blocks the holes in silicon from flowing into the rear contact. In other words, the TiO_x/n-Si heterojunction blocks the photo-generated holes while allowing electrons to pass through. The champion solar cell, which exhibits a V_{oc} of 632 mV, a J_{sc} of 39.3 mA/cm^2, and a *FF* of 79.4% resulting in an efficiency of 19.7%, is achieved with a 4.5 nm TiO_x film. The *FF* decreases as the TiO_x thickness increases, which might be caused by the increasing contact resistivity at the TiO_x/n-Si interface as shown in Fig. 6. A highest *FF* value of 80.3% has been achieved with a TiO_x thickness of 3.5 nm. A relatively high J_{sc} (>39 mA/cm^2) has been achieved for all cells thanks to the excellent optical property at the cell front, featuring a random pyramid structure coated with Al_2O_3/SiN_x stack. However, the solar cells' efficiency is mainly limited by a relatively low V_{oc} value, which is not consistent with the passivation results shown in Fig. 3a. We have demonstrated excellent passivation to the p^+ emitter by the Al_2O_3/SiN_x stack (emitter recombination current density J_{oe}(25 fA/cm^2), so the low V_{oc} must be related to high recombination at the rear passivated by the ultrathin TiO_x film. To form the front contact, these n-type solar cells experienced a final FGA annealing at 300 °C for 30 min, which causes the TiO_x passivation degradation at the rear side, as indicated in Fig. 4. After contact with the aluminum, we speculate that further passivation degradation might occur due to a possible reaction between TiO_x film and Al during the FGA annealing. Therefore, a low V_{oc} within those cells can be attributed to the degraded TiO_x passivation at the rear side.

Table 2
Parameters of the champion silicon heterojunction solar cell featuring an electron-selective SiO_2/TiO_x contact at the rear side under AM 1.5. For comparison, parameters of solar cells with a 3.5 nm TiO_x or a tunnel SiO_2 at the rear side are shown together. The pseudo fill factor (*pFF*) measured by Suns-V_{oc} and the calculated series resistance (R_s) are listed together.

Device	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	*pFF* (%)	η (%)	R_s (mΩ cm^2)
TiO_x (3.5 nm)	603	39.1	80.3	83.3	18.9	0.55
SiO_2 (1.5 nm)	608	39.0	74.8	80.1	17.7	1.03
SiO_2/TiO_x	650	39.5	80.0	83.0	20.5	0.59

3.5. N-type solar cells with a full-area electron-selective SiO_2/TiO_x contact

To improve the efficiency of solar cells with an electron selective TiO_x contact, a tunnel SiO_2 was inserted between TiO_x and silicon interfaces. The SiO_2/TiO_x stack with a thin capping TiO_x layer of 3.5 nm was selected based on the passivation quality shown in Fig. 5. A tunnel SiO_2 was thermally grown before the TiO_x film deposition at the rear, and then annealed in FGA at 350 °C for 30 min to improve the passivation of SiO_2/TiO_x stack. The final contact formation anneal was also performed in FGA at 350 °C for 30 min this time instead of 300 °C. Control cells without TiO_x after tunnel SiO_2 growth at the rear were prepared with the same processing. The parameters of the champion n-type solar cells with SiO_2/TiO_x stack, TiO_x (3.5 nm) and tunnel SiO_2 at the rear side are shown together in Table 2. Solar cells efficiency was improved to 20.5% by the implementation of the electron selective SiO_2/TiO_x contact, which exhibits a stable surface passivation during the final contact annealing. Insertion of a tunnel SiO_2 interlayer between the TiO_x and n-Si interface leads to an obvious increase of the V_{oc} (+47 mV) and J_{sc} (+ 0.4 mA/cm^2), which can be attributed to reduced recombination at the rear. The *FF* slightly decreases from 80.3% to 80.0%, due to the increasing R_s, resulting in an absolute efficiency gain of 1.6%. The cell without TiO_x at the rear (tunnel SiO_2 only) shows the lowest efficiency (17.7%), which is mainly limited by a relatively low *FF* value that might be attributed to a high contact resistance at the rear. The parameters of the cell with SiO_2/TiO_x contact are comparable to that of passivated-emitter, rear totally diffused (PERT) cell (average V_{oc} 661 mV, J_{sc} 40.0 mA/cm^2, *FF* 80.4% and η 21.1%) with the same front features [39], which indicates that the electron selective TiO_x contact could act as a simpler alternative to a phosphorous diffused region and passivation layer for solar cells. The results demonstrate that the SiO_2/TiO_x stack is an efficient electron selective contact with a better thermal stability, which shows great potential for future high efficiency silicon solar cells.

Fig. 7 shows the internal quantum efficiency (IQE) of the n-type solar cells with an electron-selective TiO_x or SiO_2/TiO_x contact at the rear. IQE was calculated by the measured reflectance and external quantum efficiency (EQE) data using IQE=EQE/(1−*R*). All solar cells show a very high IQE in the short wavelength range (300–800 nm), which indicates an excellent front passivation with Al_2O_3/SiN_x stack and low recombination at the front. However, an obvious lower IQE in the long wavelength range (>800 nm) is observed for the cell with an electron-selective TiO_x contact at the rear side. The poor long-wavelength response can be attributed to the high recombination at the rear surface passivated by TiO_x films. Insertion of a tunnel SiO_2 interlayer between the TiO_x and n-Si interface leads to a much better long-wavelength response, resulting in an obvious increase of V_{oc} and J_{sc}. The IQE result

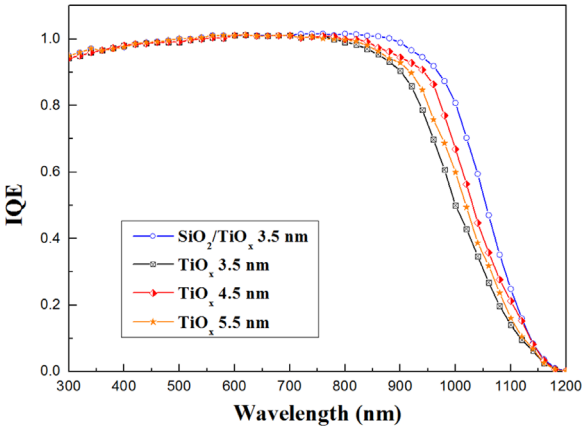

Fig. 7. IQE of the n-type silicon solar cells with an electron-selective TiO_x or SiO_2/TiO_x contact at the rear.

confirms that the conversion efficiency improvement is achieved by reducing the recombination at the rear side, which is passivated by the SiO_2/TiO_x stack.

3.6. *Potential efficiency of n-type solar cells with a full-area electron selective TiO_x contact*

Although the initial work shown above has illuminated the great potential of TiO_x selective contact for silicon solar cells, the efficiency achieved here is still much lower than solar cells with a-Si: H and SiO_2-based selective contacts. The efficiency is expected to be improved significantly by maintaining the high quality surface passivation of ultrathin TiO_x on the devices. Based on the recombination parameter (J_{oe}) measurements, we calculate the maximum V_{oc} value of the n-type solar cells featuring a 4.5 nm TiO_x selective contact using the equation:

$$V_{oc} = V_T \ln\left(\frac{J_{sc}}{J_{oe}} + 1\right)$$

where V_T=25.7 mV is the thermal voltage at a temperature of 25 °C and J_{sc}= 41.1 mA/cm^2. A high resistivity (100 Ω cm) silicon wafer was double side passivated by a 4.5 nm TiO_x film and then FGA anneal at 250 °C for 30 min, and a J_o value of ~25 fA/cm^2 has been extracted by QSSPC measurement using the Kane and Swanson technique [40]. The Al_2O_3/SiN_x passivated p^+ emitter and the metalized region show a J_o value of ~25 and ~1500 fA/cm^2, respectively. The total J_{oe} of the n-type solar cells featuring a full-area TiO_x selective contact at the rear is calculated as follows:

$$J_{o,\ total} = (1-f)\,J_{o,\ p+} + f \cdot J_{o,\ metal} + J_{o,\ rear} = 72\ \text{fA/cm}^2$$

where f=1.5% is the metallization fraction of our front grid. The recombination within the base is neglected due to high quality FZ silicon wafers are used for the cells. A realistic reachable V_{oc} value of ~696 mV can be achieved by the calculation. By assuming an upper fill factor of 82.7% obtained in Table 1 and a maximum J_{sc} value of 41.1 mA/cm^2, a potential efficiency of as high as 23.7% can be achieved on the n-type solar cells with a full-area TiO_x contact. Further improvement with the efficiency > 24% is also expected by reducing the front J_{oe} value by the implementation of a selective emitter.

4. Conclusions

We have investigated the electron-selective contact characteristic of ultrathin TiO_x films on silicon. Ultrathin TiO_x films deposited by ALD have been demonstrated to provide not only good passivation to the n-type silicon surface, but also allow a relatively low contact resistivity. A simple silicon heterojunction solar cell with an efficiency of up to 19.7% has been achieved with the implementation of a TiO_x/Si heterojunction at the rear side. Insertion of a tunnel SiO_2 interlayer between the TiO_x and silicon interface improves the efficiency significantly to 20.5%. Based on realistic assumptions, a calculated potential efficiency of up to 23.7% can be achieved with n-type silicon solar cells featuring an electron selective TiO_x contact at the rear. The results show that replacement of the phosphorus diffusion regions and passivation layers with a TiO_x-based electron-selective contact at the rear results in a high efficiency n-type solar cell with a simplified fabrication process. This work highlights the great application potential of TiO_x-based electron-selective contacts in future high efficiency, low cost silicon solar cells.

Acknowledgment

The authors acknowledge financial support from the Australian Renewable Energy Agency (ARENA) (No. 6-F007) under the Post-doctoral Fellowship. We also would like to thank Andres Cuevas (ANU) and Andrew Thomson (ANU) for the helpful discussion.

References

[1] J. Zhao, A. Wang, Martin A. Green, 24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates, Prog Photovolt. 7 (1999) 471–474.
[2] J. Benick, B. Steinhauser, R. Müller, J. Bartsch, M. Kamp, A. Mondon, A. Richter, M. Hermle, S. Glunz, High efficiency n-type PERT and PERL solar cells, in: Proceeding of the 40th IEEE Photovoltaics Specialist Conference, Denver, USA, 3637 (2014).
[3] J. Benick, B. Hoex, M. Sanden, W. Kessels, O. Schultz, S. Glunz, High efficiency n-type Si solar cells on Al_2O_3-passivated boron emitters, Appl. Phys. Lett. 92 (2008) 253504.
[4] M.A. Green, A.W. Blakers, N.R. Willison, T. Szpitalak, E.M. Keller, E. Gauja, P.J. Bart, The MINP solar cell- a new high voltage, high efficiency silicon solar cell, in: Proceeding of the 15th IEEE Photovoltaics Specialist Conference, 1981, pp. 1405–1408.
[5] A. Metz and R. Hezel, Recorded efficiency above 21% for MIS-contacted diffused junction silicon solar cells, in: Proceeding of the 26th IEEE Photovoltaics Specialist Conference, 1997, pp. 283–286.
[6] X. Loozen, J.B. Larsen, F. Dross, M. Aleman, T. Bearda, B.J. O'Sullivan, I. Gordona, J. Poortmans, Passivation of a metal contact with a tunnelling layer, Energy Procedia 21 (2012) 75–83.
[7] D. Garcia-Alonso, S. Smit, S. Bordihn, W. Kessels, Silicon passivation and tunneling contact formation by atomic layer deposited Al_2O_3/ZnO stacks, Semicond. Sci. Technol. 28 (2013) 082002.
[8] J. Bullock, D. Yan, A. Cuevas, Passivation of aluminium$^-$n$^+$ silicon contacts for solar cells by ultrathin Al_2O_3 and SiO_2 dielectric layers, Phys. Status Solidi (RRL) 7 (2013) 946–949.
[9] J. Bullock, D. Yan, Y. Wan, A. Cuevas, B. Demaurex, A. Hessler-Wyser, S. De Wolf, Amorphous silicon passivated contacts for diffused junction silicon solar cells, J. Appl. Phys. 115 (2014) 163703.
[10] K. Masuko, M. Shigematsu, T. Hashiguchi, D. Fujishima, M. Kai, N. Yoshimura, T. Yamaguchi, Y. Ichihashi, T. Mishima, N. Matsubara, T. Yamanishi, T. Takahama, M. Taguchi, E. Maruyama, S. Okamoto, Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell, IEEE J. Photovolt. 4 (2014) 1433–1435.
[11] F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, S.W. Glunz, Tunnel oxide passivated contacts as an alternative to partial rear contacts, Sol. Energy Mater. Sol. Cells 131 (2014) 46–50.
[12] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, J. Benick, M. Hermle, Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO_2 layers, Sol. Energy Mater. Sol. Cells, ⟨http://dx.doi.org/10.1016/j.solmat.2015.06.048⟩.
[13] D. Zielke, C. Niehaves, W. Lövenich, A. Elschner, M. Hörteis, J. Schmidt, Organic-silicon solar cells exceeding 20% efficiency, Energy Procedia 77 (2015) 331–339.
[14] S. Murase, Y. Yang, Solution processed MoO_3 interfacial layer for organic photovoltaics prepared by a facile synthesis method, Adv. Mater. 24 (2012) 2459.
[15] Y. Zhao, A.M. Nardes, K. Zhu, Effective hole extraction using MoO_x-Al contact in perovskite $CH_3NH_3PbI_3$ solar cells, Appl. Phys. Lett. 104 (2014) 213906.

[16] M.D. Irwin, D.B. Buchholz, A.W. Hains, R.P.H. Chang, T.J. Marks, p-Type semiconducting nickel oxide as an efficiency-enhancing anode interfacial layer in polymer bulk-heterojunction solar cells, PNAS 105 (2007) 2783.
[17] S. Bai, M. Cao, Y. Jin, X. Dai, X. Liang, Z. Ye, M. Li, J. Cheng, X. Xiao, Z. Wu, Z. Xia, B. Sun, E. Wang, Y. Mo, F. Gao, F. Zhang, Low-temperature combustion-synthesized nickel oxide thin films as hole-transport interlayers for solution-processed optoelectronic devices, Adv. Energy Mater. 4 (2014) 1301460.
[18] D. Gebeyehu, C.J. Brabec, N.S. Sariciftci, D. Vangeneugden, R. Kiebooms, D. Vanderzande, F. Kienberger, H. Schindler, Hybrid solar cells based on dye-sensitized nanoporous TiO_2 electrodes and conjugated polymers as hole transport materials, Synth. Met. 125 (2011) 279–287.
[19] S. Cho, J. Yeo, D. Kim, S. Na, S. Kim, Brush painted V_2O_5 hole transport layer for efficient and air-stable polymer solar cells, Sol. Energy Mater. Sol. Cells 132 (2015) 196–203.
[20] C. Battaglia, S.M. Nicolas, S.D. Wolf, X. Yin, M. Zheng, C. Ballif, A. Javey, Silicon heterojunction solar cell with passivated hole selective MoO_x contact, Appl. Phys. Lett. 104 (2014) 113902.
[21] J. Bullock, A. Cuevas, T. Allen, C. Battaglia, Molybdenum oxide MoO_x: a versatile hole contact for silicon solar cells, Appl. Phys. Lett. 105 (2014) 232109.
[22] S. Avasthi, W. McClain, G. Man, A. Kahn, J. Schwartz, J. Sturm, Hole-blocking titanium-oxide/silicon heterojunction and its application to photovoltaics, Appl. Phys. Lett. 102 (2013) 203901.
[23] J. Jhaveri, S. Avasthi, K. Nagamatsu, J.C. Sturm, Stable low-recombination n-Si/TiO_2 hole-blocking interface and its effect on silicon heterojunction photovoltaics, in: Proceeding of the 40th IEEE Photovoltaics Specialist Conference, Denver, 2014, pp. 1525–1528.
[24] S. Avasthi, K. Nagamatsu, J. Jhaveri, W.E. McClain, G. Man, A. Kahn, J. Schwartz, S. Wagner, J. Sturm, Double-heterojunction crystalline silicon solar cell fabricated at 250 °C with 12.9% efficiency, in: Proceeding of the 40th IEEE Photovoltaics Specialist Conference, Denver, 2014, pp. 949–952.
[25] K. Nagamatsu, S. Avasthi, G. Sahasrabudhe, G. Man, J. Jhaveri, A. Berg, J. Schwartz, A. Kahn, S. Wagner, J.C. Sturm, Titanium dioxide/silicon hole-blocking selective contact to enable double-heterojunction crystalline silicon-based solar cell, Appl. Phys. Lett. 106 (2015) 123906.
[26] D. Suh, D. Choi, K. Weber, Al_2O_3/TiO_2 stack layers for effective surface passivation of crystalline silicon, J. Appl. Phys. 114 (2013) 154107.
[27] X. Yin, C. Battaglia, Y. Lin, K. Chen, M. Hettick, M. Zheng, C. Chen, D. Kiriya, A. Javey, 19.2% Efficient InP heterojunction solar cell with electron-selective TiO_2 contact, ACS Photon. 1 (2014) 1245.
[28] R.A. Sinton, A. Cuevas, and M. Stuckings, Quasi-steady-state photoconductance, a new method for solar cell material and device characterization, in: Proceedings of the 25th IEEE Photovoltaic Specialists Conference, USA, 1996, pp. 457–460.
[29] R. Cox, H. Strack, Ohmic contacts for GaAs devices, Solid-State Electron. 10 (1967) 1213–1218.
[30] G. Dingemans, W.M.M. Kessels, Aluminumm oxide and other ALD materials for Si surface passivation, ECS Trans. 41 (2011) 293–301.
[31] I. Chang Yu, H. Cheng, Y. Lin, Surface Passivation of c-Si by atomic layer deposition TiO_2 thin films deposited at low temperature, in: Proceedings of the 40th IEEE Photovoltaics Specialist Conference, Denver, 2014, pp. 1271–1274.
[32] I. Yu, Y. Wang, H. Cheng, Z. Yang, C. Lin, Surface passivation and antireflection behaviour of ALD TiO_2 on n-type silicon for solar cells, Int. J. Photoenergy (2013) 431614.
[33] B. Liao, B. Hoex, A.G. Aberle, D. Chi, C.S. Bhatia, Excellent c-Si surface passivation by low-temperature atomic layer deposited titanium oxide, Appl. Phys. Lett. 104 (2014) 253903.
[34] X. Yang, J. Bullock, Q. Bi, K. Weber, High efficiency n-type silicon solar cells featuring passivated contact to laser doped regions, Appl. Phys. Lett. 106 (2015) 113901.
[35] J. Bullock, A. Cuevas, C. Samundsett, D. Yan, J. McKeon, Y. Wan, Simple silicon solar cells featuring an a-Si:H enhanced rear MIS contact, Sol. Energy Mater. Sol. Cells 138 (2015) 22–25.
[36] X. Yang, J. Bullock, L. Xu, Q. Bi, S. Surve, M. Ernst, K. Weber, Passivated contacts to laser doped p^+ and n^+ regions, Sol. Energy Mater. Sol. Cells 140 (2015) 38–44.
[37] R.A. Sinton and A. Cuevas, A quasi-steady-state open-circuit voltage method for solar cell characterization, in: Proceedings of the 16th Eur. Photovoltaic Solar Energy Conference, U.K., 2000, pp. 1152–1155.
[38] M.A. Green, Solar cells: Operating Principles, Technology and System Applications, Univ. New South Wales, Sydney, Australia (1998), p. 96.
[39] Y. Wan, C. Samundsett, T. Kho, J. McKeon, L. Black, D. Macdonald, A. Cuevas, J. Sheng, Y. Sheng, S. Yuan, C. Zhang, Z. Feng and P.J. Verlinden, Towards industrial advanced front-junction *n*-type silicon solar cells, in: Proceedings of the 40th IEEE Photovoltaic Specialists Conference, USA, 2014, pp. 862–865.
[40] D.E. Kane and R.M. Swanson, Measurement of the emitter saturation current by a contactless photoconductivity decay method, in: Proceedings of the 18th IEEE Photovoltaic Specialist Conference, Las Vegas, USA , (1985), pp. 578–583.