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RESEARCH ARTICLE

Large area tunnel oxide passivated rear contact *n*-type Si solar cells with 21.2% efficiency

Yuguo Tao[1]*, Vijaykumar Upadhyaya[1], Chia-Wei Chen[1], Adam Payne[2], Elizabeth Lori Chang[1], Ajay Upadhyaya[1] and Ajeet Rohatgi[1,2]

[1] Georgia Institute of Technology, 777 Atlantic Drive, Atlanta, GA, 30332-0250, USA
[2] Suniva Inc., 5765 Peachtree Industrial Blvd., Norcross, GA, 30092, USA

ABSTRACT

This paper reports on the implementation of carrier-selective tunnel oxide passivated rear contact for high-efficiency screen-printed large area *n*-type front junction crystalline Si solar cells. It is shown that the tunnel oxide grown in nitric acid at room temperature (25°C) and capped with n^+ polysilicon layer provides excellent rear contact passivation with implied open-circuit voltage iV_{oc} of 714 mV and saturation current density J_{0b}' of 10.3 fA/cm^2 for the back surface field region. The durability of this passivation scheme is also investigated for a back-end high temperature process. In combination with an ion-implanted Al_2O_3-passivated boron emitter and screen-printed front metal grids, this passivated rear contact enabled 21.2% efficient front junction Si solar cells on 239 cm^2 commercial grade *n*-type Czochralski wafers.

KEYWORDS
tunnel oxide; passivated contact; room temperature; large area; *n*-type Cz wafer; screen-printed

***Correspondence**
Yuguo Tao, School of Electrical and Computer Engineering, Georgia Institute of Technology, 777 Atlantic Drive, Atlanta, GA 30332-0250, USA.
E-mail: yuguo.tao@ece.gatech.edu

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1. INTRODUCTION

As the photovoltaic industry strives towards higher energy conversion efficiency, carrier-selective passivated contact with low minority carrier recombination and efficient majority carrier transport has become an active area of investigation for high-efficiency *n*-type Si solar cells [1–4]. The best example of the potential of passivated contact is the heterojunction Si cell with intrinsic thin amorphous layer (HIT) solar cell. HIT cells have produced outstanding cell V_{oc} of 750 mV [1] and cell efficiency exceeding 25% [2]. However, this passivation scheme cannot withstand temperature above 250°C for the metallization process and, hence, is not compatible with the widely used industry standard low-cost screen-printed metallization, which requires high temperature contact firing (>700°C). Another example of outstanding carrier-selective passivated contact scheme involves an ultra-thin tunnel oxide capped with a phosphorus-doped polycrystalline Si (*poly*-Si) layer. This scheme is referred as TOPCon or tunnel oxide passivated contact, which has shown great thermal stability at high temperatures [3]. By applying boron-diffused homogeneous emitter and photolithographically defined front contacts (Ti/Pd/Ag), Feldmann, *et al.* [5] have demonstrated TOPCon cells with 24.0% efficiency on a small area *n*-type float-zone Si substrate. The tunnel oxide layer in this TOPCon structure was grown in 68 wt% nitric acid at a temperature of 110°C, close to its boiling point of 120°C [6,7]. In order to apply the TOPCon concept to a more manufacturable device, in this work, we demonstrate large area screen-printed and ion-implanted *n*-type Czochralski (Cz) Si solar cells with a tunnel oxide grown at room temperature (25°C). This tunnel oxide layer plays a crucial role in providing excellent interface passivation and allows transport of majority carriers to the back metal contact while blocking minority carriers. This is partly due to the difference in barrier height and effective mass in the oxide, which dictates the tunnelling probability for a given tunnel oxide thickness [8]. In addition, the tunnel oxide layer prevents epitaxial regrowth of as-deposited *n*-type *a*-Si layer

during thermal crystallisation and dopant activation anneal [9]. In this work, the n^+ *poly*-Si layer on top of tunnel oxide is formed by depositing a phosphorus-doped *a*-Si layer by low temperature (≤300°C) single-side plasma-enhanced chemical vapour deposition (PECVD) followed by thermal crystallisation and dopant activation anneal at high temperature (>850°C). This n^+ *poly*-Si layer enables the quasi-Fermi level splitting of the absorber by the n–n^+ high–low junction, which reflects minority carriers from the surface (field passivation function). The single-side deposition simplifies the cell process sequence. The optimization of n^+ *poly*-Si layer is described in our previous report [10].

2. EXPERIMENTS

The interface quality of passivated rear contact was studied by the quasi-steady-state photoconductance (QSSPC) measurements [11] on symmetrical test structures Si(n^+)/SiO_x/*c*-Si(*n*)/SiO_x/Si(n^+). Symmetrical samples were made on commercially available 5 Ωcm 200-μm-thick *n*-type Cz wafers with a bulk lifetime of over 2 ms. The sample preparation involved surface damage removal in a heated KOH solution, followed by a chemical cleaning and tunnel oxide growth in 68 wt% HNO_3 acid at room temperature for 10 min. The resulting tunnel oxide thickness was ~15 Å, determined by spectral ellipsometry, which is thinner than the maximum allowed oxide thickness of 20 Å for efficient tunnelling [12]. Next, a thin (<20 nm) phosphorus-doped Si layer was deposited on both sides using a PECVD tool from Unaxis, followed by a 875°C 30 min anneal in an inert atmosphere to facilitate crystallisation and dopant activation. It is noteworthy that appreciable hydrogen gas flow was used during the *a*-Si deposition to achieve the desired passivation quality [10], which eliminated the need for post-hydrogenation by atomic hydrogen [6] or forming gas anneal [13] after the crystallisation anneal. Finally, the QSSPC technique proposed by Kane and Swanson [14] was used to determine the passivation quality by extracting the implied V_{oc} (iV_{oc}) from the injection level at one sun according to the following equation:

$$iV_{oc} = \frac{kT}{q} \ln\left(\frac{\Delta n(\Delta n + N_D)}{{n_i}^2}\right), \quad (1)$$

where Δn is the excess carrier density at 1 sun, k the Boltzmann constant, T the temperature, q the elementary charge, N_D the bulk doping density and n_i the intrinsic carrier density.

In order to investigate the performance of our rear side tunnel oxide-passivated contact in a finished device, large area front junction *n*-type Si solar cells were fabricated on a 4.5 Ωcm Cz wafers (Figure 1). Note that there are five cells in a batch during process. The fabrication process involved saw damage removal in a heated KOH solution followed by alkaline texturing on both sides of the wafers.

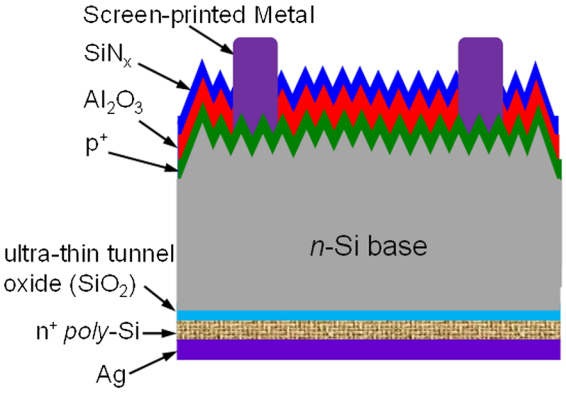

Figure 1. Schematic of the solar cell structure with tunnel oxide/n^+ *poly*-Si passivated rear contact and the screen-printed front contact.

Next, a SiN_x mask on the front side was deposited, followed by a heated KOH treatment to planarize the back. After the planarization, the wafer thickness was reduced to about 175 μm. The boron ion implantation with proper dose and energy was performed on a production line implanter at Suniva Inc. Then, a high temperature anneal (>1000°C) was used to restore the lattice [15,16] and eliminate the boron-rich layer formation [17,18]. The resulting sheet resistivity was ~110 Ω/□ for the boron emitter. Next, the room temperature tunnel oxide and n^+ *poly*-Si layers were grown on the rear side according to the process described above. Then a thin Al_2O_3 was deposited by atomic layer deposition and capped with PECVD SiN_x film for front surface passivation and anti-reflection coating. The optimised screen-printed Ag/Al grid coverage on the front was ~5.6% with 89 grid lines and grid line width of ~52 μm. A high temperature firing (~730°C) was performed in an industrial-style belt furnace to achieve good ohmic contact [17,19]. Finally, approximately 1-μm-thick Ag film was deposited by thermal evaporation on the entire rear side.

3. RESULTS AND DISCUSSIONS

3.1. The interface passivation on symmetrical structure

Table I summarises the QSSPC results. A high iV_{oc} of 714 mV was obtained after the thermal crystallisation and dopant activation anneal, with corresponding saturation current density (J_{0b}') of 10.3 fA/cm^2 for the back surface field region. This is comparable with the one realised with 110°C 10 min tunnel oxide growth in nitric acid on a similar TOPCon structure (9–13 fA/cm^2) [3] as well as the one formed by 650°C 5 min growth of SIPOS (10 fA/cm^2) [20]. The measured high implied fill factor (*iFF*) of 84.3% indicates that our passivated contact has very low interface recombination at maximum power point [21]. However, after the high temperature firing at ~730°C (for the

Table I. Summary of QSSPC measurements on symmetrical structure with various tunnel oxides.

Tunnel oxide growth temperature	Process status	iV_{oc} [mV]	J_{ob}' [fA/cm^2]	*iFF* [%]
25°C (room temperature)	After anneal	714	10.3	84.3
	After firing	707	13.9	84.0
100°C	After anneal	726	5.7	84.5
	After firing	709	12.8	84.1
poly-Si without tunnel oxide layer	After anneal	601	1138	82.4

screen-printed Al/Ag grid lines on the front for device fabrication [17]), the iV_{oc} and *iFF* dropped to 707 mV and 84.0%, and the J_{0b}' increased from 10.3 to 13.9 fA/cm^2. This degradation may be attributed to small local disruptions or breaking up of the tunnel oxide layer [9] during the rapid thermal firing. We also experimented with tunnel oxide grown in 100°C nitric acid for 10 min. The resulting data on symmetrical structures in Table I show that the passivation quality for tunnel oxide grown at 100°C with iV_{oc} of 726 mV is superior to the one grown at room temperature. However, after the high temperature firing at ~730°C, the passivation quality of two tunnel oxides become comparable with iV_{oc} of 707–709 mV. It is also important to note that without the tunnel oxide layer, iV_{oc} was only 601 mV with J_{0b}' of 1138 fA/cm^2 for our passivation scheme (Table I).

3.2. Solar cells with room temperature tunnel oxide passivated rear contact

Table II summarises the solar cell data for the 21.2% ion-implanted screen-printed large area *n*-type front junction cell with passivated rear contact formed by room temperature tunnel oxide capped with n^+ *poly*-Si and metal layers. A high V_{oc} of 683.4 mV was achieved, without the selective emitter, supporting excellent rear passivation. The cell also showed a high short-circuit current density J_{sc} of 39.66 mA/cm^2 and fill factor *FF* of 78.1%. The cell was tested using the Fraunhofer ISE certificated 20.2% efficient large area *n*-type cell [22] as a reference. The photoluminescence image [23,24] of the finished device (Figure 2) shows a reasonable uniformity of our passivated rear contact with the exception of some intrinsic defects along wafer edge. This could be due to the defects induced during the fabrication processes (such as cassette contact during production line texturing and boat contact during the furnace anneal). The high shunt

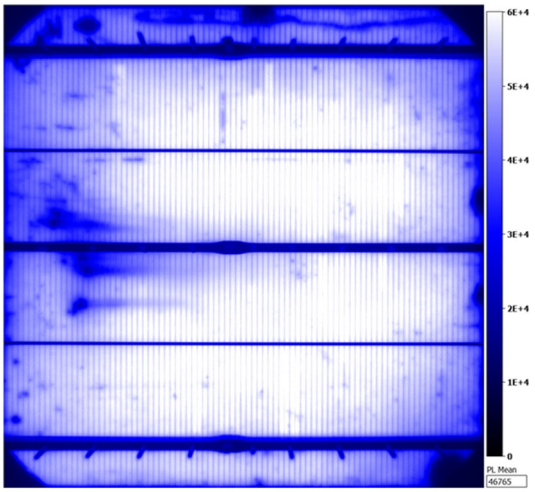

Figure 2. Photoluminescence (PL) image measured at open-circuit condition on the finished cell. Note that only three bus bars are available on our PL imaging equipment, but five bus bars were printed.

resistance R_{sh} value of 13.4 kΩcm^2 (Table II) supports no wrap-around issues during the single-side PECVD deposition. The average results of a batch of five cells are also shown in Table II, indicating that the process conditions can be controlled and the results can be repeated.

In order to understand and quantify the recombination losses in the finished cell, a V_{oc} loss analysis was performed using detailed characterisation and one-diode model equation:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_{0e} + J_{0b}} + 1\right), \quad (2)$$

First, emitter saturation current density (J_{0e}) of Al_2O_3/SiN_x passivated boron emitter [25] was measured (24 fA/cm^2) using the QSSPC measurement on the unmetallized symmetrical emitter structure (SiN_x/Al_2O_3/p^+/*n*/p^+/Al_2O_3/SiN_x). Because of the 5.6% metal coverage, contribution from the passivated field region $J_{0e,pass} = 24 \times (1–0.056) \approx 23$ fA/cm^2. Using the Sentaurus simulation program [26–28] and the boron emitter profile, the simulated emitter saturation current density as a function of the front surface recombination velocity (SRV) was obtained and shown in Figure 3. It is indicated in Figure 3 that SRV is about 590 cm/s for J_{oe} of 24 fA/cm^2 without metal. According to Figure 3, metallised saturation current density becomes 900 fA/cm^2 for this boron profile at SRV

Table II. The *I–V* parameters of 21.2% *n*-type front junction Si solar cell featuring passivated rear contact with tunnel oxide grown at room temperature.

	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	Efficiency [%]	*n*-factor	R_s [Ωcm^2]	R_{sh} [Ωcm^2]
Average (5 cells)	678.5 ± 4.9	39.46 ± 0.2	78.6 ± 0.5	21.0 ± 0.2	1.16 ± 0.04	0.74 ± 0.10	13228 ± 2000
Best	683.4	39.66	78.1	21.2	1.18	0.75	13400

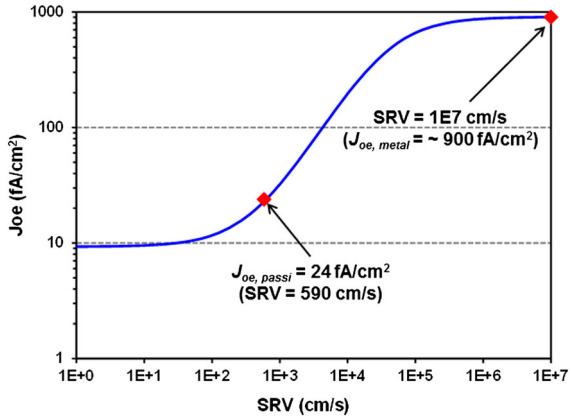

Figure 3. Simulated emitter saturation current density (J_{oe}) as a function of surface recombination velocity (SRV).

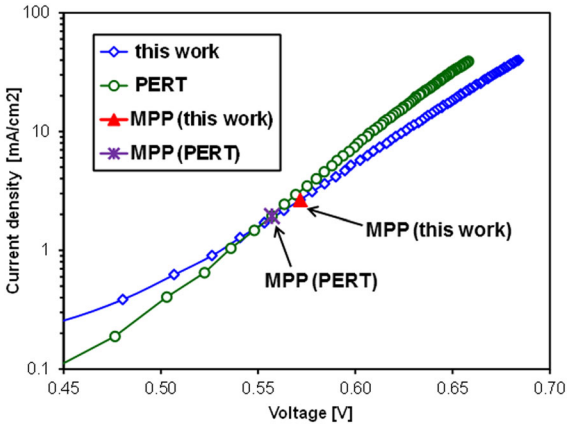

Figure 4. Comparison of the shifted *I–V* curves and the maximum power point (MPP) of the passivated contact from this work and PERT cells from early work [31].

of 10^7 cm/s (assuming surface recombination velocity of contact $S_{contact} = 10^7$ cm/s). Compared with the reported metal-induced emitter saturation current density values from other groups [29,30], 900 fA/cm^2 is relatively low, because our boron emitter has deeper profile (~1.0 µm vs ~0.6 µm). So, this corresponds to metal grid contribution to saturation current density $J_{0e,metal} = 900 \times 0.056 \approx 50$ fA/cm^2. Accounting for the measured J_{0b}' of 14 fA/cm^2 from the passivated rear contact and the $J_{0b,bulk}$ of 25 fA/cm^2 for 2 ms bulk lifetime base, $J_{0,total} = J_{0e} + J_{0b} = 23 + 50 + 14 + 25 = 112$ fA/cm^2. This combined with the measured J_{sc} of 39.66 mA/cm^2 gives a calculated V_{oc} of 683 mV, which is in excellent agreement with the experimental cell V_{oc} (Table II). These calculations also reveal that about 65% of the total recombination is attributed to the front side, and the 68% of the emitter side recombination is associated with the screen-printed metal contacts. This suggests that the cell V_{oc} can be improved further by introducing a selective emitter underneath the metal contact.

In addition to providing excellent interface passivation, the tunnel oxide passivated rear contact must allow an efficient transport of majority carriers to enable high *FF*. However, the *FF* of 78.1% obtained in this paper is relatively low, compared with 80.4% achieved for our screen-printed PERT (passivated emitter, rear totally diffused) cells [31]. This is attributed to slightly higher ideality factor (*n*-factor) and higher series resistance (R_s) in our current tunnel oxide passivated devices. Detailed analysis of the individual components contributing to R_s [32] in this cell showed that high sheet resistance ($R_{sheet} = 0.29\ \Omega$cm^2) and high grid line resistance ($R_{grid} = 0.30\ \Omega$cm^2) on the front side contributed to higher R_s. High sheet can be explained by the higher sheet resistance (110 Ω/□) of these cells compared with the PERT cell (90 Ω/□). High contact resistance is explained by lower surface concentration of the boron emitter. Note that exactly same screen-printed Al/Ag paste and firing conditions were used for these and PERT cells. Figure 4 shows the comparison of J–J_{sc} curves (shifting the J_{sc} from the fourth into the first quadrant) and the maximum power point for these and PERT cells. Lower slope of the passivated contact cell of this work confirms the higher *n*-factor. The exact reason for higher *n*-factor is not fully understood at this time. Better understanding and minimization of these losses and further optimization of tunnel oxide passivated contact can drive the cell efficiency beyond 22%.

The high internal quantum efficiency in Figure 5 confirms the effective surface passivation on both front and rear surfaces. The excellent internal reflection of light at the rear side is also supported by the high escape reflectance in the long wavelength range (1000–1200 nm), which reduces the probability of absorption in the passivated rear contact [33]. Figure 6 shows the measured light *I–V* data of the cell achieved on a 239 cm^2 Cz wafer (~4.5 Ωcm after annealing), with a V_{oc} of 683.4 mV, J_{sc} of 39.66 mA/cm^2, *FF* of 78.1% and cell efficiency of 21.2%.

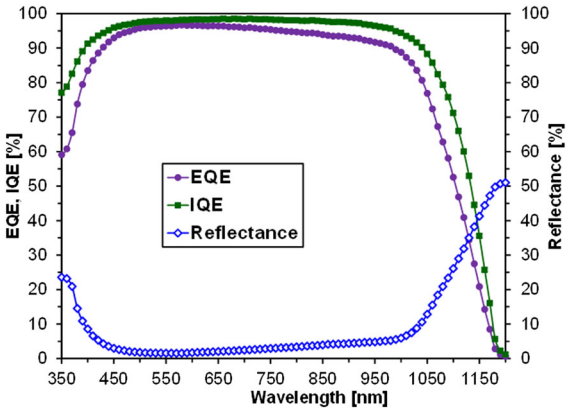

Figure 5. External quantum efficiency (EQE), internal quantum efficiency (IQE) and reflectance of large area *n*-type front junction cell with passivated rear contact and screen-printed front contacts.

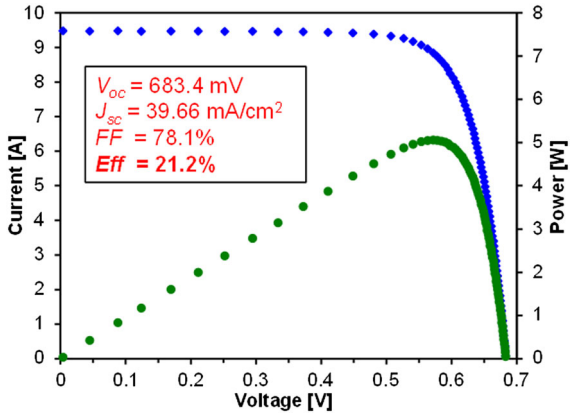

Figure 6. Light *I*–*V* curve of 21.2% efficient screen-printed *n*-type front junction cell featuring passivated rear contact with a tunnel oxide grown at room temperature (measured in-house using the Fraunhofer-certificated 20.2% efficient large area *n*-type cell [22] as a reference).

4. SUMMARY

In summary, a high quality rear contact passivated with chemically grown tunnel oxide at room temperature has been successfully integrated into screen-printed ion-implanted boron emitter on large area *n*-type Si wafers. For complete cell fabrication, tunnel oxide was capped with n^+ *poly*-Si formed by 875°C anneal of a PECVD deposited <20 nm *a*-Si layer. A J_{0b}' of 13.9 fA/cm^2 was achieved after the 875°C anneal and simulated contact firing process at 730°C, supporting excellent thermal stability and compatibility with the traditional low-cost screen-printing technology. The finished cells with tunnel oxide passivated rear contact showed excellent performance with V_{oc} of 683.4 mV after screen-printed metallization on a homogeneous ion-implanted boron emitter. This resulted in a J_{sc} of 39.7 mA/cm^2 and 21.2% efficiency, demonstrating the promise of this technology option for industrial production of high-efficiency Si solar cells.

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REFERENCES

1. Taguchi M, Yano A, Tohoda S, Matsuyama K, Nakamura Y, Nishiwaki T, Fujita K, Maruyama E. 24.7% record efficiency HIT solar cell on thin silicon wafer, in *Proceedings of the 39th IEEE Photovoltaic Specialist Conference*, Tampa, Florida, USA, 2013; pp. 96–99.
2. Masuko K, Shigematsu M, Hashiguchi T, Fujishima D, Kai M, Yoshimura N, Yamaguchi T, Ichihashi Y, Mishima T, Matsubara N, Yamanishi T, Takahama T, Taguchi M, Maruyama E, Okamoto S. Achievement of more than 25% conversion efficiency with crystalline silicon heterojunction solar cell. *IEEE Journal of Photovoltaics* 2014; **4**(6): 1433–1435.
3. Feldmann F, Bivour M, Reichel C, Hermle M, Glunz SW. Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent transport characteristics. *Solar Energy Materials and Solar Cells* 2014; **120**: 270–274.
4. Heng JB, Fu J, Kong B, Chae Y, Wang W, Xie Z, Reddy A, Lam K, Beitel C, Liao C, Erben C, Huang Z, Xu Z. >23% high-efficiency tunnel oxide junction bifacial solar cell with electroplated Cu gridlines. *IEEE Journal of Photovoltaics* 2015; **5**(1): 82–86.
5. Feldmann F, Bivour M, Reichel C, Steinkemper H, Hermle M, Glunz SW. Tunnel oxide passivated contacts as an alternative to partial rear contacts. *Solar Energy Materials and Solar Cells* 2014; **131**: 46–50.
6. Feldmann F, Simon M, Bivour M, Reichel C, Hermle M. Efficient carrier-selective p- and n-contacts for Si solar cells. *Solar Energy Materials and Solar Cells* 2014; **131**: 100–104.
7. Asuha HK, Maida O, Takahashi M, Iwasa H. Nitric acid oxidation of Si to form ultrathin silicon dioxide layers with a low leakage current density. *Journal of Applied Physics* 2003; **94**: 7328–7335.
8. Lee WC, Hu C. Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction-and valence-band electron and hole tunneling. *IEEE Transactions on Electron Devices* 2001; **48**(7): 1366–1373.
9. Wolstenholme GR, Jorgensen N, Ashburn P, Booker GR. An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations. *Journal of Applied Physics* 1987; **61**: 225–233.
10. Tao Y, Chang EL, Upadhyaya AD, Roundaville B, Ok YO, Madani K, Chen CW, Tate K, Upadhyaya V, Zimbardi F, Keane J, Payne A, Rohatgi A. "730 mV implied Voc enabled by tunnel oxide passivated contact with PECVD grown and crystallized n^+ polycrystalline Si", in Proceedings of the 42nd IEEE Photovoltaic Specialists Conference, New Orleans, Louisiana, USA, 2015.
11. Sinton RA, Cuevas A, Stuckings M. "Quasi-steady-state photoconductance, a new method for solar cell material and device characterisation", in Proceedings

of the 25th IEEE Photovoltaic Specialists Conference, Washington D.C., USA, 1996; p. 457.
12. Shewchun J, Singh R, Green MA. Theory of metal-insulator-semiconductor solar cells. *Journal of Applied Physics* 1977; **48**: 765.
13. Nemeth B, Young DL, Yuan H, Lasalvia V, Norman AG, Page M, Lee BG, Stradins P, "Low temperature Si/SiO_x/pc-Si passivated contacts to n-type Si solar cells", in Proceedings of the 40th IEEE Photovoltaic Specialist Conference, Denver, Colorado, USA, 2014; p. 3488–3452.
14. Kane DE, Swanson RM, "Measurement of the emitter saturation current by a contactless photoconductivity decay method (silicon solar cells)", in Proceedings of the 18th IEEE Photovoltaic Specialists Conference, Las Vegas, Nevada, USA, 1985; pp. 578–583.
15. Hermle M, Benick J, Rüdiger M, Bateman N, Glunz SW, "N-type silicon solar cells with implanted emitter", in Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, 2011; p. 875.
16. Ryu K, Upadhyaya A, Song H, Choi C, Rohatgi A, Ok Y. Chemical etching of boron-rich layer and its impact on high efficiency n-type silicon solar cells. *Applied Physics Letters* 2012; **101**: 073902.
17. Tao Y, Rohatgi A, "High-efficiency large area ion-implanted n-type front junction Si Solar cells with screen-printed contacts and SiO2 passivated boron emitters", in Proceedings of the 40th IEEE Photovoltaic Specialists Conference, Denver, Colorado, USA, 2014; pp. 3654–3658.
18. Böscke TS, Kania D, Schöllhorn C, Stichtenoth D, Helbig A, Sadler P, Braun M, Dupke M, Weiß M, Grohe A, Lossen J, Krokoszinski H-J. Fully ion implanted and coactivated industrial n-type cells with 20.5% efficiency. *IEEE Journal of Photovoltaics* 2014; **4**(1): 48–51.
19. Ok Y, Upadhyaya AD, Zimbardi F, Tao Y, Cooper IB, Rohatgi A, Carroll AF, Suess T. Effect of Al content on the performance of Ag/Al screen printed n-type Si solar cells", in Proceedings of the 39th IEEE Photovoltaic Specialists Conference, Tempa, Florida, USA 2013; pp. 2247–2249.
20. Yablonovitch E, Gmitter T, Swanson RM, Kwark YH. A 720 mV open circuit voltage SiO_x:c-Si:SiO_x double heterostructure solar cell. *Applied Physics Letters* 1985; **47**: 1211–1213.
21. Reusch M, Bivour M, Hermele M, Glunz SW. Fill factor limitation of silicon heterojunction solar cells by junction recombination. *Energy Procedia* 2013; **38**: 297–304.
22. Tao Y, Ok Y-W, Zimbardi F, Upadhyaya A, Lai J, Ning S, Upadhyaya V, Rohatgi A. Fully ion-implanted and screen-printed 20.2% efficient front junction silicon cells on 239 cm^2 N-type Cz substrate. *IEEE Journal of Photovoltaics* 2014; **4**(1): 58–63.
23. Trupke T, Bardos RA, Schubert MC, Warta W. Photoluminescence imaging of silicon wafers. *Applied Physics Letters* 2006; **89**(4): 044107.
24. Trupke T, Nyhus J, Haunschild J. Luminescence imaging for inline characterisation in silicon photovoltaics. *Physica Status Solidi (RRL)* 2011; **5**(4): 131–137.
25. Hoex B, Schmidt J, Bock R, Altermatt PP, van de Sanden MCM, Kessels WMM. Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al_2O_3. *Applied Physics Letters* 2007; **91**: 112107.
26. Renshaw J, Kang MH, Meemongkolkiat V, Rohatgi A, Carlson D, Bennett M, "3D-modeling of a back point contact solar cell structure with a selective emitter", in Proceedings of the 34th IEEE Photovoltaic Specialists Conference, Philadelphia, Pennsylvania, USA, 2009; pp. 375–379.
27. Mäckel H, Varner K. On the determination of the emitter saturation current density from lifetime measurements of silicon devices. *Progress in Photovoltaics: Research and Applications* 2013; **21**(5): 850–866.
28. Altermatt PP. Models for numerical device simulations of crystalline silicon solar cells—a review. *Journal of Computational Electronics* 2011; **10**(3): 314–330.
29. Edler A, Mihailetchi VD, Koduvelikulathu LJ, Comparotto C, Kopecek R, Harney R. Metallization-induced recombination losses of bifacial silicon solar cells. *Progress in Photovoltaics: Research and Applications* 2015; **23**: 620–627.
30. Kiefer F, Peibst R, Ohrdes T, Krügener J, Osten HJ, Brendel R, "Emitter recombination current densities of boron emitters with silver/aluminum pastes", in Proceedings of the 40th IEEE Photovoltaic Specialists Conference, Denver, Colorado, USA, 2014; pp. 2808–2812.
31. Tao Y, Payne A, Upadhyaya VD, Rohatgi A. 20.7% efficient ion-implanted large area n-type front junction silicon solar cells with rear point contacts formed by laser opening and physical vapor deposition. *Progress in Photovoltaics: Research and Applications* 2014; **22**(10): 1030–1039.
32. Meier DL, Good EA, Garcia RA, Bingham BL, Yamanaka S, Chandrasekaran V, Bucher C, "Determining components of series resistance from measurements on a finished cell", in Proceedings of the 4th IEEE World Conference, Waikoloa, Hawaii, USA, Vol. **2**, 2006; pp. 1315–1318.
33. Bivour M, Reichel C, Hermle M, Glunz SW. Improving the a-Si:H(p) rear emitter contact of n-type silicon solar cells. *Solar Energy Materials and Solar Cells* 2012; **106**: 11–16.