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TOPCon – Technology options for cost efficient industrial manufacturing

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ABSTRACT

Formation of an interfacial tunnel oxide capped by the polysilicon (poly-Si) layer is one of the most promising methods to realize carrier-selective contacts as it offers an evolutionary upgrade to the current mainstream PERC. Currently, PV industry is looking towards different technologically feasible options of transferring this cell concept from laboratory research towards industrial manufacturing. In this paper, we devise cost-driven strategies towards industrial manufacturing of TOPCon-based solar cells after assessing various process routes based on currently production-ready and upcoming future alternative process technologies. Our techno-economic assessment suggests that higher capital and operational costs required for TOPCon concept is distributed unevenly in the process value chain, with a significant fraction in diffusion/annealing and metallization steps. Nevertheless, under given assumptions, TOPCon-concepts are found to remain economically competitive against bifacial PERC in terms of levelized cost of electricity (LCOE), if a minimum absolute gain in cell efficiency $\Delta\eta >$ 0.55% for most-conservative and $\Delta\eta >$ 0.40% for most-progressive scenarios respectively can be maintained.

1. Introduction

Tunnel oxide passivated contacts (TOPCon) solar cells [1] are widely seen as the forthcoming technology to the current state-of-the-art passivated emitter and rear cell (PERC)-concept. The cell architecture is based on the concept of 'passivating and carrier selective contacts', where the recombination of minority charge carriers is suppressed by a stack of thin tunnel oxide and heavily-doped polysilicon (poly-Si) layers. The efficiency potential of this concept is already proven in laboratory scale solar cells by reaching open circuit voltages (V_{OC}) of up to 725 mV and conversion efficiencies over 26% [2,3]. Moreover, initial industrial adoption of this technology by PV manufacturers also shows promising results [4–7].

The envisioned industrial TOPCon process routes consist of the process steps that are either fully/partly transferable from the state-of-the-art PERC cell, with inclusion of few extra process steps that are necessary to increase the conversion efficiency. The technological maturity and the proven industrial readiness of process technologies used in PERC is widely believed to provide an easy transition of PV industry towards the higher efficiency cell concepts such as TOPCon. Another potential advantage of carrying this evolutionary approach is the possibility of upgrading the existing PERC production lines for TOPCon processing with addition of minimum number of process steps, provided that the required area is available in the PERC facility.

Formation of tunnel oxide and deposition of intrinsic/doped poly-Si are the two crucial processing steps that are additional to the current PERC processing, and mainly define the process routes for TOPCon processing. The properties of these layers are vital towards designing the subsequent cell processing steps, aiming to achieve high open-circuit voltage (V_{OC}) and a low series resistance promised by the TOPCon-concept. Apart from these steps, industrial TOPCon cells are mainly based on more expensive *n*-type substrates, and require integration of the boron emitter diffusion process with less industrial maturity in comparison to the phosphorous diffusion process typically used in *p*-PERC cells.

Low pressure chemical vapour deposition (LPCVD) of a-Si layers after an in-situ grown thermal tunnel oxide is the current production-ready technology for industrial processing of TOPCon cells. Meanwhile, the TOPCon process routes that are based on alternative a-Si deposition technologies are currently being investigated in research facilities, and are expected to be ready for mainstream production in the near future. In fact, various process routes and a wide range of technology options for the TOPCon concept are currently in consideration by the PV industry both in terms of their technological and economic viability. However, for the mass production of each of these TOPCon-concepts, the economic competitiveness against the current

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mainstream PERC cell is still an open question. Current PERC-concept is reported to reach up to 23% average conversion efficiencies in mass production with a fairly mature process sequence [8]. These continuous improvements in the price-performance ratio up-to-now enable PERC to be the preferred option for utility-scale installations. Therefore, the additional capital and operating costs required to establish and operate a TOPCon manufacturing facility needs to be offset by an increment in conversion efficiency in the cell/module/system level, in order to further lower the levelized cost of electricity (LCOE) in large scale PV installations. An in-depth look at the cost-effective manufacturing options for TOPCon is highly relevant for the PV industry, which is currently looking at different options of transferring the TOPCon concept from laboratory research to production lines as the potential next evolutionary solar cell technology upgrade to PERC.

In this work, we aim to devise cost-driven strategies towards mass manufacturing of TOPCon-based solar cells using bottom-up total cost of ownership (TCO) calculations of individual process steps in the PV value chain and the associated cell processing routes. Based on the available literature, feedback from industry, and technological developments at Fraunhofer ISE, we first discuss the up-to-now industrialized LPCVD based process routes for the TOPCon concept. We then outline and discuss status of various alternative technologies. Based on the results of the production readiness, we perform cost of ownership (COO) calculations of different amorphous silicon (a-Si) deposition technologies, with the intent of identifying and outlining technologically feasible process routes for the industrial TOPCon solar cell architecture, and analyze their competitiveness to the mainstream bifacial PERC cell in terms of cell/module/system costs, and levelized cost of electricity (LCOE) for a utility-scale green field installation. Finally, sensitivity analysis is performed for the selected TOPCon routes in order to identify the minimum required increment in conversion efficiency to PERC in order to reach economic competitiveness. Based on our findings, current and future technology options for the mass production of TOPCon solar cells will be discussed.

2. Approach

We focus on TOPCon architecture featuring screen-printed contacts on both-sides of *n*-type Si substrate as they promise the highest potential gain in conversion efficiency over the bifacial *p*-PERC-concept, with the best prospects for mass production. The investigated cell architecture is shown in Fig. 1.

The TOPCon solar cell is based on an *n*-type *c*-Si substrate with boron (p^+) emitter on the textured (front) side. The front side is passivated by a dielectric stack of passivation and anti-reflection layer. The rear side with either textured/semi-polished or polished surface features tunnel oxide and doped polysilicon layer acting as passivating carrier-selective contact, stacked with amorphous hydrogenated silicon nitride (a-SiN_x) layer as the source of hydrogenation to passivate the dangling bonds in Si–SiO_2 interface [9,10]. Metallization is performed by screen-printing of Ag or Ag–Al grid on front and Ag-grid on rear considering bifacial application. The reference PERC cell is a *p*-type bifacial solar cell, featuring phosphorus (n^{++})-emitter, front and rear passivation layers and both-sided screen-printed contacts. Detailed process routes for the investigated cell types are outlined in respective sections of the paper.

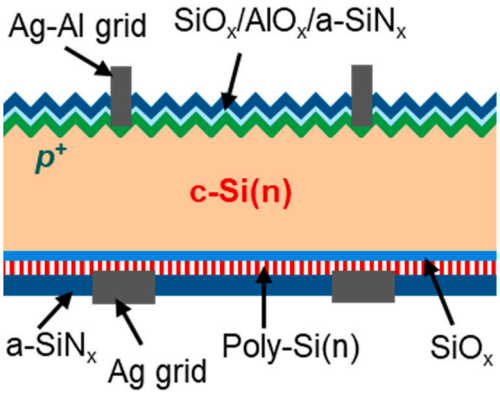

Fig. 1. Schematic showing the TOPCon cell architecture investigated in the present work.

The bottom up total cost of ownership (TCO) calculations are performed along the PV value chain by using the internally developed 'SCost' model at Fraunhofer ISE [11,12]. The model calculates the cost of ownership (COO) for individual manufacturing process steps at each stage of the PV value chain in accordance with the SEMI standards E35 [13] and E10 [14], and builds a process route considering equipment interdependencies, production overhead costs and cost of capital at the factory level to estimate the TCO for the desired solar cell architecture. Different industrially feasible a-Si deposition technologies are identified and compared based upon equipment and process parameters, which are based on data provided by industrial equipment manufacturers as well as our own process parameters for industrial equipments within Fraunhofer ISE's PV-TEC pilot line. For each deposition technology, process routes that show the most promise towards mass production are identified based upon the technological and economic feasibility of the entailed process steps. The following are the primary selection criteria set for the best manufacturing scenario: a) availability of an industrial tool, b) process compatibility, c) availability of all process parameters required for the COO modeling, d) lean process flow, and e) successful demonstration of the process functionality. A LCOE sensitivity analysis is performed to identify the minimum gain in conversion efficiency needed for TOPCon concepts in order to remain competitive against the bifacial *p*-PERC benchmark at LCOE level.

3. LPCVD based TOPCon routes

To date, industrial screen-printed TOPCon solar cells on *n*-type substrates are based on LPCVD a-Si/poly-Si deposition technology. Typically, silicon layers that are predominantly amorphous in nature are first deposited and then subjected to a high temperature annealing step in order to form polycrystalline silicon (poly-Si) layer with mixed fractions of amorphous and crystalline phases.

3.1. LPCVD for a-Si deposition

LPCVD is used as one of the important processes established in the semiconductor facilities to deposit highly conformal layers of a-Si/poly-Si layers at low-pressure conditions [15]. The main advantages of this technology are: a) good thickness distribution along the wafer and the boat, b) pin-hole free layers with good step coverage, c) maintaining the impurity profile previously formed in the wafer due to the use of relatively low deposition temperatures close to 600 °C, d) large number of wafers per batch, and e) option of in-situ doping with constant doping profile [16].

For the TOPCon concept investigated in this work, a phosphorus-doped a-Si/poly-Si layer (a-Si(n)/poly-Si(n)) is required to be deposited on the rear side of the solar cell. Here, silane (SiH_4) is used as a precursor for silicon deposition, optionally using diluted PH_3 (in N_2) to incorporate dopants in the layer. The layer properties are influenced by the deposition pressure, the silane concentration, the dopant content, and most significantly by the deposition temperature. For the identical process conditions, inclusion of doping gas significantly influences the film growth, i.e. the silicon deposition rate. For instance, depending upon the process conditions, inclusion of PH_3 flux is reported to lower the deposition rate by several times [17] that is further exacerbated by an increase in PH_3 flux [16]. This leads to two approaches of LPCVD a-Si deposition – a) deposition of intrinsic a-Si/poly-Si layers, followed by an ex-situ $POCl_3$ tube diffusion process to form poly-Si(n) layers, b) deposition of in-situ doped a-Si(n)/poly-Si(n) layers and subsequent thermal

annealing in N_2. In Fig. 2, we calculate the COO of intrinsic and phosphorus-doped layers for the same thickness of 150 nm, considering about 36% lower deposition rate for in-situ doped grown layers in comparison to intrinsic layers. LPCVD depositions are performed here in a front-front configuration, i.e. placing two wafers facing front sides in a single slot.

It can be observed that the COO of LPCVD step increases by almost $15\%_{abs.}$ if in-situ phosphorus- doped layers are deposited instead of intrinsic a-Si layers. Here, one of the major cost driving factors is the reduced throughput of the LPCVD tool due to a significantly longer process duration, which directly increases all the fixed costs. A small cost contribution of additional PH_3 flux for phosphorus doped layer is found to be less significant as the corresponding SiH_4 flux is about 20 times higher and is mainly responsible for the process consumables costs.

3.2. Industrially viable LPCVD TOPCon routes

Fig. 3 schematically shows the TOPCon process routes based upon LPCVD a-Si technology, and the reference process route for bifacial *p*-PERC. For *p*-type PERC cell (*Bifacial p-PERC*), alkaline textured wafers receive a phosphorus emitter by a $POCl_3$-based low pressure tube diffusion furnace. Afterwards, highly phosphorous-doped regions are selectively formed on the front side by using a laser source, aiming to drive phosphorous atoms from the phosphorsilicate glass (PSG) layer into the silicon substrate. Such a selective-emitter approach is intended mainly to lower the recombination of minority charge carriers beneath the metal contacts. This is followed by the rear-emitter removal or chemical edge isolation (CEI) process, PSG etching and ozone-based cleaning [18] in the same wet-chemical inline tool. Ozone cleaning oxidizes the silicon surface, the oxide then being removed with a final HF-dip before the surface passivation steps. Advanced passivation of front and rear side is envisioned by growing thin thermal silicon oxide of about 2 nm before passivation of rear (PECVD AlO_x/a-SiN_x stack) and front (PECVD a-SiN_x), which is deemed here a necessary step to reach a high average conversion efficiency of 23.0% in bifacial *p*-PERC production. After passivation process, screen-printing of rear is performed by first printing Ag contact pads before printing Al grid, followed by the printing of Ag grid on the front. After fast-firing (FFO), a regeneration process is required to compensate the losses in conversion efficiency due to light induced degradation (LID), which is related to the formation of boron-oxygen complexes [19].

The two TOPCon routes differ mainly by the method used to form doped a-Si/poly-Si layers. After the texturing process, boron doping is performed for TOPCon cells using BBr_3 precursor in a tube diffusion furnace to form boron (p^+) emitter. This is followed by an inline wet-chemical process to single-sided removal of rear-side emitter, whereas keeping the BSG layer in front-side intact; before performing ozone-based cleaning sequence. The BSG is kept intact on the front side in order to protect the boron emitter from being etched during the single-sided etching (SSE) of poly-Si. Afterwards, tunnel oxide is formed in-situ by oxidizing *c*-Si surface inside LPCVD furnace, which is followed by deposition of either intrinsic (*LPCVD TOPCon exsitu*) or phosphorus (n^+-) doped a-Si/poly-Si layer (*LPCVD TOPCon insitu*) in a front-front process (two wafers per slot facing front sides). The a-Si/poly-Si deposition by LPCVD is inherently both-sided, therefore leading to the parasitic deposition of layers on the undesired (front) side, even if the wafers are placed in front-front configuration (two wafers placed per slot). For the *LPCVD TOPCon exsitu* process route, an additional $POCl_3$ diffusion is required to incorporate dopants into a-Si/poly-Si layer, which simultaneously acts as a thermal annealing step required to cause phase change of predominantly amorphous layer to a polycrystalline layer, so called polycrystalline-silicon (poly-Si). The ex-situ doping of the poly-Si layer is also possible to achieve using an ion implantation process [6], however, we focus on poly-Si doping using the tube furnace as it is more widely established in research and industry leading to a more accessible process parameter dataset availability.

The $POCl_3$ diffusion process is optimized to dope the polysilicon layer with a constant doping concentration. During the ex-situ doping of poly-Si, the interfacial tunnel oxide acts like a barrier layer and helps in uniform distribution of dopants within the entire thickness of the poly-Si layer [20]. Consequently, there is a strong reduction in phosphorus doping concentration at SiO_x-Si interface, although some dopants typically also diffuse through the tunnel oxide into the silicon base to form a so called 'diffusion-tail'. The thermal tunnel oxide formed inside LPCVD furnace is reported to be stable enough to withstand the typical temperatures (850–900 °C) used in the $POCl_3$ diffusion process [21]. The doping level of poly-Si layer is not only crucial for carrier selectivity, but also to maintain a high lateral conductivity in poly-Si layer, which facilitates easier current transport to metal contacts. However, an excess doping into *c*-Si substrate should be avoided to limit the Auger recombination of charge carriers. The front-side poly-Si layer needs to be removed using a single sided etching (SSE poly) process, before proceeding further with the passivation of the boron emitter. For *LPCVD*

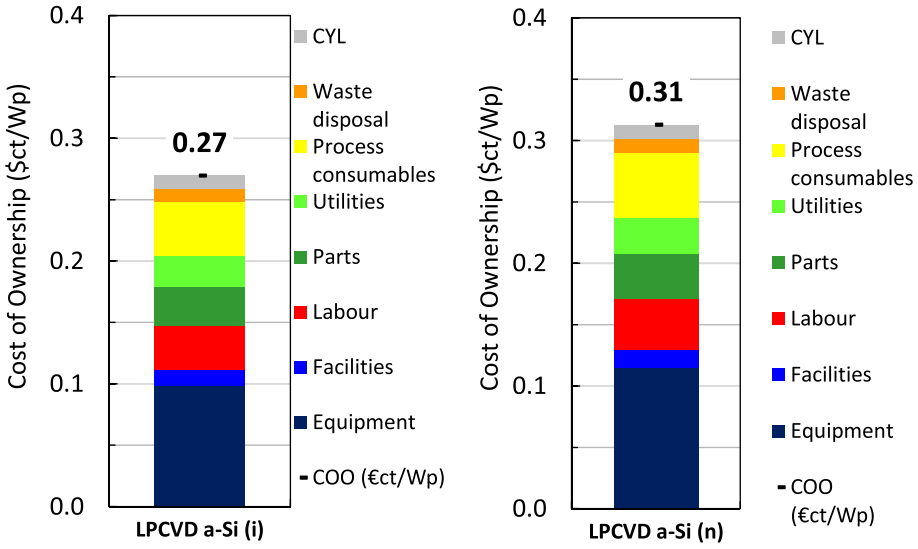

Fig. 2. Cost of ownership (COO) of 150 nm LPCVD deposited intrinsic (left) and phosphorus-doped a-Si/poly-Si (right) layers. Cell conversion efficiency of 23.5% on M4 size wafers is assumed here in both cases to calculate $ct/Wp costs. Here, CYL refers to the cost of yield loss.

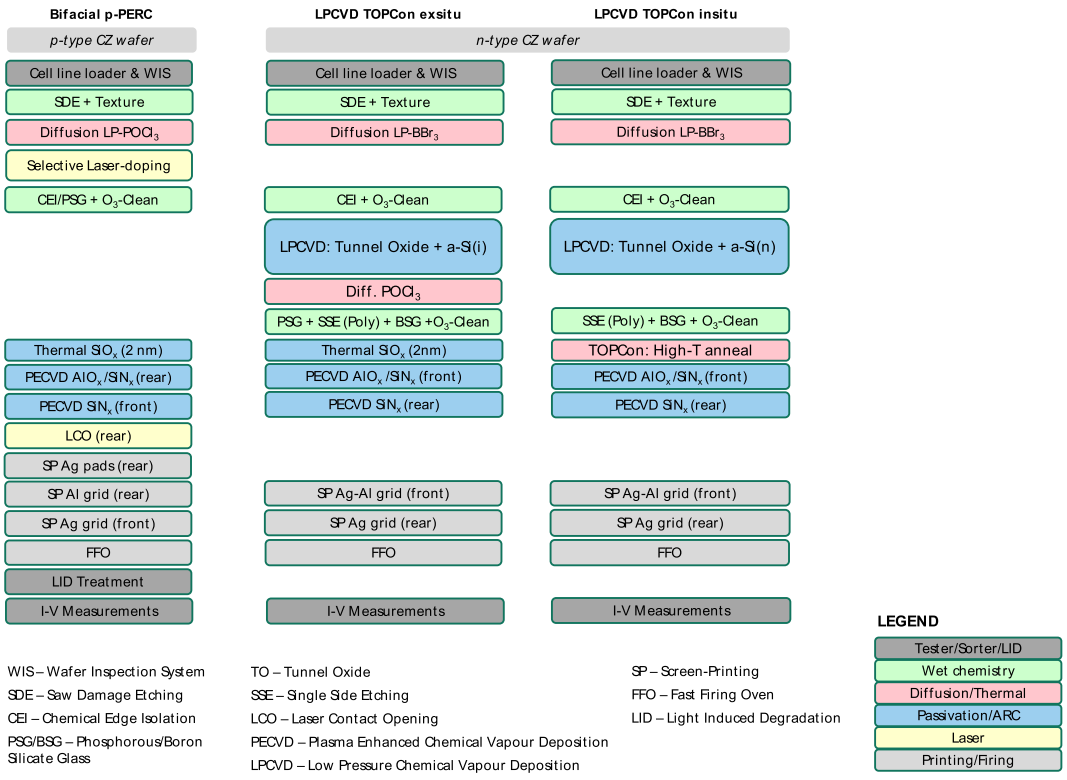

Fig. 3. Process routes for bifacial *p*-PERC and both side contacted *n*-TOPCon-concepts based upon LPCVD a-Si/poly-Si layer.

TOPCon exsitu, this is assumed to be performed wet-chemically in an inline wet-etching tool after $POCl_3$-diffusion, which after removing the PSG layer subsequently performs single-sided etching of polysilicon (SSE), followed by BSG removal and finally ozone-based wet-chemical cleaning step. The SSE process is assumed to be performed in a diluted alkaline solution [22], where the intact BSG layer on the textured side prevents etching of p^+ emitter by acting as a barrier layer. Afterwards, boron emitter passivation is performed by first growing a thin low-temperature thermal oxide of 1–2 nm in a tube furnace before deposition of PECVD AlO_x/a-SiN_x layer stack on the front side. Afterwards, PECVD a-SiN_x:H is also deposited on top of poly-Si layer in the rear side as a hydrogenation source. For *LPCVD TOPCon insitu*, the deposition of phosphorus doped LPCVD layers is followed in an inline wet-chemical tool to perform SSE of a-Si layer on the front-side, with a subsequent BSG etching and ozone-based wet-chemical cleaning. Afterwards, a high temperature annealing process is required to form poly-Si layers at the rear. Looking into reducing the COO of *LPCVD TOPCon insitu* process route burdened by a costlier LPCVD deposition, we assume technological feasibility of optimizing the high temperature annealing step to form a high quality thin SiO_x oxide on the boron emitter at the front side. This avoids the use of an extra thermal oxidation step, which is otherwise required to realize high quality passivation of the boron emitter before deposition of PECVD AlO_x/-a-SiN_x stack. It should be mentioned that the high temperature steps performed after a-Si/poly-Si deposition ($POCl_3$ diffusion for *LPCVD TOPCon exsitu*, and annealing for *LPCVD TOPCon insitu*) should be carefully developed not to substantially alter the boron emitter profile on the textured-side of the solar cell. Afterwards, front and rear metallization is performed by using screen-printing Ag-Al and Ag grids respectively on front and rear sides, followed by the fast-firing process and I–V measurements.

Before comparing the TCO results of PERC and TOPCon cells, it is intuitive to closely look at the major difference in process steps for the two investigated TOPCon process routes from cost perspective. In Fig. 4, COO of individual process steps that are not common for both TOPCon routes are plotted, together with the cumulative sum of all those steps. Here, the *LPCVD TOPCon exsitu* route features four process steps: LPCVD a/poly-Si(i) deposition, LP $POCl_3$, inline wet-chemical process (PSG etch, SSE, BSG etch and O_3 cleaning), and low temperature thermal oxidation (SiO_x B-emitter). *LPCVD TOPCon insitu* features three process steps that are unique to this route in comparison to the other TOPCon route: LPCVD a-Si(n) deposition, inline wet-chemical process for SSE,

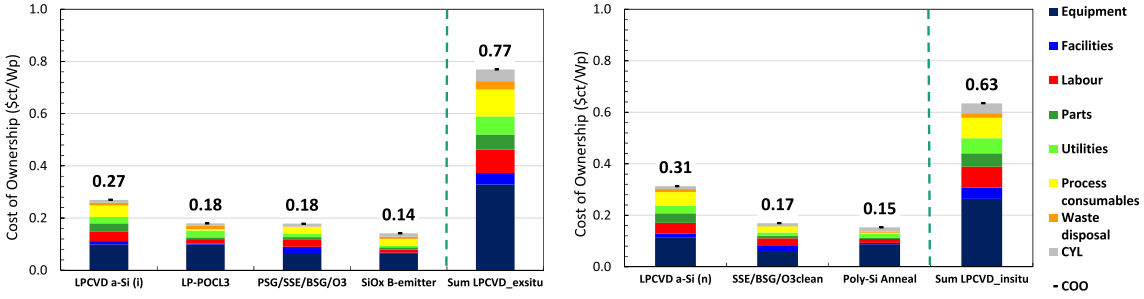

Fig. 4. COO ($ct/Wp) of individual process steps that are unique for TOPCon concepts - *LPCVD TOPCon exsitu* (left) and *LPCVD TOPCon insitu* (right). Cell conversion efficiency of 23.5% on M4 size wafers is assumed here for TOPCon concepts to calculate $ct/Wp costs. Here, CYL refers to cost of yield losses.

BSG etch and O_3 cleaning, and high temperature annealing process (Poly-Si Anneal). It is noticeable that although the COO of 150 nm LPCVD a/poly-Si(n) is almost 15%$_{abs.}$ higher than 150 nm LPCVD a/poly-Si(i), the process route for doped a/poly-Si layer can be adapted to allow almost 18%$_{abs.}$ lower cumulative COO for the combined TOPCon steps. Here, *LPCVD TOPCon insitu* benefits from the absence of the $POCl_3$ diffusion step. Additionally, under given assumption of combining both annealing and oxidation processes within a single processing step, *LPCVD TOPCon insitu* also features less number of process steps in comparison to *LPCVD TOPCon exsitu*.

3.3. Comparison of total cost of ownership (TCO) to PERC

In Fig. 5, the total cost of ownership of PERC and TOPCon processes is distributed into wet-chemical, diffusion and annealing, passivation, and metallization process categories. Wet-chemical processes include alkaline texturing, CEI, glass removal (PSG/BSG), O_3 cleaning, and SSE of polysilicon layer. It is observed that there is an increase in total COO of the wet-chemical processes for TOPCon routes, mainly due to the requirement of additional glass etching, SSE(poly) and cleaning process step. Diffusion and annealing processes include $POCl_3$ and BBr_3 doping, selective laser-doping, and high temperature annealing step for a-Si layer. COO for TOPCon routes are here significantly higher for diffusion/anneal processes due to: a) a longer process duration of BBr_3 diffusion in comparison to $POCl_3$-based process leading to a significantly reduced throughput, and b) requirement of either an additional $POCl_3$-doping process or a high temperature annealing step for a-Si layers. Passivation processes include thermal oxidation, LPCVD polysilicon depositions, and PECVD depositions of PECVD AlO_x/a-SiN_x stack, and a-SiN_x:H layer. For TOPCon routes, requirement of an additional LPCVD deposition step to PERC is typically expected to increase the costs for passivation process, as seen for *LPCVD TOPCon exsitu*. However, for *LPCVD TOPCon insitu*, process costs are lowered by combining high temperature annealing with oxidation in a single process step. Metallization costs include screen-printing of pads (Ag) and grids (Al and Ag/Ag-Al), and the fast-firing process. For bifacial *p*-PERC cell, the laser contact opening and regeneration process steps are also included in the 'Metallization' category. A significantly higher metallization cost is required for TOPCon cells, mainly due to the requirement of printing Ag-based grids on both sides to form contacts with low contact resistivity. In fact, a huge share of process consumables costs in COO of a TOPCon cell is predominantly related to a high Ag consumption during metallization. Thus, in order to further lower COO of a TOPCon cell, significant reduction in Ag consumption is required.

Moreover, the recent volatility in Ag prices and an increasingly growing share of industrial Ag use by the PV industry is expected to drive efforts towards lowering the Ag consumption in solar cells. Fig. 6 compares COO of the metallization step for bifacial *p*-PERC and TOPCon cells for various scenario of Ag reduction. The most optimistic scenario of reducing Ag consumption of the cell by 50% of its current value is

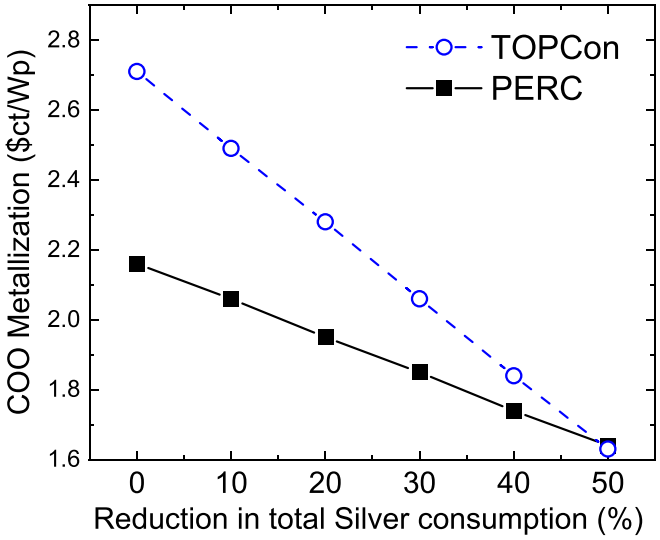

Fig. 6. Cost of ownership ($ct/Wp) of the metallization step projected for percentage reduction in total Ag consumption during industrial screen printing of front and rear grids (including busbar and fingers) for bifacial *p*-PERC and LPCVD TOPCon process routes. For *p*-PERC cells, it is assumed that total Ag consumption is dominated by the front-side (Ag fraction utilized for rear-tabbing kept constant), and aluminum consumption for the rear-side is kept unchanged for all scenarios. For *p*-PERC cells, laser contact opening (LCO) and regeneration processes are grouped under metallization category together with screen-printing and firing processes.

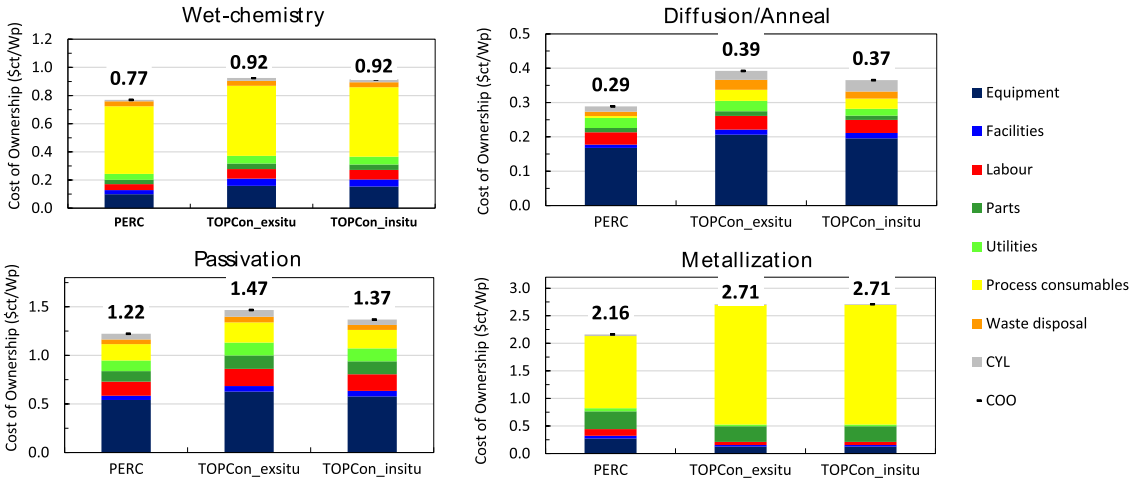

Fig. 5. Cost of ownership ($ct/Wp) comparison of bifacial *p*-PERC vs LPCVD TOPCon process routes with costs of individual process steps categorized under as wet-chemistry, diffusion & annealing (Diffusion/Anneal), passivation and metallization. For bifacial *p*-PERC solar cell, selective laser-doping is grouped under Diffusion/Anneal together with $POCl_3$ diffusion process, whereas laser contact opening (LCO) and regeneration processes are grouped under metallization category together with screen-printing and firing processes. In the legend, CYL represent cost of yield losses. Here, cell efficiencies of 23.0% and 23.5% on M4 wafer sizes are assumed for bifacial *p*-PERC and TOPCon cells respectively.

based upon the estimates of International Roadmap for Photovoltaics (ITRPV) [42]. Here, we assume that the Aluminum consumption for rear-side grid formation and the amount of Ag required for rear tabbing of PERC cells remain unchanged. COO of the metallization step dips dramatically for both cell types with lowering consumable costs related to Ag. Nevertheless, the slope is much higher for the TOPCon cells due to their usage of Ag on both front and rear contacts. It is interesting to note that if the metallization concepts in future allow 50% reduction in Ag usage, metallization costs of TOPCon cells are on-par with PERC cells, with former potentially even achieving lower watt-peak costs ($/Wp) due to a higher cell power.

In summary, the TCO in cell level is significantly higher for TOPCon concept in comparison to *p*-PERC cell. Nevertheless, *LPCVD TOPCon insitu* route offers lower COO between the two investigated LPCVD-based TOPCon routes.

4. Alternative TOPCon process routes

As mentioned earlier, deposition of a-Si layer is one of the most important process steps required to realize a TOPCon solar cell. Although LPCVD is currently the only industrialized process for a-Si deposition, there are several alternative technologies that are currently being tested and are in different stages of development. Besides, the tunnel oxide formation is also possible to realize using alternative oxidation methods, other than thermal oxidation that is used for LPCVD-based TOPCon process routes. In this section, different methods to form tunnel oxide and deposit a-Si layer are briefly summarized, as these steps are vital towards designing the subsequent cell processing steps.

4.1. Tunnel oxide formation

A thin interfacial oxide layer is grown on *c*-Si surface before depositing either intrinsic or doped amorphous silicon layers. The oxide layer not only provides an excellent passivation of *c*-Si surface, but also allows the transport of majority charge carriers from *c*-Si towards the metal contacts through the doped poly-Si layer. The stoichiometry and the thickness of the oxide layer mainly determine the thermal stability of the layer, which is a crucial aspect considering the current PV manufacturing process route that features several high temperature steps [23,24]. Table 1 outlines the available processes in literature and important characteristics to consider while choosing the method. The oxides are formed either by wet-chemical or dry methods. Among wet-chemical methods, DI-O_3 oxide is shown to have very good thermal stability [23]. Among dry methods, in-situ thermal oxide followed by the LPCVD a-Si deposition is the current mainstream process to form TOPCon layers in industry [25]. An appealing candidate is O_3-based oxidation induced by dissociation of O_2 by UV light sources [23]. This highly cost-effective method is able to form thermally stable stoichiometric SiO_x layers [23] for high-efficiency TOPCon cells, and potentially can be easily mounted at the end of the wet-chemical cleaning tool to ensure a lean process flow. Plasma-based oxidation is also a promising approach to form in-situ and thermally stable SiO_x layer using a PECVD tool [26–28], which can also be simultaneously used to deposit a-Si layers. In summary, although most of the above discussed oxidation methods are principally applicable in PV manufacturing, their choice largely depends upon the used a-Si/poly-Si deposition technology.

Table 1
Overview of oxidation technologies to form tunnel oxide layer. The symbols used are qualitative representation of: '✓'for favourable/possible with different degree, '×' for not favourable/not-possible.

Characteristics/ Technology	**Thermal** [10,24,29]	**UV-O_3** [21, 23]	**Plasma** [26,28, 30]	**HNO_3** [23,24, 31]	**DI-O_3** [23]
Dry or wet processing	Dry	Dry	Dry	Wet	Wet
In-situ growth with polysilicon deposition	✓	×	✓	×	×
Thermal stability	✓✓✓	✓✓✓	✓✓✓	✓	✓✓

4.2. Deposition of a-Si layer

Typically, a-Si layers are first deposited and then subjected to a high temperature annealing step in order to form poly-Si layer. Depending upon the deposition technology, the doping of poly-Si is performed either during the deposition process (in-situ) or by a follow up diffusion process (ex-situ). Importantly, the choice of a-Si deposition technology dictates almost all the other important cell processing steps. Table 2 lists the a-Si deposition technologies, which fully or partially fulfil the requirements to be considered for high volume PV manufacturing. Some of the most promising technologies that are closer to production-readiness, apart from LPCVD, are briefly discussed here. Plasma enhanced chemical vapour deposition (PECVD) is a well-proven technology in PV industry to deposit dielectric passivation layers, and one of the most promising candidates for a-Si deposition. In fact, ITRPV predicts a fast adoption of this a-Si deposition technology in expense of LPCVD in the near-future [42]. PECVD deposition of a-Si layers offers higher deposition rates in comparison to LPCVD technology, thereby promising cost-effectiveness. Another advantage of using PECVD is a possibility of in-situ doping of a-Si layers without any compromise to layer homogeneity and deposition rates. One of the key challenges is to avoid blistering in thick layers ($d > 100$ nm), which are currently required for industrial TOPCon architecture due to an inherently high hydrogen concentration in the deposited a-Si layer. Although PECVD is loosely considered as a single sided deposition process, avoiding wrap-around of a-Si layers remains a technological milestone for equipment manufacturers. Industrial tools allowing depositions in either batches [10,31,43] or inline mode [30,34] are available, and cell integration results are also published in literature [10,30]. In this paper, we assume batch-type PECVD tool for a-Si(n) deposition in all our calculations. PECVD-deposited a-Si layers require an additional high temperature annealing step to crystallize into poly-Si layers.

Atmospheric pressure chemical vapour deposition (APCVD) is another potential technology to deposit intrinsic and doped a-Si layers in inline mode with high deposition rates [15,36,44]. The process utilizes thermal dissociation of silane (SiH_4) that is inserted in a heated chamber using injector heads. Since the chemical reactions occur directly at the heated substrate, APCVD is also expected to provide good single-sidedness. Furthermore, in-situ doping is reportedly easily achieved by directly inserting doping precursors in the SiH_4 flow, and cell integration results are also reported [35]. In Fig. 7, normalized COO of the discussed deposition technologies is plotted against varying thickness of the a-Si layer.

It can be observed that COO of the deposition process scales significantly with the thickness of the a-Si layer. For LPCVD technology, process costs for the a-Si(n) reduce more with the deposition thickness as compared to the a-Si(i) layer. The cost advantage for thinner layers is, however, significantly higher for PECVD and APCVD deposited layers. For instance, the calculations show that COO reduction of almost 50% for PECVD and 65% for APCVD is achievable by lowering the a-Si layer thickness from 200 nm to 50 nm. The reduction of COO for PECVD a-Si is mainly due to a significant increase in throughput for lower thicknesses, which consequently leads to a significant reduction of process consumable costs. For APCVD, lower COO for thinner layers are mainly due to lower process consumables' costs as these costs occupy significant fraction of total COO. Although current screen-printing technology still requires thicker (150–200 nm) poly-Si layers to avoid shunting losses, advances in paste developments and better understanding of contact formation are expected to drive further reduction of poly-Si thickness in future.

Table 2
Overview of available a-Si/poly-Si deposition technologies and qualitative comparison based upon available literature (adapted from Ref. [32]). The symbols used represent: '✓'for favourable/possible with different degree, '×' for not favourable/not-possible, and '–' for work in progress/not yet demonstrated.

Characteristics/Technology	**LPCVD** [3–6,29,33]	**PECVD** [1,2,10,30,31,34]	**APCVD** [35,36]	**PVD** [37–40]	**Evaporation** [41]
Single-sided deposition	×	✓	✓	✓✓	✓✓
In-situ doping	✓	✓✓	✓✓	✓	–
Availability of industrial tool	✓✓✓	✓✓	✓✓	✓✓	–
Process demonstrated in lab-size cells	✓✓✓	✓✓✓	✓	✓✓	–
Application in large area industrial cell	✓✓✓	✓✓	–	–	–
Deposition mode (Batch/Inline)	Batch	Both	Inline	Inline	Batch

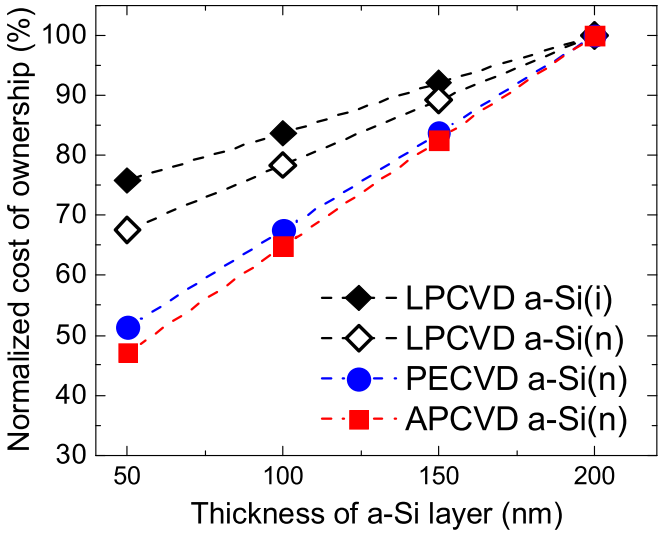

Fig. 7. Normalized COO calculated for various a-Si/poly-Si deposition technologies vs the thickness of the deposited layer. Here, two wafers per slot are assumed for LPCVD depositions. PECVD layer deposition is assumed for a batch type tool.

4.3. Process routes for PECVD and APCVD-based TOPCon

In Fig. 8, the relevant industrial process routes for TOPCon cells on *n*-type *c*-Si substrate, when using either PECVD or APCVD a-Si deposition technologies, are schematically shown alongside the reference bifacial *p*-PERC route. Two process routes are envisioned for each PECVD and APCVD based a-Si deposition technologies, mainly based upon the perspective of single-sidedness of the deposition process. The process routes *PECVD TOPCon high & APCVD TOPCon high* represent the current knowledge where the wrap-around of a-Si(n) layer on front-side needs to be removed by using a single-sided etching (SSE) process. For *PECVD TOPCon low & APCVD TOPCon low*, both a-Si deposition technologies are assumed to offer an excellent single-sidedness so that no SSE process is required after the high temperature annealing of the a-Si layer. In all four cases, the tunnel oxide is formed by coupling an UV excimer lamp array (UV-TO) [23] with the wet-chemical tool used for chemical edge isolation (CEI), BSG etching and ozone cleaning steps.

For all TOPCon routes, alkaline texturing is followed by boron diffusion step to form p^+ emitter. For *PECVD TOPCon high & APCVD TOPCon high*, BSG is kept intact during the wet-chemical step for rear-emitter removal in order to protect boron emitter against chemicals used in SSE process. After performing ozone cleaning in the same wet-chemical tool used for CEI/BSG processes, UV-TO is grown. Afterwards, a 150 nm thick in-situ phosphorous doped a-Si layer is deposited on the rear-side either by using PECVD (batch-type) or APCVD technology, with undesired wrap-around of a-Si layer on the front-side. The SSE process is performed to remove the wrap-around of a-Si, followed by BSG etching and subsequent ozone cleaning in the same wet-chemical tool. Here, it is assumed that the high temperature annealing process can be optimized in such a way that a thin thermal oxide grows on top of boron emitter, and that an excellent passivation of the textured (front) side can be achieved after PECVD AlO_x/a-SiN_x layer deposition.

For *PECVD TOPCon low & APCVD TOPCon low*, CEI is followed by BSG etching as no SSE process is envisioned later for both of these process routes. After ozone cleaning and UV-TO growth, PECVD/APCVD a-Si(n) layers are deposited with excellent single-sidedness. Here, we assume the best-case scenario of no additional cleaning required between PECVD/APCVD of a-Si(n) deposition and the subsequent thermal annealing step to form poly-Si(n) layer. However, it should be noted that contact of boron emitter with pins/trays used in the PECVD/APCVD deposition tools could demand an extra cleaning step (for example short HF/HCl dip) in large volume manufacturing. Thermal annealing to form poly-Si(n) layer is coupled with simultaneous growth of thin oxide on boron emitter, before deposition of PECVD AlO_x/a-SiN_x on the front side. For all TOPCon routes, rear-side deposition of a-SiN_x:H is performed on top of poly-Si(n) layer, followed by the screen-printing metallization using Ag pastes and fast-firing process to form bifacial solar cells.

5. Techno-economic analysis along the PV value chain

5.1. TCO of TOPCon routes against PERC

For TCO calculations, average production efficiencies of 23.0% and 23.5% are assumed for PERC and TOPCon cells respectively, for a greenfield production with an annual production output of 5000 MWp/a. To account for uncertainties in the performed bottom-up TCO calculation featuring numerous input parameters for each processing step, we account an uncertainty margin of ±10% for the COO result of each of the individual process steps that are already in use in mass production, i.e. all process steps for *Bifacial p-PERC*. To account for a higher uncertainty of the process and financial parameters, a higher COO uncertainty margin of ±20% is assumed for each of the additional steps that are exclusive to the investigated industrial TOPCon concepts and not yet demonstrated in mass production. These process steps include BBr_3 diffusion, formation of UV-TO after CEI and BSG etching, a-Si deposition, high temperature annealing, and the SSE process. For all TOPCon concepts, polysilicon layer thickness of 150 nm is assumed for TCO calculation.

In Fig. 9, calculated All-in cell costs (left), All-in module costs (center), and LCOE (right) for the aforementioned bifacial *p*-PERC, and TOPCon process routes featuring LPCVD, PECVD and APCVD technologies are shown. Looking at the calculated TCO values, TOPCon-concepts show 13.5–18.6% higher All-in Cell costs and 3.6–5.5% higher All-in Module costs in comparison to PERC benchmark, calculating with equivalent module manufacturing costs for all concepts. The additional cost for TOPCon module is mainly related to a higher CAPEX and facility-related costs for the cell production facility, a significantly higher process consumable costs in the cell processing due to the additional process steps required compared to a PERC cell, and the higher price of *n*-type as to the PERC *p*-type wafer substrate. From the TCO calculations up to module level, no clear winner among TOPCon concepts can be declared looking at the uncertainty margin. Nevertheless, assumption of in-situ deposition of a-Si(n) for LPCVD-based concepts,

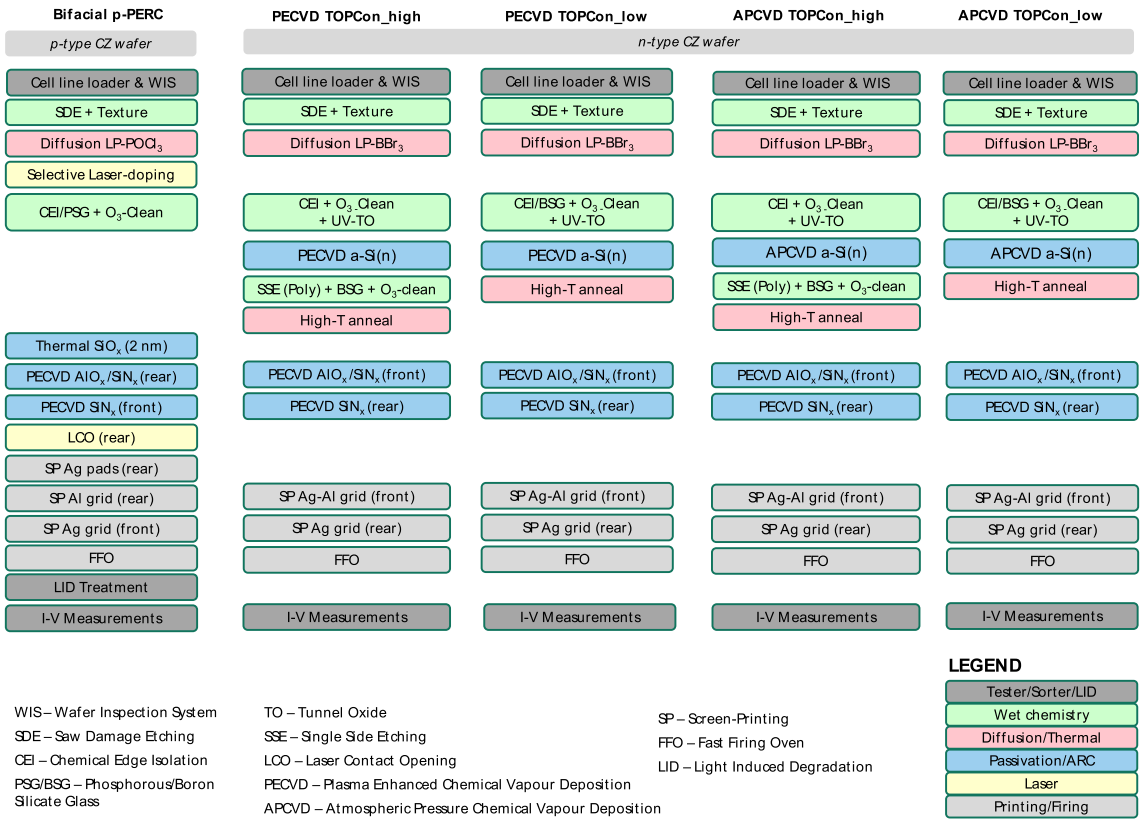

Fig. 8. Process routes for bifacial *p*-PERC and both sides contacted *n*-TOPCon-concepts based upon on PECVD and APCVD-deposited a-Si layers.

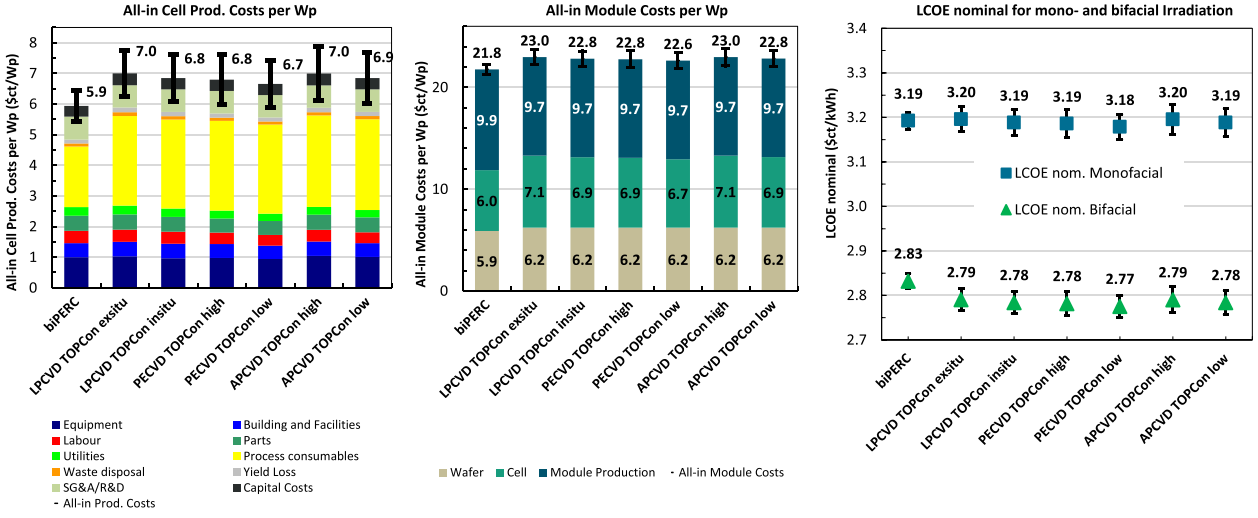

Fig. 9. All-in cell costs (left), module costs (center), and LCOE (right) calculated for the bifacial *p*-PERC and *n*-TOPCon process routes. The TCO analyses of the production includes CAPEX, material and labor costs for a green field production site with an annual output of 5000 MWp/a. Here, the numbers shown for cell concepts in each graph represent the as-calculated TCO values prior to the error approximation. Cell efficiencies of 23.0% and 23.5%, module efficiencies of 20.42% and 20.86%, and module power of 424 Wp and 433 Wp are assumed for *p*-PERC and *n*-TOPCon cells respectively, assuming an equivalent cell-to-module loss. The LCOE calculations are performed for a utility-scale installation in a location with a global horizontal irradiation of 1700 kWh/m^{2}a. For the *n*-TOPCon concepts, a higher bifaciality of 80% is assumed in comparison to *p*-PERC (70%) for the calculation of the LCOE under bifacial irradiation (Albedo: 0.2). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

and possibility of single-sided deposition for PECVD and APCVD concepts show great promise towards lowering the cell and module production costs. At LCOE level, all of the evaluated TOPCon concepts under monofacial illumination show similar values to the *p*-PERC technology under assumption of lower first year degradation of TOPCon cells based on *n*-type substrates and lower temperature coefficient of TOPCon (−0.34%/K) to PERC (−0.37%/K) modules. Assumption of a higher bifaciality of TOPCon concept (80%) to *p*-PERC (70%), significantly increases the advantage in LCOE level for the former in utility scale installations under bifacial irradiation (Albedo: 0.2). The LCOE parameters are listed in Table 4.

5.2. LCOE sensitivity to cell efficiency

For the TCO calculations performed in the last section, an efficiency gain of 0.5%$_{abs.}$ is assumed for TOPCon-concepts against the mainstream PERC cell. Meanwhile, it is intuitive to compare the LCOE costs of PERC and TOPCon production at different conversion efficiency levels. Fig. 10 compares the nominal LCOE costs for *p*-PERC cell with two of the most conservative and most progressive TOPCon concepts, for a range of conversion efficiencies under monofacial illumination conditions. It is observed that at LCOE level, an efficiency gain >0.55%$_{abs.}$ is required to achieve an economic advantage for the most conservative TOPCon-concept over *p*-PERC. For the most progressive case, an efficiency gain of >0.40%$_{abs.}$ is sufficient for the TOPCon based cell concepts to remain competitive over *p*-PERC under the given assumptions (irradiation: 1700 kWh/m^2, system size: 5 MWpa).

6. Summary

We analyzed process routes for industrial manufacturing of TOPCon cells, which are designed to mainly integrate LPCVD a-Si deposition technology in cell processing. In comparison to bifacial *p*-PERC, the LPCVD based TOPCon concepts on *n*-type silicon substrates show higher cell production costs that are distributed in all relevant cell processing clusters – wet-chemistry, diffusion/annealing, passivation, and metallization processes. Higher COO in diffusion/annealing process is mainly related to the lower throughput of BBr_3 diffusion process and requirement of an extra $POCl_3$-diffusion & the high temperature annealing steps, whereas a-Si deposition technology is one of the major cost drivers among passivation process steps. A significantly higher process consumable cost related to Ag-paste leads to a higher COO for TOPCon cell metallization. For LPCVD-based TOPCon concept, LPCVD deposition step shows almost 15%$_{abs.}$ higher COO for in-situ doped layers in comparison to intrinsic layers, mainly due to a significant difference in the deposition rate. Nevertheless, for the process route featuring in-situ deposited LPCVD a-Si/poly-Si layers, we identify a possibility of combining the high temperature annealing and oxidation of boron emitter in a single step, which makes this approach economically competitive in comparison to the process route featuring ex-situ LPCVD a-Si/poly-Si layers.

Meanwhile, alternatives to LPCVD-based process routes are identified and some of the most promising process routes for industrial TOPCon manufacturing are designed and evaluated. A comparison of normalized COO between LPCVD, PECVD and APCVD a-Si deposition technologies is performed. It is observed that COO of a-Si deposition step scales down significantly with the thickness of the a-Si layer, although interestingly the cost reduction is largely dependent upon the used deposition technology. A much stronger reduction in COO for thinner layers is observed for PECVD and APCVD-deposition technologies, which is mainly related to their significantly higher a-Si deposition rates in comparison to LPCVD. For instance, up to 50% reduction in COO can be achieved by lowering the thickness of PECVD and APCVD a-Si layer from 200 nm to 50 nm. For PECVD and APCVD a-Si technologies, two process routes are investigated based upon whether or not the single-sided polysilicon etching process is required in the envisioned TOPCon process sequence.

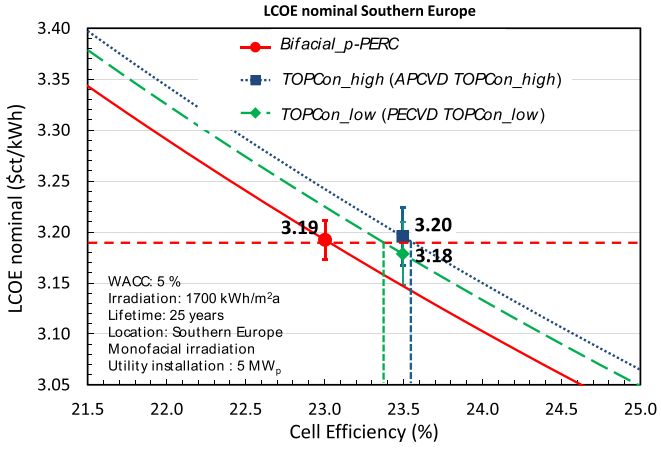

Fig. 10. Progression of nominal LCOE under monofacial irradiation with an increase in cell efficiency for *Bifacial_p-PERC*, and TOPCon routes achieving the highest (*TOPCon high*) and lowest (*TOPCon low*) LCOE values. The LCOE of cell concepts at the assumed conversion efficiencies (23.0% for PERC & 23.5% for TOPCon) are also shown as data points.

For the techno-economic analysis, a TCO calculation for a green-field production with an annual production output of 5000 MWp/a is performed. The TOPCon-concepts show higher cell and module costs in comparison to the PERC benchmark, which is mainly dominated by a higher CAPEX and OPEX due to additional equipment need, an increased usage of process consumables, and a higher price of the *n*-type substrate. Looking at the TCO results, no clear winner could be elected among TOPCon concepts, especially looking at uncertainty margins of our assumptions. Nevertheless, especially in-situ deposition of a-Si(n) for LPCVD-based concept, and single-sided deposition of a-Si(n) layer for PECVD and APCVD concepts show great promise towards further reduction of the cell and module production costs of the industrially manufactured TOPCon solar cell. At LCOE level, all the evaluated TOPCon concepts under monofacial illumination show slightly lower LCOE values to the bifacial *p*-PERC technology, assuming a TOPCon cell efficiency advantage of 0.5%$_{abs.}$ over PERC at 23.5% and 23.0% respectively. Sensitivity of the LCOE to the cell efficiency is analyzed for TOPCon routes that previously showed highest and lowest LCOE values in comparison to bifacial *p*-PERC. At LCOE level, considering the most conservative TOPCon concept, a minimum gain of 0.55%$_{abs.}$ in conversion efficiency to bifacial *p*-PERC concept is required to be economically viable. For the best-case TOPCon concept, a cell efficiency gain >0.40%$_{abs.}$ to bifacial *p*-PERC already allows cost-effective high-volume manufacturing of TOPCon solar cells. A further reduction in cell/module production costs & LCOE of TOPCon-concepts could be expected with the advances in screen-printing technology, by allowing deposition of thinner polysilicon layers that would not only reduce the related process costs but would also increase the bifacial performance of TOPCon cells. Apart from that, lowering Ag consumption in screen-printing metallization step remains a very important technological milestone for TOPCon manufacturers to further lower the COO and LCOE of the TOPCon-concept. Last but not least, it should be noted that the economic viability of each of the analyzed TOPCon routes requires a stable 24/7 production with equivalent uptime and utilization rates to current PERC cell manufacturing facilities, as it is assumed throughout this analysis. Additionally, it is worth emphasizing that the COO can significantly increase with a decrease in process yield. Especially for the case of TOPCon route, where various equipment types and processing routes are currently being assessed for high-volume manufacturing, this parameter should be carefully assessed prior to implementation.

CRediT authorship contribution statement

Bishal Kafle: Conceptualization, Data curation, Formal analysis, Methodology, Visualization, Writing – original draft, Writing – review & editing. **Baljeet Singh Goraya:** Data curation, Formal analysis, Methodology. **Sebastian Mack:** Data curation, Project administration, Writing – review & editing. **Frank Feldmann:** Data curation, Writing – review & editing. **Sebastian Nold:** Conceptualization, Formal analysis, Methodology, Writing – review & editing. **Jochen Rentsch:** Data curation, Funding acquisition, Project administration, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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APPENDIX

Table 3
Production parameters

Input	Assumed Value
Operating Time / utilization	8520 hours/year (355 d/a, 24h/d)
Annual production capacity	5 GW_p
Product: Glass-glass module	
Wafer type	Cz, M4 size (258.39 cm^2)
Cell η (PERC / TOPCon)	23.0 / 23.5 %
Module η (PERC / TOPCon)	20.42 / 20.86 %
Module power (PERC / TOPCon)	424 / 433 W_p
Cell to module power loss/gain	-0.9%
Metallization	H-pattern (5 Busbar)
No. of cells per module	72
Interconnection technology	Ribbon
Encapsulation	EVA
Module area	2.08 m^2
Ag paste consumption	
Front (PERC / TOPCon)	90 mg / 90 mg
Rear (PERC / TOPCon)	25 mg (Ag pads) / 100 mg

Table 4
LCOE parameters

Input	Assumed Value
Global horizontal irradiation	1700 kWh/m^2a (South Europe)
Irradiation on module plane	1870 kWh/m^2a
System size	5000 kWp
System type	Green field
System life	25 years
Degradation parameters	
1^{st} year (PERC / TOPCon)	2.0% / 1.5%
2+ year (PERC / TOPCon)	0.5% / 0.5%
Temperature Coefficient	
P_{mpp} (PERC / TOPCon)	-0.37 / -0.34 %/K
Bifaciality (PERC / TOPCon)	70% / 80%
Albedo	0.2 (340 kWh/m^2a)

Table 5
Total production yield of process routes. Process yield is calculated by multiplying the individual yield of each processing step, with the related equipment, over the processing route.

Process route	Yield
Bifacial p-PERC	98.47%
LPCVD TOPCon_exsitu	98.24%
LPCVD TOPCon_insitu	98.36%
PECVD TOPCon_high	98.36%
PECVD TOPCon_low	98.46%
APCVD TOPCon_high	98.36%
APCVD TOPCon_low	98.46%

Table 6
Balance of system (BOS) costs

Cost category	Utility case
Inverter costs	4.0 €ct/W_p
Area proportional BOS costs	43 €/m^2
Power proportional BOS costs	9.0 €ct/W_p
Soft BOS costs	4.1 €ct/W_p
Annual costs	1.0% of system CAPEX

Table 7
Financial parameters. Please note that Building CAPEX is applied on whole building area including production area, warehouse, labs, offices etc., whereas the Facility CAPEX is applied on production area only.

Input	Assumed Value
Labor Costs	(FTE = Full Time Equivalent)
Operation	10000 €/a per FTE
Technician	15000 €/a per FTE
Supervision	20000 €/a per FTE
Engineering	30000 €/a per FTE
Scientist	35000 €/a per FTE
Cell production CAPEX (Equipment+Building+Facility)	
Bifacial p-PERC	70.8 Mn €/GWp
LPCVD TOPCon_exsitu	77.4 Mn €/GWp
LPCVD TOPCon_insitu	73.3 Mn €/GWp
PECVD TOPCon_high	73.3 Mn €/GWp
PECVD TOPCon_low	69.6 Mn €/GWp
APCVD TOPCon_high	78.0 Mn €/GWp
APCVD TOPCon_low	74.3 Mn €/GWp
Module production CAPEX (Equipment+Building+Facility)	
Bifacial p-PERC	37.7 Mn €/GWp
TOPCon concepts	36.2 Mn €/GWp
Building CAPEX	800 €/m^2
Facility CAPEX	1500 €/m^2
Additional OPEX (Building & Infrastructure)	1.5 €ct /cell
Depreciation Periods	
Equipment CAPEX	7 years
Facility CAPEX	10 years
Building CAPEX	20 years
Cost of Capital	
Debt / equity rate	80 / 20%
Cost of debt / Cost of equity	5 / 10%
Corporate tax rate	25%
WACC (all assets – Equipment, facility & materials in stock for 14 days)	5.0%
M4 Wafer price	
p-type	34.7 $ct/piece
n-type	37.5 $ct/piece
Electricity price	5.99 $ct/kWh
Ag price	19.67 $/Oz.tr. (12-month average Nov.2019-Nov.2020)
Currency conversion (€/$)	0.9

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