

Process challenges of high-performance silicon heterojunction solar cells with copper electrodes

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ARTICLE INFO

Keywords:

Copper plating
Parasitic plating
Damp heat performance
Heterojunction
Solar cell

ABSTRACT

Substitution of expensive silver paste becomes essential for mass production of silicon heterojunction (SHJ) solar cell, which calls for high efficiency and low-cost metallization techniques. Copper metallization together with multi-busbar cell interconnection is considered as effective way to low shading loss and electrode ohmic loss. While, the electrode adhesion and parasitic plating are the key process challenges limiting the copper metallization of SHJ solar cells. In this research, the copper plated SHJ solar cells with high electrode aspect ratio and an efficiency of 23.35% have been achieved on M2 wafers. The SEM images show the holes in the plated layers will deteriorate the adhesion between plated copper and seed-layer. The glass/back sheet structure (GBS) modules have been laminated to evaluate the influence of parasitic plating on damp-heat (DH) performance. The degradation in output power (P_{max}) is up to 4.90%, which is primarily due to a decreased open-circuit voltage (V_{oc}) and fill factor (FF). It can be ascribed to the deteriorated surface recombination and interconnection. Although the parasitic plating on the wafer edge has ignorable influence on damp heat test after etch-back process, it is still necessary to protect the cell edge to avoid parasitic plating. The research evaluates the process challenges of copper metallization of SHJ solar cells, which offers a refer for achieving high reliability and low leveled cost of energy (LCOE) of photovoltaic power generation.

1. Introduction

To achieve CO₂ neutrality, the future of our electricity supply will see a massive increase in solar power generation. The annual photovoltaic (PV) module production rate must dramatically increase from ~135 GW (GW) in 2020 to ~3 TW (TW) around 2030, and requires a total of 20–80 TW photovoltaics until 2050 and 80–170 TW until 2100 [1–3]. Highly conductive silver paste is the dominated electrode material for PV industry, which requires a significant material consumption reduction to meet the multi-TW scale manufacturing target in about ten years from now. High efficiency silicon heterojunction (SHJ) solar cell applies ultra-thin amorphous silicon films as passivation layer and doping layer [4,5]. The bulk resistivity of low-temperature silver pastes (~6 $\mu\Omega$ cm) is three times higher than that of the high-temperature counterparts (~2 $\mu\Omega$ cm) due to the temperature limitation [6–8]. With a SHJ solar cell demanding ~210 mg usage of silver paste (9 busbars, 24.5%, bifacial, M6 size wafer), the cost of low temperature silver paste is ~3.4

UScents/W at today's price (~1100 USD/kg), which occupies a dominant proportion of the non-silicon cost. Thus, the urgent innovation on screen printing technologies is required for SHJ solar cells to reduce silver consumption.

The formation of copper plated contact is assumed to be one of the most promising technologies for low-cost mass production of SHJ solar cells, as it is a good solution to improve the efficiency with high aspect ratio and low contact resistance [9–11]. There have been many innovative contributions in seed layer deposition [12–16], selective pattern formation [17–20], simplification of process [21–23], etc. The copper plated SHJ solar cell has just achieved the outstanding efficiency of 26.41% (certified by ISFH) on M6 size wafer (274.5 cm²) by Sundrive and Maxwell [24]. However, there are still some barriers hindering the application of the copper plating on SHJ solar cell, such as complicated plating process, copper-induced degradation and reliability [25].

On the module level, the damp heat reliability of copper plated SHJ solar module is another issue restricting the commercialization of

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copper metallization. Benefiting from the glass/glass (GG) structure module, Silevo's copper plated modules have only -2.45% output power loss after 2000 h damp heat stress [26]. It also has been proven that the polyolefin encapsulant material has lower water vapor transmission rate (WVTR) value, which helps to reduce the degradation in damp heat test [27,28].

The electrode adhesion and parasitic plating are the key process challenges limiting the copper metallization of SHJ solar cells. The organic-based resists (such as, laminated dry film resist and screen-printed photoresist) are considered as the potential pattern solution for the mass production of SHJ metallization. While, the edge of the SHJ solar cell is not covered with resist after development process, making copper easily to be plated on the cross-section of silicon wafer. The complete copper plating metallization process is challenging, such as complicated plating process, long-term copper-induced degradation and reliability. In this work, the copper plated SHJ solar cells with a high electrode aspect ratio and an efficiency of 23.35% have been achieved. The glass/POE/back sheet structure modules have been encapsulated to evaluate the potential influence of parasitic plating after etch-back. The damp heat performance of SHJ modules were evaluated up to 1000 h under 85 °C, 85% relative humidity (RH). The photoelectric performance of SHJ solar cells and the damp heat performance of modules were analyzed. The results show great potential to achieve highly reliable and efficiently SHJ solar cells after careful optimization.

2. Experimental details

2.1. Preparation of SHJ solar cells

The M2 size, n-type c-Si (100) wafers with resistivity of 1–3 Ω cm were used as the substrates. The wet-chemical process was applied to remove saw damage and create a random pyramid surface texture. Both intrinsic and doped a-Si:H layers on the front and rear side were deposited for the emitter and back surface field by plasma enhanced chemical vapor deposition (PECVD), respectively. Then, tin doped indium oxide films (ITO), with the thickness of 80 nm on the front side and 75 nm on the rear side (both on textured wafer), were deposited by using a physical vapor deposition (PVD) system. After ITO deposition, the samples were sorted into two groups. Group A was used for copper plating and the substrates were annealed at 200 °C for 20 min in air. Each side was connected to DC power source by electrical deposition contact pads. Copper was plated under the conditions of ~ 8 ASD, 6 min with phosphorous-copper anode (0.02%–0.1% phosphorous content) on 200 nm copper seed-layer on ITO film. The light sensitive dry film was used as the plating resist. The detailed process could be found in our previous papers [20,29]. Group B was metallized by screen printing silver grids on both sides and annealed at 200 °C for 20 min in air.

2.2. Module encapsulation and damp heat stress set-up.

The monofacial glass/back sheet (GBS) single cell modules (three single cell modules and one 2×2 cells module) with copper plated were laminated for damp heat test. The Polyolefin elastomer (POE) was used as encapsulant materials. Detailed lamination parameters can be found in support information Table S1. We applied high-temperature and humidity acceleration tests (85 °C temperature and 85% humidity for 1000 h) according to standard IEC 61215 procedure. We removed the module from the damp heat chamber and measure the electrical properties at 100, 200, 300, 500, 700, 1000 h, respectively.

2.2. Measurement systems

The geometries were measured by Olympus optical microscope with a CCD camera and 3D measuring laser microscope (Olympus OLS-4100). External quantum efficiency (EQE) spectra measurement was performed within the 300–1100 nm wavelength range using a xenon (Xe) lamp. The cross-section and the element distribution were measured by Scanning Electron Microscopes (SEM) and Energy Dispersive

Spectrometer (EDS). SHJ solar cells were characterized by using current-voltage (I-V) measurements and Suns- V_{oc} system. After each time interval during the damp heat experiment, the electrical performances of SHJ modules and electroluminescence (EL) measurement were all measured by Wavelabs PV system. The solar simulator is provided from Wavelabs SINUS 220, with spectrum, homogeneity and stability matching class AAA according to IEC 60904 standard. All the I-V measurement is under standard test conditions (AM 1.5 G, 25 °C, 1000 W/m²).

3. Result and discussion

3.1. Photoelectric performance and power loss analysis of copper plating schemes

Fig. 1 presents the surface morphologies of electrodes with screen-printing (a), (c) and copper-plating (b), (d) process, respectively. The screen-printed finger width is around 44 μm and the morphology of silver finger is unsmooth. It can be seen there are also some silver particles near the silver finger on the ITO film, which could be ascribed to the extrusion of the squeegee or the residual silver paste on the screen, making a little bit silver paste is printed on the non-designed electrode area during the screen-printing process. Benefiting from the smoother morphology of resist after development, the finger width of copper finger is around 21 μm and the shape of copper plated finger is clear, whose morphology is significantly improved compared to silver finger. According to the electrode thickness results by 3D laser microscope, the cross section of copper plated finger is rectangular, with the height of around 12 μm and surface roughness less than 2 μm. While, the max electrode height of screen-printed finger is around 24 μm, that is a ~ 9 μm height gap between highest position and lowest position. Thus, the plated copper finger is much smoother than screen-printed silver finger and its aspect ratio (~ 0.6 , 12 μm/21 μm) is higher than screen-printed finger (~ 0.34 , 15 μm/44 μm). Considering the remarkably narrower finger width, the shading loss of SHJ solar cell with copper metallization is significantly limited, which has the potential to boost short-circuit current.

The electrical performance of screen-printed cell and copper plated cell with same SHJ substrates is presented in **Fig. 2**. Both are bifacial solar cells and the electrical properties are measured on copper chuck. Benefits from the excellent passivation, an impressive V_{oc} of 739.9 mV and Eff of 23.45% has been obtained for screen-printed cell. According to the finger morphologies in **Fig. 1**, the copper plated electrode has been obtained with obviously reduced finger width and shading loss ($\sim 5\%$ decrease of shading compared to screen-printed cell), resulting in a significant improvement of I_{sc} (0.38 A, 1.56 mA/cm² J_{sc} gain). It should be noted that the V_{oc} is 6 mV lower than screen-printed cell, we can ascribe to the edge recombination due to manual operation (will be discussed in EL measurement). The reduction of the electrode shading area leads to the remarkably decreased contact area and increased contact resistance between the electrode and ITO film, which results in a decrease in FF . Even so, we still achieve an efficiency of 23.35% for copper plated cell and can be further improved by carefully operation and optimization of electrode design. The photos of copper plated SHJ solar cell and encapsulated module are shown in **Fig. S1** in Support document. A recent average cell efficiency of $>23.7\%$ has been obtained shown in **Fig. S2**. The calculated photogenerated current density from EQE spectrum of either screen-printed sample or copper plated sample is ~ 40.0 mA/cm² at the wavelength range of 300–1100 nm (shown in **Fig. S3**). The photogenerated current density difference calculated from EQE is only 0.3%, while the J_{sc} difference tested in **Fig. 2** is 1.56 mA/cm² ($\sim 4\%$). Therefore, the current gain of copper plated SHJ solar cell is mainly boosted from remarkably reduced shading loss. The transparent conductive oxide (TCO) has been identified as a kind of chemically-stable materials [30,31]. The ITO films will not be etched under the protection of plating resist. Compare with screen-printed SHJ solar cell,

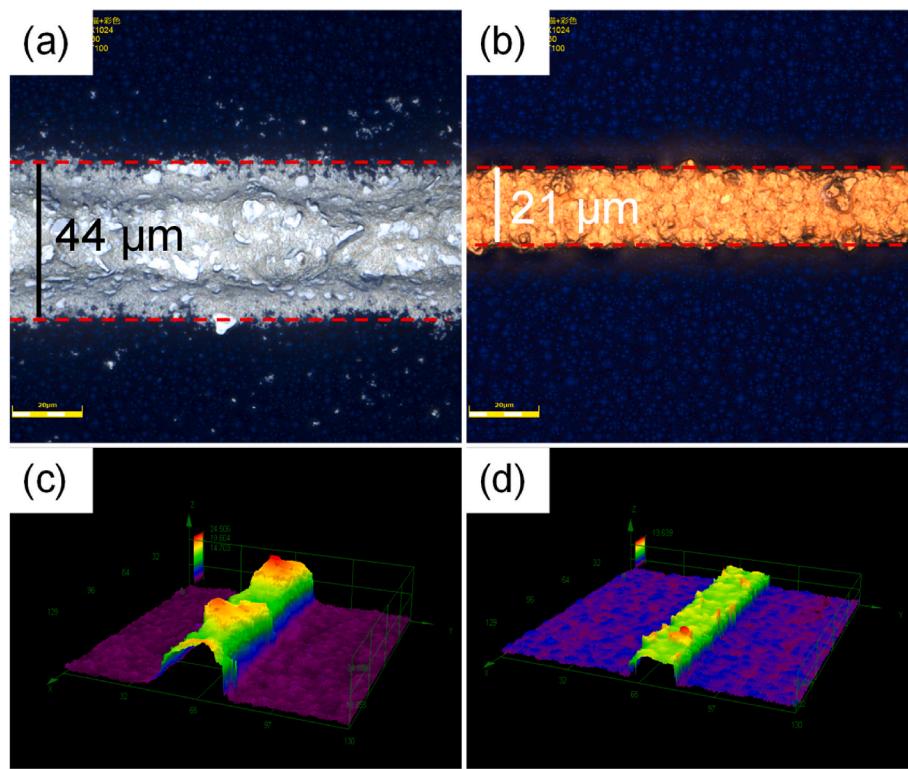


Fig. 1. SHJ solar cells (a) (c) with screen printed finger, (b) (d) with electroplated finger.

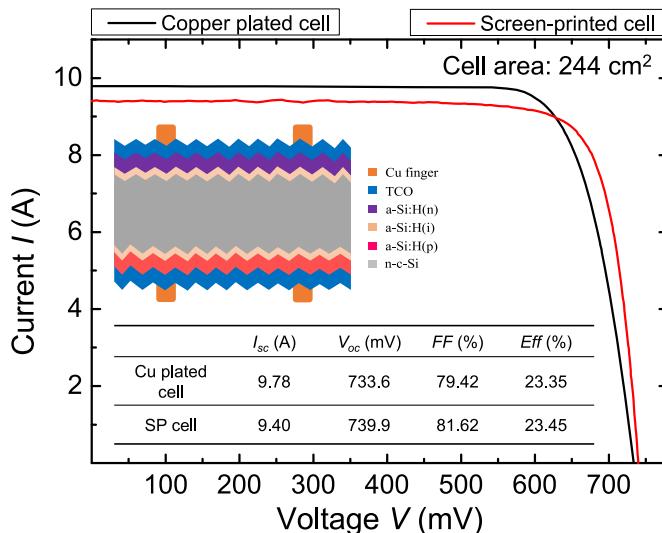


Fig. 2. Current-Voltage curve and parameters of SHJ solar cell with copper plated finger and screen-printed finger.

there is no evidence of photocurrent degradation when the samples were immersed in the plating solution. The main factor affecting the short-circuit current is the shading loss caused by the width of electrodes, which is consistent with the analysis in Fig. 1.

The ultimate purpose of solar module technology is to achieve highest possible power out for a given solar cell efficiency class. Generated current is collected by fingers to busbars, then flows to soldered ribbon. The front side metallization of solar cell affects the power loss obviously and should balance the optical and electrical loss. For copper plated SHJ solar cell, the electrode-related power loss has a significant decrease due to the bulk resistivity of finger reduces to $2 \mu\Omega \text{ cm}$. Thus, benefited from extremely low resistivity of copper finger, finer

finger width ($20 \mu\text{m}$ or below) and bigger finger pitch can be applied to reduce shading loss without increasing girds power loss. On the other hand, denser finger design is possible to control the electrical loss and increase fill factor without sacrificing J_{sc} , which helps reduce cell to module loss. The photo-generated current transports out of the solar cell to another one by the ribbons. Recent trend of solar cell is utilizing more busbars (9 BB for M6 cell, 12 BB for M12 cell), which is driven mainly by cell efficiency and silver consumption. Its cell efficiency is higher than that of SHJ solar cell with five busbars. The transport distance of carrier is an important factor affecting electrode-related power loss. Shorter transport distance of electrons means Ohmic power loss per finger drops and more power can be extracted from each individual solar cell. The evolution to multi busbars encapsulation is driven by the similar idea. The multi-busbars technology applies copper wires with low-temperature alloy coating layer and finger interconnected in a vertical direction to transport current. The power loss analysis of different metallization schemes is shown in Fig. 3 (a). The colored scale on the right of Fig. 3 (a) is the Power loss (P_{loss}). When solar module encapsulated with 18 wires of 0.2 mm in diameter, the finger length can be decreased from 15.6 mm (5 BB cell) to $\sim 4 \text{ mm}$, making the finger's ohmic power loss negligible. Meanwhile, it can be easily calculated that a reduced busbar optical shading (2.3% compared to 3.2%) compared to 5 busbars.

Based on the above analysis, the power losses of different metallization schemes with optimized parameters are illustrated in Fig. 3 (b). The power loss of screen-printed scheme is higher than 8% due to its higher resistivity of low-temperature silver paste and increased shading loss. That is the advantages of copper metallization compared to screen-printed grids. The total power loss of multi busbars interconnection is $\sim 6.5\%$, which could be ascribed to negligible electrodes ohmic loss by shorten finger length and reduced busbar optical shading. Take advantage of both copper metallization and multi busbars interconnection, the total power loss can reach as low as 5.36%. It should be noted that the power loss of emitter ($P_{emitter}$) for plating + MBB is a little bit higher than for SP + MB. The $P_{emitter}$ has a negative correlation with contact area

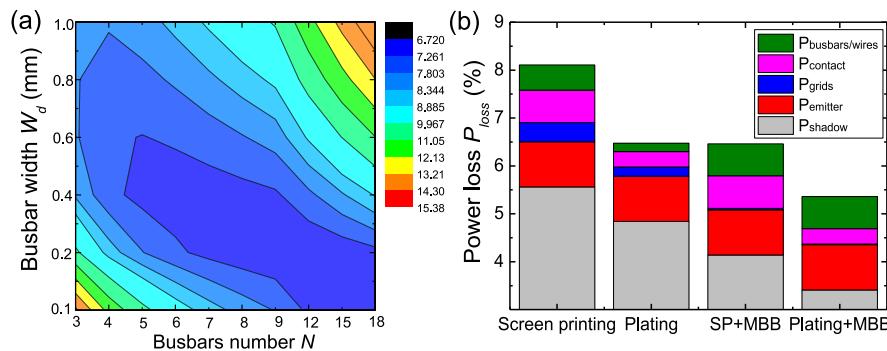


Fig. 3. The power loss analysis of multi-busbar design and different metallization schemes. (a) the influence of bus bars number and bus bar width on power loss, the color bar presents the power loss. (b) the power loss of different metallization scheme. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

between electrode and TCO, the wider finger with the lower P_{emitter} . Thanks to the higher bulk resistivity, lower contact resistivity and finer finger width, copper plating has great potential to achieve high-efficiency and low-cost metallization and interconnection solution for SHJ solar cells.

3.2. Influence of copper plating process on SHJ solar cells

To obtain better adhesion between plated electrode and TCO, a 200 nm copper seed layer is deposited on TCO surface, following by subsequent copper and tin plating process. Therefore, both seed layer and TCO interface, plated electrode and copper seed layer interface significantly influence the adhesion. To detailed investigate the interface between copper and SHJ solar cell, SEM with EDS appendix are used to measure the cross-sectional morphology and the distribution of Cu and Si elements (shown in Fig. 4). It can be seen from the figure that the electroplated copper is very dense, and the copper is covered on the surface of SHJ solar cell uniformly. Several micro-voids can be found, which could be ascribed to the high deposition rate, the bubbles released during the plating process do not have enough time to break away from the surface. We further measure the plated SHJ solar cell with poor peel force in Fig. 4 (f), many voids can be found and the electrode peeled at the interface are observed, resulting in deteriorated adhesion. It should be noted the voids could be also found at both seed layer and TCO interface, which is considered that the copper seed layer is partly corroded in the copper sulfate solution with very low PH (hydrogen ion concentration). The peel force of copper plated electrodes is presented in

Fig. 5. It is clear that the copper electrodes with gradient low-to-high plating current density process (Fig. 5 (a)) display better adhesion, compared to that of electrodes with high current density plating process (Fig. 5 (b)). That means the plating current density should not be too high in the early stage of copper plating process, otherwise it will easily introduce the voids at the interface and deteriorate the adhesion.

PECVD are applied to deposit amorphous silicon thin films as electron contact or hole contact for SHJ solar cells. During the deposition process, the plasma fills the vacuum chamber, it is possible to deposit amorphous silicon films on the edge side and cross-section of wafer (shown in Fig. S4). Therefore, these areas not covered by resist provide the pathways for current, results in parasitic plating during the electroplating process. The influence of parasitic plating at the edge side is shown in Fig. 6. It is clear to observe that copper and tin are deposited on the edge side and cross-section of SHJ solar cell if there is no edge protection. We also provide the detailed images of parasitic plating before and after etch-back process. The 200 nm Cu seed layer is deposited full area on the ITO surface. Therefore, the seed layer must be etched after plating process. Usually, a mixed solution of oxidizer and acid to etch Cu seed layer to form selective copper finger as the last plating process. Since the adhesion of copper plated on silicon is very poor, making it easy to be peeled off during this etch-back process. It should be noted that the ITO film is not deposited to cover full area of wafer to avoid edge shunt. The main reason the cross-section area seems a little bit different in Fig. 6 (a) and Fig. 6 (b) is the possible substrate movement during ITO deposition. It is also proved in Fig. S5 that the parasitic plating thickness is different from cell to cell (from ~2 μm to

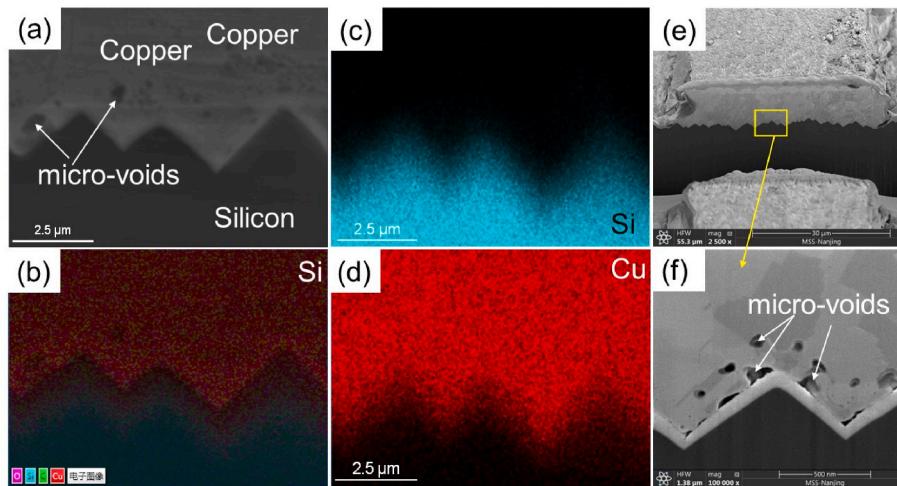


Fig. 4. The cross-section and EDS images between copper and SHJ solar cell interface.

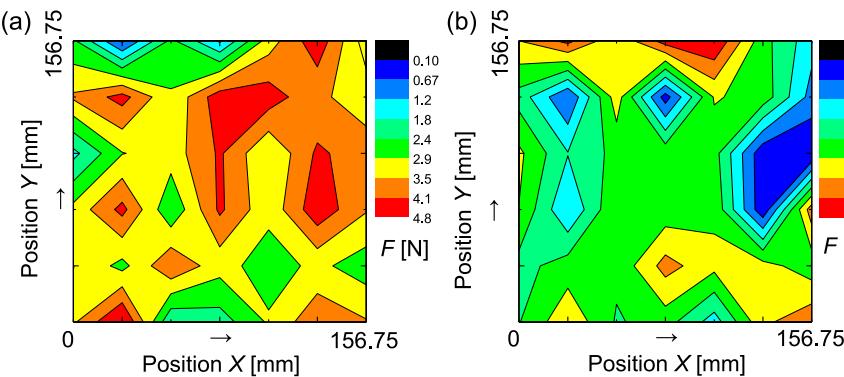


Fig. 5. The peel force of copper plated electrodes, (a) gradient low-to-high plating current density process (the plating recipe starts from 3 ASD to 6 ASD, and increase to 8 ASD), (b) high current density plating process (the plating recipe starts from 8 ASD directly). The color bar presents the distribution of peel force (N). The peel force at different positions of SHJ solar cells are measured. (For interpretation of the references to color in this figure legend, the reader is referred to the Web version of this article.)

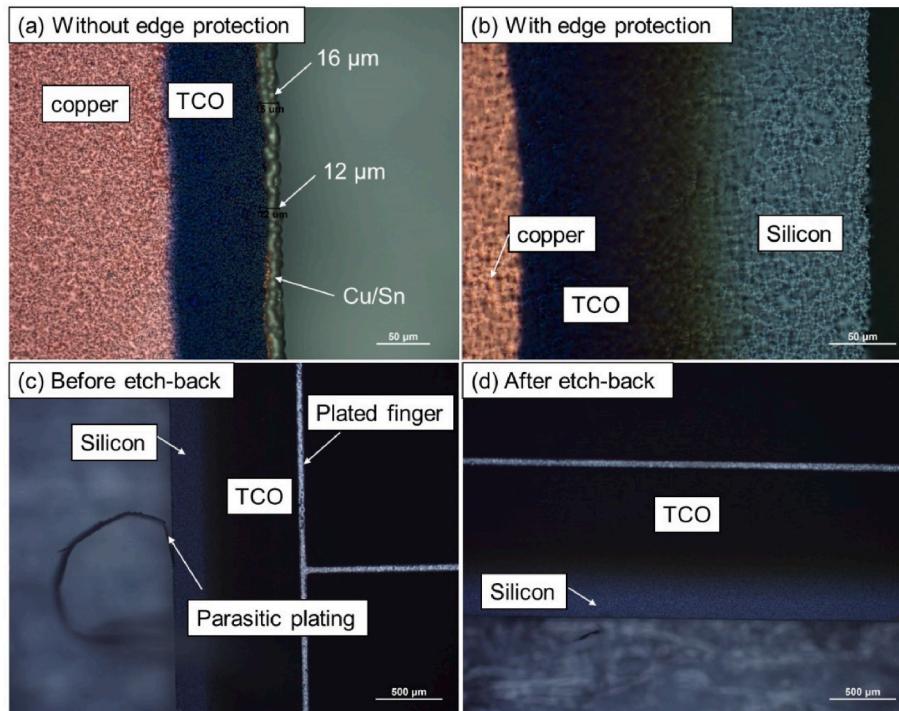


Fig. 6. The images of edges in copper plated SHJ solar cells, (a) without edge protection, (b) with edge protection, (c) the parasitic plated metal before etch-back, (d) the edge image of parasitic plating after etch-back. All the images are phototted from the front side.

10 μm , and possible to 15 μm in Fig. 6). The edge side and cross-section of SHJ solar cell is clear and without any plated metal when the edge is protected by the resist (shown in Fig. 6 (b)). However, the protection process requires additional resist to cover the edge, which will increase the complexity of the copper metallization and the cost.

It is known to all that copper acts as a deep level impurity, this causes the risk that copper diffuses into the wafer and deteriorates the device performance. Usually, very small amount of metal is plated on the edge side, which will be etched during the subsequent etch-back process. Fig. 7 presents the SEM image and EDS elemental analysis of parasitic plated copper after etch-back process. It is clearly shown in Fig. 7 (d) that there is still copper element detected on the wafer surface. The presence of the oxygen element signal is due to the use of oxidant during etch-back process. It can be found the Cu signal is rather low in EDS. Considering the EDS test area is far from the copper electrode, the copper covered the test location before etch-back process and the distribution of the N element signal (not shown here), we speculate that there are still little amounts of copper on the surface after corrosion. Thus, the influence of parasitic plating for SHJ solar cell should be

evaluated carefully to avoid long term reliability degradation. Further investigation is ongoing.

In this work, we try to evaluate its influence on cell level and module level. Fig. 8 presents the influence of copper plating process on photo voltage of SHJ solar cells under different irradiation density by Suns- V_{oc} measurement. We found that the parasitic plating at the cell edge mainly affect photo voltage under low light irradiation. The photo voltage is nearly not affected when the light irradiation exceeds 0.3 Suns. The low level of carrier recombination in SHJ solar cells, making them highly sensitive to any additional defects. It seems the plating process has a negative effect on passivation, resulting in the worse response at low irradiation. Detailed parameters can be found in Table S2. The ideality factor at 0.1 Suns increases significantly from 1.22 to 2.16 after coppering plating and subsequent annealing process. The ideality factor reflects the quality of the PN junction. We have measured many SHJ samples, both copper plated cells and screen-printed cells. Statistically, the plating process has negative effect to SHJ solar cells, which proven by Suns- V_{oc} measurement. Meanwhile, we have also analyzed the effect of copper on SHJ substrates (shown in Fig. S6). The results find that the

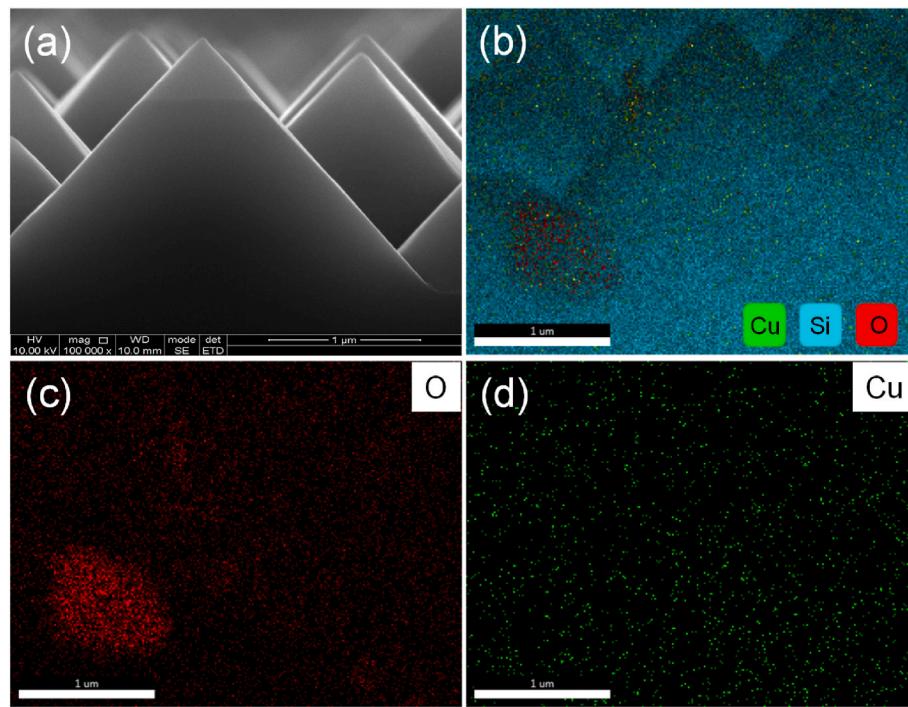


Fig. 7. SEM image and EDS elemental analysis of parasitic plated copper after etch-back process.

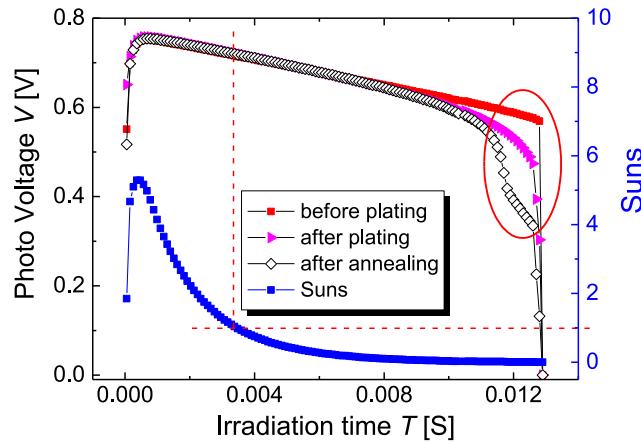


Fig. 8. Influence of copper plating process on photo voltage of SHJ solar cells under different irradiation density.

minority carrier lifetime τ , implied V_{oc} and implied FF are almost unchanged, which proves ITO is an effective copper diffusion barrier. Therefore, we speculate that the degradation detected from $Suns-V_{oc}$ could be ascribed from the parasitic plating at the edge area, where has been proved the existence of copper even after etch-back. More detailed work needs to be carried out to validate our inferences in the future.

To further evaluate the influence of parasitic plating on reliability, the single-cell modules with glass/POE/back sheet structure are encapsulated. The normalized changes in the electrical performance of the test modules at 85 °C and 85% RH with increasing ageing time, are depicted in Fig. 9. A similar evolution trend of V_{oc} , I_{sc} and FF could be found, with ~1.5% degradation after 1000 h damp heat stress, resulting in a relatively obvious power loss finally. A maximum output power (P_{max}) changes of -4.90% is obtained for copper plated SHJ module. The drop in FF goes along with a gradually increasing series resistance, which could be ascribed to deteriorated interconnection between copper

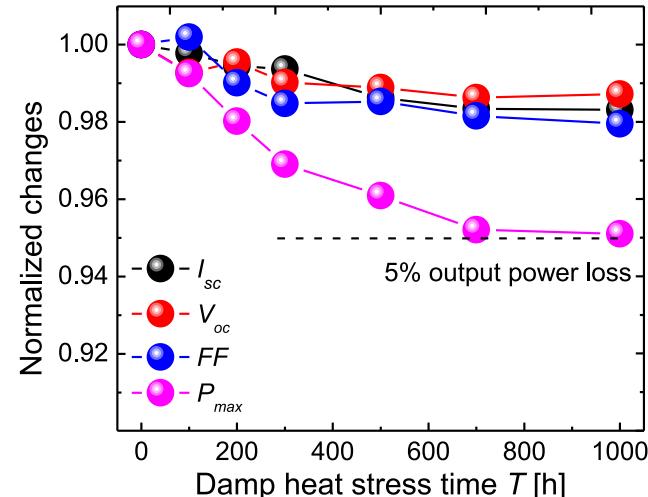


Fig. 9. I-V measurements of copper plated SHJ modules during 1000 h damp heat stress.

plated fingers and copper wire. In the further work, denser finger design could be applied to control the electrical loss and increase fill factor, which help reduce cell to module loss.

To further analyze the electrical homogeneity and entirety of the copper plated SHJ solar module, EL measurements were performed in Fig. 10. For EL measurement, the module is operated as a light-emitting diode, meaning that current is applied in reverse direction. The emitted radiation due to recombination effects can be detected with a sensitive NIR Si-CCD-camera. As the increasing damp heat stress time, the light intensity of EL images at the edges around copper plated SHJ solar cell starts to reduce, while there is nearly no visible change in the center. This performance change is in good agreement with the degradation of module output power loss. The luminous intensity is stronger near the busbar area, which means the more effective collection of carriers. After

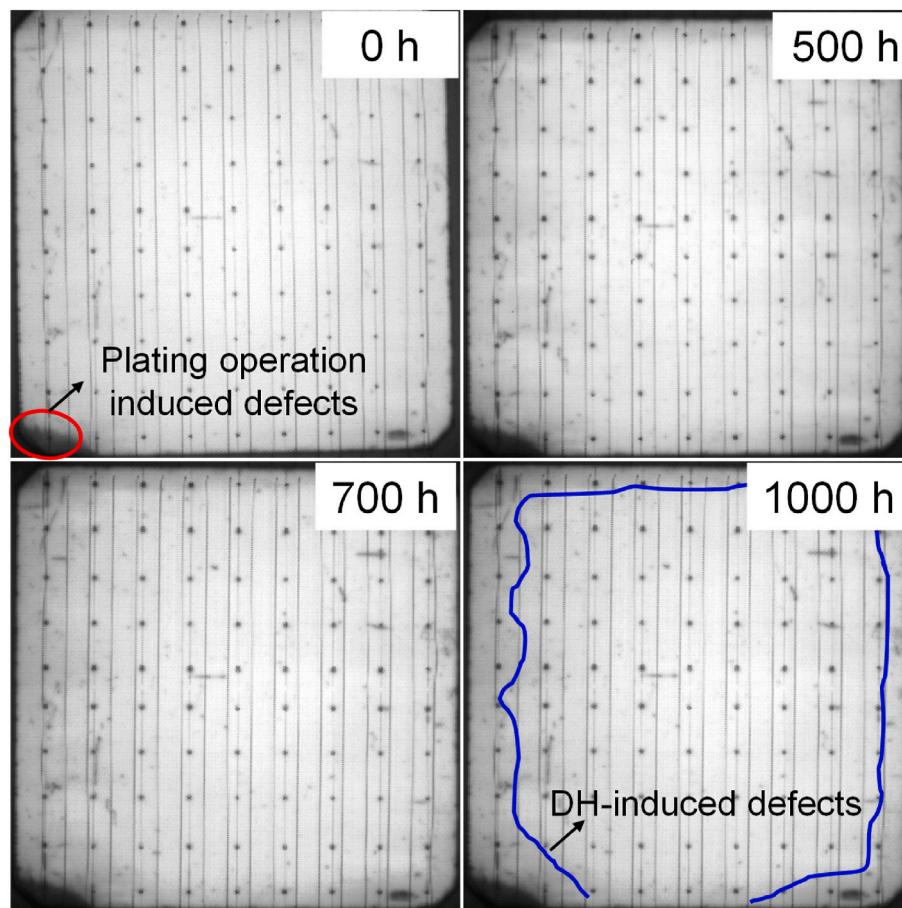


Fig. 10. Electroluminescence images of copper-plated solar module before and after 500, 700 and 1000 h of damp heat stress.

1000 h damp heat stress, it is clearly that copper plated solar module is substantially degraded around cell edges (blue frame). The entry of water vapor leads to passivation and interconnection defect as expected. The front encapsulant is hydrolyzed, which deteriorates the connection between copper wire bus bars and plated copper fingers, firstly at the perimeter of the cell, then advancing toward the center with continued DH exposure. That's result is consistent with the previous work by Wenzhu Liu [32]. The detailed influence of different encapsulants on SHJ solar cells is carrying out and will be released later.

4. Conclusion

The copper metallization technology for SHJ solar cells needs to break through the complicated process limits before mass production application. This work focuses on some process challenges during copper metallization process on solar cell level and module level. The copper plated SHJ solar cell has a high electrode aspect ratio and an efficiency of 23.35% on M2 size wafer. The SEM images show the holes in the plated layers will deteriorate the adhesion between plated copper and seed-layer. The GBS structure modules have been laminated to evaluate the influence of parasitic plating on DH performance. The degradation of GBS module in output power (P_{max}) is up to 4.90% after 1000 h damp-heat stress, which is primarily due to a decreased open-circuit voltage and fill factor. The parasitic plated metal on the wafer edge side will be etched in the etch-back process and seems have ignorable electrical properties influence on module level, it is still suggested to protect the cell edge to avoid parasitic plating. After further optimization of SHJ solar cell process, encapsulant material and glass/glass structure, the copper plated SHJ solar modules show great potential for high reliability and low leveled cost of energy (LCOE) of

photovoltaic power generation.

CRediT authorship contribution statement

Jian Yu: Writing – review & editing, Writing – original draft, Supervision, Resources, Project administration, Methodology, Investigation, Funding acquisition, Data curation, Conceptualization. **Yu Bai:** Writing – review & editing, Writing – original draft, Resources, Investigation, Data curation. **Junjun Li:** Writing – review & editing, Validation, Methodology, Investigation. **Qingqing Qiu:** Visualization, Investigation, Formal analysis. **Tao Chen:** Writing – review & editing, Project administration, Conceptualization. **Yuelong Huang:** Supervision, Resources. **Junsheng Yu:** Supervision, Resources, Conceptualization. **Jiaxuan Liao:** Supervision, Resources.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgement

This work was supported by National Natural Science Foundation of China (Grant No. 61904154), Sichuan Science and Technology Program (Grant No. 2022YFG0229), Science and Technology Project of Chengdu

(Grant Nos. 2022-YF05-00384-SN, 2020-GH02-00014-HZ). This work is also sponsored by the Sichuan Province Key Laboratory of Display Science and Technology.

Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.solmat.2022.112057>.

References

- [1] J.C. Goldschmidt, L. Wagner, R. Pietzcker, L. Friedrich, Technological learning for resource efficient terawatt scale photovoltaics, *Energy Environ. Sci.* 14 (2021) 5147.
- [2] Y. Zhang, M. Kim, L. Wang, P. Verlinden, B. Hallam, Design considerations for multi-terawatt scale manufacturing of existing and future photovoltaic technologies: challenges and opportunities related to silver, indium and bismuth consumption, *Energy Environ. Sci.* 14 (2021) 5587–5610.
- [3] P.J. Verlinden, Future challenges for photovoltaic manufacturing at the terawatt level, *J. Renew. Sustain. Energy* 12 (2020), 053505.
- [4] Z. Wu, L. Zhang, R. Chen, W. Liu, Z. Li, F. Meng, Z. Liu, Improved amorphous/crystalline silicon interface passivation for silicon heterojunction solar cells by hot-wire atomic hydrogen during doped a-Si:H deposition, *Appl. Surf. Sci.* 475 (2019) 504–509.
- [5] Z. Wu, W. Duan, A. Lambertz, D. Qiu, M. Pomaska, Z. Yao, U. Rau, L. Zhang, Z. Liu, K. Ding, Low-resistivity p-type a-Si:H/AZO hole contact in high-efficiency silicon heterojunction solar cells, *Appl. Surf. Sci.* 542 (2021), 148749.
- [6] J. Levrat, C. Alleb  , N. Badel, L. Barraud, M. Bonnet-Eymard, J. Champliaud, F. Debrot, A. Descoedres, A. Faes, A. Lachowicz, S. Nicolay, L. Sansonnens, C. Ballif, J. Geissb  hler, S. De Wolf, M. Despeisse, High-performance heterojunction crystalline silicon photovoltaic technology, in: IEEE 40th Photovoltaic Specialist Conference, PVSC, 2014.
- [7] S.D. Wolf, A. Descoedres, Z.C. Holman, C. Ballif, High-efficiency silicon heterojunction solar cells: a review, *Greenpeace* 2 (1) (2012) 7–24.
- [8] J. Yu, Y. Qiu, J. Bian, Y. Liu, F. Meng, J. Liu, Z. Liu, Electroplated Copper Electrodes for Silicon Hetero-Junction Solar Cells >21%, Grand renewable energy, 2014.
- [9] J. Chang, F. Chen, M. Chen, W. Hsieh, M. Huang, Development of copper electroplating technique for silicon heterojunction solar cells with efficiency over 23.1%, in: 29th European Photovoltaic Solar Energy Conference and Exhibition, 2014.
- [10] D. Adachi, J.L. Hern  ndez, K. Yamamoto, Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency, *Appl. Phys. Lett.* 107 (2015), 233506.
- [11] J. Geissb  hler, S.D. Wolf, A. Faes, N. Badel, Q. Jeangros, A. Tomasi, L. Barraud, A. Descoedres, M. Despeisse, C. Ballif, Silicon heterojunction solar cells with copper-plated grid electrodes: status and comparison with silver thick-film techniques, *IEEE J. Photovoltaics* 4 (4) (2014) 1055–1062.
- [12] A. Rodofili, W. Wolke, L. Kroely, M. Bivour, G. Cimiotti, J. Bartsch, M. Glatthaar, J. Nekarda, Laser transfer and firing of NiV seed layer for the metallization of silicon heterojunction solar cells by Cu-plating, *Sol. RRL* (2017), 1700085.
- [13] J. Li, J. Yu, T. Chen, H. Zhang, Q. Wang, P. Wang, Y. Huang, In-situ formation of indium seed layer for copper metallization of silicon heterojunction solar cells, *Sol. Energy Mater. Sol. Cells* 204 (2020), 110243.
- [14] S. Lee, D. Lee, K. Lim, W. Shin, J. Kim, Copper-nickel alloy plating to improve the contact resistivity of metal grid on silicon heterojunction solar cells, *Electron. Mater. Lett.* 15 (2019) 314–322.
- [15] H. Kim, S. Lee, D. Lee, A. Lee, K. Lim, W. Shin, J. Kim, Improvement of ohmic contact between the indium tin oxide and copper-plated contact of solar cells by using the Cu-Sn alloy film, *J. Nanosci. Nanotechnol.* 20 (1) (2020) 245–251.
- [16] M. Glatthaar, R. Rohit, A. Rodofili, Y.J. Snow, J. Nekarda, J. Bartsch, Novel plating processes for silicon heterojunction solar cell metallization using a structured seed layer, *IEEE J. Photovoltaics* 7 (6) (2017) 1569–1573.
- [17] M. Aleem, R. Vishnuraj, B. Krishnan, B. Pullithadathil, Realization of micropatterned, narrow line-width Ni-Cu-Sn front contact grid pattern using maskless direct-write lithography for industrial silicon solar cells, *ACS Appl. Energy Mater.* 4 (2021) 10682–10696.
- [18] A. Khanna, K. Ritzau, M. Kamp, A. Filipovic, C. Schmiga, M. Glatthaar, A.G. Aberle, T. Muellera, Screen-printed masking of transparent conductive oxide layers for copper plating of silicon heterojunction cells, *Appl. Surf. Sci.* 349 (2015) 880–886.
- [19] T. Hatt, J. Bartsch, V. Davis, A. Richter, S. Kluska, S. Glunz, M. Glatthaar, A. Fischer, Hydrophobic AlO_x surfaces by adsorption of a SAM on large areas for application in solar cell metallization patterning, *ACS Appl. Mater. Interfaces* 13 (2021) 5803–5813.
- [20] J. Yu, J. Bian, Y. Liu, F. Meng, Z. Liu, Patterning and formation of copper electroplated contact for bifacial silicon hetero-junction solar cell, *Sol. Energy* 146 (2017) 44–49.
- [21] T. Hatt, S. Kluska, M. Yamin, J. Bartsch, M. Glatthaar, Native oxide barrier layer for selective electroplated metallization of silicon heterojunction solar cells, *Sol. RRL* (2019), 1900006.
- [22] D. Adachi, T. Terashita, T. Uto, J. Hern  ndez, K. Yamamoto, Effects of SiO_x barrier layer prepared by plasma-enhanced chemical vapor deposition on improvement of long-term reliability and production cost for Cu-plated amorphous Si/crystalline Si heterojunction solar cells, *Sol. Energy Mater. Sol. Cells* 163 (2017) 204–209.
- [23] J. Yu, L. Zhang, T. Chen, J. Bian, J. Shi, F. Meng, Y. Huang, Z. Liu, Dual-function light-trapping: selective plating mask of SiO_x/SiN_x stacks for silicon heterojunction solar cells, *Sol. RRL* (2019), 1800261.
- [24] Maxwell, SunDrive set 26.41% efficiency record for HJT cell, Sep. 05, <https://www.solarbeglobal.com/maxwell-sundrive-set-26-41-efficiency-record-for-hjt-cell/>, 2022.
- [25] J. Yu, J. Li, Y. Zhao, A. Lambertz, T. Chen, W. Duan, W. Liu, X. Yang, Y. Huang, K. Ding, Copper metallization of electrodes for silicon heterojunction solar cells: process, reliability and challenges, *Sol. Energy Mater. Sol. Cells* 224 (2021), 110993.
- [26] J. Heng, J. Fu, B. Kong, Y. Chae, W. Wang, Z. Xie, A. Reddy, K. Lam, C. Beitel, C. Liao, C. Erben, Z. Huang, Z. Xu, 23% high-efficiency tunnel oxide junction bifacial solar cell with electroplated Cu gridlines, *IEEE J. Photovoltaics* 5 (1) (2015) 82–86.
- [27] J. Hernandez, K. Yoshikawa, A. Feltrin, N. Menou, N. Valckx, E. Assche, D. Schroos, K. Vandersmissen, H. Philipsen, J. Poortmans, D. Adachi, M. Yoshimi, T. Uto, H. Uzu, T. Kuchiyama, C. Allebe, N. Nakanishi, T. Terashita, T. Fujimoto, G. Koizumi, K. Yamamoto, High efficiency silver-free heterojunction silicon solar cell, *Jpn. J. Appl. Phys.* 51 (2012) 10NA04.
- [28] J. Karas, A. Sinha, V. Buddha, F. Li, F. Moghadam, G. TamizhMani, S. Bowden, A. Augusto, Damp heat induced degradation of silicon heterojunction solar cells with Cu-plated contacts, *IEEE J. Photovoltaics* 10 (2) (2020) 372–382.
- [29] J. Yu, J. Bian, W. Duan, Y. Liu, J. Shi, F. Meng, Z. Liu, Tungsten doped indium oxide film: ready for bifacial copper metallization of silicon heterojunction solar cell, *Sol. Energy Mater. Sol. Cells* 14 (2016) 359–363.
- [30] W. Liu, W. Chen, T. Tsai, S. Hsieh, C. Liu, Effect of tin-doped indium oxide film thickness on the diffusion barrier between silicon and copper, *Thin Solid Films* 515 (2006) 2387–2392.
- [31] S. Hsieh, C. Chien, W. Liu, W. Chen, Failure behavior of ITO diffusion barrier between electroplating Cu and Si substrate annealed in a low vacuum, *Appl. Surf. Sci.* 255 (2009) 7357–7360.
- [32] W. Liu, L. Zhang, X. Yang, J. Shi, L. Yan, L. Xu, Z. Wu, R. Chen, J. Peng, J. Kang, K. Wang, F. Meng, S. Wolf, Z. Liu, Damp-heat-stable, high-efficiency, industrial-size silicon heterojunction solar cells, *Joule* 4 (2020) 913–927.