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The Passivated Emitter and Rear Cell (PERC): From conception to mass production

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ABSTRACT

Improved solar cell efficiency is the key to ongoing photovoltaic cost reduction, particularly as economies of scale propel module-manufacturing costs towards largely immutable basic material costs and as installation costs become an increasingly large contributor to total system costs. To enable manufacturers to move past the 20% cell energy conversion efficiency figure in production, high-efficiency PERC (Passivated Emitter and Rear Cell) sequences are being increasingly brought online. Most new photovoltaic manufacturing capacity added in the second half of 2014 was PERC-based, making PERC now the cell technology with second-highest production capacity, with the latest industry roadmap anticipating PERC will become the dominant commercial cell technology by 2020. The first paper describing the PERC cell appeared in 1989, although the structure was conceived several years earlier. The attractive technical features were the reduction of rear surface recombination by a combination of dielectric surface passivation and reduced metal/semiconductor contact area while simultaneously increasing rear surface reflection by use of a dielectrically displaced rear metal reflector. The key issues in the development of this technology and its commercial implementation are described, including a review of recent adoption rates and the way these are likely to evolve in the future.

1. Background technology

The first paper describing the PERC cell appeared in 1989 [1], although this device was first described in 1983 in a UNSW (University of New South Wales) final grant report [2] and as a deliverable in a subsequent grant proposal [3], accompanied in both cases by the drawing shown in Fig. 1. The attractive feature was the elegant way in which the PERC cell incorporated three attributes into the rear contacting scheme that earlier work at UNSW and elsewhere had shown were important to obtaining high efficiency. These were the reduction of rear surface recombination by a combination of dielectric surface passivation and reduced metal/semiconductor contact area, with simultaneously increased rear surface reflection by use of a dielectrically displaced rear metal reflector.

Around the time the PERC cell was proposed, the highest confirmed efficiency for a Si cell was 19.1% [4], estimated as 18.4% efficient by present standards [5]. The cell structure was a relatively simple UNSW planar PESC cell (Passivated Emitter Solar Cell) of Fig. 2 with the main feature responsible for its high efficiency being its high open-circuit voltage (V_{oc}). A contributor to this high voltage (658.4 mV at 25 °C) was the reduced area of the top surface contact, the first demonstration of improved conversion efficiency by this approach, and surface passivation by dielectric oxide, both features that the PERC cell sought to emulate on the rear surface. The PESC cell retained the Al alloyed BSF/BSR (back surface field/ back surface reflector) developed in the late 1960s [6] that had featured in earlier generations of high efficiency cells and has been used in most commercial cells to date.

Any solar cell can be associated with an effective diode saturation current density, J_o, calculated from its measured V_{oc} and short-circuit current density, J_{sc}, as:

$$J_o = J_{sc}/[\exp\left(\frac{qV_{oc}}{kT}\right) - 1] \quad (1)$$

where T is the absolute temperature and kT/q is the thermal voltage (25.693 mV at 298.15 K or 25 °C). This cell had a creditable J_o of 270 fA/cm^2 at 25 °C, almost evenly divided between contributions from the combination of top surface and contact recombination and from bulk and rear contact recombination [7].

Apparently the first published suggestion of reduced contact area as a way of reducing contact recombination and its contribution to J_o was made at UNSW almost a decade earlier [8]. In the Crowell-Sze thermionic-emission/diffusion theory of metal/

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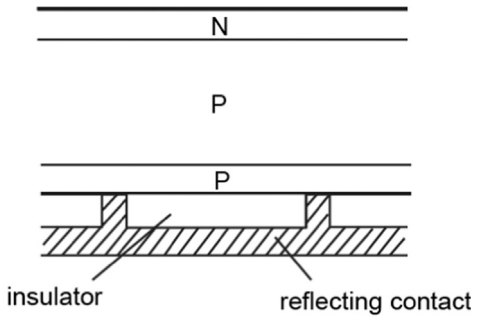

Fig. 1. First diagram of PERC cell [2,3] (PERT configuration: Passivated Emitter, Rear Totally-diffused). More information on different PERC configurations is given subsequently in Fig. 8, with redefined acronyms to better reflect present usage.

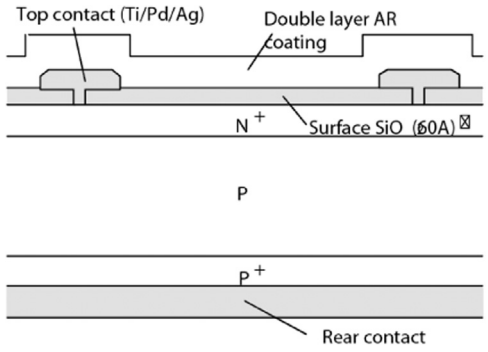

Fig. 2. The PESC solar cell, the most efficient Si cell at the time of PERC cell proposal [4].

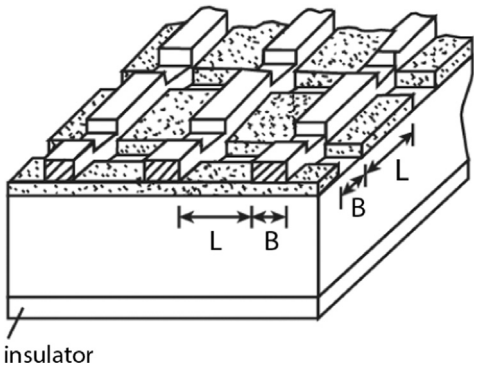

Fig. 3. Reduced contact area as a way of reducing contact recombination [8].

semiconductor contacts [9], currents associated with these contacts are described in terms of effective recombination velocities for both electrons and holes [10]. It was suggested reducing contact area as in Fig. 3 could reduce such effective velocities [8], improving the open-circuit voltage of Schottky diode solar cells. The specific approach shown in Fig. 3 to reduce contact area was employed in the first experimental PESC cells, prior to delivery of the photolithography masks used to fabricate the 19.1% cell of Fig. 2, with 687 mV V_{oc} confirmed for a device with this structure by NASA-Lewis in Sept. 1983 [2], the highest ever independently confirmed value at this stage.

Almost contemporaneously with the UNSW paper [8], Lindmayer and Allison of COMSAT Laboratories, inventors of the violet cell that led to substantial efficiency improvements in the early 1970s, also suggested use of reduced contact area in a subsequently published patent application [11]. The shallower emitters (top diffused layers) in these devices had directed attention to emitter surface recombination, negligible in earlier generations of cells because of their deep emitter diffusions. Independently, these

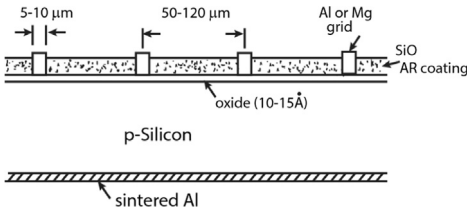

Fig. 4. Oxide passivation as a way of reducing surface recombination in MIS solar cells as well as related MINP cells, with the latter differentiated by an n-type diffused layer under the oxide.

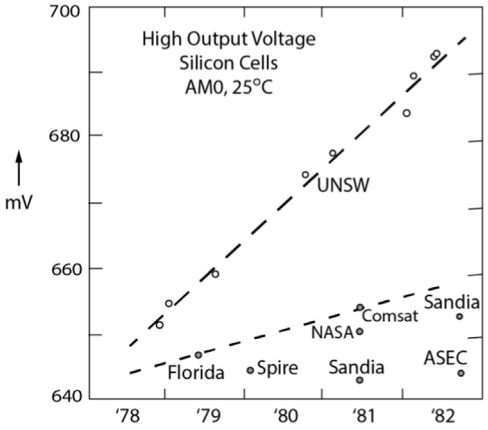

Fig. 5. Early history of V_{oc} improvement in Si cells, demonstrating the effectiveness of UNSW oxide passivation.

researchers suggested the same approach as in Fig. 3 as a way of achieving this low contact, implemented by COMSAT Labs nearly a decade later, slightly earlier than in PESC cells, but with less resounding outcomes [12].

For similar reasons, dielectric passivation of the top surface also had not been important in earlier generations of silicon cells. The good interfacial properties of thermally grown oxides were well known from their use in Metal/Oxide/Semiconductor (MOS) transistors. UNSW led efforts to improve open circuit voltage in the late 1970s, using the inversion layer MIS (Metal/Insulator/Semiconductor) cell structure of Fig. 4, relying on oxide passivation in non-contacted areas as well as charge in the overlying dielectric. These MIS devices were first reported as giving V_{oc} above conventional cells in 1976 [13].

MIS and related MINP (Metal/Insulator/N–P junction) devices subsequently became the first silicon cells to display V_{oc} above 650 mV in 1978 and 678 mV in 1981 (Fig. 5). The latter voltage corresponds to J_0 values of 100 pA/cm^2 with 26 pA/cm^2 assigned to recombination at the top oxide-passivated surface [14]. This oxide passivation has been maintained through successive generations of UNSW high voltage, high efficiency devices.

The first paper applying the benefits of such thin oxide passivation to more conventional *p–n* junction device structures appeared in 1978 [15]. This was also an important paper in that it also seems to be the first to use PECVD silicon nitride, now the industry standard, as an antireflection (AR) coating, although Motorola had been using non-PECVD nitrides in production since 1977 [16].

The UNSW interest in dielectrically displaced rear reflectors arose from the results shown in Fig. 6, published by Solarex in 1976 [17], showing the measured reflectance nominally at the rear Al/Si BSF/BSR interface as a function of alloying conditions. Trying to understand these data (later realising drop at high temperature was due to surface roughening and consequent light-trapping), expected reflection values were calculated theoretically.

This led to the realisation that the high refractive index of silicon considerably supressed rear metal reflection and that inserting a lower index dielectric layer between the metal and silicon would significantly increase this reflection. Experiments subsequently conducted at UNSW as part of an undergraduate thesis project produced the results shown in Fig. 7, showing reflection from as-deposited Al could be increased from 89% to an almost ideal 98%. Knowledge of these large optical benefits provided additional incentive for implementing the PERC structure.

Successful implementation of the PERC cell was not immediate. Introducing top-surface texturing of the PESC cell of Fig. 2, also suggested in the previous grant documents [2,3], gave more rapid progress with 20% cell efficiency demonstrated in 1985 [5]. Attention was then diverted to applying these developments to silicon concentrator cells to meet contractual requirements, with this work resulting in the first 20% efficient photovoltaic module [18]. For the PERC cell, boron diffusion capability needed to be established and perfected, with this proving more challenging than for the phosphorus diffusions already established. Some tips from the solar cell group at Stanford University regarding the advantages of chlorine-based furnace processing proved most helpful here, allowing the whole family of PERC cells (Fig. 8) to be experimentally investigated. The first high efficiency PERC cells were fabricated in 1988, with 21.8% efficiency confirmed at Sandia in October 1988 (20.9% by present standards).

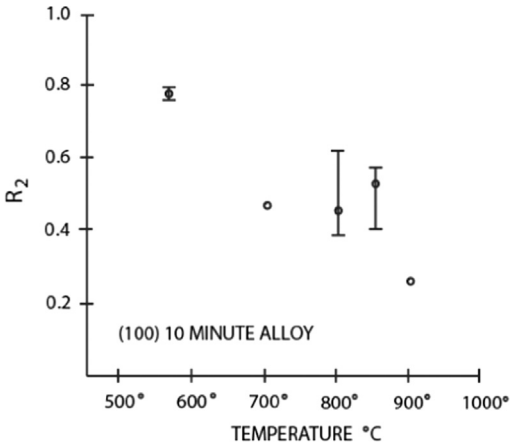

Fig. 6. Measured reflectance nominally at the rear alloyed Al/Si interface as a function of alloying conditions [17].

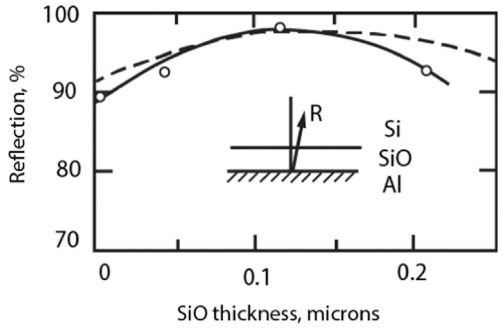

Fig. 7. Early UNSW measurements of effects of intervening dielectric layer on rear Al reflection (evaporated SiO was used as a dielectric since the ability to grow thick thermal oxides had not been established at UNSW at the time).

2. Efficiency and processing optimisation

These initial results fuelled the ongoing improvements in silicon cell efficiency on p-type monocrystalline substrates to 25% (Fig. 9). Applying the approach to multicrystalline substrates led to the first multicrystalline cell of efficiency above 20%, by present standards, in 1998 [5]. Initial UNSW application to n-type substrates using reversed doping polarities gave lower efficiency than on p-type substrates, with an efficiency of 21.9% (22.1% by present standards [5]) demonstrated in 1991, with the lower efficiency arising from the increased challenges involved in performing large-area B diffusions. Much later in 2005, an inverted rear emitter structure increased this efficiency to 22.7% (22.9% by present standards), equalling the efficiency of the best ever n-type solar cell at that time. A significant subsequent independent development was the recognition of the excellent surface passivation properties of Al_2O_3. This material had long been used as the low-index layer in double-layer AR coatings for space cells. An early report [19] of its excellent passivation properties for p-type surfaces went largely unnoticed until a new efficiency mark of 23.2% (23.4% by present standards) on n-type substrates [20] was established in 2006. This dielectric has proved important for subsequent PERC commercialisation.

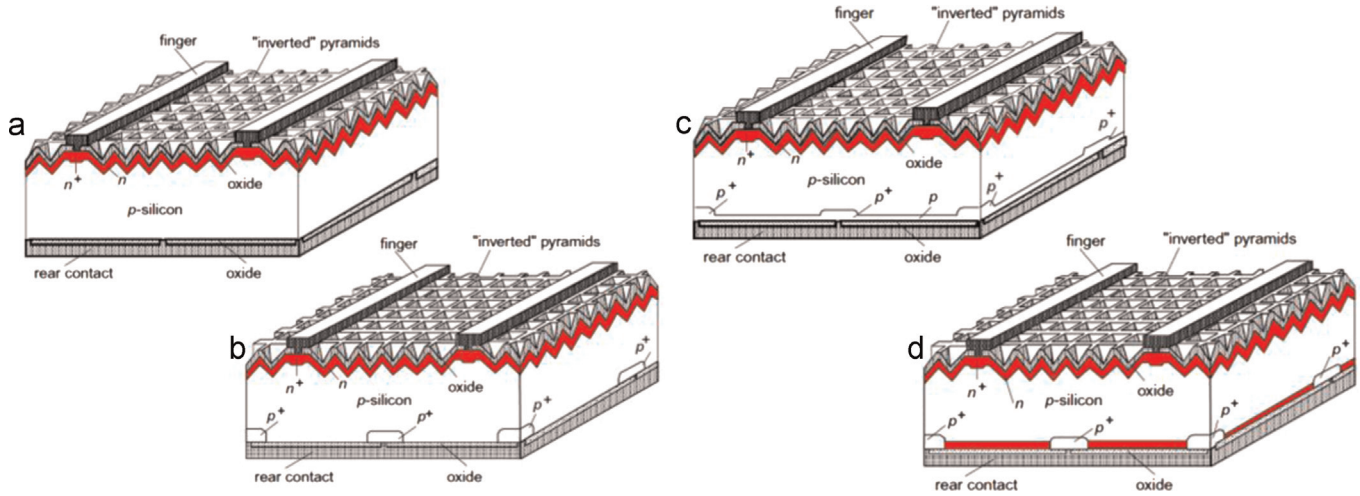

Fig. 8. The Passivated Emitter and Rear Cell (PERC) family. (a) Simple PERD cell (Passivated Emitter, Rear Directly-contacted); (b) PERL cell (Passivated Emitter, Rear Locally-doped); (c) PERT cell (Passivated Emitter, Rear Totally-diffused); (d) PERF cell (Passivated Emitter, Rear Floating-junction). The PERC configurations now most widely implemented are the PERL and PERT.

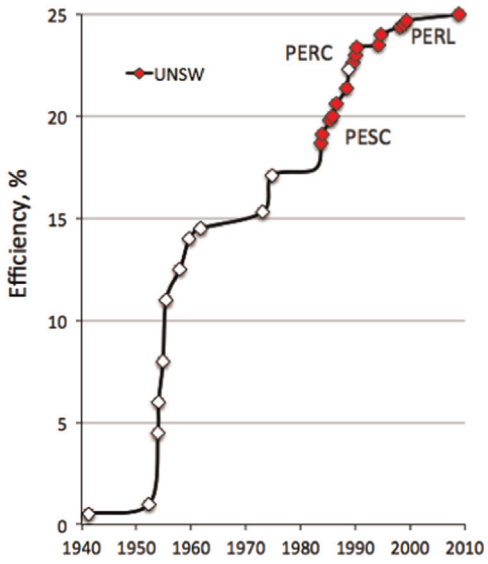

Fig. 9. Evolution of Si cell efficiency [5].

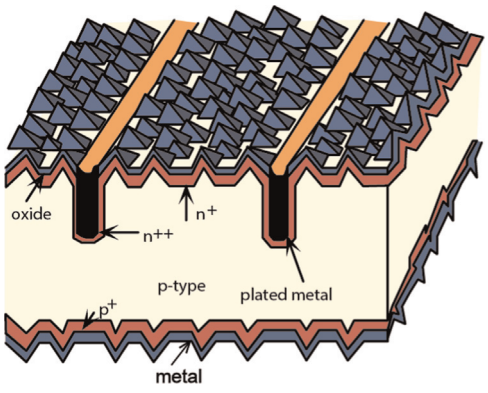

Fig. 10. Buried contact solar cell.

3. Large area cells and modules

UNSW had earlier pioneered the use of lasers in solar cell processing [21,22] with this resulting in the buried contact solar cell of Fig. 10 [23], developed as a commercial version of the PESC cell. These cells relied upon plated Ni/Cu metallisation, with excellent field performance from early modules deployed by licensee BP Solar recently reported after 20 years field exposure [24].

A pilot line was established at UNSW in the late 1980s to assist in transferring this technology to licensees. In 1990, this pilot line was diverted to the fabrication of large areas of cells for solar car racing, at that time attracting the interest of major automobile companies as a promotional vehicle. The 68 mm × 68 mm cells fabricated on this line used the "finger intensive" cell metallisation pattern of Fig. 11, made possible by the high conductivity and reduced width of the buried contacts.

Two laser-based processing approaches were investigated in the early 1990s as a way of integrating the new PERC rear structure into this laser-based sequence. One was to use the laser to ablate small openings in a rear oxide to provide the desired small area contact points, with Al subsequently deposited and sintered. This was the most successful in our work, producing cells with high V_{oc} and good fill factors [25]. The equivalent of this contacting approach is also the most widely used in present commercial PERC sequences. The second involved deposition of Al on top of the oxide and driving it through the oxide by laser heating at localised points. We found this approach to be more problematic, with difficulties attributed to the layer of phosphorus that wraps around to the rear during the top surface diffusion. Although it was possible to control the thermal environment during normal buried contact cell processing to prevent detrimental consequences from this layer [26], this was not possible in the transient laser-processing environment. Subsequently, this problem was resolved and the approached perfected at the Fraunhofer Institute [27], by the simple expedient of masking the rear during front surface diffusion.

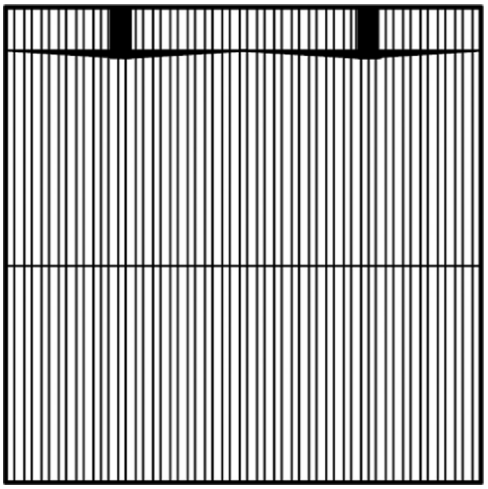

Fig. 11. Metallisation pattern used for 68 mm × 68 mm buried contact cells.

The lasers available both to us and to our licensees at that time were better suited to forming continuous grooves than dot or dash patterns when large cell quantities were involved. Buried contact cell work consequently took the direction of exploring bifacial rear grooved structures. PERC integration was achieved by a hybrid sequence, using laser processing for the top cell surface but chemical etching to open holes in the rear oxide, with hole positions defined by photolithography. This approach took hybrid, large area cell performance well above 20%. Sixteen of these early PERC hybrid cells were encapsulated into a nominally 800-cm^2 module in 1992 resulting in the first confirmed 20% flat-plate photovoltaic module efficiency (19.9% certified in 1992, equivalent to 20.1% under present standards). These results were improved upon in 1993 [28] by implementing an all-photolithographic PERC process that retained the metallisation pattern of Fig. 10, to allow the cells to be used interchangeably with previous pilot line output. About 5 kW of UNSW pilot line cells were supplied to 3 teams for the 1993 Solar World Challenge, the solar car race across Australia, including about 1 kW of PERC cells representing the first commercial PERC cell sales. For the 1996 race, a further 8 kW of PERC/PERL cells were supplied to 3 teams. Forty cells made during this period were encapsulated into a nominally 800-cm^2 module giving confirmed 22.7% module efficiency [29] (22.9% by present standards, still the highest for a silicon module at the time of writing).

4. Commercialisation

Since the mid-1980s, most manufacturers have used a common manufacturing process for fabricating silicon solar cells based on the use of phosphorus diffused, boron doped silicon wafers with screen-printed silver paste top contacts and rear contacts based on screen-printed Al pastes [30]. The latter are alloyed to form an "Al-BSF" under the rear contact. Multicrystalline wafers and plasma

deposited silicon nitride antireflection coatings have been used commercially from about the same time. Over recent years, the standard Al-BSF process accounted for over 90% of silicon solar cell production, itself accounting for over 90% of total photovoltaic module production. The remainder of the latter production is made up of thin-film technologies based on CdTe, CIGS (Copper–Indium–Gallium–Selenide), and amorphous silicon (a-Si), with slowly declining combined market share. By 2013, the performance of this dominant silicon Al-BSF technology had steadily improved to the stage where standard commercial cells were approaching the efficiency level reached by PESC cells in the laboratory in the 1980s using a similar rear Al-BSF approach. To progress further, a similar rear contact improvement was required.

Nothing is as powerful as an idea whose time has come. As the push to efficiencies above 20% in production intensified, many companies reported on progress with implementing PERC technology. Suntech Power was one of the first, reporting on such progress in production implementation in 2009 [31] as the company's "Pluto" product series. Generation 1 product incorporated a laser-based selective emitter process co-developed with UNSW with standard Al-BSF, reaching production volumes of 0.5 GW/year [32]. Generation 2 product incorporated PERC rear contacts, demonstrating 20.3% efficiency as independently confirmed in 2011 [32]. Schott Solar reported 18.7% efficiency using multicrystalline wafers and the PERC approach in 2010, resulting in a confirmed world-record 17.6% efficient module efficiency [33]. In 2012, Schott reported 21% monocrystalline silicon efficiency, the imminent release of a high-efficiency PERC cell module and licensing the company's version of PERC technology to equipment supplier Schmid. Q-Cells reported 19.5% multicrystalline PERC cell efficiency in 2011, increasing confirmed module efficiency to 17.8% and then 18.5% [34]. Trina Solar recently increased the multicrystalline cell efficiency to a world record 20.8% and corresponding module efficiency to 19.2%, again using PERC cells. Taiwanese company, Global Sunrise, founded by former UNSW researchers, was one of the first companies to report on actual PERC production experience. Working with equipment supplier, Roth and Rau, a PERC production process compatible with screen-printed pastes went into production in 2012, with average cell efficiency above 20% reported [35].

GTM Research documents subsequent activity in 2013 and 2014 [36]. Equipment suppliers Schmid, Centrotherm, RENA, Solaytec, Levitech, SINGULUS and Meyer Burger are mentioned as well as manufacturers Neo Solar Power, SunEdison, JA Solar and WINAICO. NDP Solarbuzz reported on the rapid rate of adoption of PERC into manufacturing [37], with 2.5 GW PERC capacity estimated worldwide in August, 2014, with this growing quickly (Fig. 12).

According to a separate NDP Solarbuzz report [38], the new PERC capacity additions shown in Fig. 12, accounted for a growing

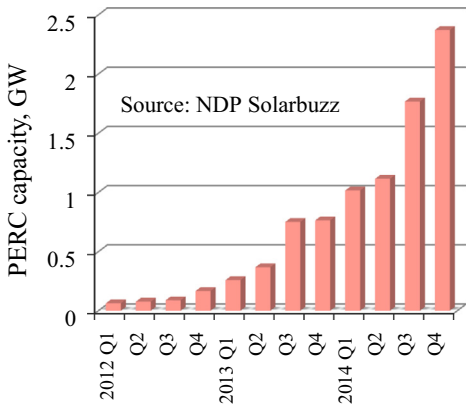

Fig. 12. Rapid increase in PERC manufacturing capacity (2012–2014) [37].

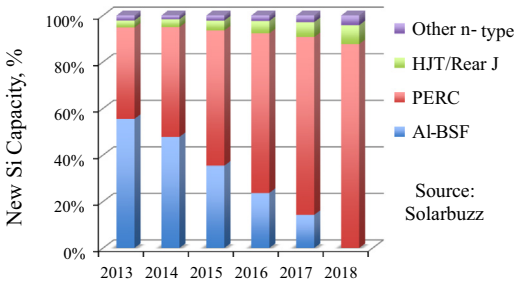

Fig. 13. Share of new silicon-based manufacturing capacity of different cell approaches [38].

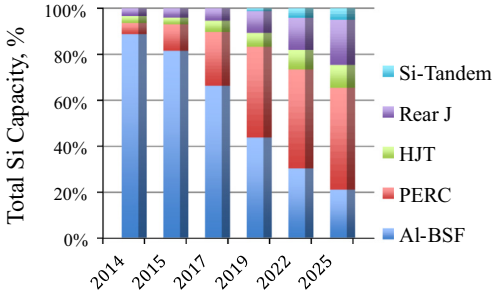

Fig. 14. Expected market share of different Si cell technologies [39].

share of total new capacity additions in 2013 and accounted for the majority of new additions by the second half of 2014 (Fig. 13). This displacement of the standard Al-BSF approach is expected to continue, with no new Al-BSF capacity expected to be added after 2017.

This view is reiterated in the independent April 2015 photovoltaic industry roadmap (ITRPV) [39]. As indicated in Fig. 14, the rapid growth of PERC production capacity in 2014 made PERC, after the standard Al-BSF technology, the cell technology with the second highest established production capacity by year-end (ahead of rear junction and HIT/HJT a-Si heterojunction silicon cells, as well as CdTe, CIGS and a-Si thin-film cells). Over the next few years, the dominance of new production capacity by PERC (Fig. 13) will steadily increase its share of total capacity with the most recent ITRPV roadmap [39] showing PERC likely to become the dominant cell production technology by 2020 (Fig. 14).

This trend is being accelerated by the consolidation policies of the Chinese government whereby manufacturers without access to good technology are being closed down by imposing cell efficiency standards [40].

5. Production sequences and costings

Although PERC manufacturing capacity is growing quickly, the technology is still early in its developmental cycle (Fig. 12) with far more differences between sequences in production than with the much better established Al-BSF approach. Nonetheless, the simplified process flow diagram for PERC cell fabrication, shown compared to the standard Al-BSF approach in Fig. 15, broadly captures the key features. As apparent from this figure, one attraction of the PERC sequence is that it is largely compatible with the standard Al-BSF sequence.

The first step in both cases is a wafer saw damage removal etch and texturing, followed by emitter diffusion and etch. Often, a rear side polish etch is included at this stage for the PERC sequence, to increase rear reflection and to reduce rear recombination [35,41]. This is a low-cost step since usually done in conjunction with the required edge-junction isolation step. Usually a few microns of

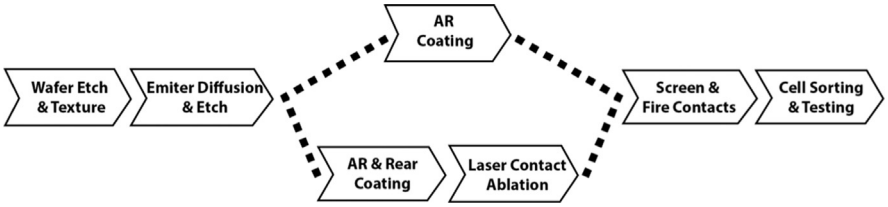

Fig. 15. Simplified process flow for Al-BSF (upper) and PERC (lower) sequences.

silicon are removed in this polishing step, with consequent energy conversion efficiency gains reported as in the 0.4% to 1.5% (absolute) range [42,43], depending on the details of the process.

Instead of a simple silicon nitride AR coating deposition as in the standard Al-BSF sequence, both AR and rear dielectric coating of the cell is required in the PERC process, with the rear coating generally taking the form of either an aluminium oxide/silicon nitride stack [35,44] or a silicon oxide/silicon nitride stack [45]. In some processes, both the front and the rear depositions are done in the same item of equipment [35]. The contact holes through the rear dielectric are generally formed by laser ablation, although chemical etching is feasible. Contact screening and printing, cell testing and sorting occurs similarly in both sequences, although different paste compositions would be used for the rear contact for PERC cells, to avoid damage to the rear dielectrics and void formation at the locally alloyed regions [43]. Voids arise from migration of some silicon through the rear Al layer away from the openings during alloying, never to return, although addition of silicon to the pastes can prevent this from becoming an issue.

To allow soldering of the rear, Ag solder pads also need to be screened to the rear side of the cell, as in the standard Al-BSF approach. This is reported as being less harmful to cell performance for PERC cells [46], since the area of high recombination velocity contact between the Ag layer and substrate is much smaller in this case, occurring only where there are openings in the rear dielectric. Contact between the pads and the Al rear metallisation areas occur through carefully controlled overlap regions [47].

Since at least three extra processing steps are involved, extra cell processing costs are involved for PERC cells. One early study [48] estimates the cell processing cost as 26% higher/cell, reducing to 20% higher/W when the rather low assumed 5.6% performance advantage is taken into account. At the cell level, with wafer costs included but similarly leveraged by the higher efficiency, the additional manufacturing cost is estimated at 6%/W. At the module level, the same leveraging reduces the additional cost to 2%/W. At the system level, PERC costs become marginally lower, in this study. A manufacturer of both PERC and Al-BSF devices considers a much higher 11% performance advantage as a reasonable estimate, with 90% of this advantage able to be captured as lower transport costs, 70% as lower installation costs and over 50% as lower balance of systems costs [49].

PERC cells are now available in sufficient quantities that at least one market research company tracks spot prices for PERC cells as a separate category [50]. In mid-March 2015, the company reported average spot prices for multicrystalline Al-BSF cells as 29.5–31.5 c/W, depending on efficiency with 17.8% efficiency providing a demarcation point, and 38.5 c/W for monocrystalline Al-BSF devices. PERC monocrystalline spot prices were reported as 46–48 c/W for cells of efficiency in the 20.4–20.6% range [50], corresponding to a 19–25% market premium that would seem to more than offset the increased processing costs.

With ongoing streamlining and standardisation of PERC sequences, the processing cost premium/cell relative to Al-BSF devices is expected to reduce [51]. At the same time, the performance advantage over Al-BSF cells might be expected to increase as the higher voltage capability of the PERC approach is fully exploited. In the laboratory, the performance of PESC devices, representative of a fully developed Al-BSF approach, peaked at just below 21% by present standards, while PERC/PERL sequences reached 25%, suggesting a 20% margin could eventually open up.

6. Performance potential

In mid-2015, the best performing near-commercial PERC multicrystalline cells have efficiencies in the 20–21% range, while the best PERC monocrystalline cells have slightly higher values in the 21–22% range. There were confident expectations for both values soon to surpass the top of these respective ranges, but how far can the technology go?

Several recent studies throw some light on this issue [52–55]. The most recent [55] shares the author's view that, now the industry has invested in a transition to PERC technology, this provides a path for manufacturers for incremental improvements to values of cell efficiency to close to the 25% value demonstrated in the laboratory. Commercial PERC cells still perform well short of the best laboratory devices in many ways, particularly in terms of V_{oc} as determined by total cell J_o (Eq. (1)) and resistive losses [56]. The 25% efficient PERL devices have a total J_o of only 50 fA/cm^2 while a typical 20–21% efficient commercial PERC cell may have a value over 300 fA/cm^2 with over half of this coming from the emitter region [53,55,56].

This makes attention to emitter design important for realizing the highest efficiencies in the near term. The 25% devices have a J_o contribution from this region of only 15 fA/cm^2 [56], showing what is ultimately feasible. Values below 80 fA/cm^2 are suggested as feasible for commercial devices in the near term using a selective emitter approach [53], as in the PERC cells of Fig. 8, although advanced homogeneous emitters are also regarded as an option [55]. Reducing emitter contributions to J_o will then bring the rear contact of the PERC cell into focus as the performance-limiting feature.

Attention to the surface recombination velocity along the non-contacted regions of the rear surface [52] as well as to the formation of the doped region in the contact areas [53,55] is expected to bring the rear surface contribution to J_o below that of the emitter, then elevating recombination in the bulk of the device to being the major contributor to J_o, determined by the combination of minority carrier lifetime and doping level in these regions. B-doped, p-type wafers presently dominate commercial production. A key advantage is the near-unity liquid to solid segregation coefficient of B that means its concentration remains reasonably constant along the manufactured ingots, whether mono- or multicrystalline. A disadvantage is that B forms a complex with O that is activated under illumination, restricting the bulk minority carrier lifetime in fielded devices [57–59].

For this reason, there have been suggestions that the industry needs to move as a whole to P-doped, n-type monocrystalline wafers, which is also a feasible substrate for high-performance PERC cells. Since P does not form such detrimental defects with O, this allows higher lifetimes in standard Czochralski (CZ) grown

ingots. Companies such as SunPower and Panasonic use n-type wafers to produce modules attracting premium prices for the high-efficiency end of the present market (double to triple those of standard product [60]). However, the lower P segregation coefficient means that there is a greater resistivity variation along the CZ ingot than with B.

To maintain tight production spreads and performance levels close to champion devices, some manufacturers are said to use as little as 35% of each P-doped ingot [61]. Using a greater portion of the ingot may be one reason for the large differences noted with other technologies, such as heterojunction devices, between champion and production devices. Going to continuous CZ growth provides an opportunity to reduce resistivity variations, but this may be self-defeating, since the longer growth times are likely not consistent with obtaining the desired highest possible carrier lifetimes [61]. In any case, P-doping does not appear suitable for the multicrystalline ingots that form the backbone of the present industry, due to this dopant segregation issue.

Given these issues and the present industry momentum, it seems likely that p-type wafers will remain the industry norm well into the future. If recently reported progress [57–59] with rapid and permanent deactivation of the B–O defect can be brought into production, millisecond bulk lifetimes might be a standard option using p-type CZ wafers. This corresponds to a bulk contribution to J_o of less than 40 fA/cm^2[53]. Alternatively, other p-type dopants such as Ga or In that do not form harmful defects with O could be used for monocrystalline material, while maintaining processing compatibility with B-doped multcrystalline material. Lifetimes in the latter material are rapidly improving, with recent reports of lifetimes of 0.4 ms averaged over a grown ingot [62].

With such improved bulk lifetime, the emitter region may then again require further refinement, putting another cycle of incremental improvements into effect. Resistive losses can be lowered towards those of laboratory devices by increasing the number of busbars, with a multi-wire approach suggested as the ultimate solution in this regard [55]. This allows contact by narrow plated top contacts, with 24.4% efficiency for a 156 mm by 156 mm cell predicted by detailed modelling by such continuous development of existing fabrication technology, leading to the conclusion that PERC cells will set a moving target and dominate the market for some time to come [55].

7. Conclusion

As manufacturers move past the 20% efficiency mark in production, the standard Al-BSF approach that has been the dominant commercial approach for the last 30 years is in the process of being surpassed by a fundamentally higher efficiency approach. Although high silicon cell efficiency has been obtained in production with both rear junction and heterojunction approaches, these require specialized high-quality, n-type monocrystalline wafers. The PERC cell approach has the advantage of being able to tolerate both monocrystalline and multicrystalline substrates of either polarity, while demonstrating similar efficiencies to the above approaches on good quality substrates.

This robustness and compatibility with existing product production lines is considered likely to see the approach surpass the standard approach by 2020 in terms of capacity share [39]. PERC uptake is likely to lead to an era of accelerated silicon solar cell performance increase as the full capabilities of this technology are exploited. Just as commercial solar cell efficiencies have approached the performance of the best laboratory Al-BSF solar cells, it is anticipated that the PERC technology will also approach that of the best laboratory cells with efficiency of 25% [5] through a process of on-going incremental improvements. Recent simulations confirm the feasibility of such efficiencies through the continuous development of existing technologies [55].

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