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Model based continuous improvement of industrial p-type PERC technology beyond 21% efficiency

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Abstract

In this work, we present our progress in the industrial p-type PERC technology [1, 2]. Based on device simulations we continuously develop an efficiency roadmap for a steady improvement of our PERC (passivated emitter and rear cell) process. Following this simulation based approach, we effectively improve the front side metallization and the emitter characteristics. Currently, our best prototype process has reached a conversion efficiency well over 21% which enables the manufacturing of a 60-cell based module with a power of 310W. Our best cell so far has a conversion efficiency of 21.5% which has been confirmed by the calibration laboratory of Fraunhofer ISE. This is to our knowledge the highest efficiency reported for industrial-size silicon solar cells with screen-printed metal front and rear contacts.

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Keywords: PERC; device simulations, continuous improvement

1. Roadmap

In recent publications we have developed methods to simulate the efficiency distribution for a cell concept under different scenarios with a combined statistical and TCAD model [3]. Based on this approach we derive the efficiency

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roadmap for our PERC technology (see Fig. 1). Starting from an average production efficiency of 20.2% we aim at continuously improving the manufacturing processes for front side metallization, emitter diffusion, passivation and rear contact formation. Regarding the module technology, the multi bus-bar design is assumed to be the main optimization step. With these optimization steps, we expect 22.5% efficient p-type solar cells with PERC technology available in the market within the next few years.

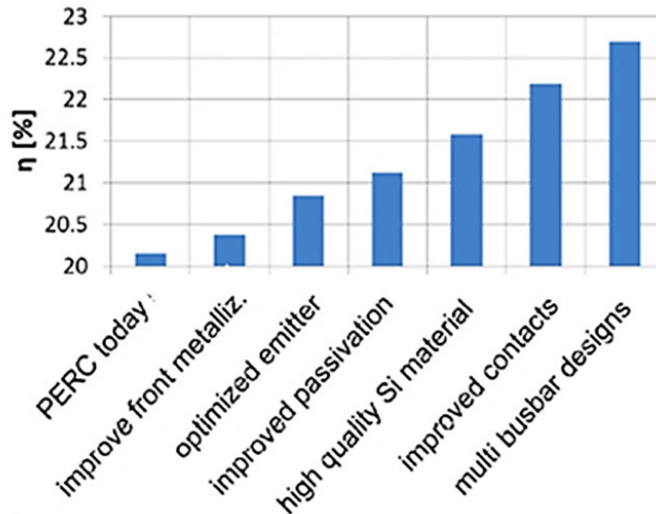


Fig. 1. Efficiency roadmap for our PERC technology; based on device simulations.

2. Technological optimizations

2.1. Front side metallization

According to our roadmap, the first step is the optimization of the front side metallization. We used standard single-print screen printing technology to circumvent the higher process complexity of double printing, hence busbars and fingers are printed within one squeegee stroke. The grid layout consisted of 90 fingers as well as 3 busbars with optimized design to reduce paste consumption and shadowing. Starting from 55 μm finger screen opening, we compare 49- μm to 45- μm finger openings for this investigation. Both groups consisted of about 50 solar cells each. The resulting grid lines and IV-data are displayed in Fig. 2 left and right, respectively. The smallest screen opening allowed for a fired gridline width of remarkable 48 μm . This leads to slightly higher J_{SC} due to reduced shading compared to the cells printed with the wider finger opening. However, the higher series resistance of the cells with lower finger width could not be compensated by the higher J_{SC} in this experiment, resulting in a slight efficiency drop of 0.04%abs. Improved pastes and screens are necessary to benefit from the lower finger opening.

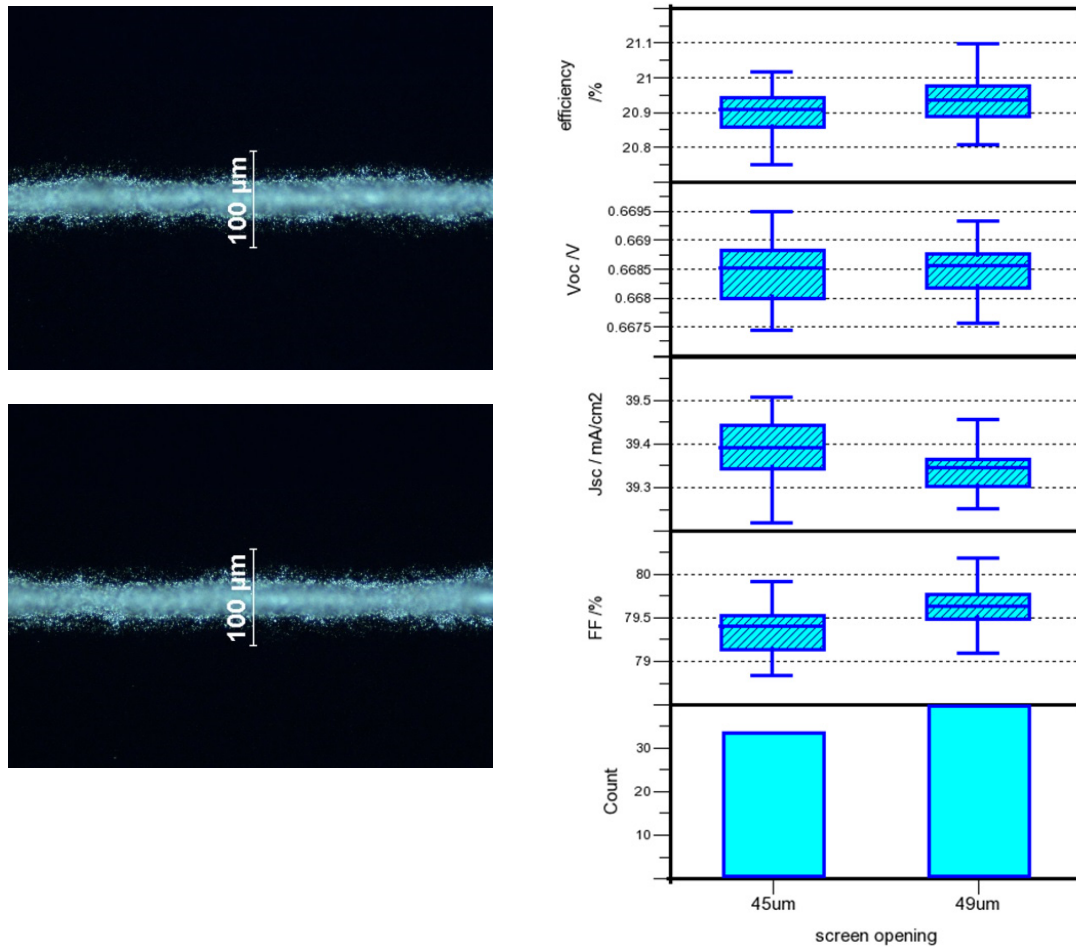


Fig. 2. Optical microscope images of the fine-line screen printed Ag grid lines measured after firing on completely processed PERC cells (left) and IV-data of the screen opening split experiment (right).

2.2. Emitter

The next important progress in our roadmap is a further emitter optimization. Thus, we have to balance the series resistance and the recombination losses. The well-known correlation between emitter sheet resistance $\rho_{\text{SH,em}}$ and emitter saturation current density J_{0e} can be modified by improved P-diffusion [4] and surface passivation. In Fig. 3 we compare different options for the emitter, including selectively versus directly contacted emitters and different front side passivation options.

For the determination of the emitter saturation current density J_{0e} high-ohmic Cz wafers are used which are textured, diffused and passivated identically on both sides and finally fired in a belt furnace. J_{0e} is derived using the procedure of Kane and Swanson [5] in combination with the quasi-steady state photoconductance (QSSPC) method [6]. For the evaluation the Richter Auger model and Band-gap narrowing (BGN) is used [7], i.e. the effective intrinsic carrier density depends on the boron doping concentration.

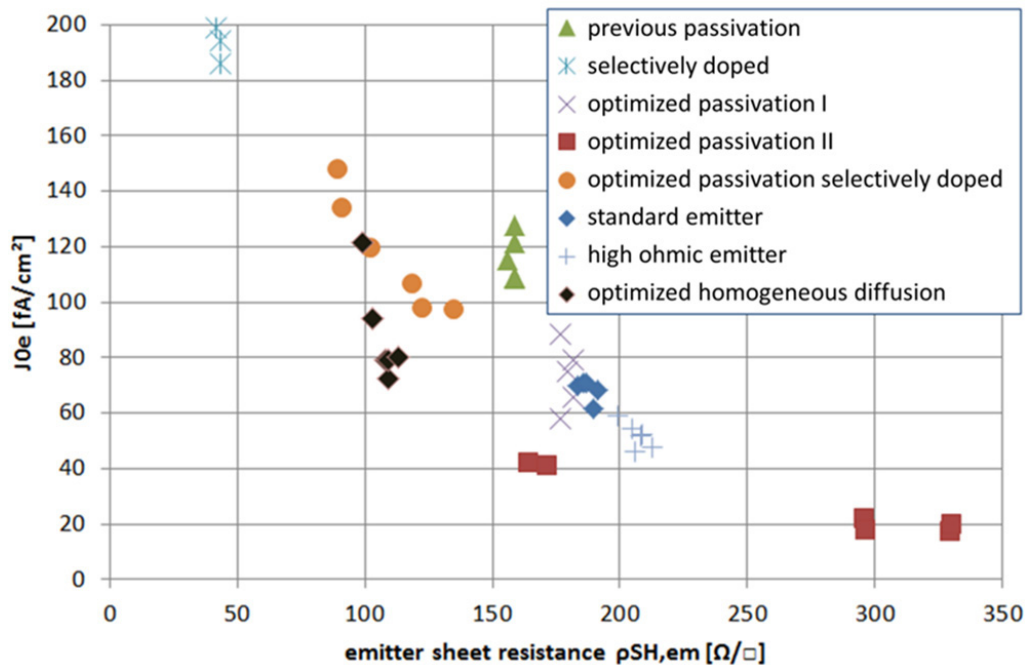


Fig. 3. Emitter sheet resistance $\rho_{SH,em}$ and emitter saturation current density (J_{0e}) for different P-diffusion and surface passivation processes. For the evaluation the Richter Auger model and Band-gap narrowing (BGN) is used [7].

3. Results

In order to demonstrate the potential of our improvements we implemented the above discussed optimizations.

Table 1. Experimental cell results of 200 wafer group production experiments and subsequent runs with module assembling.

Cell results	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	η (%)
Mean	671	39.3	80.1	21.12
St. Dev.	1.82	0.30	0.53	0.12
Median	671	39.3	80.1	21.14
Best Cell [‡]	671	39.7	80.9	21.51
60-cell based module*	V_{oc} (V)	I_{sc} (A)	FF (%)	P_{MPP} (W)
	40.06	9.91	78.1	310.2

[‡] independently measured by ISE CalLab

*independently confirmed by TÜV Rheinland

We used the standard wafer format of a 156.5x156.5 mm² p-type wafer with an as-cut thickness of 180 μm. Saw damage removal and texturing were done using alkaline solutions. The rear side passivation stack was adjusted in respect of low surface recombination velocity S_{rear} , high internal reflection and thermal stability. The rear contacts were implemented with a local BSF underneath. In terms of contacting the emitter and base we used standard screen printing technologies. We selected a 5 busbar design with the identified optimal 49 μm finger openings. The emitter

with optimized passivation II (see Fig. 3) and a selectively doped emitter (see Fig. 3) underneath the grid lines are used.

Currently our best median efficiency of a 200 wafer group processed in our clean room environment at Solarworld Innovations GmbH with the above discussed optimized processes has reached 21.1% with a very small standard deviation of only 0.12%abs (see Table 1). Our best cell has a conversion efficiency of 21.51% which has been independently measured at the Fraunhofer ISE calibration laboratory. This is to our knowledge the highest efficiency reported so far for industrial-size silicon solar cells with screen printed metal front and rear contacts.

For the module assembly we chose a half cell design to have lower resistance losses due to the higher voltage and lower current flow [8]. Therefore, first a laser carves the cell in the middle. Subsequently the cells are broken in half. This cutting process has only a very minor impact on the cell performance due to a slightly increased edge recombination. The module demonstrates independently confirmed 310Wp with a module conversion efficiency of 19.4%.

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