

An industrially viable TOPCon structure with both ultra-thin SiO_x and n^+ -poly-Si processed by PECVD for p-type c-Si solar cells

Tian Gao^{a,b}, Qing Yang^{b,d}, Xueqi Guo^b, Yuqing Huang^b, Zhi Zhang^b, Zhixue Wang^b, Mingdun Liao^b, Chunhui Shou^c, Yuheng Zeng^{b,*}, Baojie Yan^{a,b}, Guofu Hou^a, Xiaodan Zhang^a, Ying Zhao^{a,***}, Jichun Ye^{b,***}

^a Institute of Photo-electronic Thin Film Devices and Technology, Nankai University, Tianjin, 300350, PR China

^b Ningbo Institute of Material Technology and Engineering, Chinese Academy of Sciences, Ningbo, 315201, PR China

^c Zhejiang Energy Group R&D, Hangzhou, 310003, PR China

^d University of Chinese Academy of Sciences, Beijing, 100049, PR China



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ABSTRACT

We report an industrial compatible tunnel oxide passivated contact (TOPCon) structure on solar-grade p-type c-Si wafer as the rear emitter for high-efficiency solar cells, where the ultrathin silicon oxide (SiO_x) is made by plasma-assisted oxidation and the P-doped n-type poly-Si (n^+ -poly-Si) contact layer by plasma-enhanced chemical vapor deposition (PECVD) of hydrogenated amorphous silicon (a-Si:H) with in-situ doping with PH_3 and following the high-temperature annealing. The fabrication processes of SiO_x and n^+ -poly-Si layers are systematically optimized. It is found that the optimized annealing temperature for the crystallization and dopant activation is in the range of 850 °C and 880 °C, which is higher than the similar structure with chemically oxidized SiO_x (820 °C). In addition, the samples made with higher PH_3/SiH_4 doping ratio during the a-Si:H deposition need a lower annealing temperature to reach the similar dopant distribution within the samples made with lower doping ratio but annealed at higher temperature, it means that the optimized annealing temperature decreases with the increase of the PH_3/SiH_4 doping ratio during the deposition of a-Si:H precursor. The optimized process with post-hydrogenation yields excellent surface passivation on the p-type Si substrate with the implied open-circuit voltage (iV_{oc}) of ~742 mV, the single-side saturated recombination current density (J_0) of ~3.0 fA/cm², the contact resistivity (ρ_c) of ~2–4 mΩ cm², and the effective minority carrier lifetime (τ_{eff}) of ~1050 μs ($\Delta n = 1 \times 10^{15} \text{ cm}^{-3}$). With these passivation parameters, a simulation study demonstrates the advantage of rear emitter over the conventional front emitter TOPCon solar cell with ~22.8% achievable efficiency on solar-grade p-type wafers with current industrial constraints, and ~24.9% on high quality p-type c-Si wafers with the optimized conditions in R&D laboratories. Our study suggests that the p-type c-Si solar cell with a rear n^+ -poly-Si TOPCon emitter is a viable structure for high-efficiency solar cell production.

1. Introduction

Crystalline silicon (c-Si) solar cell technology has dominated the photovoltaic (PV) industry with high energy conversion efficiency, low cost, and well-developed manufacturing process. The cell and module efficiencies have been improved steadily with new cell structures and advanced fabrication technologies incorporated. The current mainstream high-efficiency c-Si PV technology is based on the passivated emitter and rear cell (PERC) technology, which was developed in the

late 80's with an efficiency of 22.8% [1] and achieved a record efficiency of 25% with the passivated emitter and rear local contact (PERL) [2]. In recent years, the PERC cell structures have been incorporated in c-Si solar panel production with the cell product efficiency in the order of 21.5–22.0%. The major improvement of PERC cell over the traditional aluminum back surface field (Al-BSF) structure is the separation of the semiconductor and metal contact by an insulating dielectric passivation layer, which avoids the high recombination at the Si and metal interface. However, in order to allow the current flow from the

* Corresponding author.

** Corresponding author.

*** Corresponding author.

E-mail addresses: yuhengzeng@nimte.ac.cn (Y. Zeng), zhaoygds@nankai.ac.cn (Y. Zhao), jichun.ye@nimte.ac.cn (J. Ye).

cell, localized back contacts are normally formed by opening the passivation layer with laser ablation, where the carriers have to transport to laterally, and the high recombination still occurs. To eliminate these two limiting factors, full area carrier selective contact has been developed with two successful cell structures of hydrogenated amorphous silicon (a-Si:H) and c-Si heterojunction solar cell (abbreviated as HIT after Heterojunction with thin Intrinsic a-Si:H Tunnel layer) [3–6] and Tunnel Oxide Passivated Contact (TOPCon) solar cells [7–11]. The HIT solar cell has been well developed with a record efficiency of 25.1% [4] alone and 26.7% [5,6] with HIT plus Interdigitated Back Contact (IBC). On the other hand, the TOPCon solar cell has demonstrated record efficiency of 25.7% without IBC structure [11] on n-type FZ c-Si and 26.1% with a similar structure called poly-Si on passivating interfacial Oxides (POLO) plus IBC on p-type c-Si wafer [12].

The advantages of TOPCon solar cells include 1) the compatible fabrication process with the well-developed PERC lines such as the high-temperature firing process for the metal contact and front passivation and anti-reflection coatings, 2) the full area contact avoiding lateral carrier transport for high fill factor (FF), 3) no laser opening requirement for cost reduction, and 4) a wide process window with less restriction for the thin film a-Si:H precursor layer made by low-pressure chemical vapor deposition (LPCVD) [13–16], plasma-enhanced chemical vapor deposition (PECVD) [6,8–11,17–20], and even sputtering [21]. In the literature, most of the TOPCon works have been made with high quality n-type c-Si wafer with a conventional B diffused emitter in the front and an ultrathin SiO_x plus a P-doped n-type poly-Si rear contact layer, for which the high bulk minority carrier lifetime ensures the high cell efficiency potential; while limited attempts have been made with p-type c-Si wafers [17,21,22] because of the lower bulk carrier lifetime, and the poorer interface passivation with B-doped poly-Si TOPCon structure. However, from solar module mass production's point of view, a much higher demanding is for making TOPCon solar cells on p-type c-Si wafers than on n-type c-Si wafers since the lower wafer price and well-developed solar cell fabrication process with p-type c-Si wafers. For this purpose, the developing of viable industrial TOPCon solar cell technology on p-type c-Si wafers has obtained some attention, and great efforts have been made to resolve these issues [23,24]. For example, Krügener et al. [23] have improved carrier lifetime by impurity gettering. Therefore, along this line, the first objective of this paper is to develop a TOPCon cell structure and fabrication process with solar grade p-type c-Si wafers to promote the TOPCon technology to close to industrial viability.

The ultrathin SiO_x tunnel passivation layer is one of the critical elements for TOPCon solar cells. The reported methods for the SiO_x preparation include the chemical oxidation with nitric acid at high temperature of ~90–110 °C [8–11,25–27] or mixed sulfuric and nitric acids at relatively low temperature of ~60 °C [28], thermal oxidization at elevated temperature of ~600–700 °C [27], H₂O₂ oxidization [16], ozone oxidization [29], and plasma-assisted oxidation with N₂O plasma [30,31]. Although the solution based acidic oxidation has been proven to produce high-quality SiO_x with a very well controlled thickness of ~1.5 nm, the high concentration acid at high temperature might require a very high-level environmental measure. From manufacturing friendly point of view, thermal oxidization, ozone oxidization, and PECVD assisted oxidation are the promising technologies. Especially, the plasma-assisted oxidation can be intergraded with the a-Si:H deposition into one machine, and therefore it becomes a logical selection for TOPCon solar cell production, which adds a second feature to

promote the industrial viability with a reduced manufacturing cost and complicity.

In this paper, we systematically studied the TOPCon structure on the solar-grade p-type c-Si wafers, where the ultrathin SiO_x layer was made using plasma-assisted oxidization with N₂O gas and the P-doped ploy-Si (n⁺-poly-Si) contact layer using PECVD deposition of a-Si:H with in-situ PH₃ doping following the high-temperature annealing. The required properties, including the effective minority carrier lifetime (τ_{eff}), implied open circuit voltage (iV_{oc}), single-side recombination current density (J_0) [32,33], and contact resistivity (ρ_c), for high-efficiency solar cell were studied as a function of a fabrication process. In addition, the material structural properties and dopant distribution were also measured by the 325-nm UV-Raman spectroscopy [34] and electrochemical capacitance-voltage (ECV) technique, respectively. With the optimized process conditions, high-quality passivation and low contact resistance have been achieved with iV_{oc} of ~730 mV, J_0 of 4.1 fA/cm², τ_{eff} of ~800 μs ($\Delta n = 1 \times 10^{15} \text{ cm}^{-3}$), and ρ_c of ~3.8 mΩ cm². With the Al₂O₃-capping post-hydrogenation process, the passivation quality is improved further with the iV_{oc} of ~742 mV, J_0 of 3.0 fA/cm², and τ of ~1050 μs ($\Delta n = 1 \times 10^{15} \text{ cm}^{-3}$). These parameters satisfy the high-efficiency solar cells with the p-type c-Si substrate. To prove this, we did a simulation using Quokka 2 [35–38] with the obtained passivation parameters and showed an efficiency of ~22.8% using the TOPCon as the rear emitter, which has a higher efficiency than the front P-diffused emitter and rear B-doped poly-Si TOPCon contact structure on the solar grade or high-quality p-type c-Si wafers by ~0.4%. Our studies demonstrate that the p-type c-Si solar cell with a rear TOPCon emitter is a viable technology for the low-cost high-efficiency solar module production.

2. Experimental details

Solar-grade p-type Czochralski (CZ) c-Si wafers (156 × 156 cm²) with <100> crystal orientation, 1–3 Ω cm resistivity, and 170 μm thickness are used for the passivation study. The substrates were cut into 4 × 4 cm², etched by KOH solution to remove the saw damage, cleaned using the standard RCA procedure, and then immersed in the 5% HF solution for 2 min to remove the native oxide layer before loading into the PECVD system. An ultrathin SiO_x layer was created on both sides in an N₂O plasma for 10 min in the PECVD (13.56 MHz) system. Following, a P-doped a-Si:H layer was deposited on both sides as well in the same PECVD chamber with SiH₄, H₂, and PH₃ as the process gases with the deposition parameters listed in Table 1. The SiO_x and a-Si:H layer thicknesses were obtained by spectroscopic ellipsometry from the samples deposited on polished c-Si wafers. The oxidation and deposition processes were optimized for high-quality passivation with no peeling off or bubbling after the high-temperature crystallization. An annealing process was carried out at an elevated temperature between 780 °C and 920 °C in a diffusion furnace for 30 min with the high-purity nitrogen atmosphere. After that, post-crystallization annealing in an annealing furnace with forming gas (FGA) was implemented for 30 min at 450 °C. Also, the post-hydrogenation with the atomic-layer-deposited (ALD) Al₂O₃ capping and the annealing at 400 °C was also carried out for the further improvement of surface passivation.

The schematic structure of the double-sided symmetrically passivated sample is shown in Fig. 1(a). The passivation quality was measured using the quasi-steady-state photoconductivity (QSSPC) method

Table 1

The PECVD process parameters for the SiO_x fabrication and P doped a-Si:H deposition. The PH₃ is 2% diluted in H₂.

Layer	T (°C)	Pressure (Torr)	Power (W)	N ₂ O (sccm)	SiH ₄ (sccm)	H ₂ (sccm)	PH ₃ (sccm)
SiO _x	150	0.8	5	20	–	–	–
n ⁺ -a-Si:H	200	0.8	6	–	2.5	5	1.5/3.0/4.5

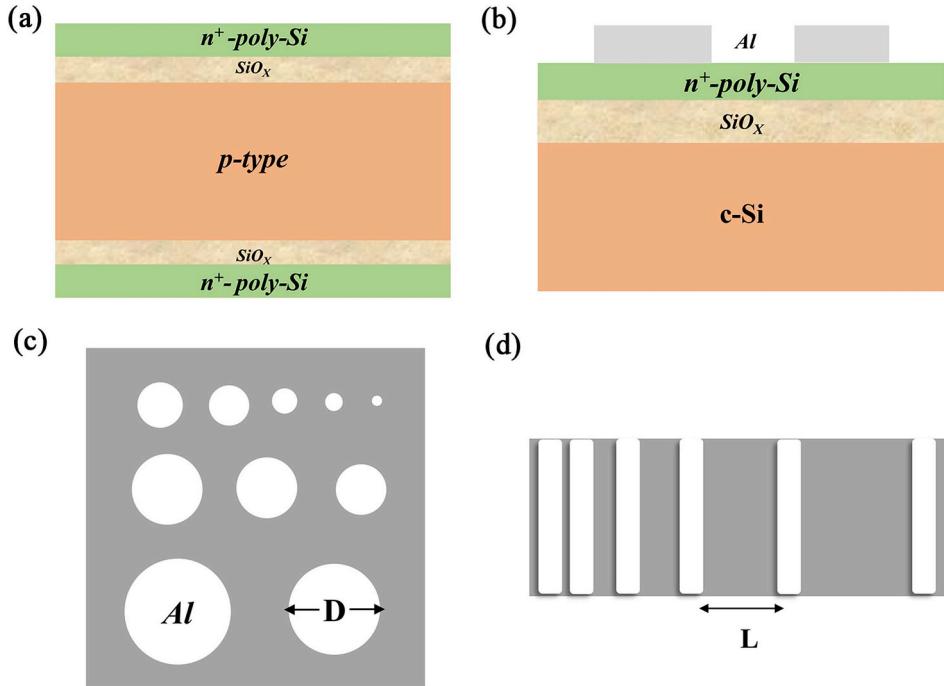


Fig. 1. Schematics of (a) the double-sided passivated sample for passivation quality measurement, and (b) the cross-sectional view of the single-side passivated samples for contact resistivity measurements, (c) and (d) top views of the Al contacts for contact resistivity measurements with the CS and TLM methods, respectively.

(Sinton-WCT-120). The same layer structure was also fabricated on one side of the substrates with Al contacts with various gap distances on it for contact resistivity measurement using the transmission line method (TLM) as shown in Fig. 1(b). In addition, the n-TOPCon structures were also made on n-type *c*-Si wafers, and circular Al electrodes with various diameters were deposited on the top surface to measure the contact resistivity using the Cox-Strack (CS) method. Although the SiO_x is very thin, the 40-nm thick poly-Si and the thick Al electrodes ensure no spike through the TOPCon structure by the probe during the contact resistivity measurements. An ECV (Buchanan, CVP21) system was used to measure the doping concentration profiles of the annealed samples. The crystalline structure after annealing at different temperatures was characterized by UV-Raman spectroscopy with the 325-nm laser as the excitation to avoid the contribution from the substrate [34]. Also, we used Quokka 2 for the device simulation and the OPAL2 [39] for the optical simulation. According to OPAL2, the generation current density in the substrates are 41.51 and 41.44 mA/cm² in the B-doped TOPCon rear-BSF, and P-doped TOPCon rear-emitter solar cells, respectively.

3. Results and discussion

The optimization of the ultrathin SiO_x process by the plasma-assisted oxidation has been made by Huang et al. [31] on n-type *c*-Si wafers. It has been found that the N_2O plasma oxidized SiO_x also have a self-controlled thickness limitation as observed in the acidic oxidation [29]. The saturated thickness depends on the process parameters such as substrate temperature and RF power. By tuning the process conditions, one can obtain the desired thickness for the TOPCon structure. Here we used the same deposition process to prepare the ultrathin SiO_x and P-doped a-Si:H precursor layers with the main focus on the optimization of annealing process for high-quality passivation, in which the SiO_x thickness is ~ 2 nm as estimated from spectroscopic ellipsometry measurements and the a-Si:H thickness of ~ 40 nm as controlled by the deposition rate and time. Fig. 2 shows the passivation results from three sets of samples with different doping-gas (PH_3 , 2% diluted in H_2) flow rates, from which three observations are found. First, the passivation quality increases as the annealing temperature increase before reaching

the optimized passivation conditions (the highest iV_{oc}) and then it declines as the temperature increases further; second, the optimized annealing temperature increases with the decrease of doping gas flow rate; and third, the highest iV_{oc} achieved in each set of samples decreases with the increase of doping gas flow rate. The best passivation was obtained with the samples made with the PH_3 flow rate of 1.5 sccm and annealed at 880 °C, under which the $iV_{oc} = 730$ mV, $J_0 = 4.1$ fA/cm², and $\tau_{eff} = 800$ μ s ($\Delta n = 1 \times 10^{15}$ cm⁻³, the injection level close to the condition under AM1.5 illumination) were achieved. After the deposition of Al_2O_3 capping layer on both sides by the ALD and the annealing at 400 °C, the best passivation effect reaches to the $iV_{oc} = 742$ mV, J_0 of 3.0 fA/cm², and τ_{eff} of ~ 1050 μ s ($\Delta n = 1 \times 10^{15}$ cm⁻³). Noted that, the iodine-passivated *p*-type Si wafers only display the typical τ_{eff} of approximate 100–200 μ s, much lower than those of the P-doped TOPCon passivated *p*-type wafers. The employment of P-doped TOPCon is helpful to improve the wafer effective lifetime significant, which would be critical for raising the efficiency.

Several factors affect the passivation quality, including the crystalline structure of the n^+ -poly-Si, the dopant diffusion passing through the SiO_x and dopant profile in the *c*-Si bulk, the chemical bond structures in the SiO_x , and the interface-states density (D_{it}) at the SiO_x /*c*-Si interface. Here, we first investigated the crystalline structure of the poly-Si layers annealed at different temperatures using the 325-nm UV-Raman spectroscopy to study if the crystalline structure affects the passivation quality. As previously reported [34], the UV-Raman probes the top poly-Si layer only with little influence from the *c*-Si substrate, and it not only provides the crystalline structural information by analyzing the Si TO mode at ~ 470 –520 cm⁻¹, but also yields the Si–O bond information in the wave number range from 700 to 1100 cm⁻¹. Fig. 3 shows the UV-Raman spectra of (a) the Si TO mode and (b) the Si–O related modes. The results indicate that the a-Si:H layers are fully crystallized and the crystallinity of all the samples are the same within the experimental errors, implying that the crystalline structure is not the critical factor affecting the passivation quality in the experimental conditions. However, the UV-Raman does not provide the crystal orientations and grain sizes, especially for large crystallites, therefore,

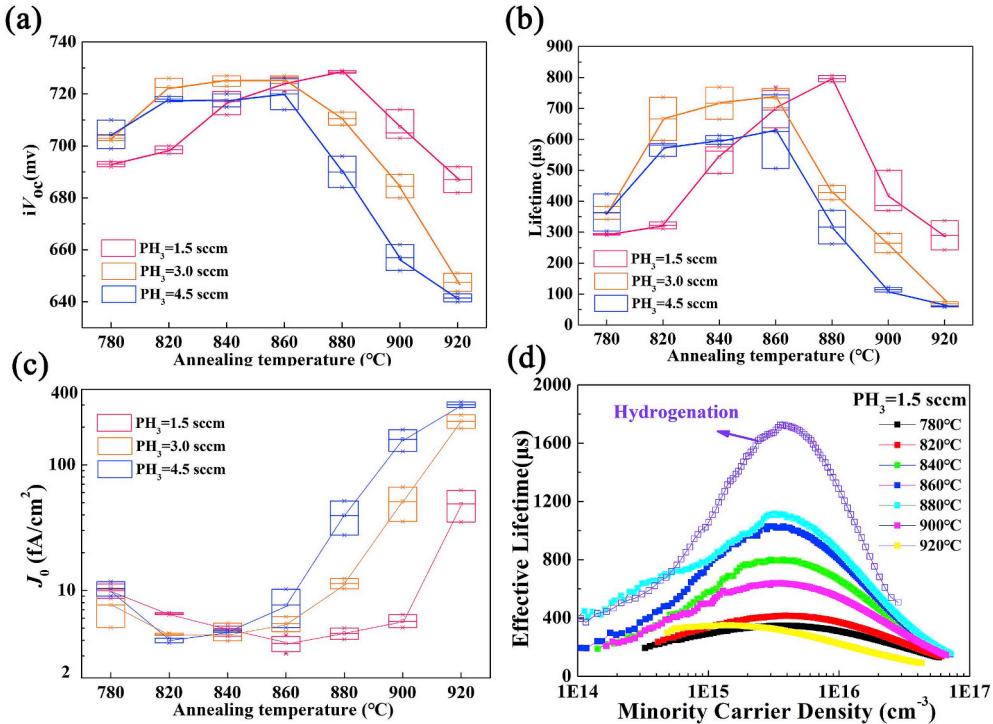


Fig. 2. (a) iV_{oc} , (b) τ_{eff} ($\Delta n = 1 \times 10^{15} cm^{-3}$), (c) J_0 of three sets of samples with different PH_3 flow rates for different annealing temperatures. (d) Injection-dependent effective minority carrier lifetime of the samples with the PH_3 flow rate of 1.5 sccm including the best passivation after the post-hydrogenation.

detailed characterizations on the poly-Si layers such as high-resolution transmission electron microscopy (TEM) may be needed to reveal the influence of crystalline structure on the passivation quality, which is beyond the scope of this work. Two peaks are observed at $800 cm^{-1}$ and $975 cm^{-1}$ in Fig. 2(b), which could be from the native SiO_x on the poly-Si surface and the ultra-thin SiO_x passivation layer, respectively, as discussed in our previous publication [34]. Note that all of the samples have the same Si-O related spectrum within the measurement noise, and therefore we might conclude that the Si-O bond structures have no change or the same change during the annealing at the examined temperature ranging from $780 ^{\circ}C$ to $920 ^{\circ}C$, or if any difference in changes, it is below the UV-Raman detect limit. Although no detectable changes in the Si-O bonding configurations are observed by the UV-Raman spectroscopy, the annealing at different temperatures might cause other changes such as the pinhole formation and dopant diffusion as shown in the following.

The dopant diffusion is another potential factor determining the passivation quality [40,41]. It has been reported that a proper dopant diffusion through the SiO_x and getting into the c-Si benefits to the passivation by pushing the junction moving away from the SiO_x /c-Si interface and avoiding the recombination at the SiO_x /c-Si interface

where a high density of interface defects might exist. However, too much dopant diffusion might lead to an increased Auger recombination [42] and decrease the passivation quality. Fig. 4 plots the active P-dopant profiles in the samples prepared with various conditions, where (a) is for the samples with the same PH_3 flow rate of 1.5 sccm but annealed at different temperatures and (b) for the samples with different PH_3 flow rates but annealed at the two temperatures of $780 ^{\circ}C$ and $880 ^{\circ}C$. It is observed from Fig. 4(a) that the P concentration drops sharply at the SiO_x position with limited diffusion tail into the c-Si when the annealing temperature is relatively low such as $780 ^{\circ}C$ and $820 ^{\circ}C$; a diffusion tail forms gradually as the annealing temperature increases; and the tail gets longer as the annealing temperature gets higher and eventually it penetrates the bulk of the c-Si substrate. It is further observed from Fig. 4(b) that at the relatively low annealing temperature ($780 ^{\circ}C$) the dopant profiles are very close to each other, indicating a weak concentration dependence with the speculation of the effective barrier formed by the SiO_x for P diffusion. However, at a relatively high temperature of $880 ^{\circ}C$, the P profiles show a strong PH_3 flow rate dependence as the higher the PH_3 flow rate, the deeper the diffusion tail gets into the c-Si wafer. By comparing with the passivation quality results as shown in Fig. 2, we conclude that the diffusion tail of

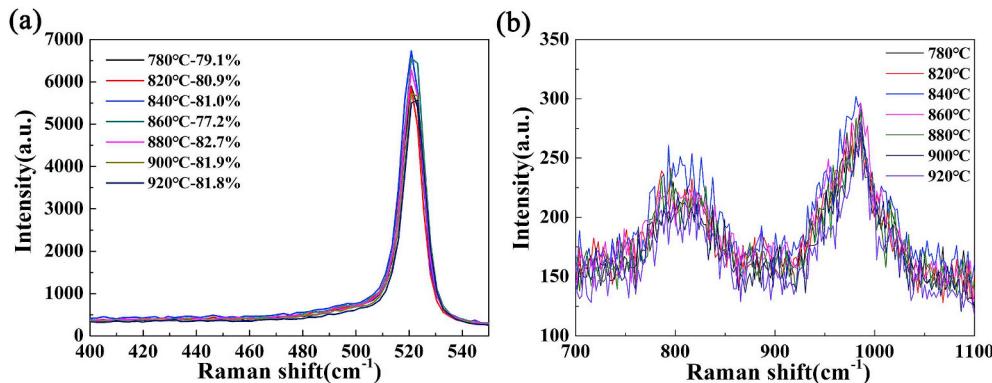


Fig. 3. The 325-nm UV-Raman spectra of (a) Si-Si TO vibration mode and (b) Si-O related modes of the poly-silicon thin films of the lifetime sample with the PH_3 flow rate of 1.5 sccm. The percentages in the plot (a) represent the crystalline volume fraction estimated by fitting the Raman spectra using Gaussian distributions of a-Si and c-Si components. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

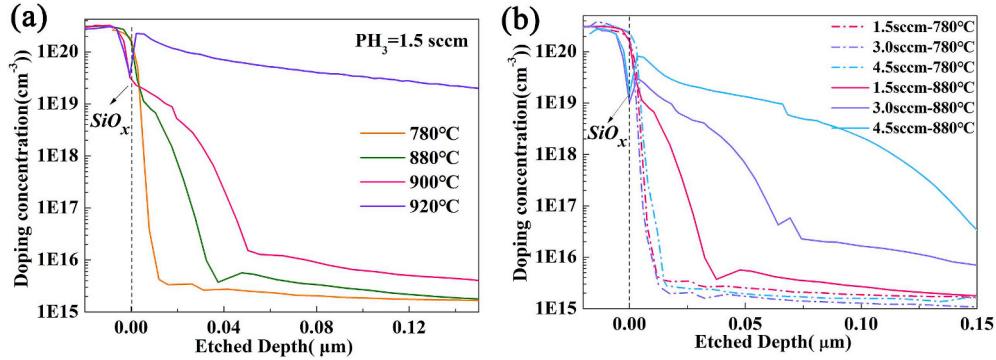


Fig. 4. Dopant distribution profiles for samples (a) annealed at different temperatures with the same PH_3 flow rate of 1.5 sccm, and (b) with different PH_3 flows but at the same annealing temperature of 780 °C and 880 °C.

~30–40 nm could be preferred for the effective passivation. Within the same structure such as the same SiO_x on the same c-Si wafer, the diffusion profile is determined by the annealing conditions such as the temperature and time, as well as the concentration of the dopants in the a-Si:H precursor. A higher dopant concentration needs a lower annealing temperature for reaching the similar dopant distribution in the c-Si wafer.

For high efficiency c-Si solar cells, except for the passivation quality, the contact resistivity is another critical parameter influencing the solar cell performance [43–45]. Two methods have been used for the contact resistivity measurement, namely the transmission line method (TLM) [43] and Cox-Strack (CS) [44] methods. The CS method measures the current flow through the whole layer structure vertically and suitable for a structure of Ohmic contact in all the interface; while the TLM method measures the current flow in parallel with the surface and suitable for the situation where a non-Ohmic contact in some interface outside the region of the metal contact and layer where the majority carrier passing through. Since we study a P-doped TOPCon on the p-type c-Si wafer, which forms a p/n junction and the current-voltage follows the diode characteristics and therefore the CS method is not suitable for the contact resistivity measurements, while the conductivity of the n^+ -poly-Si layer is high enough allowing the current flows mainly in the n^+ -poly-Si layer, and therefore the contact resistivity between the metal and the n -type ploy-Si can be properly measured using the TLM method on the sample structure as shown in Fig. 1(b). An example of measurements is shown in Fig. 5, where (a) plots the current-voltage characteristic (I-V) for the samples with the same doping rate ($\text{PH}_3 = 1.5 \text{ sccm}$) during the a-Si:H deposition and annealed at various temperatures. The sample prior annealing shows a non-linear characteristic, implying a Schottky junction formed by Al and n-a-Si:H; while the annealed samples all have the Ohmic characteristics, which could result from the narrowed barrier by the

activation of the dopants such that the carriers could tunnel through as if no barrier exists. The line slope in Fig. 5(a) increases with the increase of the annealing temperature, which means a decrease of contact resistivity as shown in Fig. 5(b). It notes that the contact resistivity of the sample annealed at 780 °C is high with a value of $\sim 14.1 \text{ m}\Omega \text{ cm}^2$, decreases sharply with increasing the annealing temperature, and reaches to $\sim 0.7 \text{ m}\Omega \text{ cm}^2$ at the annealing temperature of 920 °C. For the samples with good passivation quality such as the ones with $\text{PH}_3 = 1.5 \text{ sccm}$ and annealed at 880 °C, the contact resistivity is $\sim 3.8 \text{ m}\Omega \text{ cm}^2$, which satisfies the requirement for high efficiency solar cells. However, as the current mainly flows through the poly-Si layer in the TLM structure, but does not go through the SiO_x layer, the measured contact resistivity by the TLM reflects only the contact resistivity between the metal contact and the poly-Si layer. However, carrier transport through the SiO_x layer is important for determining the cell performance. If one makes the assumption that the carrier transport across the SiO_x layer is not affected by the underneath c-Si layer, one could examine the current flow through the SiO_x layer by measuring the contact resistance of n-TOPCon on n-type c-Si wafer using the CS method. In this case, the measured resistivity includes the contact resistivity between the metal and ploy-Si as well as the poly-Si and the c-Si wafer across the SiO_x . Under this assumption, we did the measurements by making a separate sister set of n-TOPCon structures on n-type c-Si wafers and measured the contact resistivity using the CS method as also plotted in Fig. 5(b). It shows that the contact resistivity measured by the CS method is higher than those measured by the TLM and it also decreases with the increase of annealing temperature. With a simple mind thinking, the difference between the two measurements gives the contact resistivity across the SiO_x layer. From these results, we may conclude that the contact resistivity of the n-TOPCon on the p-type c-Si wafers in this study is low enough for high-efficiency TOPCon solar cells even we used a relatively thick SiO_x ($\sim 2.0 \text{ nm}$) layer. As studied in

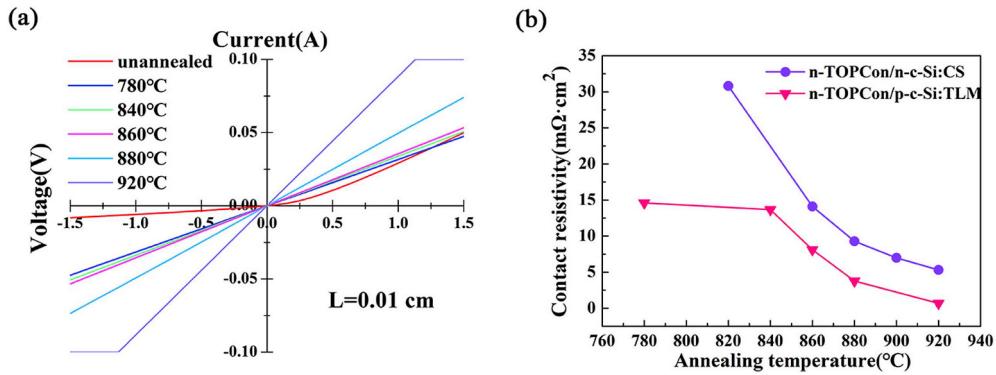
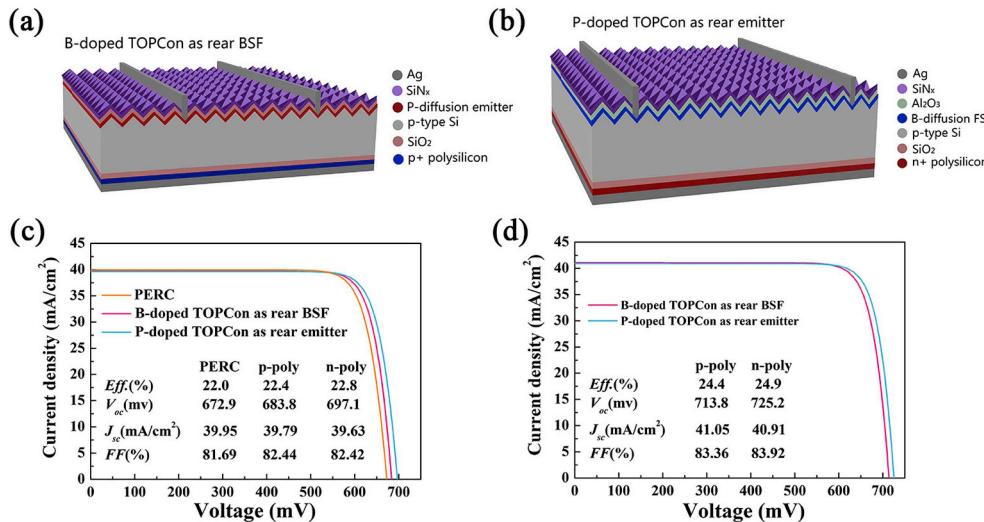


Fig. 5. (a) I-V characteristics for the contact resistivity (ρ_c) measurements with the finger distance of 0.01 cm in the TLM configuration, (b) ρ_c values obtained using both the CS and TLM methods as a function of the annealing temperature.



the literature, the current flow through the TOPCon structure could be by the quantum tunneling and directly through pinholes [19,46–48]. In the current situation, we speculate that the transport through pinholes is the dominant mechanism and the higher optimized annealing temperature than the TOPCon structure with thinner SiO_x layer fabricated by nitric or mixed acids [28] could be related to the breaking down for the thicker SiO_x at a higher temperature. To confirm this speculation, more detailed studies such as cross-sectional transition electron microscopy are in progress.

For real TOPCon solar cells with the p-type c-Si wafer, two cell structure options have been studied [36]: one with the rear P-doped poly-Si TOPCon emitter and B-diffused front-surface field (FSF) layer as shown in Fig. 6(a) and the other one with the conventional front P-diffused emitter and the rear B-doped poly-Si TOPCon contact as shown in Fig. 6(b). We did a simulation study and found that when a low-quality c-Si with bulk lifetime shorter than 350 μs, the regular front emitter has a better performance than the rear emitter structures [36], while when the bulk lifetime is longer than 350 μs, the rear emitter has a better performance than the front one.

As demonstrated in Fig. 2, the effective lifetime for the well-passivated samples with the n⁺-poly-Si TOPCon is in the order of ~1050 μs; then we put this value into the simulation to expect an ideal efficiency based on the best passivation we have achieved. Therefore, the rear emitter should perform better than the front emitter structures. Fig. 6(c) and (d) shows the examples of the comparison of simulation results for the rear emitter and front emitter structures, in which (c) with the passivation parameters obtained from the experiments ($J_{0,\text{p-doped TOPCon}} = 3.0 \text{ fA/cm}^2$, $\tau_{\text{passivated}} = 1050 \mu\text{s}$) and (d) with the ultra-high lifetime ($\tau_{\text{high}} = 100 \text{ ms}$). Noted that the other parameters used in the simulation are referred to the previous paper and listed in Table 2 with (c) the industrial-level and (d) the lab-level technologies [36], and the J_0 of the B-doped TOPCon is set as 30 fA/cm². Also in Fig. 6(c), a standard PERC cell is simulated using the same passivation parameters as used in the TOPCon cells. For the front and rear emitters with the solar-grade p-type c-Si wafers, two simulations were made using the as-obtained passivation parameters with the B-doped TOPCon and P-doped TOPCon. It shows that with our best passivation parameters achieved so far, the front and rear emitters can reach the efficiencies of 22.4% and 22.8% respectively, and both are higher than the standard PERC cell (22.0%). From these results, we believe that the efficiency of ~22.8% in Fig. 6(c) corresponds to the achievable cell efficiency with the industrial constraints using the solar-grade p-type wafers, in which the rear emitter is better than the front emitter structures. Based on these results, we may conclude that the rear emitter TOPCon solar cell is an industrial favorable structure. In addition, the results with the

Fig. 6. Schematics of (a) front emitter and (b) rear emitter TOPCon solar cells with p-type c-Si wafers, and the simulated J-V characteristics of the front emitter and rear emitter TOPCon solar cells with (c) our best passivation parameters ($J_{0,\text{p-doped TOPCon}} = 3.0 \text{ fA/cm}^2$, $\tau_{\text{passivated}} = 1050 \mu\text{s}$) and the industrial-level technology, and with (d) the ultra-high lifetime ($\tau_{\text{ultra-high}} = 100 \text{ ms}$) and the lab-level technology. The J_0 of the B-doped TOPCon is set as 30 fA/cm², and the other detailed parameters can be referred to the paper [36].

ultra-high lifetime (100 ms) as shown in Fig. 6(d) demonstrate a significant difference between the rear emitter and front emitter by more than 0.5% in absolute efficiency, for which ~24.9% cell efficiency could be expected in R&D laboratories.

From the simulation study, we demonstrated that the rear emitter with n-TOPCon on p-type c-Si wafer is better than the front emitter with p-TOPCon as the back surface field. Because a front field contact layer improves the cell efficiency as shown by Ref. [21], a B diffusion for the front field contact and a back n-TOPCon are needed for completing the cell fabrication. In this case, the rear emitter TOPCon solar cell fabrication on p-type c-Si wafer is essentially the same as the front emitter TOPCon cell on n-type c-Si wafers, which has been already developed recently to the manufacturing mode. Therefore, the viability for making the rear emitter TOPCon cells on p-type c-Si wafers has been proven in principle. In addition, our experimental study has demonstrated that 1) both the ultrathin SiO_x passivation layer and the P doped poly-Si layer can be made in a PECVD system and 2) a very high passivation quality on p-type c-Si wafers can be achieved by the n-TOPCon structure. One could image that the two layers are fabricated in two separate PECVD chambers in an in-line PECVD system or fabricated sequentially in one PECVD chamber such as a tube PECVD system. The cross contaminations in the same chamber for the fabrication would not be an issue as demonstrated in this study because some dopants diffuse through the SiO_x layer that benefits the passivation quality, and therefore, the dopants incorporated during the SiO_x fabrication would not cause any problem at all; the O and N impurities incorporated into a-Si:H during the deposition would not influent the passivation quality as well because both O and N form shallow donors in poly-Si. From cost-effective point of view, one could retrofit a PERC production line into a TOPCon production line by modifying the SiN_x and Al₂O₃ PECVD deposition system with a limited investment. Of course, significant work needs to be done to demonstrate a real retrofitted TOPCon production line from an existing PERC line.

4. Summary

We have systematically studied the TOPCon passivation on solar-grade p-type c-Si wafers with ultrathin SiO_x made by plasma-assisted N₂O oxidation and P-doped poly-Si made with PECVD deposited a-Si:H precursors following a thermal annealing process. We found that the optimized annealing temperature for high-quality passivation is higher than those with acidic oxidized SiO_x, and the optimized annealing temperature depends on the PH₃ doping ratio during the PECVD deposition with the lower the doping ratio, the higher the optimized annealing temperature. The UV-Raman results show the same

Table 2

Parameters of the PERC, p-type and n-type polysilicon passivated-contact silicon solar cells (p-type substrate) with the industrial-level or advanced-level technologies.

	PERC	p-type polysilicon	n-type polysilicon	p-type polysilicon	n-type polysilicon
		industrial	industrial	Advanced	Advanced
Bulk properties:					
Background bulk Lifetime, τ_{bulk} (μs)	200	Variable (default:1050)	Variable (default:1050)	Variable (default:10 ⁵)	Variable (default: 10 ⁵)
Wafer thickness, W (μm)	180	180	180	180	180
Wafer resistivity, ρ (Ωcm)	1	Variable (default: 1)	Variable (default: 1)	Variable (default 1)	Variable (default 1)
Auger recombination	Ref. [42]				
Radiative recombination	Ref. [49]				
Mobility	Ref. [50]				
Intrinsic carrier concentration	Ref. [51]				
Bandgap narrowing	Ref. [52]				
Front metal grid:					
Space between fingers (μm)	650	900	1300	500	700
Finger width (μm)	40	40	40	10	10
Shading percentage (%)	6.2	4.4	3.1	2	1.4
Front emitter (n⁺,+ for PERC and p-type polysilicon) or front surface field (p^{+,++} for n-type polysilicon)					
Sheet resistance, $R_{\text{sheet},n,+}/p_{++}$ (Ω/sq)	90	30	30	30	30
Width of n ⁺ /p ⁺⁺ (μm)	80	80	80	20	20
J_{0e} , n ⁺⁺ /p ⁺⁺ , met contact (fA/cm^2)	600	800	800	400	400
J_{0e} , n ⁺⁺ /p ⁺⁺ , pass (fA/cm^2)	100	100	100	100	100
Contact resistivity ρ_c , n ⁺⁺ /p ⁺⁺ ($\text{m}\Omega\text{cm}^2$)	0.1	0.1	0.1	0.1	0.1
Junction depth, n ⁺⁺ /p ⁺⁺ (nm)	600	600	600	600	600
$R_{\text{sheet},n,+}/p_{++}$ (Ω/sq)	120	80	80	80	80
J_{0e} , n ⁺⁺ /p ⁺⁺ ,pass (fA/cm^2)	40	50	30	30	15
Junction depth, n ⁺⁺ /p ⁺⁺ (nm)	400	400	400	400	400
Total $J_{0,\text{front}}$ (fA/cm^2)	56	65.6	48.7	38.6	24.0
Rear of PERC					
Distance between opening points (μm)	500	–	–	–	–
Radius of opening points (μm)	60	–	–	–	–
$J_{0,\text{Al}}$ contact (fA/cm^2)	500	–	–	–	–
ρ_c ($\text{m}\Omega\text{cm}^2$)	10	–	–	–	–
$J_{0,\text{remaining area}}$ (fA/cm^2)	10	–	–	–	–
Rear passivating contact (polysilicon):					
$J_{0,\text{poly}}$ (fA/cm^2)	–	Variable (default: 30)	Variable (default: 8)	10	4
ρ_c ($\text{m}\Omega\text{cm}^2$)	–	Variable (default: 10)	Variable (default: 10)	10	5
Parallel resistance R_p ($\text{k}\Omega\text{-cm}^2$)	1×10^5	1×10^5	1×10^5	1×10^5	1×10^5
Series resistance R_s ($\Omega\text{-cm}^2$)	0.2	0.2	0.2	0.2	0.2
Optical model:					
Passivation & Reflectance Layer (nm), (SiN _x n = 2)	SiO ₂ 5/SiN _x 80	SiO ₂ 5/SiN _x 70	Al ₂ O ₃ 7/SiN _x 70	SiO ₂ 5/SiN _x 70	Al ₂ O ₃ 7/SiN _x 70
Shading width of fingers	100%	100%	100%	100%	100%
Z_0	6	6	6	6	6

crystalline structure for the samples annealed in the temperatures between 780 °C and 920 °C, which means that the crystalline structure is not the limiting factor for the passivation quality; while the dopant diffusion has a strong correlation with the passivation quality, where the diffusion depth increases with the increase of annealing temperature and the doping ratio. Comparing the passivation quality and dopant diffusion profiles, we conclude that a tail about 30–40 nm is preferred for high-quality passivation for the p-type wafers with the n⁺-poly-Si TOPCon structure, with which high-quality passivation with $iV_{\text{oc}} = 742 \text{ mV}$, $\tau = 1050 \mu\text{s}$, $J_0 = 3.0 \text{ fA}/\text{cm}^2$, and $\rho_c = 3.8 \text{ m}\Omega\text{cm}^2$ has been obtained after the post-hydrogenation process. Our simulation results show that the rear emitter solar cell performs better than the front emitter solar cells and ~22.8% efficiency is expected for industrial products and ~24.9% efficiency for R&D laboratories with high-quality c-Si wafers.

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Appendix A. Supplementary data

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