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Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?

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ABSTRACT

We present arguments that additional effects besides laterally homogenous tunnelling might occur in carrier-selective poly-Si/*c*-Si junctions: (*i*) the symmetrical electrical behaviour of n^+ and p^+ poly-Si/*c*-Si junctions, (*ii*) direct observation of structural modifications of the interfacial oxide upon thermal treatment by transmission electron microscopy, even for poly-Si/*c*-Si junctions with good passivation quality, and (*iii*) the achievement of low junction resistances even for interfacial oxide thicknesses >2 nm after thermal treatment. We present an alternative picture, essentially based on a localized current flow through the interfacial oxide, mediated either by local reduction of the oxide layer thickness or by pinholes. In consequence, the local current flow implies transport limitations for both minority and majority carriers in the *c*-Si absorber, and thus a correlation between recombination current and series resistance. Thus, a poly-Si/*c*-Si junction can also be explained within the framework of a classical *pn* junction picture for a passivated, locally contacted emitter, e.g. by the model of Fischer. Both electron selective contacts (n^+ poly-Si) and hole selective contacts (p^+ poly-Si) can be described consistently when using reasonable input parameters. Especially for p^+ poly-Si/*c*-Si junctions, our model could guideline further improvement.

1. Introduction

Carrier selective junctions based on silicon rich, mostly polycrystalline (poly-) layers deposited on an interfacial oxide grown on a crystalline (*c*-) silicon absorber are currently attracting significant research interest. Excellent junction quality with recombination current densities J_0 down to 0.7 fA/cm^2 [1], as well as efficiencies up to 25.1% [2] have been demonstrated with this approach.

Regarding the physical working principle of poly-Si/*c*-Si junctions, different pictures exist [3,4]. For interfacial oxide thicknesses of $\sim$2 nm or less, it is safe to assume that tunnelling through the oxide takes place. Nevertheless, we present in this work strong support that, at least for our samples with initial interfacial oxide thicknesses >2 nm, additional effects are relevant, which could in particular explain the excellent performance of our p^+ poly-Si/*c*-Si junctions.

2. Arguments for additional relevant effects

Our first argument for additional current transport mechanisms besides lateral homogeneous tunnelling is the experimental observation of low junction resistances ρ_c and low recombination current densities J_0 for both n^+ poly-Si/*c*-Si and p^+ poly-Si/*c*-Si junctions. This might not be consistent with the tunnelling model, as explained in the following:

As indicated in Fig. 1, the poly-Si is inherently highly defective, i.e., a high density of energy states within the band gap of the poly-Si could mediate strongly pronounced Shockley-Read-Hall recombination with minority carrier lifetimes in the range of pico- to nanoseconds [1,5]. Thus, for low recombination current densities, it's essential to prevent minority carriers from reaching the poly-Si. “Minority (majority)” refers in the following to the doping type of the poly-Si, i.e., to holes (electrons) for n^+ poly-Si and electrons (holes) for p^+ poly-Si. Typically, the poly-Si is highly

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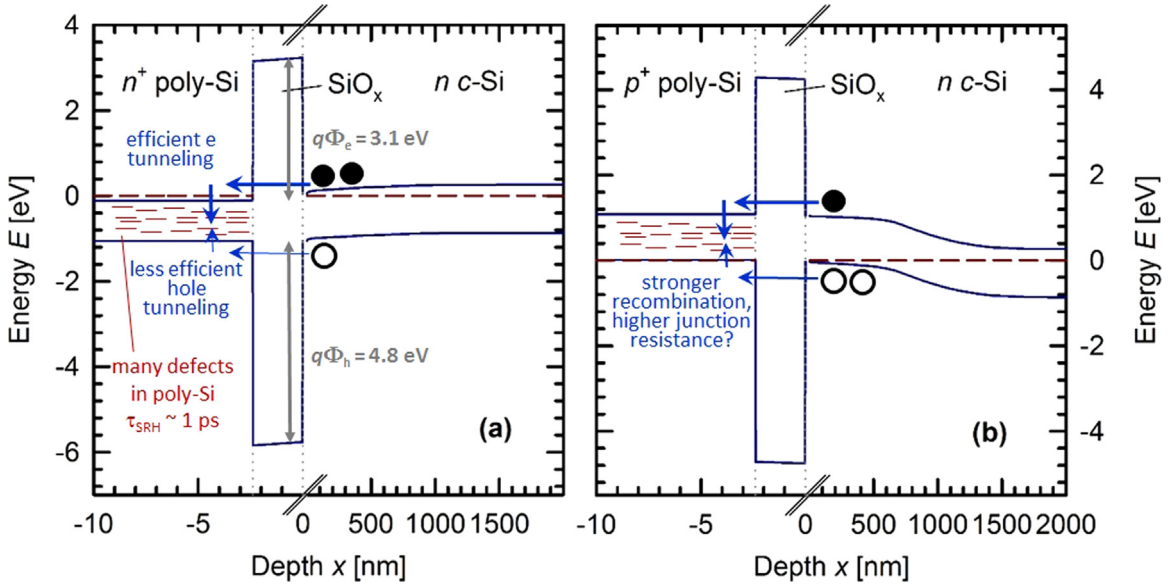

Fig. 1. One-dime · nsional energy band diagrams assuming a laterally homogeneous interfacial oxide for (a) our n^+ poly-Si/*c*-Si junction with $J_0 = 1$ fA/cm^2, and (b) for our p^+ poly-Si/*c*-Si junction with $J_0 = 4.4 \cdot$ fA/cm^2 [7]. The band diagrams are calculated with DESSIS for experimentally determined doping concentrations in the poly-Si and in the *c*-Si (i.e., in-diffusion of dopants from the poly-Si into the *c*-Si upon thermal annealing is taken into account). Defects in the poly-Si, as well as possible current paths according to the tunnelling model are illustrated.

doped and thus induces a band bending in the lower doped *c*-Si absorber, reducing the minority carrier concentration at the SiO_x/*c*-Si interface. This "field effect passivation" is already beneficial for reducing recombination in the poly-Si. However, it's not sufficient to explain the low recombination current densities down to < 1 (< 5) fA/cm^2 measured on n^+ (p^+) poly-Si/*c*-Si junctions: On samples on which the interfacial oxide has been removed prior to the poly-Si deposition, high recombination current densities > 500 fA/cm^2 are observed despite the fact that the "field effect passivation" is also present here. Thus, the interfacial oxide somehow prevents the minority carriers from reaching the poly-Si. On the other hand, as obvious due to the low junction resistances, majority carriers can efficiently surpass the interfacial oxide. Assuming tunnelling to be the dominant current transport mechanism, the question arises why majority carriers are able to tunnel through the interfacial oxide while minority carrier tunnelling should be much less efficient. An essential aspect of the answer to this question given by the tunnelling model for n^+ poly-Si/*c*-Si junctions is a difference in the tunnelling barrier heights. As known from internal photoemission spectroscopy [6], the different band offsets between Si and SiO_2 (4.7 eV for valence band, 3.2 eV for the conduction band) imply a larger barrier for holes than for electrons. As indicated in Fig. 1(a), this difference can explain the excellent performance of n^+ poly-Si/*c*-Si junctions – low recombination current densities (limited by the transport of holes through the oxide) and simultaneously low junction resistances (limited by the transport of electrons through the oxide).

Fig. 2 shows experimental J_0, ρ_c data reported by various groups for n^+ poly-Si/*c*-Si junctions (red symbols), as well as a very rough fit by a power law (red dashed line). While Gan and

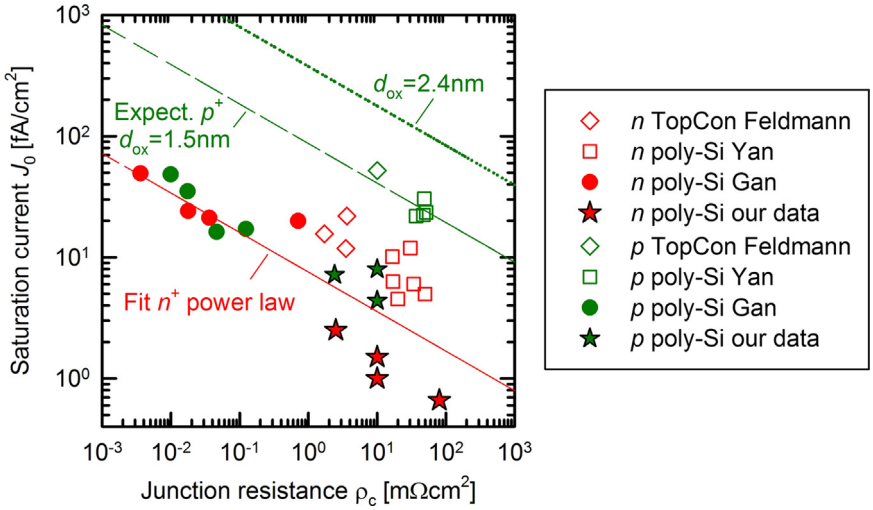

Fig. 2. Experimental J_0, ρ_c data reported for n^+ poly-Si/*c*-Si junctions (red symbols, taken from Refs. [1,7,8,12–15]) and for p^+ poly-Si/*c*-Si junctions (green symbols, taken from Refs. [7,8,14,16–18]). The dashed red line represents a power law fit of the n^+ poly-Si/*c*-Si junction values. The experimental data shown represent, to our knowledge, the currently available J_0 and ρ_c pairs for poly-Si/*c*-Si junctions. One should note that also other groups have reported on excellent J_0 values, but without a quantitative evaluation of the poly-Si/*c*-Si junction resistance. The dashed and dotted green line indicates the expected shift of the fit of n^+ poly-Si/*c*-Si data fit for p^+ poly-Si/*c*-Si junctions with an interfacial oxide thickness of 1.5 nm and 2.4 nm, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Swanson [8] reported very low junction resistances down to $3 \cdot 10^{-6}$ mΩ cm in combination with decent recombination current densities of 49 fA/cm^2, more recent results typically show higher ρ_c and lower J_0 values. Interestingly, Gan and Swanson used presumably thicker thermal grown interfacial oxides (specification <2 nm [8]) than the more recently used wet-chemically grown interfacial oxides of $\sim$1.5 nm thickness [9]. In the state-of-the art device simulation software Sentaurus Device, Si/SiO_2 band offsets of 4.73 eV (valence band) and 3.15 eV (conduction band) are implemented as standard parameters [10]. Recent numerical simulations of solar cells with n^+ TopCon junctions on the rear side performed with this software are in good agreement with the measured cell data [3]. Also, bipolar junction transistors (BJT) with n^+ poly-Si emitters can be well described by the tunnelling model [11]. Here, the barrier heights are commonly used as fitting parameters for the transistor characteristics. For BJT with n^+ poly-Si emitters, the best agreement is achieved for an electron tunnelling barrier height of 0.3 eV and a hole tunnelling barrier height of 1 eV [11]. The fact that these values are, in absolute numbers, much lower than the values determined by internal photoemission [6], may indicate the presence of an additional current transport mechanism.

For hole-collecting p^+ poly-Si/*c*-Si junctions, higher recombination current densities and higher junction resistances (as compared as the respective values for electron-collecting n^+ poly-Si/*c*-Si junctions with the same interfacial oxide thickness) would be expected for the barrier heights mentioned above (Fig. 1(b)). Within a first-order approximation (further comments on this approximation are given in the appendix), the increase in the junction resistance ρ_c (determined by the majority carrier flow) as well as the increase in the recombination current density J_0 (determined by the minority carrier flow) should be proportional to the ratio of the barrier transmission probabilities for electrons T_e and holes T_h. Disregarding the trapezoidal shape of the barrier and image charge effects and restricting to energy levels near the band edges, this ratio is given by:

$$\frac{T_e}{T_h} \propto \frac{\exp\left[-d_{ox}\sqrt{\frac{2m_{t,e}}{\hbar^2}\Phi_e}\right]}{\exp\left[-d_{ox}\sqrt{\frac{2m_{t,h}}{\hbar^2}\Phi_h}\right]} \quad (1)$$

Here, d_{ox} denotes the interfacial oxide thickness, $m_{t,e}$ (Φ_e) and $m_{t,h}$ (Φ_h) the tunnelling mass (the barrier height) for electrons and holes, respectively, q denotes the elementary charge, and $\hbar$ denotes the Planck constant divided by 2 π. As summarized in Ref. [3], various values for the electron tunnelling mass in SiO_2 have been reported, ranging from 0.3 to 0.9 times the electron rest mass m_0. For our rough estimation, we chose a value of $m_{t,e}=m_{t,h}=0.4$ m_0. One should note that the following arguments are relaxed for lower tunnelling masses, and strengthened for larger tunnelling masses. Furthermore, asymmetric tunnelling masses ($m_{t,h}<0.65$ $m_{t,e}$) could completely compensate the effect of the asymmetric tunnelling barriers described below.

We chose two interfacial oxide thickness – 1.5 nm and 2.4 nm – corresponding to typical values reported for wet chemically grown interfacial oxides [9], and to thermally grown interfacial oxides as reported previously by our group [7]. For 1.5 nm oxide thickness, Eq. (1) yields a transmission probability ratio electron/holes of 6.31, while for 2.4 nm, a respective value of 19.04 is obtained. In Fig. 2, the dashed and dotted green lines indicate the respective shift of the fit of n^+ poly-Si/*c*-Si data fit towards higher J_0 and higher ρ_c values when transferring it to p^+ poly-Si/*c*-Si junctions.

The experimental results of Feldmann et al. [16] and Yan et al. [17] (open green symbols in Fig. 2) for p^+ poly-Si/*c*-Si junctions seem to be consistent with our rough estimation.

However, the results of Gan et al. [8], as well as our own results [7,14,18] (full green symbols in Fig. 2) are clearly not consistent with this prediction of the tunnelling model. Gan et al. [8] obtained equal J_0 and ρ_c values for both doping types of the poly-Si. Our best J_0 value of 4.4 fA/cm^2 for p^+ poly-Si/*c*-Si junctions is only four times larger than that for n^+ poly-Si/*c*-Si junctions [7], while a much larger difference is expected for this interfacial oxide thickness according to the rough estimation described above.

So far, within the framework of the tunnelling model, no consistent description of n^+ and p^+ poly-Si/*c*-Si junctions with identical parameters has been reported. It is not a new finding. In the bipolar transistor community, it is known since a long time that BJT with n^+ and with p^+ poly-Si emitters can hardly be described within the framework of the tunnelling model when assuming identical barrier heights in both cases [11]. While for BJTs with n^+ poly-Si emitters, barrier heights of $q\Phi_e=0.3$ eV (electrons) and $q\Phi_h=1$ eV (holes) have been extracted, the respective values for BJTs with p^+ poly-Si emitters are $q\Phi_e=1$ eV (electrons) and $q\Phi_h=0.3$ eV (holes) [11].

For this reason, we proposed previously an alternative model based on localized current flow through pinholes formed upon thermal annealing of the poly-Si/*c*-Si junctions [4]. This model was also inspired from knowledge from the poly-Si emitter BJT community, where this local oxide breakup was observed in TEM [19], described by thermodynamically models [20] and utilized to model the majority carrier flow in BJTs [21]. Our previous model for the current transport mechanism in poly-Si/*c*-Si junctions is extended as described below. Here, we would like to remark that there is recent experimental support for the picture of localized current flow. The most striking one is the direct observation of structural modifications of the interfacial oxide upon thermal treatment in transmission electron microscopy (TEM) images. There is agreement in the community that for exaggerated long annealing durations or high annealing temperatures, the interfacial oxide breaks up at many locations, yielding direct contact between the *c*-Si and the defect rich poly-Si on large area and therefore high recombination currents [9,24]. For optimized annealing conditions, pinholes are hardly observed in TEM. This might be a consequence of the low pinhole area density ($\sim 10^7$ cm^{-2} according to Ref. [4]) in combination with the small area probed by TEM. For thermally grown interfacial oxides, we at least observe a local modification of the oxide thickness upon annealing at 1050 °C from initially $\sim$2.4 nm down to $\sim$1 nm in some regions near the centre of the grains in the poly-Si, and up to $\sim$4 nm near the grain boundaries (Fig. 3(a)). When reducing the initial oxide thickness down to $\sim$1.7 nm, we also find locations in which the lattice of the *c*-Si is in direct contact with the lattice of the poly-Si, indicating the formation of very small oxide pinholes with a low areal density (Fig. 3(b)). Please note that also for the latter sample, the J_0 value is still quite low (20 fA/cm^2). Further details on our TEM investigations, in particular on the underlying statistics, will be presented elsewhere [22].

The limitations of TEM regarding the observation of pinholes with a low areal density can be overcome with scanning methods like conductive atomic force microscopy (c-AFM). Recent (c-AFM) results presented at the SiliconPV2016 [23] indicate the presence of local spots with strongly enhanced conductivity in n^+ TopCon junctions. Their area density increases from $2.5 \cdot 10^{10}$ cm^{-2} after thermal annealing at 800 °C to $7.5 \cdot 10^{10}$ cm^{-2} after thermal annealing at 950 °C.

A further experimental finding that supports our picture that a major part of the current flow through the interfacial oxide might be localized in regions in which the oxide thickness is reduced or in which even pinholes have formed is the behaviour of the junction resistance upon thermal treatment. It is necessary to apply a sufficient temperature budget in order to reduce the

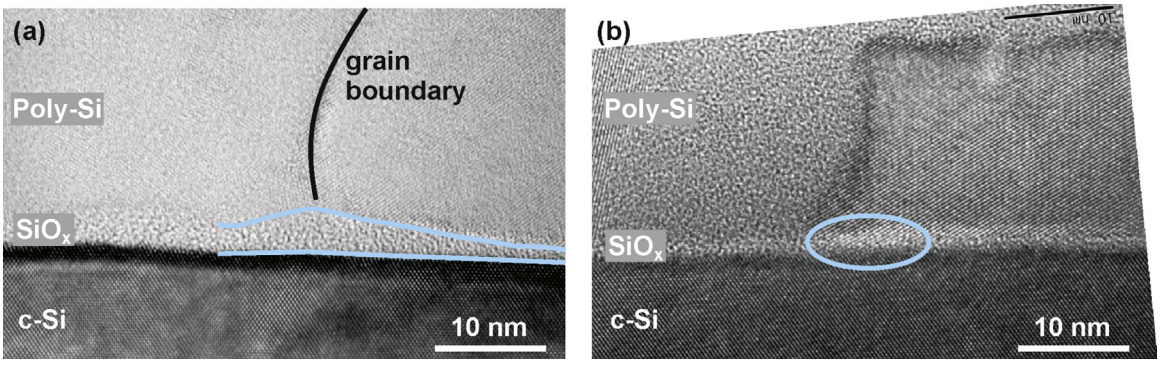

Fig. 3. High resolution TEM cross section images of n^+ poly-Si/*c*-Si junctions after junction formation at 1050 °C, showing (a) a local variation of the interfacial oxide thickness, and (b) a direct local contact of the lattice of the poly-Si and of the *c*-Si substrate, possibly indicating pinhole formation. Initial interfacial oxide thickness was ~2.4 nm for (a) and ~1.7 nm for (b). The J_0 values are (a) 10 fA/cm^2 and (b) 20 fA/cm^2.

junction resistance down to an acceptable value [13,17,24]. This observation can hardly be explained with a homogeneous current flow through an interfacial oxide which remains unaltered in thickness upon thermal annealing. Also, the low junction resistances of 2.5 m Ωcm^2 achieved for initial interfacial oxides thicknesses of 2.1 nm [14], or low ρ_c values obtained even for an initial oxide thickness of 3.6 nm [24] can hardly be explained with tunnelling through an unaltered oxide [2,17,25]. Please note that also for the latter samples, the recombination current density was very low – 2.5 fA/cm^2 [14] and 5 fA/cm^2 [24], respectively.

3. Alternative picture

The alternative picture presented in the following is a generalized version of our previous model according to Ref. [4]. A comparison of both approaches, as well as a summary of differences and similarities is given in the appendix.

As known from secondary ion mass spectrometry (SIMS) and electrochemical capacitance voltage (ECV) measurements [7,16], dopants diffuse from the poly-Si into the *c*-Si during the junction formation process, especially for boron doped poly-Si layers (Fig. 4 (a)). Fig. 4(b) shows a schematic sketch of our corresponding model for a localized current flow through an interfacial oxide into a doped poly-Si layer.

In contrast to previous work [4], we do not exclude that charge carriers surpass the oxide by tunnelling, although pinhole formation might make the necessity for tunnelling superfluous. The major aspect of the model is that the oxide is surpassed locally, e.g. due to significant local reduction of the interfacial oxide thickness or due to pinhole formation. This local current flow implies transport limitations for majority and minority charge carriers due to current crowding in the highly doped region of the *c*-Si absorber. We assume that these crowding effects in the *c*-Si are limiting both the majority and minority carrier flow, rather than the final local transport through the oxide or through the pinhole. The latter is therefore disregarded. The current flow in the *c*-Si, i.e., the recombination current densities (minority carriers) and junction resistance (majority carriers), can be calculated analytically [4]. An equivalent description is provided by the Fischer model [26], which can be applied to the highly doped region in the *c*-Si underneath the interfacial oxide. The Fischer model also takes into account recombination in regions where the interfacial oxide is still intact. For the recombination current density, we use Eq. (20) in Ref. [27] (the assumption of a minority carrier diffusion length much larger than the thickness of the doped region in the *c*-Si is valid for our samples), while for the resistance implied by the crowding of majority carriers, Eqs. (22,23) in Ref. [27] are used.

We assume the recombination velocity $S_{0,\mathrm{pinhole}}$ in the interface regions where pinholes have formed or where the interfacial oxide thickness is strongly reduced to be thermally limited ($S_{0,\mathrm{pinhole}}=10^7$ cm/s). According to the TEM results, we assume a radius r_{pinhole} of these regions of 2 nm and vary their areal density from 10^5 cm^{-2} to 10^{10} cm^{-2}. The role of the base in the original

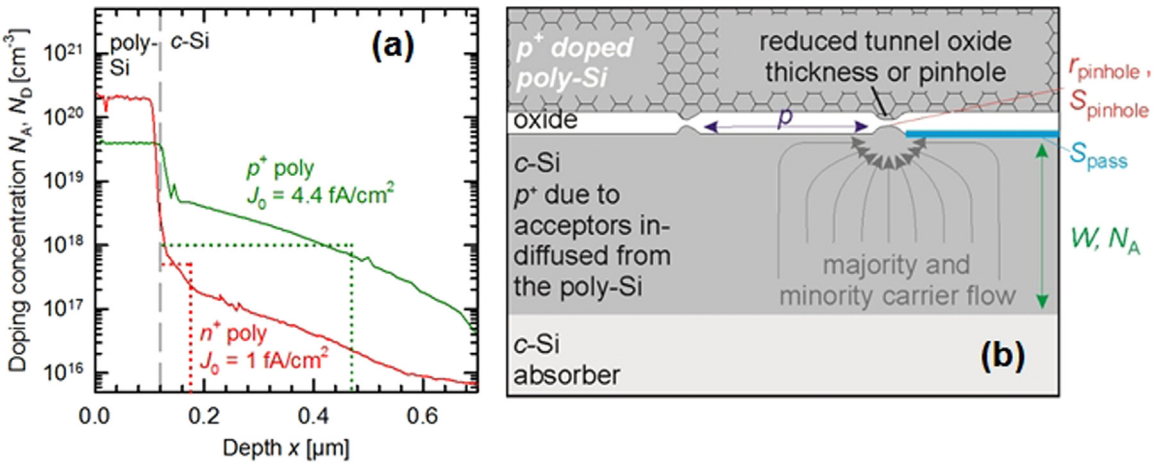

Fig. 4. (a) ECV profiles of our p^+ poly-Si/*c*-Si junction with $J_0=(4.1\pm1.1)$ fA/cm^2, and of our n^+ poly-Si/*c*-Si junction with $J_0=(1.0\pm1.1)$ fA/cm^2 [1]. The box profile approximation used for our model is indicated by the dotted lines. (b) Schematic of our picture of poly-Si/*c*-Si junctions, exemplarily shown for a p^+ poly-Si/*c*-Si junction. The junction resistance and the recombination current density is assumed to be determined by the majority and minority carrier crowding in the heavily doped region within the *c*-Si.

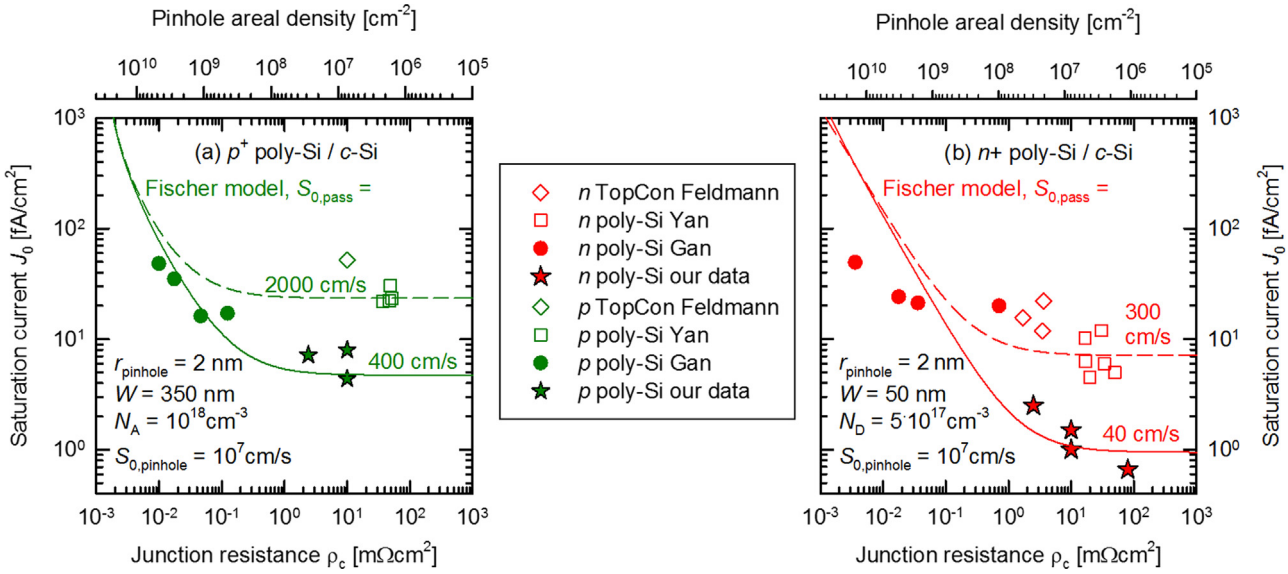

Fig. 5. (a): Comparison of experimental and modelled ρ_c, J_0 values for p^+ poly-Si/c-Si junctions. For our own data [7,14,18] as well as for the data of Gan et al. [8], a nice agreement is obtained for $S_{0,pass}$ values of 400 cm/s, while for the data of Feldmann et al. [16] and Yan et al. [17], best agreement is obtained for $S_{0,pass}$=2000 cm/s. (b) Comparison of experimental and modelled ρ_c, J_0 values for n^+ poly-Si/c-Si junctions. Here, the best agreement between model and our data [1,7,14,15] and the of Gan et al. [8] is obtained for $S_{0,pass}$=40 cm/s.

formulation of the Fischer model for the description of local rear contacts [26,27] is represented in our picture of poly-Si/c-Si junctions by the highly doped region in the c-Si, which has formed underneath the interfacial oxide due to in-diffusion of dopants from the poly-Si. For the doping concentration N_A (for p^+ poly-Si/c-Si junctions) or N_D (for n^+ poly-Si/c-Si junctions) as well as for the width W of this region, we use the box profile approximation of our measured profiles as shown in Fig. 4(a). The resulting values are N_A=10^{18} cm^{-3}, W=350 nm for p^+ poly-Si/c-Si junctions and N_D=5 · 10^{17} cm^{-3}, W=50 nm for n^+ poly-Si/c-Si junctions. The recombination velocity $S_{0,\ pass}$ in regions where the interfacial oxide is still intact (or unaltered in thickness) is used as the only fitting parameter.

As shown in Fig. 5(a), we achieve agreement between modelled and measured $J_0(\rho_c)$ data for our p^+ poly-Si/c-Si junctions and for the data of Gan et al. [8] when assuming a $S_{0,pass}$ value of 400 cm/s. Remarkably, this value agrees well to literature data for surface recombination velocities at the SiO_2/p^+ c-Si surface for a boron surface doping concentration of N_A=10^{18} cm^{-3} [28]. Obviously, recombination in the passivated regions dominates for our p^+ poly-Si/c-Si junctions, while the data of Gan et al. [8] indicates a strong contribution of recombination at the pinholes (which are, according to the very low junction resistances, present with a much higher areal density in these samples). Auger recombination in the highly doped p^+ region in the c-Si plays a minor role: its contribution to the total J_0 value of 4.4 fA/cm^2 is calculated to 0.6 fA/cm^2 by the program EDNA 2 for our ECV doping profile. As already pointed out in Ref. [4], the most sensitive input parameter of our model in the regime of low junction resistance and "pinhole-dominated" recombination is the doping level in the c-Si. Thus, a large uncertainty is implied in the simulation of experimental data from other groups when using the doping profile measured on our samples. However, for the data of Gan et al. [8], we achieve nice agreement when using the box approximation of our ECV profile. For the description of the $J_0(\rho_c)$ data for p^+ poly-Si/c-Si junctions reported by Feldmann et al. [16] and Yan et al. [17] with our model, the doping profile in the c-Si is less important since the total recombination seems to be dominated by the recombination in regions where the interfacial oxide is still intact (or unaltered in thickness). However, a higher $S_{0,pass}$ value of 2000 cm/s has to be assumed. Our hypothesis for this difference in the $S_{0,pass}$ values for samples from different groups is a difference in the interfacial oxide: While Gan et al. [8] and ourselves use thicker, mainly thermally grown interfacial oxides, Feldmann et al. [16] and Yan et al. [17] use wet chemically grown oxides with a thickness of only 1.5 nm. The smaller interfacial oxide thickness might compromise the passivation quality threefold: First, too thin interfacial oxides might not efficiently prevent the tunnelling of minority carriers (electrons in the case of p^+ poly-Si/c-Si junctions) from the c-Si into the poly-Si, implying a larger recombination current density. Second, boron can diffuse more efficiently through thinner interfacial oxides, implying a higher boron doping concentration at the SiO_x/c-Si interface and thus a higher $S_{0,pass}$ value [28]. Third, thinner oxides break up more easily, which implies high recombination current densities for too large pinhole area fractions. Thus, the annealing temperature has to be restricted to lower values than possible for samples with thicker interfacial oxides. However, a high annealing temperature might be beneficial for a re-organisation of the SiO_x/c-Si interface, which possibly exhibits a high density of interface defects directly after the wet chemical oxide growth (or the thermal oxide growth at low temperatures ~600 °C).

Nevertheless, it is possible to achieve excellent junction quality for p^+ poly-Si/c-Si junctions with wet chemically grown interfacial oxides. Our lowest J_0 value achieved on such a junction with 1.7 nm thick wet chemically grown interfacial oxide thickness is 8 fA/cm^2 [18].

As shown in Fig. 5(b), our model can also describe experimental $J_0(\rho_c)$ data for our n^+ poly-Si/c-Si junctions and for the data of Gan et al. [8] when assuming a $S_{0,pass}$ value of 40 cm/s. Again, this value in in good agreement with literature data for the SiO_2/n^+ c-Si interface for a Phosphorus doping concentration of 5 · 10^{17} cm^{-3} [29]. Auger recombination in the highly doped n^+ region in the c-Si is calculated to 0.2 fA/cm^2 by the program EDNA 2 for our doping profiles. Again, the experimental $J_0(\rho_c)$ data of Feldmann et al. [12] and Yan et al. [13] can be described by a higher $S_{0,pass}$ value (300 cm/s in this case), perhaps due to the same reasons as discussed above for p^+ poly-Si/c-Si junctions.

Also for n^+ poly-Si/c-Si junctions, it is possible to achieve excellent passivation quality with wet chemically grown interfacial

oxides. Our lowest J_0 value achieved on such a junction with 1.7 nm thick wet chemically grown interfacial oxide thickness is 1.5 fA/cm^2 [15].

4. Conclusions

We present arguments that laterally homogeneous tunnelling through an unaltered interfacial oxide is possibly not the only current mechanism present in poly-Si/*c*-Si junctions. First, excellent p^+ poly-Si/*c*-Si junction properties (low recombination current, low junction resistance) have been achieved despite a "wrong tunnelling barrier height ratio" for electrons and holes, which seems inconsistent to the expectations of the tunnelling mode. Second, structural modifications of the interfacial oxide (local thickness reduction, pinhole formation) have been directly observed in TEM even for samples with low recombination current densities. This might be consistent to recent results from (c-AFM) measurements showing a large areal density of local spots with strongly increased conductivity [23]. Third, we obtain low junction resistance down to 2.4 mΩcm^2 after sufficient thermal annealing of poly-Si/*c*-Si junctions with initial interfacial oxide thicknesses of 2.1 nm [14] (or even of 3.6 nm), which, if unaltered upon annealing, should be prevent direct tunnelling. We therefore propose an alternative picture, which considers the poly-Si/*c*-Si junction as a "classical, locally contacted emitter", assuming local current flow through the interfacial oxide at locations where the oxide thickness is reduced or even pinholes have formed. Therefore, the current flow of majority and minority carriers in the doped region formed underneath the interfacial oxide by in-diffusion of dopants from the poly-Si can be described by the Fischer model. We demonstrate nice agreement between our experimental J_0, ρ_c data and our model for n^+ and p^+ poly-Si/*c*-Si junctions for realistic input data (in particular measured doping profiles in the *c*-Si). The recombination in our junctions seems to be dominated by recombination in regions where the interfacial oxide is still intact. The respective interface recombination velocities agrees well with literature data for SiO_2 on boron or phosphorus doped *c*-Si surfaces. According to our picture, the main reasons for the carrier-selectivity of both n^+ and p^+ poly-Si junctions is a reduction of the minority carrier concentration in the vicinity of the recombination-active pinholes (or locations with very thin interfacial oxide, assumed to be equally transparent for electrons and holes). This description is in agreement with the general picture of carrier-selectivity according to Würfel et al. [30].

In real junctions, both mechanism – local current flow and laterally homogeneous tunnelling – possibly superpose. Since the latter is not symmetric with respect of the doping type of the poly-Si and more favourable for n^+ poly-Si/*c*-Si junctions, it is beneficial for the optimization of p^+ poly-Si/*c*-Si junctions if the first mechanism is dominating. This can be achieved by a sufficiently large interfacial oxide thickness. For example, a J_0 value of 8 fA/cm^2 is achieved on a p^+ poly-Si/*c*-Si junction with a 1.7 nm thick wet chemically grown interfacial oxide.

Since we think that these arguments for an existing or even dominating current flow through pinholes (or regions with locally reduced interfacial oxide thickness) for samples with pure poly-Si on top of an interfacial oxide with sufficient thickness (i.e., larger than 1.5 nm) annealed at sufficiently high temperatures (i.e., around 900 °C or above) are plausible, we prefer to denote these junctions as Polysilicon on Oxide (POLO) junctions. This denotation, which was suggested already in 2013 [31], is independent from the current transport mechanism.

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APPENDIX A. Tunnelling current

The approximation of the ratio of tunnelling currents in p^+ and n^+ poly-Si/*c*-Si junctions exclusively by considering the transmission probabilities for the respective tunnelling barrier heights requires further discussion. The tunnelling current through a barrier equals the transmission probability, multiplied by the density of occupied initial states, the density of unoccupied final sates, and by the attempt frequency. Furthermore, a net current flux from the *c*-Si into the poly-Si should be considered, including the current flow from the *c*-Si into the poly-Si and vice versa. At least for the minority carriers, the latter is negligible. It appears furthermore justified to consider the density of occupied initial states and the attempt frequency for electrons and holes in the *c*-Si to be in the same order of magnitude, thus cancelling out in Eq. (1). Indeed, when calculating the minority and majority carrier concentration at the Si/SiO_2 interface based on the band diagram shown in Fig. 6, one obtains very similar values for both – n^+ poly-Si/*c*-Si and p^+ poly-Si *c*-Si junctions.

In particular the density of unoccupied final states in the poly-Si could limit the tunnelling current for electrons or holes when considering the poly-Si as a semiconductor with a band gap comparable to that of *c*-Si. The fraction of the work function difference between the poly-Si and the *c*-Si which drops across the interfacial oxide shifts the edge of the minority carrier band edge at the SiO_2/*c*-Si interface towards an energetic position within the band gap of the poly-Si. However, the band gap narrowing within the heavily doped poly-Si, the in-diffusion of dopants from the poly-Si into the *c*-Si, as well as the (weakly pronounced) band bending within the poly-Si (over-) compensates this effect. Due to the latter two effects, the valence band edge of the *c*-Si at the SiO_2/*c*-Si interface is energetically located 1 meV below the valence band edge of the poly-Si at the poly-Si/SiO_2 interface according to our DESSIS calculations of an n^+ poly-Si/*c*-Si junction (Fig. 6(a)). Minority carrier tunnelling could thus occur from valence band to valence band in these junctions, i.e., recombination should not be limited by the density of final states.

According to our band diagram for p^+ poly-Si/*c*-Si junctions, the conduction band edge in the *c*-Si at the SiO_2/*c*-Si interface is 38 meV below the conduction band edge in the poly-Si at the poly-Si/SiO_2 interface (Fig. 6(b)). Thus, electrons (minority carriers in this case) would have to be thermally excited in order to tunnel from the *c*-Si into the poly-Si. However, since only a thermal excitation of 1.4 times the thermal energy k_BT at 300 K would be necessary, it seems not plausible to assume that this effect is limiting the electron current (i.e., the recombination) in p^+ poly-

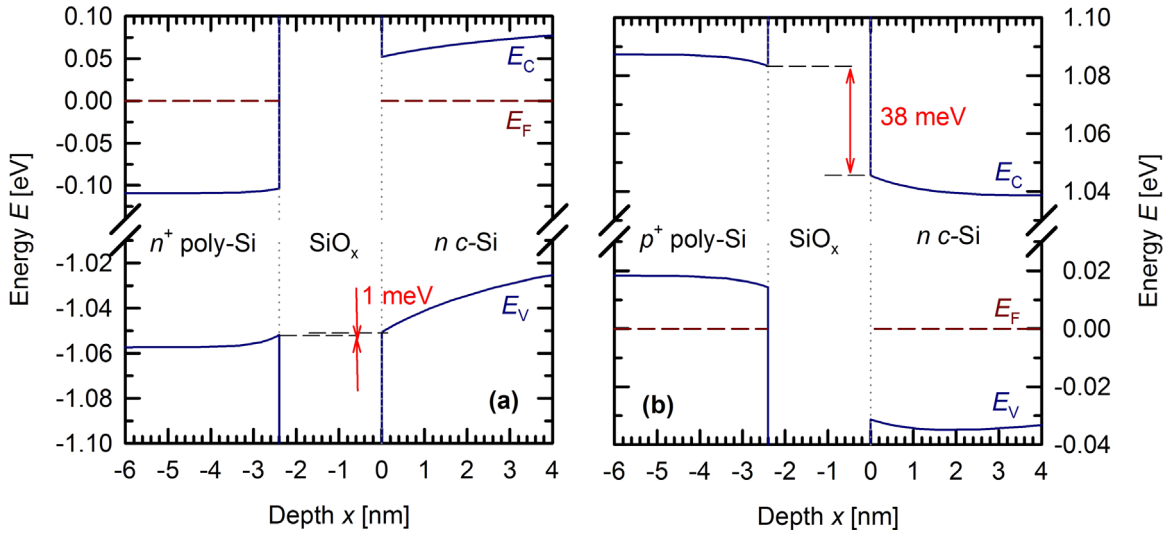

Fig. 6. Enlarged details of the band diagram for (a) $n+$ poly-Si/*c*-Si junctions, and (b) p^+ poly-Si/*c*-Si junctions as shown in Fig. 1. In (b), an offset of 38 meV between the energetic position of the conduction band edge in the *c*-Si (SiO_2/*c*-Si interface) and in the poly-Si (poly-Si/SiO_2 interface) is visible. One should note the limited accuracy of these DESSIS calculations. For example, the poly-Si is described by the models of *c*-Si, and defect levels are neither assumed to change the band structure (in particular near the band edges) nor to trap charges.

Si/*c*-Si junctions. Furthermore, in particular near the band edges, the defects in the poly-Si and at the poly-Si/SiO_2 interface possibly pose accessible final states with a high density in the band gap of the poly-Si. Under illumination, the band bending will also be relaxed, i.e., the voltage drop across the interfacial oxide will be reduced. Thus, the edge of the minority carrier band at the SiO_2/*c*-Si interface will shift out of the band gap of the poly-Si.

We therefore tentatively conclude that, within the framework of the tunnelling model, a low density of accessible final states is not likely to limit the tunnelling of minority carriers into (the recombination within) the poly-Si. Of course, the accuracy of the calculation of the band diagram has its limitations, even when using state-of-the art software like DESSIS including recent models for many import physical effects. For example, the effect of the defect states in the poly-Si, at the poly-Si/SiO_2 and at the SiO_2/*c*-Si interface is difficult to describe without further experimental input. It might therefore be worth to investigate the band alignment of poly-Si/*c*-Si junctions experimentally, e.g. by photoelectron spectroscopy of junctions with very thin poly-Si layers.

APPENDIX B. Comparison to previous work

In the following, our more generalized model presented in this work is compared to our previous model according to Ref. [4]. The underlying physics of both approaches is identical. We consider the current flow through the interfacial oxide to be localized, and calculate the resulting junction resistance and recombination current density based on the majority and minority carrier flow within a highly doped *c*-Si region in the vicinity of the pinhole (i.e., in the *c*-Si underneath the interfacial oxide). In Ref. [4], the spatial distribution of minority carriers and the resulting diffusion current is calculated straight-forward by solving the equation for minority carrier diffusion. In order to enable an analytical solution, the problem was simplified in Ref. [4] to one dimension (spherical coordinates, only radius dependence, and no angle-dependence) by utilizing radial symmetry. This is the reason why we had to neglect the recombination at the *c*-Si/SiO_x interface in Ref. [4], since otherwise the radial symmetry would have been broken. In this work, we applied the concept of Fischer [26,27] to our problem. The Fischer model does not attempt to calculate the spatial distribution of minority and majority carriers. Rather, a relation between resistance (majority carrier flow) and recombination current density (minority carrier flow) is deduced by utilizing the similarity of transport equations (Laplace equation in both cases) and boundary conditions for minority and majority carriers. The physical principal behind – that both carrier types are facing the same transport problem – also holds for our more straight-forward previous approach. The main advantage of the concept of Fischer [26,27] is that no restrictions on the symmetry are implied a-priori. Therefore, it is possible to deduce a relation between resistance and recombination (Eq. (20) in Ref. [27]) for a structure which includes both – recombination in the pinhole region, as well in the surrounding regions where the interfacial oxide is still intact. When furthermore applying appropriate models for the resistance of such a structure (Eqs. (22,23) in Ref. [27]), the Fischer concept enables a calculation of J_0 and ρ_c including the recombination at the SiO_x/*c*-Si interface. This comes to the price of a loss of information on the spatial carrier distribution, and to the price of a more indirect approach (as compared to our more straight-forward calculation in Ref. [4]). However, also the latter might not be critical since the Fischer model is well known to and widely accepted in the PV community. As a further generalization, our current picture does not exclude that the actual transport through the interfacial oxide is mediated by tunnelling in a region in which the oxide thickness is locally reduced (i.e., the formation of a pinhole is not a necessary assumption any more). However, this is only an aspect of interpretation, since the actual transport through the interfacial oxide (or through a pinhole) is not taken into account in the calculations – neither in this work nor in Ref. [4].

Fig. 7 compares for a p^+ poly-Si/*c*-Si junction the experimental data for ρ_c, J_0 with both models – the current one based on the Fischer concept, and the previous one according to Ref. [4]. The input parameters for the doping concentration in the *c*-Si region underneath the interfacial oxide ($N_A = 10^{18}$ cm^{-3}), the depth of the in-diffused region (W (or R in model [4]) = 350 nm), the radius of the pinhole ($r_{pinhole} = 2$ nm) and the recombination velocity within the pinhole ($S_{0,pinhole} = 10^7$ cm/s) are chosen identical. In the regime with high pinhole area density and low junction resistivity, recombination in the pinholes dominates the total recombination, and both models are in good agreement. However, all experimental data points except the values from Gan and Swanson [8] seem to be located within a regime with low pinhole areal density,

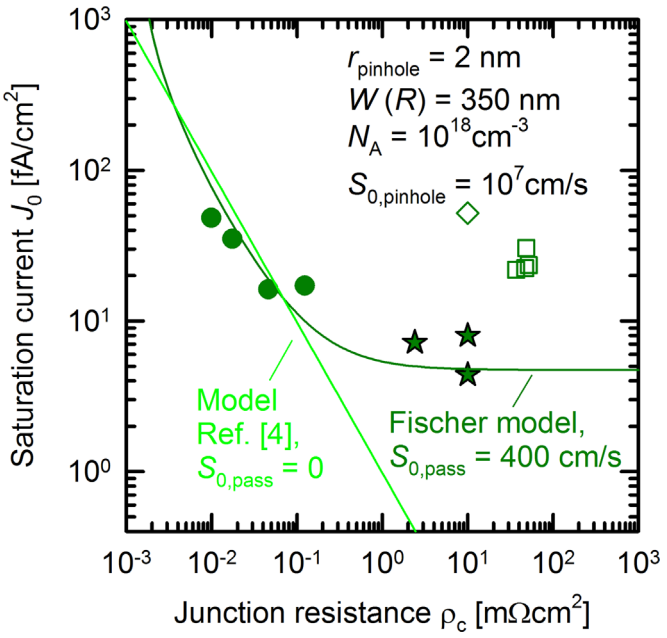

Fig. 7. Comparison of experimental ρ_c, J_0 values for p^+ poly-Si/*c*-Si junctions with two models: (*i*) the recent one presented in this work with $S_{0,pass}$ = 400 cm/s, and (*ii*) our previous model according to Ref. [4], which disregards the recombination at the *c*-Si/SiO_x interface.

in which recombination at the *c*-Si/SiO_x interface dominates. These data points can only be described correctly by our recent generalized model which takes into account a $S_{0,pass}$ value different from zero. This furthermore points out the importance of the interfacial oxide properties. Both, the *c*-Si/SiO_x interface state density and transparency for minority carriers have to be minimized.

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