

27.6% Perovskite/c-Si Tandem Solar Cells Using Industrial Fabricated TOPCon Device

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The tandem cell structure is the most promising solution for the next generation photovoltaic technology to overcome the single-junction Shockley–Queisser limit. The fabrication of a perovskite/c-Si monolithic tandem device has not yet been demonstrated on a c-Si bottom cell produced from an industrial production line. Here, a c-Si cell with a tunneling oxide passivating contact (TOPCon) structure produced on a production line as the bottom cell of a tandem device, and a top cell featuring solution-processed perovskite films to form the tandem device are used. The c-Si cell features a rough damage etched, but untextured front surface from the wafering processes. To combat the challenge of rough surfaces, several strategies to avoid shunt paths across carrier transport layers, absorber layers, and their interfaces are implemented. Moreover, the origin of reflection loss on this planar structure is investigated and the reflection loss is managed to below 4 mA cm⁻². In addition, the source of the voltage loss from the TOPCon bottom cell is identified and the device structure is redesigned to be suitable for tandem applications while still using mass production feasible fabrication methods. Overall, 27.6% efficiency is achieved for a monolithic perovskite/c-Si tandem device, with significant potential for future improvements.

1. Introduction

Organic–inorganic metal halide perovskites have shown great potential in multiple applications, particularly in photovoltaic (PV) devices, owing to their superior optoelectronic properties that can be obtained by solution processing.^[1–3] The bandgap of the perovskite film can be changed easily by modifying its composition.^[4] Compared to III–V high bandgap semiconductor materials, the perovskite film is low cost and easy to fabricate. This makes perovskite cells a potential candidate not only for single-junction but also multi-junction solar cells. Over the past 12 years, the power conversion efficiency of the perovskite solar cell has rapidly increased from 3.8% to 25.7%, which is over 80% of its thermodynamic limit.^[2,5] This great progress on single junction devices has been accompanied by equally impressive achievements on tandem

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devices, with efficiencies of well over 30% a clear possibility.^[6] Several impressive works have been reported in the past few years to improve the efficiency of monolithic perovskite/c-Si tandem devices,^[7–11] and the efficiency record is currently reported to be 29.8%,^[12,13] which is significantly more efficient than the current record for a single junction crystalline silicon solar cell (26.6%).^[14] The promising efficiency enhancement, in combination with low fabrication cost, means that perovskite/c-Si tandem technology is arguably the most competitive candidate as the next generation photovoltaic technology for mass production.

One significant challenge to mass production lies in the industrial silicon wafers used for solar cell fabrication. Following wafering and damage removal, the wafers have a micro-scale roughness on the surface which poses a challenge for common solution-processed perovskites; hereafter, we refer to this surface as “damage etched.” Chemo-mechanical polishing, which can reduce the roughness significantly, is too expensive for commercial PV production. The surface roughness following damage etching therefore represents the minimum roughness that the perovskite fabrication process must be able to handle. The roughness could be increased further through texturing, which increases the challenge but may also improve the optical properties of the tandem stack.

Sahli et al. demonstrated a two-step method to form the perovskite film conformally on top of a textured silicon surface. However, a vacuum thermal evaporation step for the deposition of PbI_2 was involved, which could significantly increase the cost of fabrication, and which may therefore not be suitable for mass production. Chen et al. and Hou et al. recently reported deposition of 0.5–1 μm thick perovskite films using solution processing on top of a sub-micron textured surface (<1 μm). It has been shown that thick perovskite films can fully cover a textured c-Si surface and form a planar perovskite surface on top.^[15,16] However it is challenging to endow such thick films

with high quality over a large area in a reproducible manner, because crystallization starts from the top surface to prevent solvents escaping during film formation.^[17] Additionally, the thick film introduces greater demands on the material quality—a greater bulk lifetime may be needed to ensure the carrier diffusion length remains sufficient for highly efficient current collection, and to retain a high open-circuit voltage (V_{OC}). Further, for industrial silicon wafers, the roughness is typically larger than 1 μm , and even such thick perovskite films may not be sufficient to ensure the fabrication of shunt path free tandem devices.

To closely partner with established industrial workflow, we report an approach to enhance both the efficiency and reproducibility of tandem devices on an industrially fabricated, tunnelling oxide passivating contact (TOPCon) c-Si bottom device. The c-Si cell employs an n-type silicon substrate. Cells based on n-type substrates generally display higher lifetimes and reduced degradation compared to cells based on p-type substrates, and are thus attractive for high efficiency devices. This device features a damage-etched (but not textured) top surface. These TOPCon sub-cells are immediately available by following a standard wafering and etching process commonly used in industry (Figure 1a). We fabricate the perovskite sub-cell conformally on the damage-etched front surface to mitigate the negative impacts of rough c-Si substrates, thus preventing shunt paths across carrier transport layers, absorber layers, and their interfaces in relevance. Moreover, we evaluate the photon harvest in the entire tandem layout with a focus on the optimization of the front transparent conductive oxide (TCO) to balance the reflectance and series resistance losses. In addition, we reveal the origin of electrical losses from the TOPCon sub-cell and demonstrate rear localized contacts with a mesa structure, which is feasible for mass production. As a result, a 27.6% efficiency (1- cm^2) was achieved for a monolithic tandem device using an industrially produced bottom c-Si cell with a TOPCon structure.

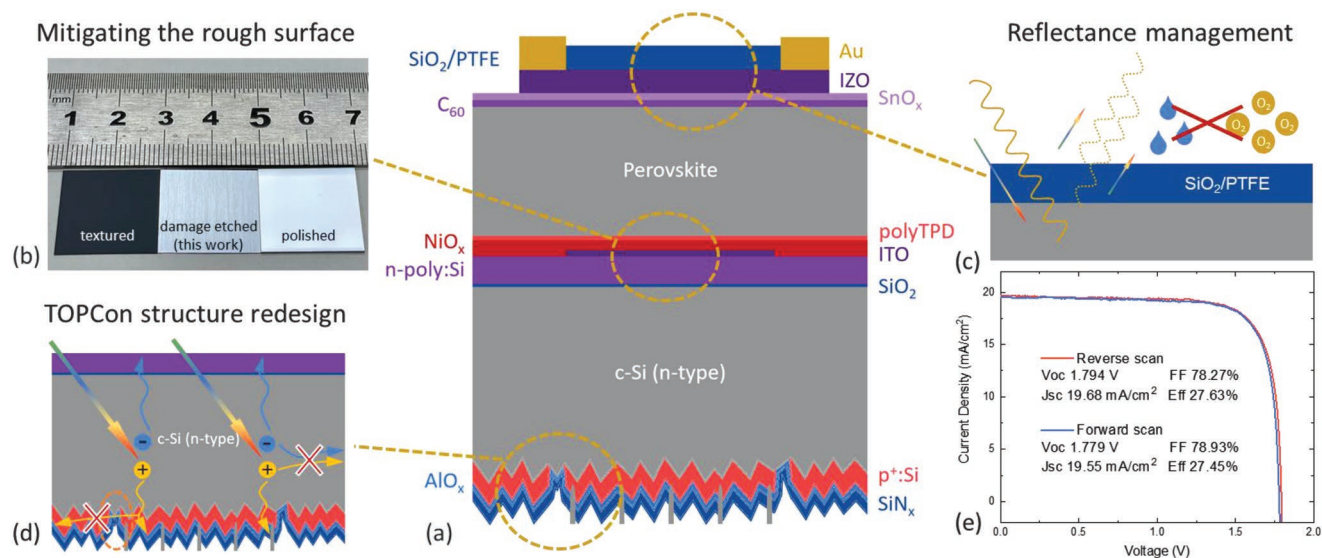


Figure 1. a) Schematics of the optimized monolithic perovskite/c-Si tandem cell fabricated in this work, b–d) illustration of the mitigation of the rough surface, reflectance management, and TOPCon structure redesign respectively. e) IV curves of the champion tandem device measured at AM1.5G with 1- cm^2 active area.

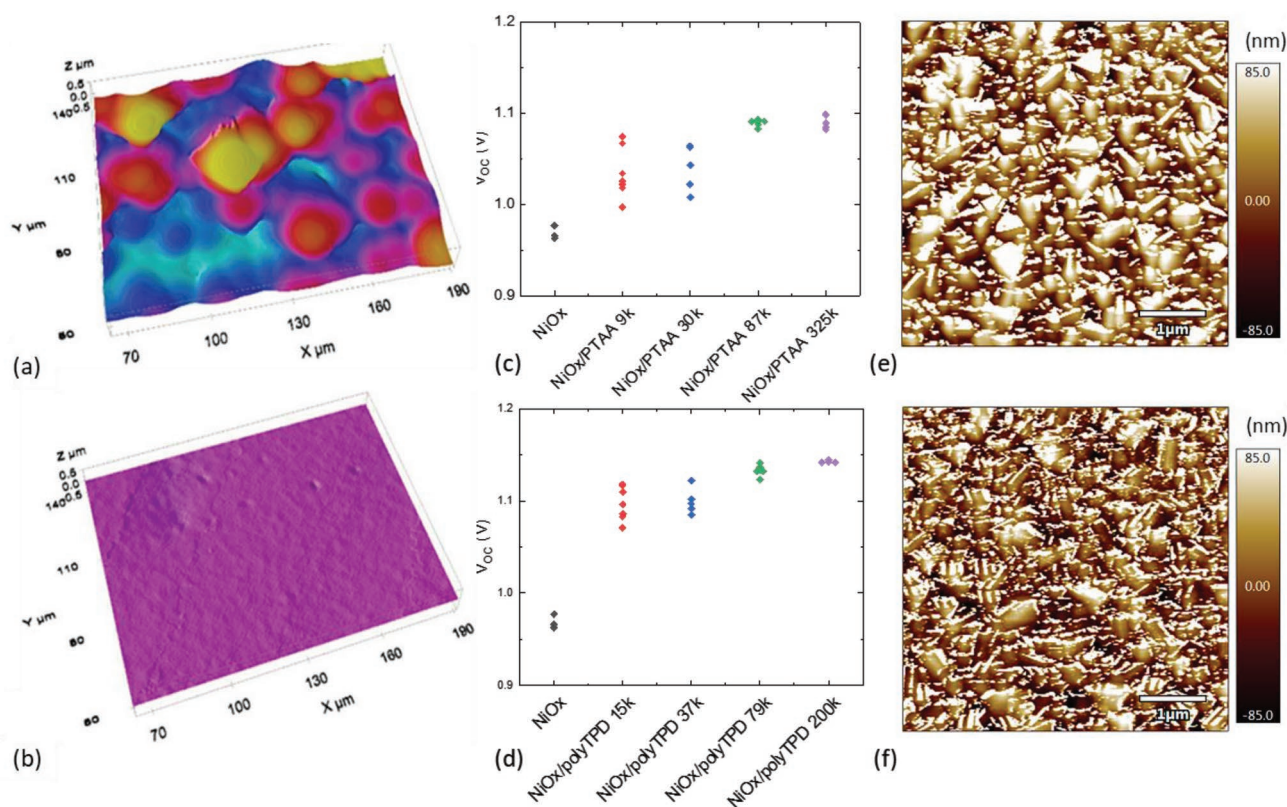


Figure 2. Confocal microscopy images of the surface morphology of a) damage etched and b) polished silicon surfaces (please note x and y-axes are not on the same scale as the z-axis). Statistics of the V_{OC} of opaque devices using c) PTAA and d) polyTPD interface passivation. CAFM and AFM image stack of e) polyTPD 15k and f) polyTPD 200k on top of the FTO glass.

2. Mitigating the Rough Surface

Figure 2a,b shows the surface morphology difference between a typical industrial and laboratory-grade, polished wafer. The industrial wafer surface is generally obtained from the diamond wire cutting process when wafering the silicon ingot, followed by a fast alkaline etch to remove the surface damage. It is not a textured surface, but a rough surface ($RMS > 1 \mu m$), which makes the subsequent deposition of perovskite films challenging. Currently, chemically-mechanically polished wafers are often used for solution deposition of perovskite absorbers. However, the use of such wafers in commercial production would dramatically increase the overall fabrication cost, rendering such devices uneconomic. The comparison of the reflectivity and surface morphology of these three types of wafer surfaces (polished, damaged etched and textured) can be found in Figures S1 and S2 (Supporting Information) and Figure 2a. Alternatively, vacuum deposition techniques can be used, which, unfortunately, slows down the throughput and hence increases fabrication costs. To overcome the challenge of depositing a shunt path-free perovskite top cell on top of the rough surface using a solution-processed perovskite film, here we employed a strategy that takes advantage of the synergetic effects of the functional layers and interfaces to minimize the shunting probability during device fabrication.

The first step was the use of a dense hole transport layer. Here we choose physical vapor deposition instead of solution

processing to sputter coat a 10 nm thick layer of NiO_x as the hole transport layer (HTL) to minimize the likelihood of pin-holes that can result in shunt paths. The sputter-coated film forms a dense and conformal layer on top of the rough silicon surface, as shown in Figure S3 (Supporting Information). However, the efficiency of p-i-n devices using NiO_x is lower than that using other HTLs such as poly(triaryl amine) (PTAA) or self-assembled molecules (SAMs),^[18–20] due to interface recombination losses.^[21] As seen in Figure 2c, the V_{OC} of the opaque device is relatively low with NiO_x as the HTL, with a V_{OC} deficit over 700 mV. In order to reduce recombination losses, here we insert a thin PTAA or poly(*N,N'*-bis-4-butylphenyl-*N,N'*-bisphenyl)benzidine (polyTPD) layer to passivate the interface between NiO_x and the perovskite film. Both polymers show significant V_{OC} enhancement (>100 mV) on the opaque device as shown in Figure 2c,d, which is consistent with the earlier reports.^[10,22]

We also studied the impact of the molecular weight of the polymers on the device's performance. Interestingly, as shown in Figure 2c,d, we found that opaque devices with higher molecular weight (Mw) PTAA and polyTPD show significantly better consistency of V_{OC} . With a rougher surface for tandem fabrication, a similar result is found on the tandem devices, shown in Figure S4 (Supporting Information). In earlier work, it was reported that low Mw polymers tend to form beads, but high Mw polymers tend to form fibers in the solution,^[23] which may result in better coverage on the rough surface. We carried out

conductive atomic force microscopy (CAFM) and atomic force microscopy (AFM) on thin polymer layers coated on top of FTO substrates. In Figure 2e,f, we superimposed the CAFM result on top of the AFM morphology result. The white patches on the image are where the CAFM measurement shows high current (i.e., high conductivity). Figure 2e shows significantly more and larger high current areas than Figure 2f. Since the polymer film has significantly lower conductivity than FTO glass substrates, it suggests that a high Mw polymer gives better surface coverage on the rough surface.

Secondly, we use the vacuum flash method to ensure conformal growth of perovskite films.^[24,25] Unlike the conventional anti-solvent method which introduces non-uniformity over a large area, the vacuum flash method uses a vacuum to extract the solvent in the wet film to facilitate nucleation. It is thus a feasible approach for the large area fabrication of perovskite films and tandem devices with satisfactory consistency.^[26] In this work, we further optimized this process for the methylammonium (MA⁺)-free high band-gap perovskite precursor (see Methods, Supporting Information). From the SEM result in Figure S5 (Supporting Information), the high bandgap perovskite film with the optimized process was found to be compact and smooth over a large area, and enabled an opaque device with over 18% efficiency.

In addition, the electron transport layer/buffer layer of SnO_x was deposited using atomic layer deposition (ALD), wherein a longer purge time was employed to form a dense layer. The thickness per cycle with various purge times is shown in Figure S6a (Supporting Information). The film growth follows a quasi-chemical vapor deposition (CVD) mode when the purge time is decreased, which compromises the film conformity significantly. Here we maximize the purge time after each pulse with a short pulse time, to ensure the SnO_x deposition step is in an ALD mode for better coverage. In Figure S6b (Supporting Information), the refractive index of the film with longer purge time is significantly increased, indicating enhanced film density. Though we are using a thinner film (7 nm) compared with all other reports using a similar structure,^[10,11,16,27] due to the exceptional conformality, the thin film shows superior quality for blocking the sputter damage and minimizing shunt paths. The low thickness is beneficial for reducing reflection losses, which will be detailed in the next section.

3. Reflectance Management

Light management is crucial for planar tandem devices to achieve high current output. We investigated the relationship between the top transparent conductive oxide (TCO) and the optical and electrical properties of the tandem device using combined optical and device simulation. We evaluated 3 TCO materials (ITO, indium zinc oxide (IZO) and indium tungsten oxide (IWO)) and tested the optical and electrical performance of the sputtered thin films (Figures S7 and S8, Supporting Information). We found that for room temperature sputtering, IZO shows superior optical and electrical properties, and this material was chosen for the top electrode of our tandem devices.

As shown in Figure 3a, the reflection loss strongly depends on the thickness of the front IZO layer. When the film is less

than 50 nm thick, the UV to visible reflection loss is mainly at wavelengths less than 400 nm, which is insignificant due to both low photon flux and internal quantum efficiency in this range. When the thickness of the film increases, the reflection peak starts to redshift and an additional reflection peak at 700 nm emerges. We summarize the simulated reflection loss, the IZO parasitic absorption loss, and the total generation of the tandem device in Figure 3b along with the sheet resistance (film thickness). We found the total generation starts to drop rapidly once the sheet resistance drops below 120 Ω □⁻¹ (thickness above 40 nm).

However, reducing the thickness of the TCO layer will increase the sheet resistance of the film, and hamper the lateral carrier transport. To quantify the loss, in Figure 3c, we simulated the resistive loss based on the finger pitch width and the sheet resistance of the front IZO film for a 1-cm² device (finger width 50 μm, height 200 nm). As expected, with decreased pitch width and sheet resistance, the resistive loss drops. But as we discussed earlier, this leads to increased reflection and absorption losses. Further, a reduced pitch width introduces more reflection loss from the metal fingers. We combined Figure 3b,c to find the sweet spot for minimal power loss due to both optical and electrical limitations. Assuming a V_{OC} of 1.8 V and a FF of 80%, we found a sheet resistance of 160 Ω □⁻¹, with 3.3 mm finger pitch, minimized overall power loss. Considering the similar refractive index of C₆₀ (2.16@500 nm), ALD deposited SnO_x (1.93@500 nm) and the sputtered IZO film (2.03@500 nm), the front reflectance loss is determined by the overall thickness of the top electron transport layer stack and the TCO layer. Hence, it is important to keep the C₆₀ and SnO_x layers as thin as possible to leave the IZO film thick enough for good lateral conductivity while keeping front reflectance low. From the simulation result, the device is not sensitive to the finger pitch due to several reasons. Firstly, evaporated fingers still have limited conductivity since they are relatively thin compared to the “tall” fingers produced by screen printing or electroplating. More importantly, the tandem device has less than half of current density compared with silicon device, and therefore it is significantly more tolerant to the resistive loss introduced by the front electrode. As illustrated in Figure 3d, overall, for a 1-cm² tandem device, the front optoelectrical loss is more sensitive to the thickness of the TCO layer due to the optical loss. Therefore, for the ease of fabrication, the front metal electrode for tandem device presented in this work is grid free.

In addition, we investigated the reflection loss due to the recombination layer between two sub-cells. The ITO film for the recombination layer does not introduce additional parasitic absorption losses but impacts total reflection loss. This is due to the considerable refractive index mismatch between ITO (1.97@800 nm) and the materials on either side which are poly:Si (3.67@800 nm) and NiO_x (2.20@800 nm). To minimize reflection loss at this interface, some authors have reported a recombination layer free design.^[28,29] However, NiO_x and n-poly:Si cannot form an ohmic contact.^[30] The alternative is to minimize the thickness of the recombination ITO layer, so that the reflection loss from this interface due to the refractive index mismatch becomes insignificant, as shown in Figure S9 (Supporting Information). Here we reduce the thickness of the ITO

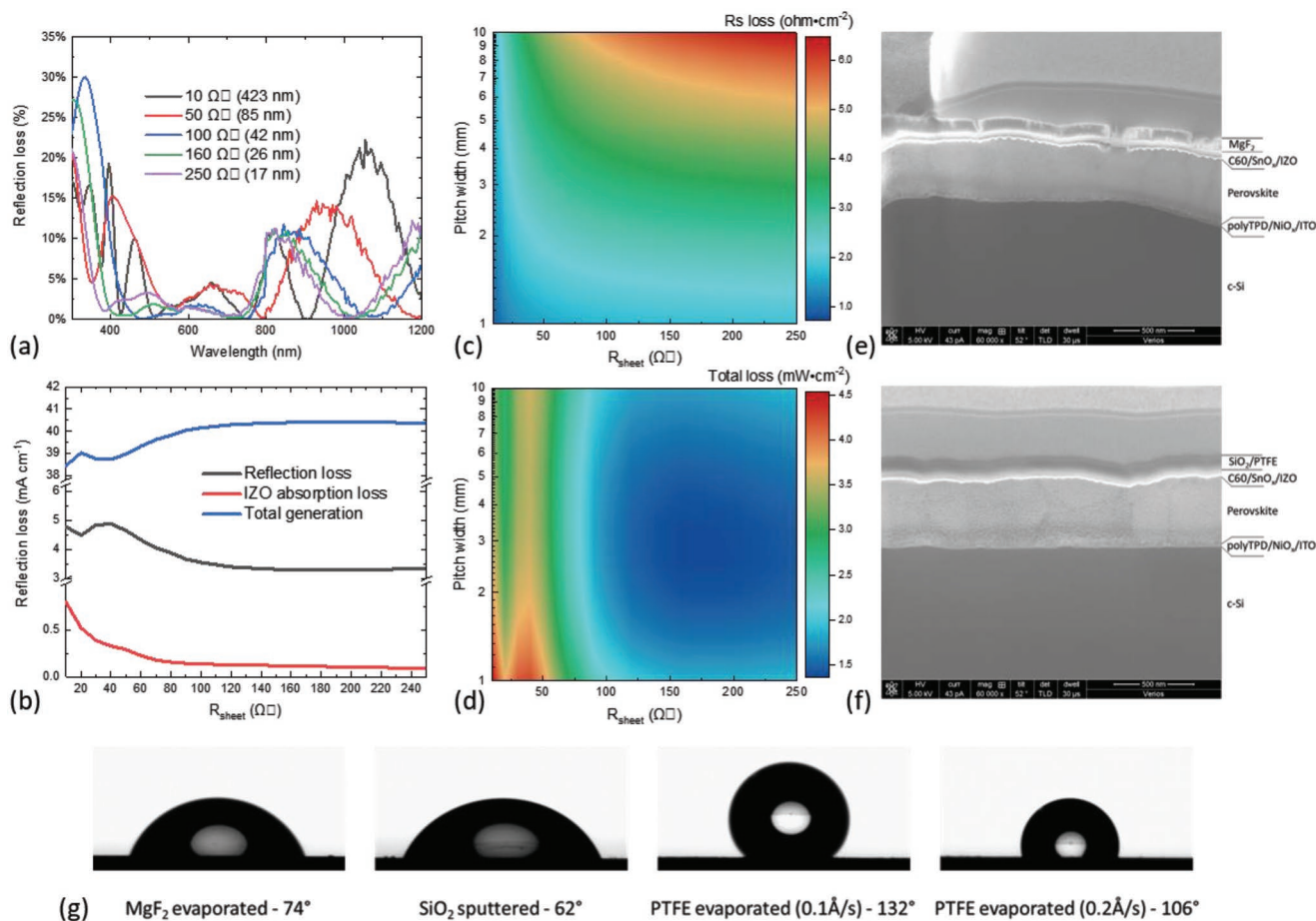


Figure 3. a) Simulated reflection spectrum of the tandem device versus variable IZO thickness, b) Integrated losses (reflection and IZO parasitic absorption loss) and total carrier generation (perovskite + c-Si) from both the perovskite and the c-Si active layers, c) simulated R_s loss for a 1-cm² device due to the front electrode, d) simulated total loss (optical + R_s) due to the front electrode. Cross-section SEM images of the tandem device with e) MgF₂ and f) SiO₂/PTFE stack as AR film, g) water contact angle measurement of the MgF₂, SiO₂, and PTFE thin films.

layer to 2 nm, which enables an ohmic contact between NiO_x and n-poly:Si while minimizing the reflection loss.

MgF₂ is commonly used as anti-reflection (AR) coating to further reduce the reflection losses of tandem cells. From the cross-sectional SEM image shown in Figure 3e, the thermally evaporated MgF₂ film shows cracks within the film, which facilitates the penetration of water or oxygen, reducing device lifetime. To form a compact AR layer, we thus deposited an SiO₂ film using reactive sputtering with a Si target. Different from thermal evaporation, ions have significantly higher kinetic energy when reaching the substrate and form a dense layer. However, SiO₂ is also hydrophilic, with a water contact angle of 62° (74° for MgF₂), as shown in Figure 3g. To combat the issue, we thermally evaporated a thin layer (20 nm) of polytetrafluoroethylene (PTFE) on top of the SiO₂, which increases the water contact angle to 132°. The cross-section in Figure 3f shows the AR film with an SiO₂ and PTFE stack is dense and continuous. Optically, the SiO₂ and PTFE composite AR layer exhibit negligible absorption with a refractive index comparable to MgF₂ (Figure S10, Supporting Information). The simulated reflection spectra with both MgF₂ and SiO₂/PTFE are similar (Figure S11, Supporting Information), indicating the SiO₂/PTFE stack can

serve as both a robust barrier layer and an excellent AR coating for the tandem device.

4. Design of the TOPCon Bottom Cell

In this work, we obtained the silicon bottom cell from an industrial production line. The cells were fabricated on a 164 × 164 mm² size wafer with a TOPCon structure. However, we found that with this device structure, the c-Si device exhibited a significantly lower V_{OC} (681 mV without shadow mask, 648 mV with shadow mask) than expected (implied V_{OC} 706 mV) under one-sun conditions, as shown in Figure 4a.

To understand the origin of this loss, we developed a 3D full device simulation in Quokka3^[31] similar to the structure shown in Figure 4a. The simulated result is listed in Table S1 (Supporting Information), using a silicon sub-cell generation profile in the tandem structure shown in Figure S12 (Supporting Information). For full area illumination, we excluded the shading from both the busbar and the shadow mask. For active area illumination, only the 10 × 10 mm area is illuminated. Finger shading is included for both conditions. From the simulation

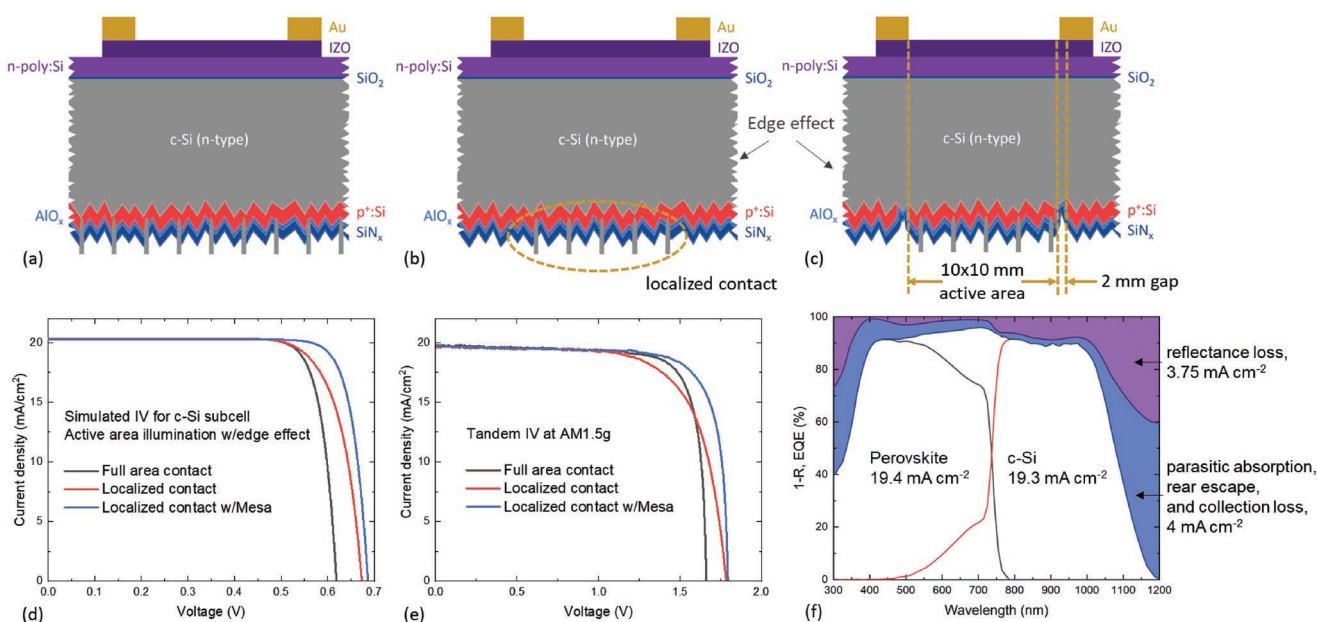


Figure 4. Schematics of c-Si cell test structures; a) full area contact, b) localized contact, c) localized contact with mesa structure for device simulation (substrate size 23×23 mm, active area 10×10 mm); d) Simulated IV curves of the c-Si device under active area illumination with edge recombination included; e) Measured reverse scan IV curves of the tandem device with different rear contact structures; f) Measured reflectance and external quantum efficiency curves of the tandem cell.

result, we find a substantial V_{OC} (42 mV) drop between full area and active area illumination. Moreover, the four edges contribute an additional 31 mV loss to the V_{OC} , which adds up to a total 73 mV V_{OC} drop due to the recombination at the edges of the substrate. To minimize the edge effect, we developed another two structures for the rear contact, namely the localized contact, and localized contact with mesa structure, as shown in Figure 4b,c, which are designed to primarily confine the majority carriers (holes) on the rear side to the active area and prevent recombination at the cell edges.

The simulation result of these two structures can be found in Table S1 (Supporting Information) and Figure 4d. Compared with the conventional device, the device with localized contact structure shows a V_{OC} loss of 21 mV, while the loss with the rear mesa structure is only 9 mV. Interestingly, simulation results show a significantly higher fill factor in the design with the mesa structure when edge recombination is included. The reduction in V_{OC} is mainly from the recombination of the metal on the rear side. When the illumination type is changed from full area to active area, the carriers generated in the active region will flow to the dark area due to the carrier concentration gradient and recombine. Therefore, the drop in V_{OC} is lower for the localized contact design. The difference is further amplified with the inclusion of edge recombination. Comparing the simulation of the localized contact design with and without mesa structure, it is obvious that the rear boron emitter facilitates the transport of carriers from the active illumination area to the area in the dark. Hence, the mesa structure can reduce this recombination loss and lower the V_{OC} drop. The mesa structure can also reduce non-ideal recombination, namely J_0 from the edge, which is observed from the FF improvement with mesa.

We fabricated full tandem devices based on the 3 different rear side designs and compared their performance (Figure 4e

and Figure S13, Supporting Information). The device with full area contact shows significantly lower V_{OC} compared with localized contact with or without mesa. Compared with the cell with localized contact but no mesa, the cell with mesa structure shows a slightly better V_{OC} , but a significantly better FF, which is in line with the simulation result. The external quantum efficiency and V_{MPP} tracking result of the device are shown in Figure 4f and Figure S14 (Supporting Information). The best efficiency on a 1-cm^2 device reaches 27.6% based on the localized contact with mesa structure, indicating its effectiveness.

5. Loss Analysis and Outlook

To improve the efficiency of the tandem device in the future, we analyze the major losses of the tandem device based on the above configuration. The voltage loss comes mainly from the perovskite device. As seen in Figure 5a, we fabricated three test structures to evaluate the implied V_{OC} using photoluminescence measurements. For quartz/perovskite, the measured implied V_{OC} is 1.25 V, which is a ≈ 430 mV voltage deficit from its bandgap (1.68 eV), or a ≈ 150 mV deficit compared to its Shockley–Queisser limit. The reason for this large voltage deficit in high bandgap mixed cation/halide perovskites may be related to halide or cation segregation and imperfections within the perovskite absorber.^[32,33] With respect to the interfaces, the voltage loss from the perovskite/hole transport layer interface is relatively small (≈ 10 mV) when polyTPD is used. However, the perovskite/C60 interface results in a significant loss of ≈ 70 mV.^[11,34]

The voltage loss from the silicon sub-cell is less significant, but the rear passivation can still be improved. As seen in the recombination loss analysis in Figure 5b, the rear

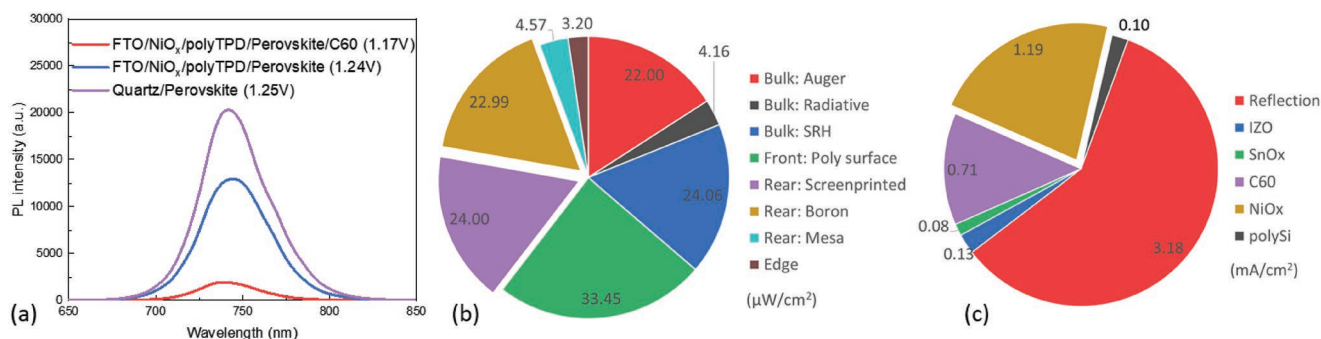


Figure 5. a) PL spectra of perovskite top cell test structures, b) recombination loss analysis of the c-Si bottom cell based on the device simulation, c) optical loss analysis of the tandem device based on ray-tracing simulation (no front metal finger).

recombination loss amounts to one-third of the total recombination loss. Currently, the rear side of the device is passivated with an Al₂O₃/SiN_x stack on the non-contact area, while the contact area is in direct contact with the screen-printed metal fingers. The latter contributes a significant portion of the recombination loss here. One way to minimize the loss is to introduce a double sided poly:Si structure, where the front and the rear side of the cell is contacted by n-poly:Si and p-poly:Si respectively to minimize the recombination loss in the contact area.

In the previous section, we have achieved the lowest optical loss reported to date for this device configuration through careful light management. We analyze the breakdown of the optical loss in Figure 5c, wherein the reflection loss accounts for most of the optical loss. As shown in Figure 3a, the most intensive reflection loss with IZO is due to the substantial mismatch of the refractive index between the polyTPD/NiO_x/ITO stack and the c-Si bottom cell as shown in Figure S15 (Supporting Information). In our previous work, we used a homo-junction c-Si as the bottom cell, and a layer of high refractive index SiN_x ($n = 2.9@800\text{ nm}$) to reduce the mismatch.^[26] However, this approach cannot be employed when a TOPCon device is used; in this case, the refractive index matched material must also be electrically conductive. For the tandem device using a heterojunction c-Si cell as the bottom cell, Mazzarella et al. developed a conductive nc-SiO_x:H ($n = 2.6@800\text{ nm}$) interlayer to minimize the effect of mismatch.^[35] However, this material is not suitable for the perovskite top cell used here, which features a high-temperature fabrication process. Hence, to further minimize the reflection loss for the planar tandem device, a material with a high refractive index and good temperature stability, conductivity and infrared transparency is needed. Another alternative is to use a sub-micrometer textured surface as front structure to reduce the infrared reflection loss.^[15,16]

There is also room for improvement in reducing the parasitic absorption loss. In our device, it is the NiO_x that leads to the most significant parasitic absorption loss. Our results suggest film absorption is related to the deposition conditions, in particular the O₂/Ar ratio (Figure S16, Supporting Information), which significantly affects film crystallinity (Figure S17, Supporting Information). It thus requires further effort to reduce the parasitic absorption loss of NiO_x, or to find a replacement in the future. C₆₀ is responsible for the second biggest parasitic absorption loss in this device. We reduced the thickness of the C₆₀ film to 10 nm to minimize the absorption loss. However,

further reduction of film thickness leads to substantial V_{OC} drop (Figure S18, Supporting Information), which is likely due to the insufficient hole blocking capability as a result of non-continuous film coverage. This indicates a more transparent but compatible electron transport material may need to be developed.

6. Conclusion

In summary, we systematically investigate strategies to mitigate the impact of the damage etched, rough silicon surface on device performance. Further, we investigate the origin of reflection losses in a planar structure, and design a bottom cell c-Si for the tandem structure that is based on the TOPCon structure, but with some modifications to improve the performance of the c-Si cell. We report a facile method to uniformly passivate the micron-scale damage etched rough surface of the industrially fabricated c-Si devices using high molecular weight polyTPD to largely suppress the interface recombination and enhance the reproducibility. Together with sputtered NiO_x, a vacuum flashed perovskite film and an ultra-dense film of ALD deposited SnO_x, the resulting perovskite/c-Si tandem device is found to display excellent reproducibility. Using ray tracing and device simulation, the balance between reflection loss and resistive loss is optimized to minimize the overall power output loss. An SiO₂/PTFE AR coating stack is presented to serve as a barrier layer for better stability. We further redesign the structure of the commercially fabricated c-Si device, incorporating a mesa structure while still using the mass production feasible fabrication methods. As a result, an efficiency of 27.6% is obtained. The methods discussed above could help in the commercialization of low-cost and efficient perovskite/c-Si tandem solar cells.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

P.Z., M.X., B.L., J.Y., X.Z., and H.J. are from Jinko Solar, one of the world's largest solar panel manufacturers.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

damage etched, industry, perovskites, silicon, tandem

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