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Long-term and annealing stable, solderable PVD metallization with optimized Al diffusion barrier

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Abstract

Since passivated emitter and rear cells (PERC) and other silicon solar cell concepts with evaporated aluminum (Al) as rear metallization are incompatible with a common solder process, in this work an annealing stable, solderable and long-term stable metallization scheme deposited by physical vapor deposition (PVD) is developed. The solder stack that complements the Al metallization consists of sputter deposited TiN/Ti/Ag or TiN/NiV/Ag, whereby the TiN layer serves as a diffusion barrier against Al. It is therefore optimized by varying sputter parameters and by stuffing the grain boundaries with oxygen. On the optimized stack a cell-interconnector can be conventionally soldered even after a strong annealing step of 15 min at 425°C, which sets this concept apart from other PVD metallization approaches. Cell efficiency is not influenced by the solder stack compared to a reference rear metallization by plain evaporated Al. Additionally, long-term stability of the solder-joints on the metallization scheme is investigated by thermal aging of solder-joints and thermal cycling of demo modules with PERC cells.

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Keywords: PVD metallization, evaporated Al, solderability, diffusion barrier, TiN, long-term stability

1. Introduction

For the rear metallization of high-efficient, industrial silicon solar cells PVD Al represents a promising alternative to screen-printing. It is favorable regarding optical and electrical properties, it enables reduced material consumption, including costly silver, and is suitable to contact both n+ and p+ regions on advanced solar cell concepts like BC-BJ structures [1,2]. A major drawback for industrial application and commercialization is the formation of a native oxide on the Al layer which hinders a conventional solder process and thus a state-of-the-art module integration. If an Al layer is combined with just a solderable top layer like sputtered Ag or NiV/Ag, it is not

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compatible with a common solder process after an annealing step that is usually required after cell metallization by PVD at the end of solar cell processing [3]. We are aware that it is crucial to protect the solderable top layer from Al indiffusion since it is the formation of Al oxide on the Ag surface which prevents solderability after an annealing step [4]. At the end of solar cell processing an annealing step in forming gas (FGA) is common if it improves passivation quality and/or contact resistance, e.g. for PERC or BC-BJ structures with SiO_x passivation and/or PVD metallization. Depending on the specific cell concept, used annealing conditions vary, but most of these cell concepts benefit most from annealing steps between 2 min at 300°C and 15 min at 425°C. Since Al diffusion is identified as the crucial process that prevents solderability, it has to be suppressed by an additional Al diffusion barrier. Therefore we introduce a sputtered TiN layer as an Al diffusion barrier, and a thin sputtered Ti layer is added to achieve a sufficient adhesion between Ag and TiN layers [5]. Alternatively, the TiN barrier layer is combined with a solderable NiV/Ag capping as in Ref. [6].

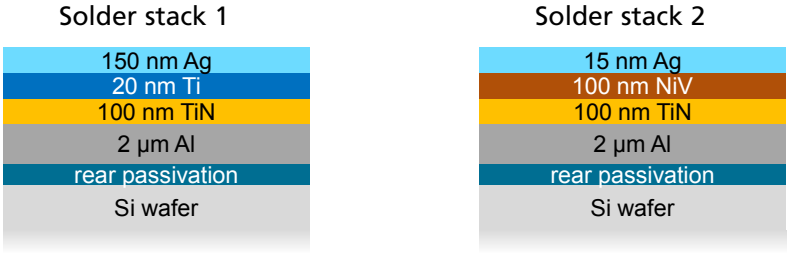

Fig. 1: Schematic view of solderable PVD metallization concepts with evaporated Al and sputtered solder stacks (including typical layer thicknesses)

It is possible to deposit these solder stacks, consisting of sputtered TiN/Ti/Ag (stack 1) or TiN/NiV/Ag (stack 2) as shown in Fig. 1, in a single deposition sequence together with an evaporated Al metallization using an ATON 500 PVD machine without breaking the vacuum. The TiN diffusion barrier enables soldering of a standard cell interconnector to the rear metallization with a conventional solder process even after annealing, thus enabling an industrial, state-of-the-art module integration.

2. Experimental

For the deposition of the metallization scheme an ATON 500 industrial prototype PVD machine is used. The Al layer is thermally evaporated in the evaporation chamber and in the same process sequence the solder stack TiN/Ti/Ag is sputtered in the sputter chamber that contains two targets, e.g. a Ti target and an Ag target. They can be used one by one with Ar as working gas. The TiN layer is reactively sputtered from the Ti target with additional N_2 gas in the process atmosphere. Cathode power, tray velocity and Ar and N_2 gas flows can be varied and we can therefore influence the composition of the sputtered TiN layer at a given cathode power by varying the N_2-to-Ar gas flow ratio. Additionally, ambient air can be let into the sputter chamber through a valve. Infrared (IR) heaters are installed close to the sputter chamber to allow preheating of the samples. The deposition temperature is measured with a Datapaq logger and thermocouples which are conductively glued to the wafers.

To characterize the sputtered TiN layers, we determine their specific electrical resistivity and density. TiN layers are deposited on polished and saw damage-etched Cz Si wafers and the specific resistivity of these TiN layers is measured by sheet resistance measurements with a 4-point-probe. The layer thickness is determined by AFM measurement over a prepared step. By measuring the mass of wafers before and after TiN deposition the density is determined. SEM images are taken to gain insight into the microstructure of the TiN layers.

To investigate the barrier quality of the TiN layer we proceed as described in Ref. [5]. We deposit the PVD metallization scheme with evaporated Al and the sputtered solder stack of 100 nm TiN, 20 nm Ti and 150 nm Ag on saw-damage etched Cz Si wafers which then undergo different annealing steps in forming gas (FGA). If subsequently a soldered cell-interconnector proves sufficient adherence of >1 N/mm in a 90°-peel-test, as required by standard DIN EN 50461, we conclude that Al could not overcome the TiN barrier despite the elevated temperature during the previous annealing step. If the solder attempt on the metallization fails due to weak wetting

and/or silver leaching or shows insufficient stability in the peel-test, it is concluded that Al has diffused to the Ag top layer and the barrier has failed.

The long-term stability of the solder-joints is tested by thermal ageing. The metallization schemes of stack 1 and stack 2 are deposited on saw-damage etched Cz Si wafers. Subsequently, the samples are annealed in forming gas for 2 min at 300°C and a common cell-interconnector with Cu core and a SnPbAg solder coating is soldered onto the metallization. For the accelerated ageing the soldered samples are then stored on a hotplate at an elevated temperature in N_2 atmosphere and all samples are aged for different amount of times. To investigate the aging duration at which the solder joint degrades at a defined ageing temperature, the interval between the longest time the solder-joint survives and the shortest time after which it fails is determined (and depicted in the result diagram Fig. 2). The degradation time is estimated to be in the middle of this time span. The solder-joint stability is evaluated by a 90°-peel-test, which is passed if the peel force of the solder joints is higher than >1 N/mm. Furthermore, to determine a relationship between solder-joint stability and temperature, e.g. an Arrhenius law, this is repeated with different samples at three temperatures: 130°C, 140°C or 150°C.

Additionally, the developed metallization scheme is applied to solar cells. Therefore n-type PERT (Passivated Emitter and Rear Totally diffused) solar cells are fabricated from 156 mm n-type Cz Si wafers. The cells possess a diffused p+-doped emitter on the front side and an n+-doped back surface field on the rear side. The front side is metallized and contacted by screen-printing and a fast-firing step. The passivation on the rear side is locally opened by laser ablation. Then the rear side is metallized with one of three PVD metallization schemes listed in Table 1 and forming gas annealed to improve the contact resistance. Finally, the cell efficiency is measured.

Table 1: PVD metallization schemes applied on n-type PERT solar cells to evaluate influence on cell efficiency

Group	# cells	Metallization scheme
I - Stack 1	11	2 µm Al / 100 nm TiN / 20 nm Ti / 150 nm Ag
II - Stack 2	10	2 µm Al / 100 nm TiN / 100 nm NiV / 25 nm Ag
III - Reference	11	2 µm Al

Furthermore, to investigate long-term stability of the metallization and interconnection on cell and module level, 5 demo modules with 4 PERC cells each are fabricated. The front side metallization is conventionally screen-printed, whereas the cells' rear sides are metallized with three different metallization schemes as listed in Table 2.

Table 2: Metallization schemes of PERC solar cells in 4-cell demo modules that undergo thermal cycling. For details of stack compare Fig. 1.

Group	# modules	Metallization scheme
A - PVD stack 1	2	2 µm Al / 100 nm TiN / 20 nm Ti / 150 nm Ag
B - PVD stack 2	2	2 µm Al / 100 nm TiN / 150 nm NiV / 15 nm Ag
C - SP Reference	1	Screen-printed with Al paste and Ag solder pads

Module integration of all cells is realized with a conventional solder process and common cell-interconnectors. The power output of the modules is measured before and after 200 cycles of thermal cycling (TC200) between -40°C and +85°C, according to standard IEC 61215, to evaluate and compare the according power loss. Afterwards the same modules undergo 1000 h of damp heat testing (DH1000) at 85°C at a relative humidity of 85% and then additionally 10 cycles of humidity freeze testing (HF10) with cycles between -40°C and 85°C at a relative humidity of 85%, each according to standard IEC 61215.

3. Barrier optimization

For the PVD metallization concept it is vital that the TiN layer is optimized regarding its barrier quality to prevent Al diffusion even during a typical annealing step. It was reported that TiN is most effective against Al diffusion when it has a dense microstructure and a stoichiometric ratio of 1:1, which coincides with the minimum of the specific resistance [7]. We can influence the composition of the sputtered TiN layer and thus the specific resistivity by varying the cathode power and the N_2/Ar gas flow. We obtain the global resistivity minimum of

58 µΩcm at an N_2-to-Ar-ratio of 1.40 at 30 kW cathode power under IR heating. Here the TiN layer is stoichiometric and it presents the global maximum within the process parameters of the machine. This TiN layer has a densified, columnar microstructure. In spite of the TiN process optimization, the vertical grain boundaries in the TiN layer offer relatively fast diffusion paths for vertical diffusion processes. This can be prevented by "stuffing" the grain boundaries. When oxygen is brought into the grain boundaries of the TiN layer, it forms Al_2O_3 with up-diffusing Al. As Al_2O_3 is known to be a very efficient diffusion barrier against Al, this stuffed TiN is a more efficient diffusion barrier than pure TiN [8]. We introduce this concept to the TiN layer in our metallization scheme (see Fig. 1) by interrupting the deposition sequence after sputtering the TiN layer. The samples are unloaded and exposed to atmosphere ('atmospheric stuffing') before Ti and Ag layers are added in a second deposition process. To evaluate the barrier quality of the stuffed TiN compared to the optimized, 'unstuffed' TiN (without process interruption), barrier structures with both TiN types are annealed under different conditions and subsequently soldered and peel tested. The results are listed in Table 3.

Table 3: Results of solder and peel tests on Al layer with solder stack 1 with 100 nm optimized, unstuffed TiN and 100 nm atmospherically stuffed TiN after different annealing conditions

TiN type	*10 min 350°C*	*10 min 400°C*	*15 min 425°C*
Unstuffed TiN	ok	fail	
Atmospherically stuffed TiN	ok	ok	ok

Table 3 shows, that samples with the optimized TiN barrier, deposited at 30 kW and 230°C, can successfully be soldered with sufficient adhesion after a moderate annealing step of 10 min at 350°C (denoted 'ok' in Table 3), but fail solder attempt or peel test after annealing for 10 min at 400°C (denoted 'fail' in Table 3). In contrast, the stuffed barrier is stable even after annealing for 15 min at 425°C, which confirms a highly improved barrier quality of the stuffed TiN.

Additionally, as annealing conditions of 15 min at 425°C are hardly ever exceeded in a final FGA of cell processing, the barrier quality of the stuffed TiN is considered sufficient for all common cell structures. However, the presented stuffing procedure requires an interruption of the deposition process and breakage of the high vacuum which entails considerable additional process costs in an industrial application. In order to clear this obstacle, an in-situ stuffing process within the PVD machine is developed in the following.

4. In-situ stuffing

The stuffing procedure is simplified by installing a valve to the sputter chamber. Thus, ambient air can be let into the process chamber to make oxygen available for a stuffing process after TiN deposition in-situ (without vacuum breakage). The barrier results in Table 4 show that the in-situ stuffed barrier is more stable than the unstuffed version, but significantly less stable than the atmospherically stuffed TiN layer. The reduction of the stuffing effect by in-situ stuffing is not surprising since the diffusion of oxygen into the grain boundaries is driven by Fick's law and thus the concentration gradient.

Table 4: Results of solder and peel tests on Al layer with solder stack 1 with 100 nm thick TiN layers (unstuffed, atmospherically stuffed and in-situ stuffed) after different annealing conditions

TiN type	*10 min 350°C*	*1 min 425°C*	*3 min 425°C*	*15 min 425°C*
Unstuffed	ok	fail		
In-situ stuffed	ok	ok	fail	
In-situ stuffed with IR heaters	ok	ok	ok	ok
Atmospherically stuffed	ok	ok	ok	ok

The partial pressure or the O_2 during in-situ stuffing is reduced by about 5 orders of magnitude compared to atmospheric stuffing. Therefore, instead of extending the time, we accelerate the stuffing procedure by increasing the sample temperature with the IR heaters to 250-280°C. We find that the barrier quality of in-situ stuffed TiN at elevated temperatures is sufficient to survive an annealing step for 15 min at 425°C, see Table 4. In-situ stuffing with heating can therefore replace atmospheric stuffing and enables a similarly stable barrier quality that is sufficient for all common cell structures. Additionally, it is an industrially applicable process.

5. Long-term stability of solder joints

Long-term stability of solder joints is an important issue regarding industrial application, therefore common cell interconnectors are soldered on the presented atmospherically stuffed and annealed metallization stacks and their long-term stability is estimated by a thermal aging investigation. We find that the durability of solder-joints on a stuffed Al/TiN/Ti/Ag (stack 1) metallization increases with the Ag layer thickness. Whereas a solder joint on a solder stack with 50 nm Ag starts to fail after about 20 h of thermal ageing at 130°C, solder joints on a stack with 100 nm Ag only start failing after about 100 h. The aging time until a solder-joint fails is observed to rapidly shorten for both Ag layer thicknesses by 1.5 to 2 orders of magnitude when the temperature of the aging process is increased by 20 K. We assume that similar to the procedure described in Ref. [6] the Ag top layer is consumed in an intermetallic reaction with the solder material whose kinetics can be described by an Arrhenius law as in (1).

$$k(T) = k_0 \cdot e^{-E_A / k_B \cdot T} \tag{1}$$

The thickness of the 'consumed' layer t_c is then given by (2),

$$t_c = 2\sqrt{k(T) \cdot t} \tag{2}$$

and we assume that the solder-joints fail when t_c reaches the initial Ag layer thickness of 50 nm or 100 nm Ag respectively. From the peel-test results after ageing at T = 130°C, 140°C, 150°C we get values for $k(T)$ which we plot in Fig. 2. The data of the 50 nm Ag stack is linearly fitted through the obtained interval and values for k_0 and the activation energy E_A are derived.

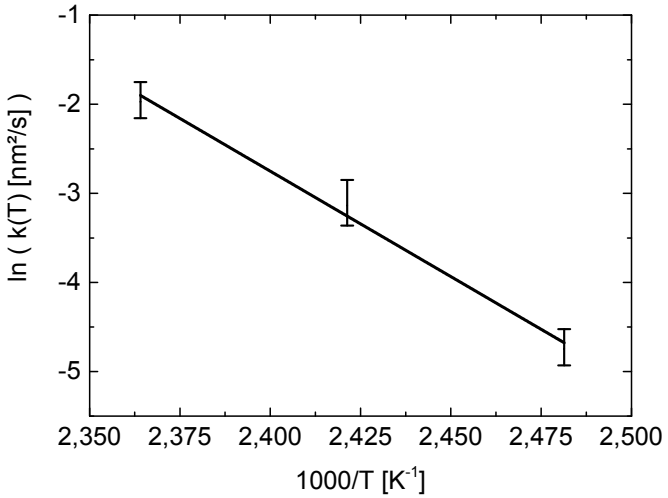

Fig. 2: Arrhenius diagram with linear fit for consumed layer of 50 nm Ag layers on solder stack 1 during thermal ageing.

The activation energies is found to be E_A = -197 kJ/mol. If this result is convoluted with the module temperatures on a German site as in Ref. [6], we obtain a yearly silver consumption of 4.65 nm. Therefore 150 nm Ag in solder stack 1 are expected to be sufficient for a module lifetime of 30 years on a German site. Cell-interconnector that are soldered after annealing on an Al/TiN/NiV/Ag metallization scheme (stack 2) with 50 nm NiV and 15 nm Ag show a strong adhesion even after thermal ageing for 360 h at 130°C and even 150°C. Since a failure of the solder-joints has not yet been observed an Arrhenius law cannot be obtained. However, the high stability after this extensive thermal ageing is considered also very promising regarding long-term stability.

6. Application to solar cells and module testing

To prove the applicability of the metallization scheme to industrial solar cells, n-type PERT solar cells are fabricated with both solder stacks and with a pure PVD Al reference group, see Table 1. The efficiencies η_i of all i=1..32 cells are measured and the median efficiencies of the different metallization groups are calculated. All results are depicted in Fig. 3 in relation to the median efficiency of the Al reference group η_m, i.e. the difference $\Delta\eta_i = \eta_i - \eta_m$ in absolute percent.

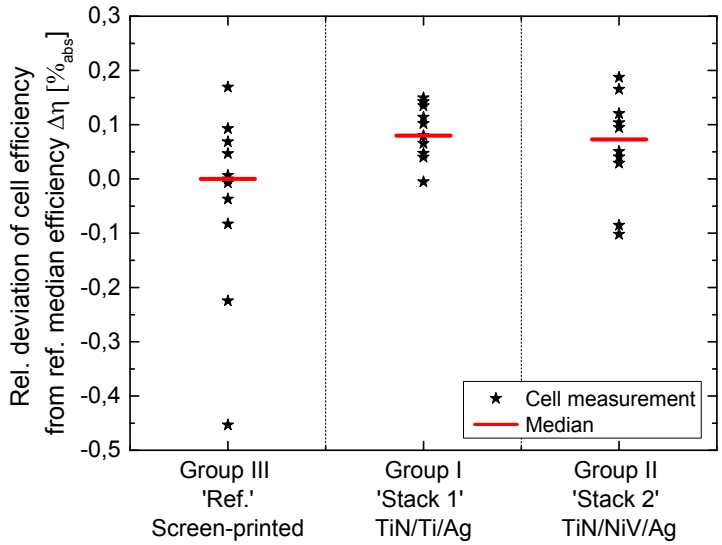

Fig. 3: The difference between the measured cell efficiencies and the median efficiency of the reference Al group III is depicted in absolute percent. Additionally, for each group the median efficiency is depicted. The results show that the efficiency of the n-type PERT cells is not influenced by an added solder stack.

Fig. 3 shows that there is no significant difference in efficiency between the groups. Therefore, we conclude that an application of the solder stack to cells does not influence cell efficiency.

Additionally, demo modules with each 4 PERC cells with solderable PVD metallization and with screen-printed reference cells (see Table 2) are fabricated. One demo module is exemplarily shown in Fig. 4. Long-term stability of solder-joints on cells with the presented PVD metallization schemes is evaluated on module level by thermal cycling of respective demo modules.

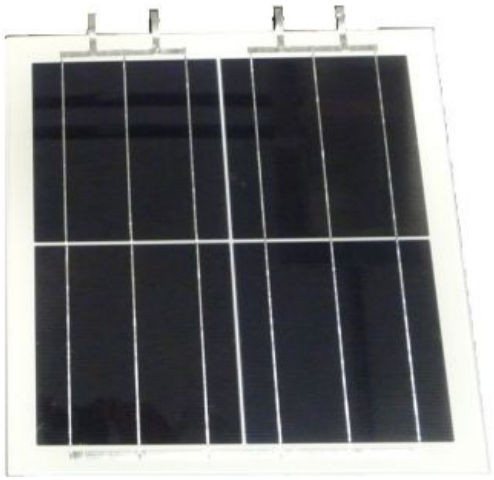

Fig. 4: Photograph of a demo module consisting of 4 156 mm PERC cells with solderable PVD rear metallization.

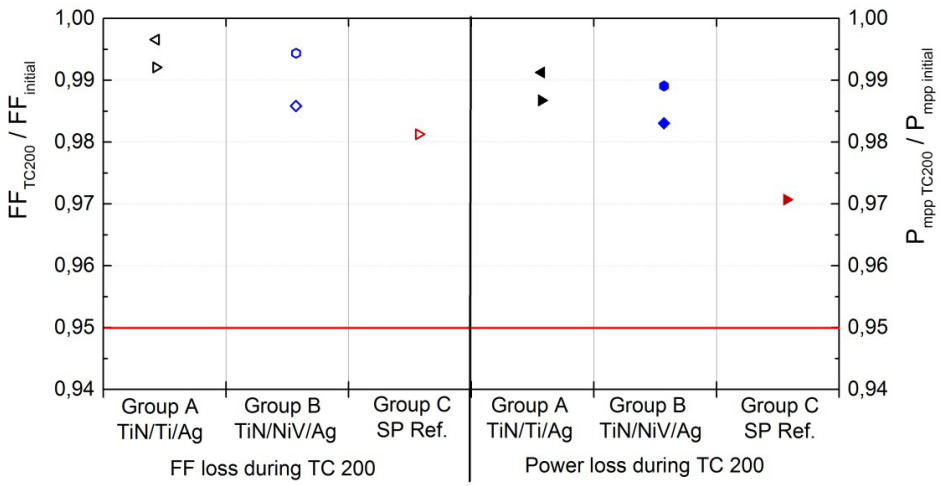

Fig. 5: Fill factor (left) and power output (right) of modules with cells with solderable PVD rear metallization (see Table 2 for metallization groups) compared to screen-printed rear metallization after 200 cycles of thermal cycling in relation to initial values. All modules show relative losses < 5 % and therefore pass the thermal cycling test.

Therefore, the power output at maximum power point (P_{mpp}) and the fill factor (FF) are measured before and after 200 cycles of thermal cycling (TC200) and the relative changes are compared to those of screen-printed references. The ratios of the values of P_{mpp} and FF after TC 200 to the initial values are depicted in Fig. 5. The relative power loss of the reference module might partly be due to light induced degradation, but is however < 3 %, and passes therefore the IEC criterion which allows a relative loss of < 5 %. The relative power loss during TC200 is even < 2 % for all demo modules with PVD metallized PERC cells. The presented solderable metallization therefore shows a good stability during 200 cycles of thermal cycling, which is a first indication that it enables a long-term stable interconnection. Also after additional damp heat and humidity freeze testing (DH1000 and HF10) the loss of each demo module with PVD metallization is < 3 %.

7. Summary and conclusion

A conventional, evaporated Al rear metallization layer is combined with a solder stack which comprises a solderable top layer, e.g. an Ag layer, a Ti adhesion layer and a TiN diffusion barrier. Through optimization of the TiN diffusion barrier by process optimization and stuffing of the grain boundaries with oxygen, Al diffusion is prevented even during a strong annealing step. We show that the stuffing procedure can also be executed in-situ within the process chamber of the PVD machine, without interrupting the high vacuum process sequence, if the stuffing process is enhanced by IR heating. Thus, on the optimized stack a cell-interconnector can be conventionally soldered even after a strong annealing step of 15 min at 425°C, which sets this concept apart from other PVD metallization approaches. We show on n-type PERT cells that the cell efficiency is not influenced by the solder stack compared to a reference rear metallization by plain evaporated Al. Additionally, a thermal aging investigation predicts a long-term stability of the solder connection in a module on a German site for a duration of 30 years if a layer thickness of 150 nm Ag is used. Furthermore, demo modules are fabricated from 4 PERC cells in 156 mm format each, which show to be stable after 200 cycles of thermal cycling.

We therefore present an annealing and long-term stable PVD rear metallization scheme which is suitable for most high-efficient silicon solar cells and is industrially feasible.

Acknowledgements

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