High-Performance TiO$_2$-Based Electron-Selective Contacts for Crystalline Silicon Solar Cells

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The main objective of technology development in the photovoltaics industry is to increase the power conversion efficiency (PCE) and reduce production costs in order to reduce the cost/watt. The standard p-type silicon solar cell with a homogeneous n$^+$ emitter and aluminum back surface field (Al-BSF) has a PCE limit of ≈19% with the current passivation and metallization concepts. A route toward higher PCE is the implementation of selective emitter (SE) or/and local back surface field (LBSF) structures into silicon solar cells. State-of-the-art high-efficiency silicon solar cells (>23%), such as the passivated-emitter rear locally diffused (PERL) and passivated emitter with rear totally diffused (PERT) cells, have been fabricated with locally doped or/and contact regions at front or rear sides.[1] However, the approach used to realize localized contact and/or doped regions for PERL and PERT cells requires cost-intensive processes, such as high temperature diffusion followed by complex patterning processes (e.g., photolithography, inkjet mask formation, laser processes), which have limited the commercial success of these high-efficiency cell concepts.

An alternative approach to achieve high PCE silicon solar cell is via the implementation of carrier selective contacts (CSCs).[2–8] A contact which extracts just one-type of carrier (electron or hole) from absorber (e.g., silicon) is termed as a CSC. A CSC is traditionally achieved by depositing a conductive layer (e.g., doped hydrogenated amorphous silicon, a-Si:H) over the thin passivation interlayer (e.g., intrinsic a-Si:H or SiO$_2$). For example, electron/hole-selective contacts can be formed by a stack of tunnel SiO$_2$ and phosphorus/boron-doped a-Si:H layer.[3] A high quality CSC not only provides excellent surface

passivation, but also extracts one-type of carrier efficiently by a simple 1D carrier transport. The incorporation of CSCs into silicon solar cell contributes to cell efficiency (excellent surface passivation at both contact and noncontact regions resulting in a high open-circuit voltage V_{oc}, and simplified current flow pattern resulting in a high fill factor FF) as well as design flexibility, process robustness and a simplified process flow by eliminating the local doping and contact opening steps. Ultra-high PCE of 25.1% and 25.6%, respectively, has been achieved in silicon heterojunction (SHJ) and silicon heterojunction interdigitated back-contact (SHJ-IBC) cells based on the intrinsic a-Si:H/doped a-Si:H CSC.[2–4] Recently, silicon solar cells featuring a tunnel SiO$_2$/doped poly-Si CSC (*TOPCon*) at the rear have been achieved a remarkably high efficiency of 25.1%.[8] Therefore, silicon solar cells based on CSCs have the potential to achieve ultrahigh efficiencies in the not so distant future.

Although a-Si:H and SiO$_2$-based CSCs have achieved great success in the development of high-efficiency silicon solar cells, there are some intrinsic challenges such as thermal instability and parasitic photon absorption of a-Si:H films, complicated deposition process, and high fabrication cost. Moreover, the doped a-Si:H layers are deposited by plasma-enhanced chemical vapor deposition (PECVD), which is a capital-intensive system with mandatory safety systems because of the pyrophoric silane and toxic boron/phosphorous gas precursors employed. Therefore, it is essential to develop high quality CSCs that can be deposited easily, economically, and safely with minimal hazardous risks.

Transition metal oxides (TMOs), which have been extensively investigated for charge injection and extraction in organic and perovskite solar cells,[9] have attracted considerable attention as alternative CSCs for silicon solar cells because of their ease of deposition at a low cost (e.g., thermal evaporation, brush painting, spin-on and spray methods). Sub-stoichiometric molybdenum oxide (MoO$_x$),[10–13] nickel oxide (NiO$_x$),[14] vanadium oxide (VO$_x$),[13] and tungstate oxide (WO$_x$)[13,15] have been investigated as hole-selective contacts for silicon solar cells. By substituting the boron-doped a-Si:H with a thin MoO$_x$ film, a SHJ solar cell with a PCE of 22.5% has been achieved with an improved short-circuit current density (J_{sc}).[12] Recently, ultrathin TiO$_2$ film on crystalline silicon has been demonstrated to form a hole–blocking interface.[16,17] This is due to a small conduction band offset ($\Delta E_c \approx 0.05$ eV), which allows electrons to pass through the TiO$_2$ layer and a large valence-band offset ($\Delta E_v \approx 2.0$ eV), which results in holes being blocked.[18] A double-heterojunction silicon solar cell with an efficiency of 12.9% has been fabricated via the implementation of a hole-blocking TiO$_2$ layer.[19,20] All of these observations suggest that

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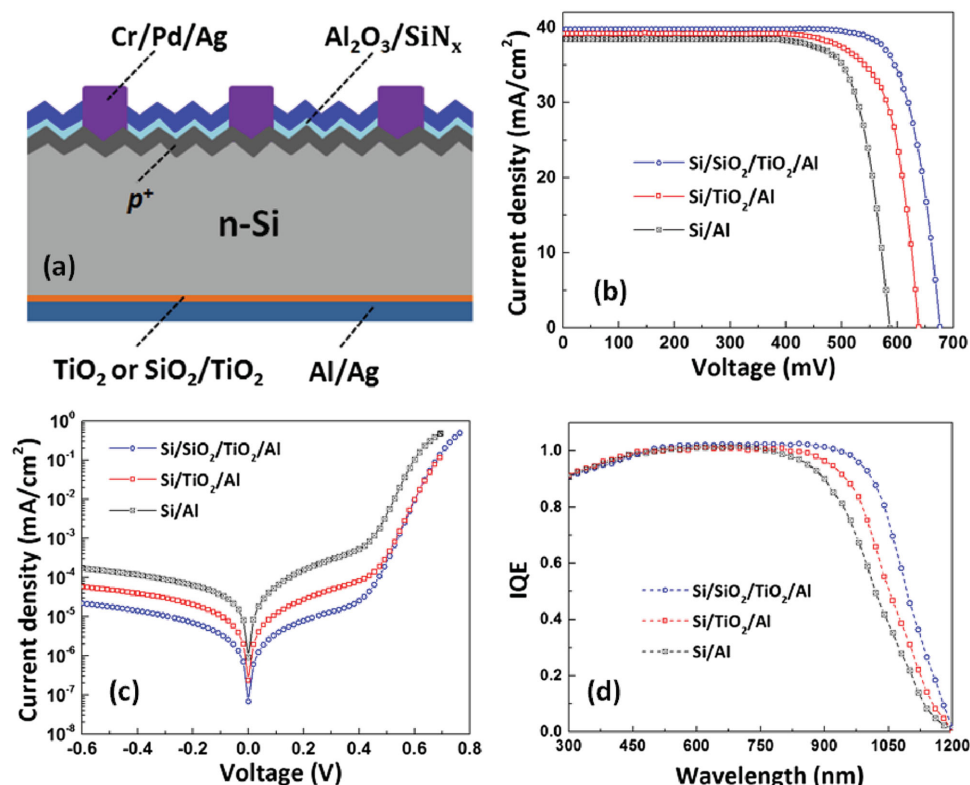Orlando, FL 32816, USA

Figure 1. a) The structure of n-type silicon solar cell featuring a full-area TiO_2 contact at the rear; b) light I–V curves under AM 1.5G; c) log-plot dark I–V curves; d) IQE spectra of silicon solar cells with and without a full-area TiO_2-based contact.

TiO_2 thin films are potentially an excellent electron-selective contact for silicon solar cells. However, the carrier selectivity characteristics of TiO_2 thin film are yet to be investigated, and the PCE of silicon solar cells with a full-area TiO_2 contact has not been fully explored to date.

In this work, we present high-efficiency silicon solar cells featuring a full-area electron-selective TiO_2 contact, which is deposited by atomic layer deposition (ALD). The performance of ultrathin TiO_2 films as an electron-selective contact is investigated by considering both the surface passivation quality and the contact resistivity on silicon surfaces. ALD is quite attractive for thin metal oxide layer deposition, providing excellent control over thickness and the ability to deposit pinhole free films. The results demonstrate that ultrathin TiO_2 films provide not only excellent passivation on silicon surfaces, but also allow a relatively low contact resistivity at the Si/TiO_2 heterojunction. A remarkably high PCE of 21.6% is achieved on a silicon solar cell featuring a full-area TiO_2-based contact.

Figure 1a shows the structure of n-type silicon solar cells with a full-area TiO_2 or SiO_2/TiO_2 electron-selective contact at the rear side. The solar cells (2 cm × 2 cm) were fabricated on n-type FZ-Si wafers (1.0 Ω cm) with a thickness of ≈175 μm. The textured front side with random pyramids has a boron diffused p^+ emitter, which was passivated by Al_2O_3/SiN_x stack. The front fingers were prepared by thermal evaporation of a Cr/Pd/Ag seed layer and subsequent electroplating of Ag. The rear side features a full-area TiO_2 (4.5 nm) or tunnel SiO_2/TiO_2 (1.2/3.5 nm) contact. This full-area contact allows a low process complexity and a simple 1D current flow pattern at the rear. A

control cell with directly Si/Al contact at the rear side was fabricated for comparison.

The current density–voltage (I–V) characteristics of silicon solar cells with different rear contact structures under the AM1.5 conditions are shown in Figure 1b, and the photovoltaic parameters of champion devices are summarized in **Table 1**. The control cell without a TiO_2-based contact exhibits a moderate efficiency (η) of 17.6%, which is mainly limited by a relatively low V_{oc} (585 mV) as well as FF (78.2%). This can be attributed to a high recombination at the Al/Si surface (as high as 10^6–10^7 cm s^{-1}) and a non-Ohmic contact between Al and n-Si.[21] By insertion of a 4.5 nm TiO_2 film between Al and n-Si interface, the cell efficiency is significantly improved to 19.8%. All the solar cell parameters, especially the V_{oc} (from 585 to 638 mV) and FF (from 78.2% to 79.1%), are improved obviously. This indicates that a reduction of carrier recombination and contact resistance occurs due to the insertion of an ultrathin TiO_2 film between n-Si and Al. A further efficiency improvement is achieved by inserting a tunnel SiO_2 (≈1.2 nm)

Table 1. Photovoltaic parameters of n-type silicon solar cells with or without a full area TiO_2-based contact.

Rear contact type	V_{oc} [mV]	J_{sc} [mA cm^{-2}]	FF [%]	η [%]
Al	585	38.5	78.2	17.6
TiO_2/Al	638	39.2	79.1	19.8
SiO_2/TiO_2/Al	676	39.6	80.7	21.6

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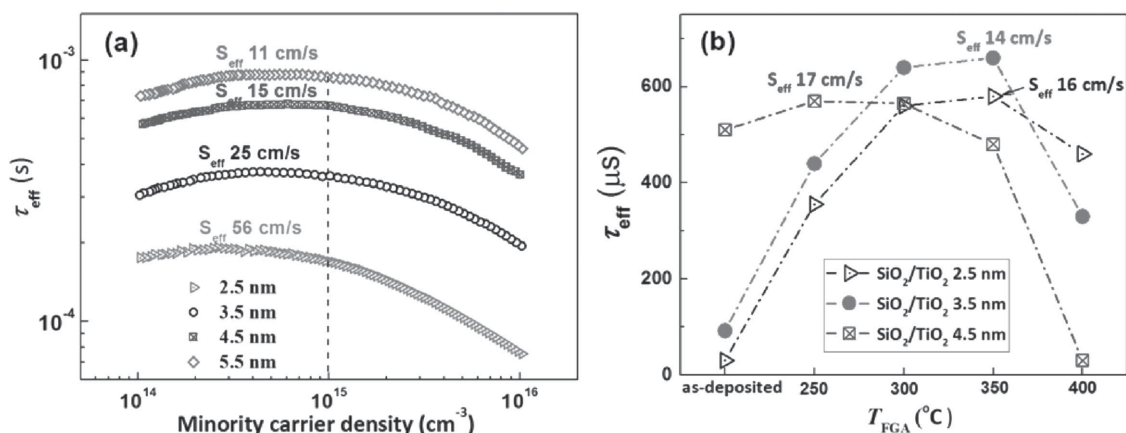
Figure 2. a) Injection-level-dependent effective lifetimes of n-type (1.0 Ω cm, 190 μm) passivated by TiO_2 film with different thickness after FGA annealing at 250 °C for 3 min; b) Dependence of effective lifetime of tunnel-SiO_2/TiO_2 stack passivated n-type (1.0 Ω cm, 190 μm) silicon wafers on FGA temperatures. The calculated upper limits of S_{eff} are shown together.

between n-Si and TiO_2 film. The champion device featuring a full-area SiO_2/TiO_2 contact exhibits a high V_{oc} of 676 mV, a J_{sc} of 39.6 mA cm^{-2} and a FF of 80.7%, resulting in a very high η of 21.6% that represents an absolute efficiency gain of 4.0% compared with the control device. The champion cell batch (four cells on one wafer) shows an average efficiency above 21.0%, a testament to the reproducibility of the silicon solar cells with a full-area SiO_2/TiO_2 contact (see Table S1, Supporting Information). The result demonstrates that the carrier recombination and contact resistance at the rear side are further reduced with the SiO_2/TiO_2 contact. This very high η of 21.6% is the highest value reported to date for the silicon solar cell with a simple and full-area TiO_2-based selective contact.

Figure 1c shows the I–V characteristics of the devices with and without TiO_2-based contact in the dark. All the devices exhibit diode properties clearly. The devices with TiO_2-based contacts exhibit a much better diode properties with a lower saturation current density and higher rectification ratio in comparison to the control device. This suggests a reduction of the series resistance and interfacial recombination, and an increase in the shunt resistance for devices with the TiO_2-based contacts, consistent with the improved cell parameters shown in Table 1. To further investigate the effects of the TiO_2 contact incorporation on the photovoltaic properties, the internal quantum efficiency (IQE) spectra of these devices were measured (Figure 1d). All the devices show a very high IQE in the short wavelength range (300–800 nm), which demonstrates a low surface recombination at the front side thanks to the excellent surface passivation by Al_2O_3/SiN_x stack. In contrast, an obvious higher IQE in the long wavelength range (>800 nm) is observed for the device with a TiO_2 contact at the rear side. The improved long-wavelength response indicates a lower carrier recombination at the rear surface due to the presence of a TiO_2 film. Insertion of a tunnel SiO_2 interlayer between the TiO_2 and n-Si interface leads to the best long-wavelength response, resulting in an obvious increase of V_{oc} and J_{sc}, and hence the efficiency. The calculated J_{sc} for the cell with a full-area SiO_2/TiO_2 contact, obtained by integrating the product of external quantum efficiency (EQE) and the air mass (AM) 1.5 spectrum and correcting for the approximate contact fraction, is proven to be

39.51 mA cm^{-2}, in good agreement with the measured J_{sc} value. The IQE spectra demonstrate that the efficiency improvement is achieved by reducing the carrier recombination at the rear side due to the presence of a TiO_2 film or SiO_2/TiO_2 stack.

A dramatic efficiency improvement in silicon solar cells has been demonstrated by the inclusion of a full-area TiO_2-based contact. The efficiency improvement is mainly attributed to a reduction of surface recombination (resulting in a higher V_{oc} as well as J_{sc}) and contact resistivity (resulting in a higher FF) at the rear side, which indicates that the TiO_2-based contact inserted between n-Si and Al not only serves as an effective electron transporting layer, but also provides good surface passivation on silicon surfaces. A detailed analysis of the surface passivation of thin TiO_2 and SiO_2/TiO_2 stack on silicon surfaces is presented below.

Figure 2a shows the injection level dependent effective lifetime (τ_{eff}) of n-type silicon wafers passivated by TiO_2 films with different thickness after forming gas atmosphere (FGA, mixture of 95% N_2 and 5% H_2) annealing at 250 °C for 3 min, and the calculated upper limits of effective surface recombination velocity (S_{eff}) values are shown together. An ultrathin TiO_2 film (2.5 nm) can significantly reduce the S_{eff} from 10^6–10^7 (Si/Al contact directly) to ≈56 cm s^{-1}. As TiO_2 film thickness increases from 2.5 to 5.5 nm, the measured τ_{eff} (at the injection level of 10^{15} cm^{-3}) increases from 170 to 850 μs. The calculated S_{eff} reduces from 56 to 11 cm s^{-1} accordingly. Ultrathin TiO_2 films also can provide excellent surface passivation on p-type surfaces (see Figure S1, Supporting Information). The very low S_{eff} values achieved by a 5.5 nm TiO_2 film are comparable to the reported value for Si/SiO_2 interface.[22] The results demonstrate that ultrathin TiO_2 films can provide excellent surface passivation to silicon surfaces, which can be attributed to the formation of Si–O–Ti bonding at the Si/TiO_2 interface[23] as well as the potential negative charge density in the TiO_x film.[24] Therefore, silicon solar cells with a full-area TiO_2 contact show an improved V_{oc} due to the reduced surface recombination at the Si/TiO_2 interface.

Although ultrathin TiO_2 can provide excellent passivation on silicon surfaces, the passivation thermal stability is only stable at the temperature of up to 250 °C. The surface passivation

performance degrades rapidly at a temperature higher than 250 °C (Figure S2, Supporting Information). It might be caused by the phase transformation from amorphous to anatase of the TiO₂ film at a temperature of ≥300 °C. Liao et al. reported that anatase phase was observed in TiO₂ film deposited at 300 °C by ALD.[24] It is well known that amorphous TiO₂ films (as-deposited) are preferred for c-Si surface passivation, as they may introduce fewer interface defects compared to crystalline TiO₂ films. Additionally, the Si–O–Ti bonding at the TiO₂/Si interface might be broken at a temperature higher than 250 °C. To form the front contact, unfortunately, n-type solar cells featuring a full-area TiO₂ contact have to be subjected to a final FGA annealing at ≥300 °C, which causes the TiO₂ passivation degradation at the rear side resulting in a lower V_{oc} (638 mV) than expected.

Inspired by the excellent surface passivation and thermal stability of SiO₂/doped poly-Si CSC,[5–8] a thermally grown tunnel SiO₂ (≈1.2 nm) is inserted between Si and TiO₂ film to improve the passivation thermal stability of TiO₂ film on silicon surfaces. The passivation quality of SiO₂/TiO₂ stacks with different thickness of TiO₂ capping on n-type silicon surfaces (1.0 Ω cm) is also investigated by quasi-steady state photoconductance (QSSPC) measurements. Figure 2b shows the dependence of effective lifetime (at the injection level of 1 × 10¹⁵ cm⁻³) of SiO₂/TiO₂ stack passivated n-type (1.0 Ω cm, 190 μm) silicon wafers on FGA annealing at different temperatures. As-deposited SiO₂/TiO₂ stacks exhibit a poorer surface passivation than that of TiO₂ film with the same thickness. It is interesting that the passivation quality improved significantly by FGA annealing at evaluated temperatures for SiO₂/TiO₂ stacks capped with a thin TiO₂ layer (2.5 and 3.5 nm). However, a gradual passivation degradation instead of improvement is observed for SiO₂/TiO₂ stack capped with a 4.5 nm TiO₂ layer. The best passivation quality with a lowest S_{eff} of 16 and 14 cm s⁻¹ is achieved for SiO₂/TiO₂ stacks capped with 2.5 and 3.5 nm TiO₂ layer, respectively, after FGA annealing at 350 °C. Significant passivation degradation is observed for all SiO₂/TiO₂ stacks when FGA annealing at 400 °C. The results demonstrate that SiO₂/TiO₂ stacks can also provide a good surface passivation on n-type silicon surface with a better thermal stability. Therefore, silicon solar cells featuring a full-area SiO₂/TiO₂ contact show a high V_{oc} value (676 mV) thanks to the stable passivation at the rear side during final FGA annealing at 350 °C.

The different passivation quality changes of TiO₂ and SiO₂/TiO₂ stacks under FGA annealing might be attributed to the different passivation mechanisms. Instead of passivating silicon surface by forming the Si–O–Ti bonding for sole TiO₂ film, the passivation of SiO₂/TiO₂ stacks to silicon surfaces is considered to be achieved by a combination of chemical passivation of SiO₂ and field-effect passivation of the TiO₂ film, which is similar to that of a-Si:H and SiO₂-based CSCs. When the TiO₂ film is too thin, the field-effect passivation is deficient, and holes are not repelled enough from the interface. This results in a low level passivation of SiO₂/TiO₂ stacks with a thin TiO₂ capping (2.5 and 3.5 nm), and a much better surface passivation is achieved with a thicker TiO₂ capping (4.5 nm). FGA annealing can improve the chemical passivation of SiO₂ by the diffusion of atomic hydrogen to the SiO₂/Si interface where it deactivates recombination centers. Therefore, the surface passivation

improvement of SiO₂/TiO₂ stacks by FGA annealing can be attributed to the improved chemical passivation of SiO₂. However, FGA annealing at high temperature will degrade the field-effect passivation of TiO₂ film due to the phase transformation from amorphous to the anatase. Yu et al. reported that an amorphous TiO₂ layer with high tensile stress forms at the beginning of the deposition, which induces the nucleation of anatase phase as the thickness of TiO₂ films increases.[25] This indicates that the thicker the TiO₂ film, the lower temperature needed for the phase transformation from amorphous to the anatase. The surface passivation of SiO₂/TiO₂ stacks degrades at a high temperature (>350 °C) can be attributed to the reduced field-effect passivation of TiO₂ film due to the phase transformation.

We have demonstrated that ultrathin TiO₂ and SiO₂/TiO₂ stack can provide high quality surface passivation on n-type silicon surface, and next we will investigate the contact resistivity (ρ_c) at the n-Si/TiO₂ and n-Si/SiO₂/TiO₂ heterojunctions. A structure (see Figure S3, Supporting Information) developed by Cox and Strack[26] was prepared to extract the ρ_c values. Most contacts with different thicknesses of TiO₂ films and diameters circular metal dots (0.5–10 mm) at the top exhibit Ohmic *I–V* behavior, which demonstrates that electrons can pass through the thin TiO₂ and SiO₂/TiO₂ layers, and allows the extraction of ρ_c by fitting the curve of resistance versus top circle contact diameter.

Figure 3a shows the dependence of ρ_c of n-Si/TiO₂ and n-Si/SiO₂/TiO₂ heterojunctions on TiO₂ film thickness before and after FGA annealing. The ρ_c between n-Si and Al without TiO₂ interlayer was measured by a transmission line method (TLM),[27] and ρ_c was extracted approximately from an extrapolation of resistance versus pad spacing. A relatively large ρ_c between 0.5 and 1.0 Ω cm² is obtained for the n-Si/Al contact, which can be attributed to a relatively large Schottky barrier height (Φ_B 0.7–0.80 eV) between n-Si and Al.[28] The electrons have to pass through this large barrier before being collected by Al, as shown in Figure 3b. A thin interfacial dielectric inserted between the semiconductor and metal can increase the carrier extraction for optoelectronic devices through the reduction of the Φ_B at the interface,[21,29] which might be caused by a reduced metal-induced gap states occupation in the semiconductor bandgap and hence Fermi level depinning.[30] Due to a very small conduction band offset (≈0.05 eV) between Si and TiO₂ interlayer,[16] the insertion of an ultrathin TiO₂ film (<4.5 nm) between n-Si and Al reduces the Φ_B to 0–0.2 eV (Figure 3c) by assuming a conduction band edge of TiO₂ at ≈4.0 eV[16] and a work function of Al at 4.0–4.2 eV, and hence the ρ_c values decrease to lower than 0.3 Ω cm². In the meanwhile, due to a large valence band offset (>2.0 eV) at the n-Si/TiO₂ interface, which would block the holes from silicon to TiO₂ layer, the carrier recombination at the interface is also suppressed. For the same TiO₂ film thickness, n-Si/TiO₂ heterojunctions show a lower ρ_c than that of n-Si/SiO₂/TiO₂ heterojunctions. Although a tunnel SiO₂ insertion between n-Si and TiO₂ interface may not change the energy barrier height (Figure 3d), ρ_c increases slightly due to the presence of tunnel resistance. The relatively large ρ_c at the n-Si/TiO₂ and n-Si/SiO₂/TiO₂ heterojunctions might be attributed to the amorphous TiO₂ interlayer with a low conductivity. The cells featuring a full-area TiO₂ or SiO₂/TiO₂ contact exhibit a low FF (<70%) before final FGA annealing
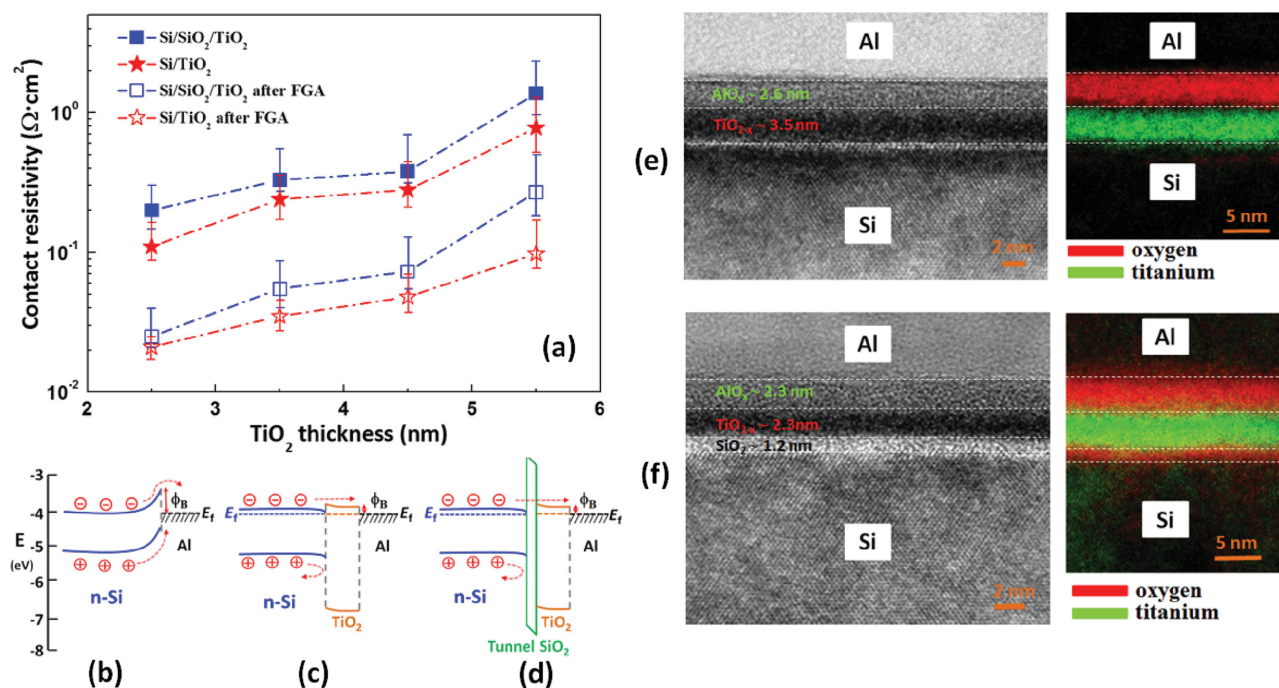
Figure 3. a) Dependence of contact resistivity of n-Si/TiO_2 and n-Si/SiO_2/TiO_2 heterojunctions on TiO_2 film thickness before and after FGA annealing; b–d) Bandgap alignments of the n-type silicon solar cells with different rear contacts (b) n-Si/Al; (c) n-Si/TiO_2/Al; (d) n-Si/SiO_2/TiO_2/Al; e,f) The cross-sectional TEM images of (e) Si/TiO_2/Al and (f) Si/SiO_2/TiO_2/Al contacts after FGA annealing. The elemental maps obtained by EFTEM are shown on the right (red for oxygen and green for titanium).

(see Supplementary Table 2, Supporting Information), because of a relatively high ρ_c at the n-Si/TiO_2 and n-Si/SiO_2/TiO_2 heterojunctions. After FGA annealing, a much lower ρ_c is achieved at the n-Si/TiO_2 and n-Si/SiO_2/TiO_2 heterojunctions, which is almost one order of magnitude lower than that before FGA. A minimum ρ_c of ≈0.02 Ω cm^2 is achieved at the n-Si/TiO_2 and n-Si/SiO_2/TiO_2 heterojunctions with a 2.5 nm TiO_2 film, which is comparable to the ρ_c obtained on a high quality n-Si/SiO_2/ phosphorus doped poly-Si heterojunctions.[31] The reduced ρ_c at the n-Si/TiO_2 and n-Si/SiO_2/TiO_2 heterojunctions after FGA annealing might be caused by the composition change of TiO_2 interlayer, which will be discussed in the Experimental Section. Therefore, the implementation of a TiO_2-based contact improves the contact resistivity at the rear side, resulting in a reduced series resistance and hence a higher FF, which is consistent with the results shown in Table 1.

We found that the parameters of the devices featuring a full-area TiO_2-based contact, especially the FF, depend on a final FGA annealing significantly (also see Supplementary Table 2, Supporting Information). The champion efficiency shown in Table 1 is achieved by FGA annealing at 300 and 350 °C for cells with a full-area TiO_2 and SiO_2/TiO_2 contact, respectively. In order to understand the mechanism involved, cross-sectional images of Si/TiO_2/Al and Si/SiO_2/TiO_2/Al contacts after FGA annealing were obtained under bright-field (BF) and high resolution transmission electron microscopy (HRTEM) conditions and elemental maps were obtained by energy-filtered TEM (EFTEM), as shown in Figure 3e,f. In both contact structures, an obvious aluminum oxide (AlO_x) with a thickness of 2–3 nm is observed between TiO_2 and Al interface. However, a very thin

and non-obvious AlO_x interlayer (≈0.5 nm) was observed in the TiO_2/Al interface before FGA annealing (see Figure S4, Supporting Information). Due to the strong oxygen affinity of Al metal, aluminum atoms easily attract oxygen atoms from the TiO_2 interlayer and a redox reaction occurs between Al and TiO_2 forming an interfacial AlO_x.[32] This interfacial AlO_x layer is assumed to be a nonstoichiometric, Al rich layer due to the low ρ_c obtained for these devices. The composition of the TiO_2 layer, which is initially considered to be amorphous and stoichiometric,[16] has been drastically changed to an oxygen-deficient TiO_{2-x} phase with high concentration of oxygen vacancies. The elemental maps obtained by EFTEM also confirm that the titanium oxide interlayer (green color) becomes highly oxygen deficient, and the oxygen concentration at the Al/TiO_2 interface is much higher, as displayed with the red color.

It is well known that titanium oxide shows a higher conductivity as the concentration of oxygen vacancies increases.[30,33] The effect of titanium oxide composition change on cell parameters can be described in two aspects. First, the contact resistivity at the Si/TiO_2 and Si/SiO_2/TiO_2 heterojunctions decreases due to a higher conductivity of titanium oxide with high concentration of oxygen vacancies, and hence cell's FF improves. Agrawal et al. reported that high conductivity interfacial layer is one of the key requirements to obtain low contact resistivity using metal–insulator–semiconductor (MIS) contact.[30] Moreover, the coarsening of TiO_2 film during FGA annealing, which has been demonstrated by Yu et al.,[25,34] might be an additional reason for the reduced contact resistivity at the Si/TiO_2 and Si/SiO_2/TiO_2 heterojunctions. The results are consistent with the reduced contact resistivity shown in Figure 3a

and improved FF shown in Table 1. Meanwhile, the surface passivation quality of titanium oxide on silicon surface degrades, resulting in a reduced V_{oc} of the cells with a $Si/TiO_2/Al$ contact. Due to the excellent surface passivation of Al_2O_3/SiN_x at the front and TiO_2 at the rear, an implied V_{oc} as high as 700 mV is expected for the cells featuring a full-area TiO_2 contact at the rear. However, a much lower V_{oc} of 638 mV is obtained, which can be attributed to a degraded surface passivation of titanium oxide with high concentration of oxygen vacancies. The out-diffusion of oxygen in the TiO_2 interlayer can destroy the Si–O–Ti bonding at the Si/TiO_2 interface, resulting in a higher surface recombination, and hence a lower V_{oc}. Fortunately, the reaction between TiO_2 and Al has only a slight effect on the surface passivation quality of SiO_2/TiO_2 stack on silicon surface, but it significantly decreases the contact resistivity at the $Si/SiO_2/TiO_2$ heterojunction. A relatively high V_{oc} of 676 mV and FF of 80.7% have been achieved with a full-area SiO_2/TiO_2 contact, due to the stable surface passivation and reduced contact resistivity at the rear $Si/SiO_2/TiO_2$ contact during the FGA annealing.

In summary, we developed a high-quality, low-cost TiO_2-based electron-selective contact for silicon solar cells. The implementation of the TiO_2-based contacts reduces the surface recombination and contact resistivity at the silicon and metal interface simultaneously, resulting in a higher V_{oc} and FF for silicon solar cells. The champion efficiency of 21.6% has been achieved on the n-type silicon solar cell featuring a full-area TiO_2-based contact. This work highlights the high potential of TiO_2-based contacts in future high-efficiency, low-cost silicon solar cells. Our findings also open up the possibility of developing low-cost transition-metal-oxide-based carrier-selective contacts for silicon solar cells.

Experimental Section

ALD-TiO₂ Film Deposition and Characterization: Thin TiO_2 films were deposited by ALD (TFS 200, BENEQ, Finland) with the titanium chloride ($TiCl_4$) titanium precursor and H_2O oxidant at a low temperature of 75 °C, and N_2 was used as the purge gas. The growth rate was determined to be ≈0.07 nm per cycle, and the cycle time was only 1.5 s. Thin TiO_2 films (2.5–5.5 nm) can be deposited within 2 min. To investigate the surface passivation quality of thin TiO_2 on silicon surfaces, symmetrical test structures were fabricated on (100)-oriented n-type (1.0 Ω cm, 190 μm) and p-type (1.0 Ω cm, 250 μm) silicon wafers to allow injection-dependent lifetime measurement utilizing the QSSPC technique.[35] The wafers were chemical-polished and RCA cleaned followed by a short dip in diluted HF before TiO_2 film deposition. TiO_2 films with different thicknesses (2.5–5.5 nm) were deposited on both sides of silicon wafers, and QSSPC measurements were performed before and after FGA annealing. TiO_2 film thicknesses were determined from ellipsometry measurement by fitting polarized reflectance data of single side polished silicon wafers. Some of the samples were subjected to a short thermal oxidation before TiO_2 films deposition. The oxidation was performed in a preheated quartz tube furnace at 700 °C for only 150 s in O_2 atmosphere, resulting in a tunnel SiO_2 thickness of ≈1.2 nm. The passivation quality of the TiO_2 and SiO_2/TiO_2 layers was quantified in terms of the effective lifetime (τ_{eff}) and effective surface recombination velocity (S_{eff}), which is calculated from τ_{eff} by the expression:[21]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \tag{1}$$

with τ_{bulk} being the c-Si bulk lifetime and W the wafer thickness. Here the bulk lifetime can be set to infinity since a high quality FZ c-Si was used, the calculated τ_{eff} is an upper limit value.

Device Fabrication: The ρ_c of Si/TiO_2 and $Si/SiO_2/TiO_2$ heterojunctions with different TiO_2 film thickness was measured by the method developed by Cox and Strack.[26] The structure, as shown in the inset picture of Figure 3a, was prepared by depositing TiO_2 or SiO_2/TiO_2 on the top side, following which Al/Ag metal stack circles with different diameters were evaporated through a shadow mask. An Ohmic rear contact ($\rho_c < 10^{-4}$ Ω cm²) was prepared using evaporated Al on a phosphorus diffused (≈60 Ω sq⁻¹) rear surface, in order to minimize the resistance associated with the rear contact. Current–voltage (I–V) measurements in the dark were performed before and after FGA annealing using a Keithley 2425 source-meter at room temperature. The ρ_c values were obtained by fitting the curve of resistance versus front circle contact diameter. The extracted ρ_c value mainly consists of the resistance of the Si/TiO_2, $Si/SiO_2/TiO_2$, and TiO_2/Al interfaces as well as the TiO_2 bulk resistivity.

Silicon solar cells featuring a full-area TiO_2 or SiO_2/TiO_2 contact at the rear were fabricated on n-type c-Si wafers (1.0 Ω cm, ≈175 μm). After surface damage etching in alkaline solution, a mask SiN_x layer (≈100 nm) was grown by low-pressure chemical vapour deposition (LPCVD) on both sides. The cell area (2 cm × 2 cm) was then realized by photolithographically defined mesa etch. Following alkaline-based surface texturing and standard RCA cleaning, a boron diffusion was performed in a clean quartz furnace, resulting in a p⁺ emitter with a sheet resistance of ≈120 Ω sq⁻¹. An Al_2O_3/SiN_x stack, which was deposited by plasma ALD (Al_2O_3 ≈20 nm) and plasma enhanced chemical vapor deposition (PECVD SiN_x, ≈50 nm), was used to passivate the front emitter. The rear TiO_2 contact was formed by depositing a TiO_2 film (4.5 nm) and evaporating an Al/Ag (20/2000 nm) stack. Cells featuring a full-area SiO_2/TiO_2 contact were subjected to a short thermal oxidation at 700 °C for 150 s for tunnel SiO_2 growth before TiO_2 films (3.5 nm) deposition. The front fingers were prepared with photolithography in combination with an evaporated stack of Cr/Pd/Ag (40/40/40 nm) that was thickened with Ag electroplating. Finally, the cells were subjected to a FGA annealing before cutting by laser for I–V measurements. A control cell without TiO_2 contact at the rear (Si/Al contact directly) was prepared together for comparison.

Device Characterization: The I–V characteristics of the solar cells were measured using a Xenon-lamp solar simulator under standard 1 sun conditions (100 mW cm sq⁻², AM 1.5 spectrum, 25 °C), which was calibrated using a certified reference cell from Fraunhofer ISE CalLab. The EQE of the solar cells was measured using a Protoflex Corporation QE measurement system (QE-1400-03). The front-side reflectance measurements were taken using a PerkinElmer Lambda 1050 UV/VIS/NIR spectrophotometer. The IQE was calculated by the measured reflectance and EQE data using IQE = EQE/(1 − R). Specimens for transmission electron microscopy (TEM) were prepared by focussed ion beam (FIB) technique with the help of FEI 200 TEM FIB. TEM studies of $Si/TiO_2/Al$ and $Si/SiO_2/TiO_2/Al$ contacts were carried out on FEI Tecnai F30 TEM operating at 300 kV. Cross-sectional images were obtained under bright-field (BF) and high resolution transmission electron microscopy (HRTEM) conditions. Compositional analysis was done with the help of energy-filtered transmission electron microscopy (EFTEM).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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