

Industrial-scale deposition of nanocrystalline silicon oxide for 26.4%-efficient silicon heterojunction solar cells with copper electrodes

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To unlock the full performance potential of silicon heterojunction solar cells requires reductions of parasitic absorption and shadowing losses. Yet the translation of the hydrogenated nanocrystalline silicon oxide (nc-SiO_x:H) window layer and copper-plated electrodes to a cost-effective and scalable production-relevant context remains one of the largest roadblocks towards mainstream adoption of silicon heterojunction technology. Here we address the first challenge by developing an industrial-scale high-frequency plasma-enhanced chemical vapour deposition system with a minimized standing wave effect, enabling the deposition of doped nc-SiO_x:H with excellent electron selectivity, low parasitic absorption and high uniformity. Next, we demonstrate seed-free copper plating, resulting in grids with a high aspect ratio and low metal fraction. By implementing the doped nc-SiO_x:H window layer, certified efficiencies of 25.98% and 26.41% are obtained for M6-size bifacial silicon heterojunction devices with screen-printed silver electrodes and copper-plated electrodes, respectively. These results underline the performance potential of silicon heterojunction technology and lower the threshold towards their mass manufacturing.

Silicon heterojunction (SHJ) technology is of great interest for next-generation commercial crystalline silicon (c-Si) photovoltaics, thanks to its high power conversion efficiency (PCE), lean and low-temperature processing, low temperature coefficient and high bifaciality^{1–5}. SHJ technology is also an ideal bottom cell for future ultra-high-efficiency silicon-based tandem devices. To date, the PCE of

SHJ solar cells in the front-back contact and interdigitated back contact implementations has reached 26.81% and 26.7%, respectively, setting the world record for single-junction c-Si solar cells^{6,7}. Nevertheless, the 26.81% efficiency was obtained on a mono-facial SHJ solar cell (instead of bifacial) with front fingers and transparent conductive electrodes prepared by a laser transfer process and reactive plasma deposition⁶,

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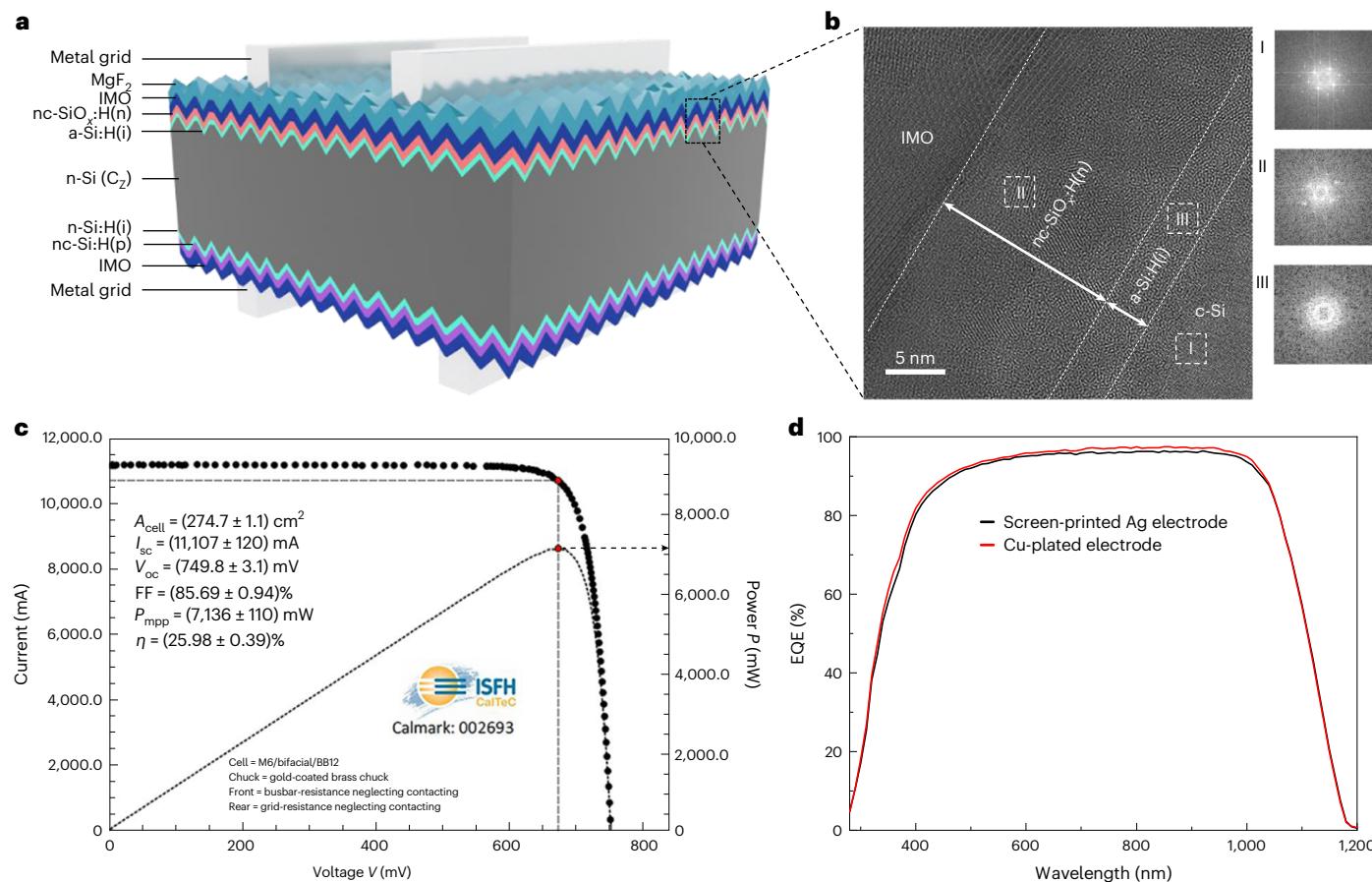


Fig. 1 | SHJ solar cell structure and performance. **a**, Schematic of a rear-junction SHJ solar cell featuring a front side nc-SiO_x:H(n) window layer as electron collector. **b**, Cross-sectional HR-TEM image of the front c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO contact stack. Insets are the Fourier transforms calculated in the corresponding areas. **c**, Certified I - V curve of the best device featuring a nc-SiO_x:H(n) window layer deposited under VHF1 with screen-printed Ag electrodes. **d**, EQE (%) of SHJ solar cells featuring a nc-SiO_x:H(n) window layer deposited under VHF1 with screen-printed Ag and Cu-plated electrodes, respectively.

A_{cell} , I_{sc} , V_{oc} , FF, P_{mpp} and η are abbreviations for the area of a solar cell, short-circuit current, open-circuit voltage, fill factor, power at the maximum power point and power conversion efficiency, respectively. Front busbar resistance and rear grid resistance are neglected in the measurement. **d**, EQE of SHJ solar cells featuring a nc-SiO_x:H(n) window layer deposited under VHF1 with screen-printed Ag and Cu-plated electrodes, respectively.

respectively, both of which are not industrially compatible for mass production. The commercial success of high-efficiency SHJ technology remains impeded by challenges in the cost-effective translation to a production environment of several process steps, such as window layer deposition and metallization.

For the first challenge, the large-scale deposition of passivating contact layers usually relies on plasma-enhanced chemical vapour deposition (PECVD) of (doped) hydrogenated amorphous silicon (a-Si:H) films, enabling excellent passivation and good carrier selectivity, but invoking high parasitic absorption and a relatively high contact resistivity with the overlying transparent conductive oxides (TCOs), limiting the short-circuit current density (I_{sc}) and fill factor (FF), respectively⁸. To resolve these issues, much research effort has been devoted to replacing doped a-Si:H with doped hydrogenated nanocrystalline silicon (nc-Si:H)^{9–11}, or its alloys with oxygen (hydrogenated nanocrystalline silicon oxide (nc-SiO_x:H) (refs. 12–15)) and carbon (nc-SiC:H (refs. 16,17)). For these films, PECVD systems with a very high frequency (VHF)^{18–23} rather than the standard radio frequency (RF, 13.56 MHz) are usually employed, to increase the deposition rate and reduce ion bombardment (as a VHF promotes SiH₄ gas dissociation and decreases the electrical field intensity^{19,24–26}). However, quite generally for PECVD systems, the size of the reactor chamber should be less than a quarter wavelength of the plasma to avoid interelectrode voltage inhomogeneities and poor uniformity of deposited films due to standing wave effects^{19,27}. This challenge sets a limit to the translation of

those SHJ processes that enable the highest power conversion efficiencies (PCEs), to large-scale manufacturing²⁸.

The second challenge relates to the high-cost metallization process for SHJ solar cells when using low-temperature silver (Ag) paste, featuring a relatively low conductivity and relatively high shadowing losses and contact resistivity^{29,30}. Furthermore, terawatt photovoltaic manufacturing urgently mandates the search for alternatives to Ag due to its scarcity³¹. This explains the great interest in copper (Cu) plating as an alternative metallization process for SHJ solar cells, given its high conductivity and narrow finger shadowing^{29,32–34}. However, it remains challenging to develop cost-effective Cu metallization with high reliability, due to the poor adhesion between a directly Cu-plated electrode and TCOs (for example, indium tin oxide, ITO) and the lack of techniques for selective deposition of the seed layer and stripping-free plating resist²⁹.

In this work we address both critical challenges by developing a large-size PECVD system with a very high frequency (27 MHz, labelled here VHF1) for high-quality phosphorus-doped nanocrystalline silicon oxide (nc-SiO_x:H(n), where n refers to n-type phosphorus doping) window layer deposition, demonstrating excellent uniformity in a production-scale chamber with a minimized standing wave effect, compared to that of a even-higher-frequency system (40 MHz, VHF2). By the implementation of optimized nc-SiO_x:H(n) window layers, a certified PCE of 25.98% is achieved on a full-area M6-size bifacial SHJ device with screen-printed silver electrodes. The device with a nc-SiO_x:H(n)

Table 1 | Photovoltaic parameters of SHJ solar cells with screen-printed Ag electrodes and nc-SiO_x:H(n) window layer deposited under RF (13.56 MHz), VHF1 or VHF2

Frequency (MHz)	V _{oc} (mV)	FF (%)	J _{sc} (mA cm ⁻²)	PCE (%)
RF	749.52	85.36	40.37	25.83
VHF1	749.80	85.69	40.44	25.98 ^a
VHF2	750.09	85.63	40.52	26.02
VHF1 and Cu plating	750.20	86.28	40.80	26.41 ^a

^aCertified by ISFH CalTec. The device with VHF1 and Cu plating is also listed. All the devices were subjected to light soaking under 80 suns at 230 °C for 40 s and capped with a 110 nm MgF₂ anti-reflection layer.

window layer deposited under VHF1 also exhibits a smaller dark degradation than devices under VHF2. Ultimately, together with the proprietary Cu-plated finger–busbar grids by SunDrive, the certified PCE is boosted to 26.41% on a M6-size bifacial device, thanks to a high J_{sc} of 40.8 mA cm⁻² and FF of 86.28%. This work demonstrates an industrially compatible strategy to integrate a high-performance nc-SiO_x:H window layer with large-area uniformity and performance-enhanced Cu plating to SHJ solar cells, which can help accelerate the commercial success of SHJ technology.

SHJ solar cell performance at different frequencies

Three optimized nc-SiO_x:H(n) window layers with a similar thickness were deposited by PECVD under excitation frequencies of RF (13.56 MHz), VHF1 or VHF2. For all, the optoelectrical properties and thicknesses of the nc-SiO_x:H(n) layers were optimized (PECVD parameters are shown in Supplementary Table 1), providing a boron-doped p-type nc-Si:H for hole collection at the rear and transition-metal-doped indium oxide (IMO) transparent electrodes at both sides (Fig. 1a). Rather than the widely used ITO, here we employed the newly developed IMO featuring a wider bandgap, higher carrier mobility and lower free carrier absorption, as discussed in our previous work³⁵. The deposition rate of the optimized nc-SiO_x:H(n) layer under VHF1 is 0.13 nm s⁻¹, which is made comparable to that under RF (0.131 nm s⁻¹) and VHF2 (0.123 nm s⁻¹) by tuning the gas flow and power density. Figure 1b displays the cross-sectional high-resolution transmission electron microscopy (HR-TEM) image of the front c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO (the ‘i’ in a-Si:H(i) refers to intrinsic) stack on a textured c-Si surface, together with the diffraction patterns calculated from Fourier transforms of the selected areas. Only a few crystalline phases can be observed within the first few nanometres of the nc-SiO_x:H(n) film, directly adjacent to the intrinsic a-Si:H(i) passivation layer, which can be considered as the crystalline incubation layer. After that, numerous microcrystalline zones appear in the nc-SiO_x:H(n) film, extending towards the nc-SiO_x:H(n)/IMO interface, which is crucial in improving both the contact properties of the nc-SiO_x:H(n)/IMO interface and FF of the device. Compared to the diffraction patterns in area I (c-Si substrate) and area III (amorphous silicon), the diffraction pattern in area II suggests a mixed phase of amorphous and nanocrystalline silicon, rather than a pure crystalline phase, which is likely due to the introduction of oxygen. Figure 1c,d displays the certified current–voltage (I–V) curve and external quantum efficiency (EQE), respectively, of the best device featuring a nc-SiO_x:H(n) window layer deposited under VHF1. By comparison, the photovoltaic parameters of the best devices under RF and VHF2 (in-house measurements) are listed together in Table 1. The device PCE increases with increasing excitation frequency, where a relatively lower PCE of 25.83% is obtained under RF. Under VHF1 and VHF2, comparable higher PCEs of 25.98% and 26.02% are obtained, respectively. The PCE enhancement at different frequencies can mainly be attributed to a lower parasitic absorption loss and contact resistivity

caused by a higher crystallinity (Supplementary Table 1) with decreasing amorphous incubation layer thickness of the nc-SiO_x:H(n) films under increasing frequencies, translating to improvements in J_{sc} and FF. Note that the devices under VHF1 and VHF2 exhibit a FF exceeding the theoretical value predicted by Green’s formula³⁶ (Supplementary Fig. 1). The main reason for this is that our devices, thanks to the excellent surface passivation, are limited by Auger recombination, resulting in a diode ideality factor of 2/3 (refs. 37,38) rather than 1 as assumed in Green’s formula. Given the high-quality nc-SiO_x:H(n) window layer deposited under VHF1, in the following section we investigate the effect of VHF1 on the optoelectrical properties and large-area uniformity of the nc-SiO_x:H(n) as well as the device performance.

We first investigate the effect of the nc-SiO_x:H(n) thickness ranging from 8 to 28 nm on the SHJ device performance, as displayed in Fig. 2. Note that all other layers were kept identical and no MgF₂ anti-reflection layer was applied to these devices. With a thin nc-SiO_x:H(n) window layer (8 nm), the device shows a moderate average open-circuit voltage (V_{oc}) and FF of ~736 mV and ~81%, respectively, resulting in a moderate average PCE of ~23.8%. The device parameters (especially the V_{oc} and FF) increase significantly by increasing the nc-SiO_x:H(n) thickness from 8 to 12 nm, resulting in a champion PCE of 25.85% for a thickness of 24 nm (V_{oc}, 749.8 mV; FF, 85.7%; and J_{sc}, 40.24 mA cm⁻²). Beyond a thickness of 12 nm, the improvements gradually diminish and ultimately saturate at thicknesses of ≥20 nm; J_{sc} increases with increasing thickness from 8 to 16 nm, followed by a gradual decrease for thicker nc-SiO_x:H(n) films. These results indicate that SHJ device performance depends notably on the nc-SiO_x:H(n) thickness, which will be further investigated in the next section.

Figure 3a shows Raman spectra of nc-SiO_x:H(n) films with different thicknesses deposited on a glass substrate under VHF1. The absence of a clear crystalline peak near 520 cm⁻¹ for the 8 nm film indicates that an amorphous phase dominates the characteristics. With increasing film thickness, the amorphous peak intensity near 480 cm⁻¹ decreases, whereas the crystalline peak emerges to saturate gradually for thicknesses of ≥20 nm. This reveals that crystalline nucleation in the nc-SiO_x:H(n) film starts after a few nanometres of amorphous incubation, adjacent to the a-Si:H(i) passivation layer, and that the crystalline fraction increases with thickness, consistent with the crystallinity (Fig. 3a, inset) obtained by fitting Raman spectra (Supplementary Fig. 2). Note that the crystalline phases observed at the a-Si:H(i)/nc-SiO_x:H(n) interface in the HR-TEM image (Fig. 1b) might grow at the later stage of the nc-SiO_x:H(n) deposition due to the hydrogen etching during the process. The contact resistivity (ρ_c) of the c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO heterocontact was measured by the Cox and Strack method³⁹, using the inset structure in Fig. 3b. The ρ_c was extracted by fitting the trend of resistance versus front circular contact diameter (Supplementary Fig. 3), and the dependence of ρ_c on the nc-SiO_x:H(n) thickness is shown in Fig. 3b. A high ρ_c of 109.8 mΩ cm² is obtained on the structure with 8 nm nc-SiO_x:H(n), which is consistent with the moderate average FF of ~81% of the device. Further increasing the nc-SiO_x:H(n) thickness to 12 nm results in a dramatically lower ρ_c to 49.5 mΩ cm², and ρ_c decreases monotonously with increasing thickness. The result indicates that contact properties of the nc-SiO_x:H(n)/IMO interface are suboptimal with only 8 nm of nc-SiO_x:H(n), which might be ascribed to the poor contact interface between the less-conductive amorphous phase and IMO¹¹. With increasing nc-SiO_x:H(n) thickness, the nc-SiO_x:H(n)/IMO contact interfaces are greatly improved as now increasingly conductive crystalline phases directly contact the IMO, as also observed in the HR-TEM image in Fig. 1b. In addition, the trend of crystallinity with thickness is in good agreement with the ρ_c of nc-SiO_x:H(n)/IMO and electrical properties (FF and V_{oc}) of the device featuring the nc-SiO_x:H(n) window layer. This indicates that the crystalline phase in nc-SiO_x:H(n) promotes vertical conduction across the nc-SiO_x:H(n)/IMO interface, resulting in a substantially lower ρ_c and increase in FF. In addition, the crystalline

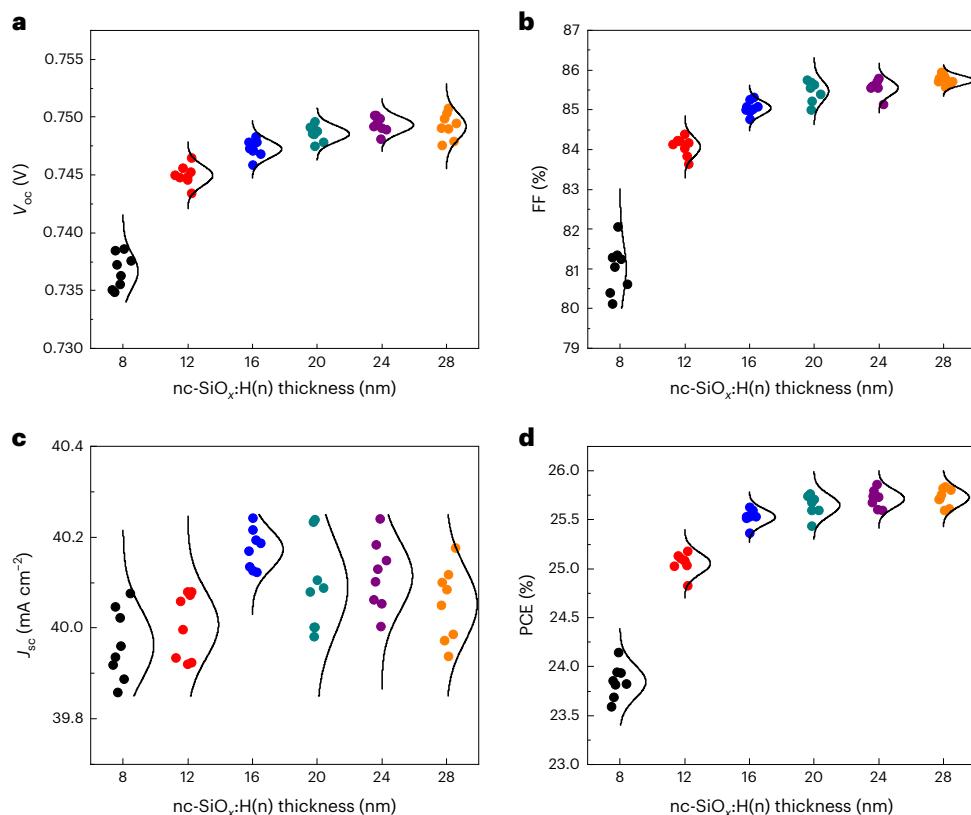


Fig. 2 | Dependence of SHJ device parameters on the thickness of nc-SiO_x:H(n) layer deposited under VHF1. **a**, V_{oc} . **b**, FF. **c**, J_{sc} . **d**, PCE. The curves are normal distributions from eight devices.

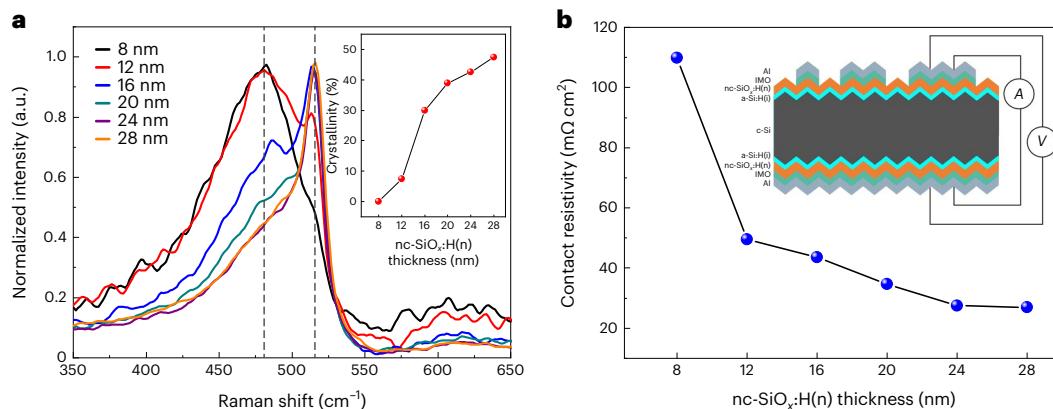


Fig. 3 | Thickness-dependent microstructure and contact resistivity of nc-SiO_x:H(n) layers deposited under VHF1. **a**, Normalized Raman spectra of nc-SiO_x:H(n) layers with thickness varying from 8 to 28 nm. Dashed lines indicate the Raman shift values of 480 cm^{-1} and 520 cm^{-1} . The inset shows the crystallinity of nc-SiO_x:H(n) with different thicknesses obtained by fitting Raman spectra.

b, Dependence of the contact resistivity of the front c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO heterocontact on the nc-SiO_x:H(n) thickness. The inset displays the structure used for the contact resistivity measurement. *A* and *V* in the inset are labels for current and voltage. The curves drawn on top of the data in the insets of **a** and **b** are guides to the eye.

phase is likely to induce a higher doping efficiency and subsequently an improved field-effect passivation, resulting in a higher V_{oc} . Furthermore, the deterioration of c-Si/a-Si:H(i) surface passivation, which may happen due to bombardment damage during the TCO sputtering process⁴⁰, can be mitigated with increasing nc-SiO_x:H(n) thickness, which further contributes to a higher V_{oc} with a thicker nc-SiO_x:H(n) layer. The absorption, transmission and reflectance spectra; the optical bandgap of nc-SiO_x:H(n) with different thicknesses; and the EQE, reflectance spectra and internal quantum efficiency (IQE) of corresponding SHJ devices are displayed in Supplementary Fig. 4. As expected, the EQE for the device with a thicker nc-SiO_x:H(n) layer decreases at short

wavelengths (Supplementary Fig. 4f), which can be ascribed to a higher parasitic absorption in the 300–600 nm spectral range (Supplementary Fig. 3a), even though the nc-SiO_x:H(n) layer exhibits a larger optical bandgap than the a-Si:H (Supplementary Fig. 4b). However, thanks to its intermediate refractive index, the increase in nc-SiO_x:H(n) layer thickness (Supplementary Fig. 4e), as part of the front contact stack, is beneficial to a lower reflectance of SHJ solar cells, which in turn increases the EQE at 600–1,200 nm for thicker nc-SiO_x:H(n) layers. As a result, the trade-off between parasitic absorption loss and reflectance gain of nc-SiO_x:H(n) leads to the slight thickness dependence of J_{sc} , as shown in Fig. 2c.

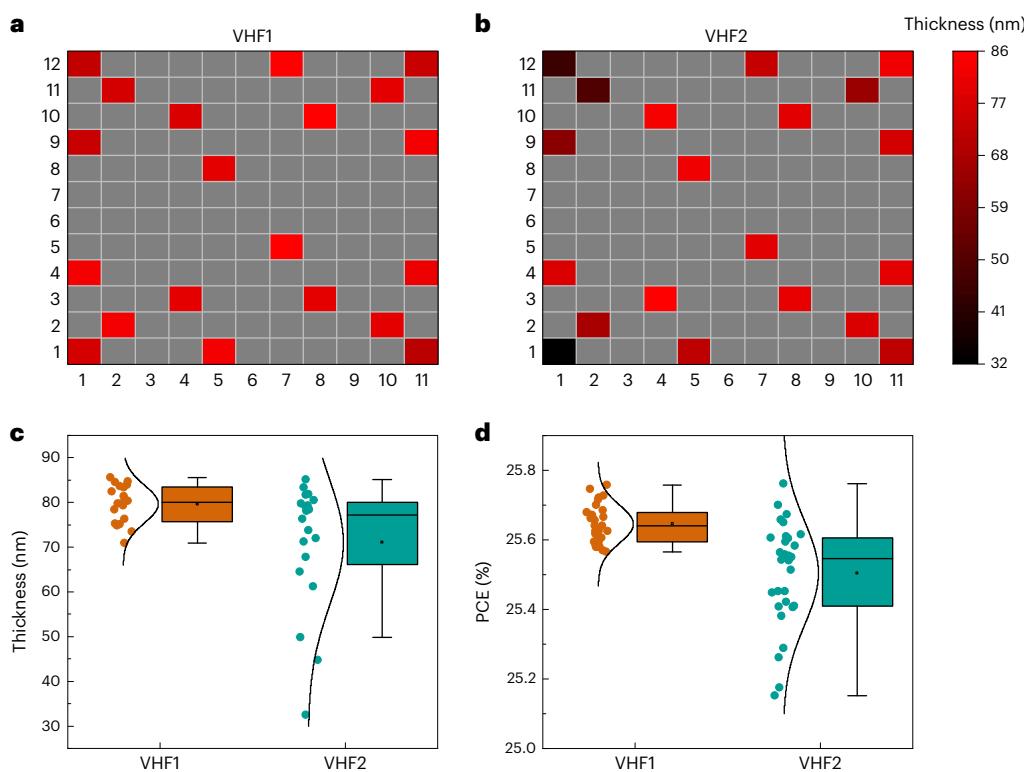


Fig. 4 | Dependence of nc-SiO_x:H(n) uniformity and device performance on frequency. **a,b**, Thickness distribution of nc-SiO_x:H(n) films deposited under VHF1 (27 MHz; **a**) and VHF2 (40 MHz; **b**) in a tray. **c,d**, Comparison of nc-SiO_x:H(n) thickness (**c**) and PCE distribution (**d**) of SHJ solar cells featuring nc-SiO_x:H(n) deposited under VHF1 and VHF2. The boxes, central lines and points in the boxes

are 25–75% distributions, median values and mean values, respectively. The upper and lower whiskers represent the largest and smallest values that are not outliers defined as >1.5 times the interquartile range. The curves are normal distributions. The sample sizes for thickness and PCE uniformity are 20 and 30, respectively.

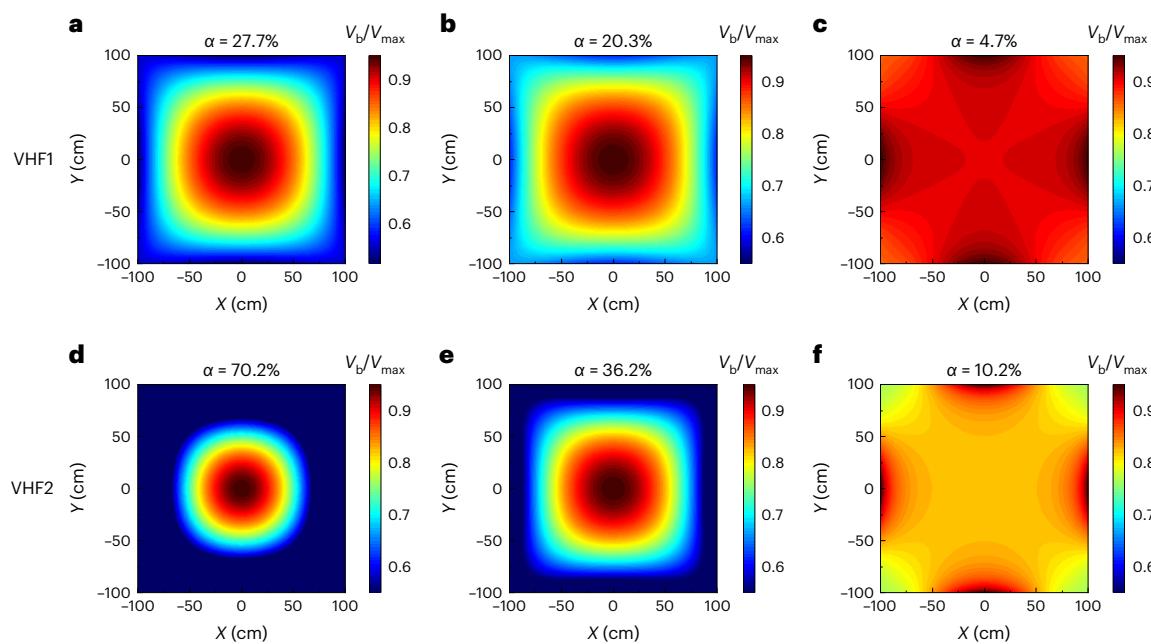


Fig. 5 | Simulative voltage distribution on frequency. **a–f**, Normalized voltage distribution between electrodes (V_b) under the excitation frequency of VHF1 and VHF2 in the case of a flat electrode (**a** and **d**), curved electrode without glass plate (**b** and **e**) and curved electrode with glass plate (**c** and **f**) for a sheath thickness

of 1 mm, electrode size of 2 m × 2 m and electrode gap of 1 cm. The area shown represents the PECVD chamber, X and Y represent the x and y axes of the chamber plane, respectively.

To demonstrate the superiority of VHF1 over VHF2 in terms of large-area uniformity, nc-SiO_x:H(n) films on M6-size glass substrates, placed regularly in different slots of the same deposition tray, were

deposited in a large-scale reactor (showerhead size is 2.03 × 2.03 m²) under VHF1 and VHF2 separately, with their thickness being measured by spectroscopic ellipsometry. As shown in Fig. 4, we can see that both

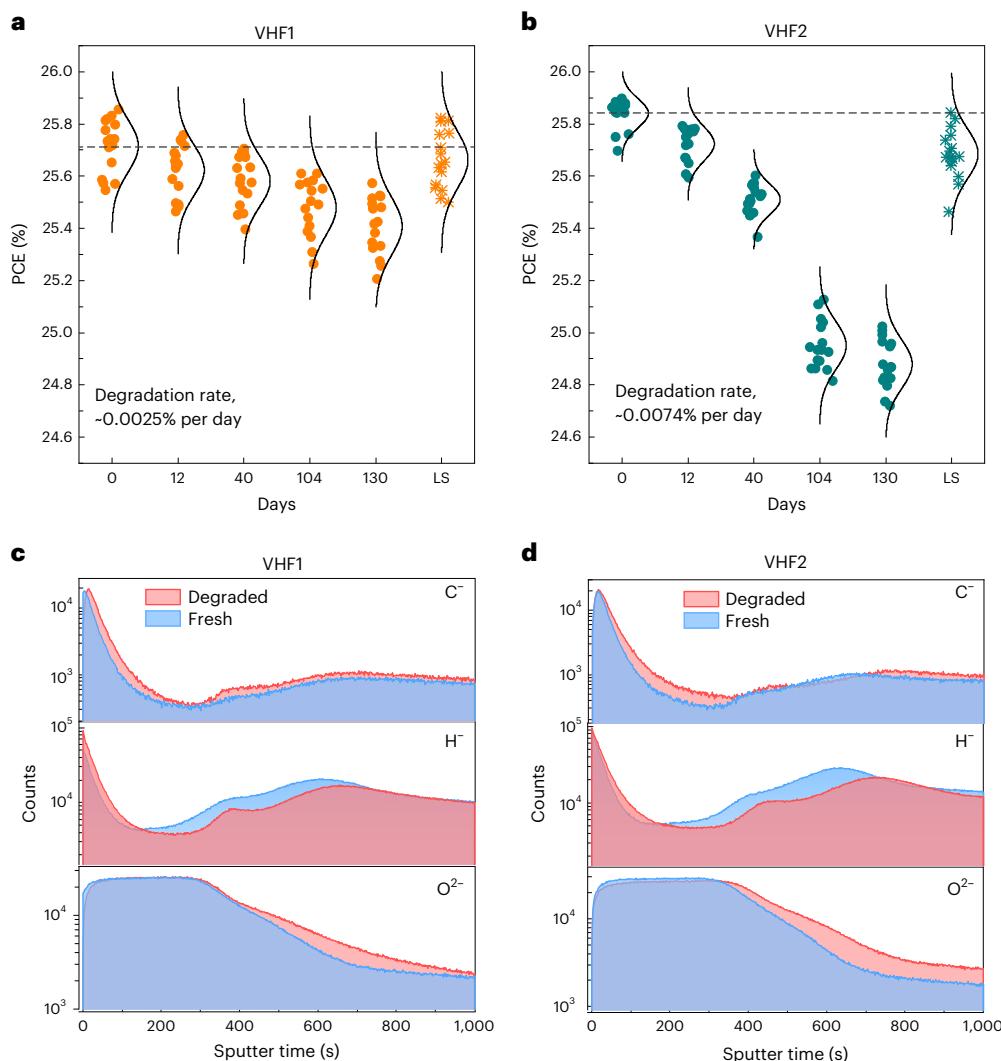


Fig. 6 | Dark degradation of SHJ solar cells and mechanism. **a,b**, Dark degradation of SHJ solar cells with nc-SiO_x:H(n) deposited under VHF1 (**a**) and VHF2 (**b**), over 130 days and with light soaking (LS); the curves are normal distributions from 16 devices and the horizontal dashed lines represent average

PCE values of as-fabricated devices (25.71% and 25.84% for VHF1 and VHF2, respectively). **c,d**, Elemental depth profiles of a-Si:H(i)/nc-SiO_x:H(n)/IMO stacks with nc-SiO_x:H(n) deposited under VHF1 (**c**) and VHF2 (**d**) on a silicon substrate measured by TOF-SIMS.

the film thickness and device PCE distributions under VHF1 are superior to those of VHF2, especially for samples located near the chamber corner. Photos of the experimental trays shown in Supplementary Fig. 5 also demonstrate visually that the nc-SiO_x:H(n) deposited at VHF1 shows a superior uniformity to that at VHF2. Although the champion PCEs are comparable under VHF1 and VHF2, the PCE distribution range under VHF1 (25.7–25.9%) is much narrower than in the case of VHF2 (25.3–25.9%), demonstrating a higher fabrication yield. The significant improvements in large-area thickness uniformity and PCE distribution under VHF1 are due to the minimization of the standing wave effect, achieved by reducing the plasma excitation frequency and optimized showerhead design. As a result, a large-size PECVD chamber under VHF1 is successfully developed for mass production, enabling the loading of 162 pieces of 210 mm half wafers in one batch (Supplementary Fig. 6), corresponding to a throughput of 14,400 pieces per hour and an annual production capacity of ~600 MW.

To clarify the different uniformity values under VHF1 and VHF2, we calculated the normalized voltage distributions under VHF1 and VHF2 for different electrode shapes (Fig. 5), by solving partial differential equations numerically with the finite element method using the commercial solver FLEXPDE (details in Supplementary Note 1).

The α is defined as the non-uniformity degree of the voltage within the chamber ($\alpha = \frac{V_{\max} - V_{\min}}{V_{\max} + V_{\min}} \times 100\%$), where V_{\max} and V_{\min} represent the maximum and minimum voltage within the chamber. With a flat electrode (Fig. 5a,d), the voltage distribution peaks at the centre, which suggests a higher plasma density and a thicker film at the centre, displaying the typical standing wave effect. This is different from the discharge driven by a conventional RF (13.56 MHz), in which the plasma density is usually higher at the radial edge of the electrode due to the edge effect⁴¹. The uniformity of the voltage distribution under VHF1 and VHF2 is $\pm 27\%$ and $\pm 70\%$, respectively, both of which are very poor. As the plasma density increases, the relative permittivity of the plasma becomes larger. So, the electromagnetic wavelength propagating in the plasma becomes shorter, resulting in an enhanced standing wave effect and a poorer voltage uniformity. By adopting a curved electrode, the voltage uniformity within the chamber is significantly improved to $\pm 20\%$ and $\pm 36\%$ under VHF1 and VHF2, respectively (Fig. 5b,e). In the PECVD system, an additional glass plate is required on the curved electrode to maintain the vacuum in the curved part of the electrode. The calculated results indicate that voltage uniformity can be significantly improved to $\pm 4.6\%$ and $\pm 10\%$ under VHF1 and VHF2,

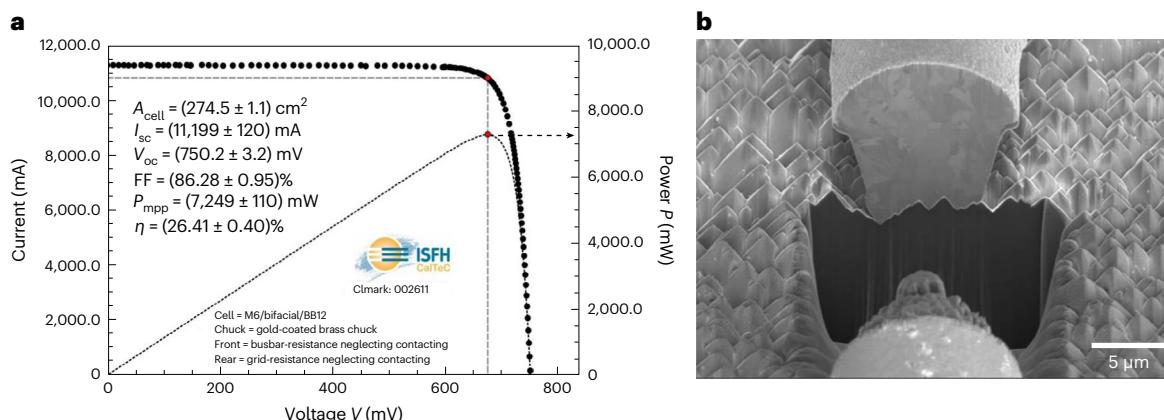


Fig. 7 | SHJ solar cell with Cu-plated electrode. **a**, Certified I – V curve of the SHJ device with Cu-plated electrode under standard test conditions. Front busbar resistance and rear grid resistance are neglected in the measurement. **b**, Cross-sectional scanning electron microscopy image of a Cu-plated finger on a textured

c-Si surface. The dark region underneath the Cu-plated finger is the Si wafer exposed through the ion-milled trench, and the foreground structure is an ion-milling artefact from the cut Cu-plated finger.

respectively (Fig. 5c,f). However, the plasma cannot be completely prevented from entering the curved part of the electrode during the deposition process, due to the need for gas input and exhaust. Thus, the uniformity improvement may be in between the ranges of curved electrodes with or without the glass plate for VHF1 (4.6–20%) and VHF2 (10–36%), which is consistent with the experimental results shown in Fig. 4a,b. Furthermore, other factors such as dust formation, gas depletion and the inhomogeneous⁴², complex structure and deformation of substrate and electrode^{43,44} may also influence the homogeneity of silicon thin films.

Dark degradation of SHJ solar cells at VHF1 and VHF2

In addition to the large-area uniformity, we also observed a lower dark degradation rate of SHJ devices under VHF1 than under VHF2, as shown in Fig. 6a,b. Both SHJ cells exhibit a similar dark degradation in the first 40 days, and then the dark degradation accelerates for the devices under VHF2. In 130 days, the devices under VHF1 show an absolute average degradation rate of ~0.0025% per day, representing only one third of that under VHF2 (~0.0074% per day). The dark degradation mainly is manifested in FF and V_{oc} decreases (Supplementary Fig. 7), while J_{sc} exhibits a negligible degradation; as a result, the degradation is likely due to a loss in surface passivation. After light soaking under 80 suns at 230 °C for 40 s, the device PCE can almost be fully recovered under VHF1 (average PCE (η_{ave}) ≈ −0.04%), whereas a relatively larger PCE loss (η_{ave} ≈ −0.15%) is observed under VHF2, as also shown in Fig. 6. With regards to the light-soaking-induced improvement, this can most likely be attributed to an anomalous Staebler–Wronski effect, known to yield improved carrier selectivity of SHJ contact stacks⁴⁵. As a possible explanation behind the dark degradation, elemental depth profiles (carbon, C[−]; hydrogen, H[−]; and oxygen, O^{2−}) in the c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO stack were measured before and after dark degradation using time-of-flight secondary ion mass spectrometry (TOF-SIMS), as shown in Fig. 6c,d. Compared with the degraded device under VHF1, a decrease of H[−] and an increase of O^{2−} near the a-Si:H(i)/nc-SiO_x:H(n) interface and in the a-Si:H(i) passivation layer are observed on the degraded device under VHF2, while C[−] exhibits negligible change. This is likely attributed to the promotion of SiH₄ dissociation induced by a high electron density under the increasing excitation frequency of the PECVD, intrinsically, resulting in a lower density of the nc-SiO_x:H(n) due to the high amount of SiH₂ and SiH₃ in the film^{19,46,47}. Hence, the porous nc-SiO_x:H(n) film, containing voids and defect states, is more likely to suffer from the effusion of hydrogen and the intrusion of oxygen

and moisture, which may lead to the oxidation and passivation degradation of a-Si:H(i), resulting in PCE degradation (especially in V_{oc} and FF), according to Liu et al.'s work^{48,49}. This is consistent with the fact that the degradation of a device under VHF2 stems from the V_{oc} and FF reduction (Supplementary Fig. 7). We also found that after light soaking, the device PCE loss under VHF2 is mainly ascribed to the V_{oc} and FF decrease, probably due to the passivation degradation and series resistance increase induced by the oxidation of the a-Si:H(i). Further systematic studies are needed to determine the effect of the PECVD excitation frequency on the microstructure of nc-SiO_x:H(n) films and the final device stability. Furthermore, our findings are directly transferrable to perovskite/silicon tandem solar cells relying on SHJ bottom-cell technologies, aiding in their race to the market.

SHJ solar cells with Cu-plated electrodes

According to optical loss analysis using EQE and reflection (Supplementary Fig. 8), front silver finger shading loss (1.30 mA cm^{−2}) is identified as one of the main PCE loss factors due to a large Ag finger width of ~43.3 μm (Supplementary Fig. 9). To further improve the device performance, an advanced Cu plating technology by SunDrive was used to replace the screen-printed Ag electrode. SunDrive incorporates a direct plating technique in which copper is directly electroplated onto the TCO film, avoiding the complications and complexity associated with an additional seed layer deposition (for example, physical vapor deposited (PVD) Cu (ref. 50) or screen-printed Ag (ref. 51)) and the etch-back process required for other well-adopted plating techniques. This allows for the finger contact widths to be defined solely by the width of the openings in the masking film. The J_{sc} and FF significantly improved to 40.80 mA cm^{−2} and 86.28%, respectively, resulting in a certified PCE of 26.41% for full-area bifacial c-Si solar cells with Cu-plated electrodes (Fig. 7a and Table 1), which agrees well with the enhancement of the EQE (Fig. 1d). The J_{sc} improvement (0.36 mA cm^{−2}) can be mainly attributed to the reduced shading loss, thanks to a much narrower Cu finger width (~9 μm), as demonstrated by the cross-sectional scanning electron microscopy image in Fig. 7b and the optical microscope images (Supplementary Fig. 10). We can observe that the dense, uniform and smooth Cu-plated finger forms a continuous contact with IMO, while the low-temperature Ag paste contact is filled with nanometre-size voids (Supplementary Fig. 9), and some organic residues remain in the fingers along with undesirable point contacts with TCO underneath (ref. 29). As a result, the bulk resistivity of the Cu finger and contact resistivity of the IMO/Cu interface are much lower than that of a screen-printed Ag electrode (Supplementary Table 2), resulting

in a higher FF. A damp heat (DH) stability test was conducted for the module with Cu-plated cells, as shown in Supplementary Fig. 11. We observe that the Cu-plated module shows a comparable degradation (<4%) to the Ag screen-printed module after the test with a DH85 meter (1,000 h). These merits demonstrate the great potential of Cu-plated electrodes for efficiency improvements in SHJ solar cells.

Conclusions

We designed and developed a production-scale PECVD system featuring a high excitation frequency (VHF1) for nc-SiO_x:H(n) window layer deposition, enabling improvements in both optoelectronic properties and large-area uniformity. With the industrially compatible nc-SiO_x:H(n) window layer, the front electron selective a-Si:H(i)/nc-SiO_x:H(n)/IMO stack displays a low parasitic absorption, a high-quality surface passivation and a low contact resistivity, resulting in a certified PCE of 25.98% on M6-size bifacial SHJ solar cells with conventional screen-printed silver electrodes. The SHJ device under VHF1 exhibits a lower dark degradation rate and a narrower PCE distribution range, compared to that under VHF2. With advanced Cu plating technology, high-quality Cu electrodes featuring a narrow width, low bulk resistivity and low contact resistivity are obtained. By replacing the screen-printed silver electrode with the Cu-plated electrode, the certified PCE is further boosted to 26.41% on an M6-size SHJ device, representing the best efficiency for full-area bifacial c-Si solar cells with Cu metallization. This work provides effective strategies for high-throughput SHJ solar cell fabrication, which can accelerate the mass production of SHJ solar cells.

Methods

Device fabrication

Commercial M6-size (274.5 cm²) n-type (100)-oriented Czochralski (C_z) silicon wafers (150 µm, 1 Ω cm) were used in this work. A wet-chemical process including saw-damage removal, texturing and cleaning was applied to the as-cut wafers. An intrinsic a-Si:H passivation layer (5 nm) was first deposited by PECVD on both sides of the wafer, and then nc-SiO_x:H(n) layers with different thicknesses were deposited as the front window layer under RF, VHF1 and VHF2 without surface pretreatment, followed by 30 nm hydrogenated nanocrystalline silicon oxide with p-type doping (nc-Si:H(p)) deposition at the rear side. All the a-Si:H(i), nc-SiO_x:H(n) and nc-Si:H(p) layers were deposited using the large-size PECVD system designed and produced by Suzhou Maxwell Technologies. Detailed deposition parameters are listed in Supplementary Table 1. After PECVD deposition, a newly developed IMO (80 nm) was sputtered on both sides; the abbreviation M stands for transition metals including titanium, cerium and tantalum. There are titanium oxide (TiO₂), cerium oxide (CeO₂) and tantalum oxide (Ta₂O₅) with corresponding mass ratios of 0.22 wt%, 0.14 wt% and 0.03 wt%, respectively, in the target. The PVD deposition parameters and optoelectronic properties of IMO can be found in our previous work^{35,52}. For metallization, silver electrodes were prepared by screen printing using a low-temperature silver paste, followed by annealing at 210 °C for 20 min.

Copper-plated electrodes

Alternatively, for the champion cell, a copper-based electrode was applied using proprietary processes at SunDrive. The wafers were first coated in a resin-based mask, deposited at room temperature using a deposition system built by SunDrive. Once coated, wafers were placed onto a heated bed at a temperature of 100 °C for a period of 6 min to allow for solvent evaporation and mask stabilization. The final thickness of the mask was determined to be 8 ± 1 µm. Once coated, the mask was selectively exposed to a collimated light source through a shadow mask consisting of the desired grid pattern, for a duration of 5 s and with an illumination wavelength between 350 nm and 450 nm using a home-built optical system (SunDrive). The mask was then selectively opened via a short 20 s submersion in an alkaline-based

solution held at a temperature of 30–40 °C. The average width of the finger openings in the mask was approximately 10 µm. The TCO surface, exposed through the openings, was then subjected to bias-assisted light-induced plating of copper in a horizontal plating tool using a proprietary acid-based copper electroplating formulation and a phosphorous deoxidized copper sacrificial anode, which was positioned ~5 mm from the wafer surface. During plating, the cell's surface was exposed to a light source with a colour temperature of 6,500 K, and an intensity tuned to enable a plating current of 42 mA cm⁻². The plating duration was set to 10 min, resulting in an average deposited contact height of 13 ± 1 µm. The copper-plated cells were rinsed in deionized water for a duration of 2 min followed by a brief dry under a fan-forced infrared dryer. Once dry, a similar plating system was then used to plate a thin coating (<100 nm) of silver on the surface of the Cu to minimize the risk of Cu oxidation. The silver plating was performed in a nitrate-based electrolyte with an inert anode for a duration of 5 s. Cells were then submerged in a deionized rinse bath for a duration of 2 min prior to drying. Surface masks on the cell were then removed by submersion in an alkaline-based solution at room temperature for a duration of 2 min, followed by a 5 min rinse in deionized water and subsequent drying.

Light soaking and MgF₂ anti-reflection layer

A light soaking process was then performed under high-intensity light-emitting diode treatment for all SHJ solar cells with screen-printed Ag electrodes and Cu-plated electrodes. This light soaking process before and after dark degradation in Fig. 6 are under the same conditions of 80 suns at 230 °C for 40 s. For cells sent to the Institute for Solar Energy Research Hamelin (ISFH) for certification, a 110-nm-thick MgF₂ film was deposited on the surface of the wafer using a thermal evaporator (VNano), with the deposited area defined by a shadow mask to ensure that the cell busbars remain uncoated.

Characterization

Raman spectra were obtained at room temperature in a backscattering geometry with an excitation wavelength of 325 nm (Renishaw). The optical transmission, absorption and reflection spectra were measured on a spectrophotometer (PerkinElmer Lambda1050). The minority carrier lifetimes of the passivated samples were measured by a Sinton flash tester (WCT-120) under transient mode. The contact resistivity of the c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO was measured using the Cox and Strack method, using the structure shown as an inset in Fig. 3b, where the front IMO/Al electrode with different diameters was deposited through a shadow mask. The dark current–voltage measurements were performed on a probe station (Supplementary Fig. 3), and the ρ_c was extracted by fitting the trend of resistance versus circular contact diameter. The contact resistivity of the metal electrodes/IMO was measured using photovoltaic tools (TLM SCAN). The cross-section of the c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO interface was observed by HR-TEM (FEI Titan Cubed Themis G2 300). Elemental profiles of the c-Si/a-Si:H(i)/nc-SiO_x:H(n)/IMO interface before and after dark degradation were analysed by TOF-SIMS (ION TOF GmbH-Muenster), using a 500 eV Cs⁺ sputter beam. For large-scale uniformity characterization, nc-SiO_x:H(n) films and SHJ devices were fabricated on 20 pieces of M6 wafers placed at various locations in the chamber. Illuminated current density (J)–V characteristics of SHJ solar cells were measured under standard conditions (25 °C, 100 mW cm⁻²) using a solar simulator, which was calibrated using a certified reference cell from Fraunhofer ISE. The EQE and reflectance spectra of SHJ devices were measured from 300 to 1,180 nm using the Bentham PVE300-IVT system. For the simulation, the voltage distribution partial differential equations were solved numerically with the finite elements method using the commercial solver FLEXPDE.

Reporting summary

Further information on research design is available in the Nature Portfolio Reporting Summary linked to this article.

Data availability

All data generated or analysed during this study are included in the published Article and its Supplementary Information. Source data are provided with this paper.

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Author contributions

X.Y. and C.Y. conceived the idea, designed the experiments and led the project. C.Y. and K.G. fabricated the devices, performed the device characterizations and wrote the paper. C.-W.P. and C.H. helped with the device optimization and analysis. S.W. and W.S. performed the Raman spectra and contact resistivity measurements. J. Zhang and D.W. performed the large-scale uniformity experiment. V.A., Y.H., J.C., Huiting Wu, L.G., D.C. and A.L. designed and carried out the copper plating. G.T., Y.Z., W.J. and Y.S. performed the simulation validation of the voltage distribution on excitation frequency and substrate size. G.D. performed the TCO deposition, and H.J. performed screen printing. Haihong Wu performed lifetime, EQE and HR-TEM measurements. C.X., Q.M. and X.W. performed HR-TEM and EQE measurements. K.L. and D.X. performed the absorption spectra and optical bandgap measurement. J.P. and W.L. helped with the TOF-SIMS result analysis and discussion. X.C. designed the PECVD chamber. S.D.W. helped with the discussion of the results. J. Zhou, X.Y. and X.Z. supervised the project. All authors contributed to the discussion of the results and revision of the manuscript.

Competing interests

C.Y., C.-W.P., C.H., J. Zhou, D.W., G.T., G.D., H.J., Haihong Wu, X.C. and J. Zhang are employees of Suzhou Maxwell Technologies Co. Ltd. V.A., D.C., A.L., Y.H., J.C., Huiting Wu and L.G. are employees of SunDrive Solar Pty., Ltd. All other authors declare no competing interests.

Additional information

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Solar Cells Reporting Summary

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► Experimental design

Please check: are the following details reported in the manuscript?

1. Dimensions

Area of the tested solar cells

- Yes
 No

274.1 square centimeter, 274.5 square centimeter

Method used to determine the device area

- Yes
 No

Device characterization in Method

2. Current-voltage characterization

Current density-voltage (J-V) plots in both forward and backward direction

- Yes
 No

Forward direction is enough for our solar cells

Voltage scan conditions

For instance: scan direction, speed, dwell times

- Yes
 No

Forward direction from -0.1 to 0.78 V; 100 points; integral time 5 ms; delay time 5 ms

Test environment

For instance: characterization temperature, in air or in glove box

- Yes
 No

Device characterization in Method

Protocol for preconditioning of the device before its characterization

- Yes
 No

Device characterization in Method

Stability of the J-V characteristic

Verified with time evolution of the maximum power point or with the photocurrent at maximum power point; see ref. 7 for details.

- Yes
 No

Figure 6a and Figure 6b

3. Hysteresis or any other unusual behaviour

Description of the unusual behaviour observed during the characterization

- Yes
 No

Silicon solar cells do not exhibit hysteresis under standard conditions

Related experimental data

- Yes
 No

Silicon solar cells do not exhibit hysteresis under standard conditions

4. Efficiency

External quantum efficiency (EQE) or incident photons to current efficiency (IPCE)

- Yes
 No

Figure 1d

A comparison between the integrated response under the standard reference spectrum and the response measure under the simulator

- Yes
 No

Certification reports do not contain this comparison

For tandem solar cells, the bias illumination and bias voltage used for each subcell

- Yes
 No

N/A

5. Calibration

Light source and reference cell or sensor used for the characterization

- Yes
 No

Device characterization in Method

Confirmation that the reference cell was calibrated and certified

- Yes
 No

Device characterization in Method; Reference cell used for certification in ISFH is unknown.

<p>Calculation of spectral mismatch between the reference cell and the devices under test</p> <p>6. Mask/aperture</p> <p>Size of the mask/aperture used during testing</p> <p>Variation of the measured short-circuit current density with the mask/aperture area</p> <p>7. Performance certification</p> <p>Identity of the independent certification laboratory that confirmed the photovoltaic performance</p> <p>A copy of any certificate(s) <i>Provide in Supplementary Information</i></p> <p>8. Statistics</p> <p>Number of solar cells tested</p> <p>Statistical analysis of the device performance</p> <p>9. Long-term stability analysis</p> <p>Type of analysis, bias conditions and environmental conditions <i>For instance: illumination type, temperature, atmosphere humidity, encapsulation method, preconditioning temperature</i></p>	<p><input type="checkbox"/> Yes Certification reports do not contain this information.</p> <p><input checked="" type="checkbox"/> No Explain why this information is not reported/not relevant.</p> <p><input type="checkbox"/> Yes total-area testing for all the devices</p> <p><input checked="" type="checkbox"/> No</p> <p><input type="checkbox"/> Yes N/A</p> <p><input checked="" type="checkbox"/> No</p> <p><input checked="" type="checkbox"/> Yes ISFH CalTec, Germany</p> <p><input type="checkbox"/> No</p> <p><input type="checkbox"/> Yes Certified J-V curves were shown in the manuscript</p> <p><input checked="" type="checkbox"/> No</p> <p><input checked="" type="checkbox"/> Yes In the main body of this work, $8+16+16+30+30+1+1= 102$ devices</p> <p><input type="checkbox"/> No</p> <p><input checked="" type="checkbox"/> Yes Figure 2, Figure 4b, Figure 6a and Figure 6b</p> <p><input type="checkbox"/> No</p> <p><input checked="" type="checkbox"/> Yes Device characterization in Method</p> <p><input type="checkbox"/> No</p>
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