M51A MIDTERM SOLUTIONS
– closed books and notes –
(6 problems, 110 minutes)

July 28, 2000

Problem 1. (6 points)

a) A 16-bit vector represents a set of positive integers {0,...,N}. Which of the following coding alternatives

1. BCD
2. Hexadecimal
3. Excess-3
4. Binary

provides the largest range? Why? (Give N for each case).

1. **BCD requires 4 bits per digit, and each digit is in the range {0,...,9}. 16 bits can represent a 4-digit number, so the largest number represented is** $N = 9999_{10}$.
2. **Hexadecimal requires 4 bits per digit, and each digit is in the range {0,...,F}. 16 bits can represent a 4-digit number, so the largest number represented is** $N = FFFF_{16} = 65535_{10}$.
3. **Excess-3 requires 4 bits digit, and each digit is in the range {0,...,9}. 16 bits can represent a 4-digit number, so the largest number represented is** $N = 9999_{10}$.
4. **Binary requires 1 bits per digit, and each digit is in the range {0,1}. 16 bits can represent a 16-digit number, so the largest number represented is** $N = 1111111111111111_2 = FFFF_{16} = 65535_{10}$.

Both (2) Hexadecimal and (4) Binary provide the largest range.

b) Let $a = (010110011000)$ and $b = (001110110101)$. If a represents a number in the BCD code and b in the binary code, what is the value in decimal of their sum $a + b$?

a	=	0101	1001	1000				(BCD coded)
	=	5	9	8				(in decimal)
b	=	0011		1011		0101		(binary)
	=	3		B		5		(hexadecimal)
	=	$3*256$	+	$11*16$	+	5		(convert to decimal)
	=	768	+	176	+	5		
	=	949						(decimal)

$$a + b = 598_{10} + 949_{10} = 1547_{10}$$

Problem 2. (5 points)

Connect the pMOS transistors so that the circuit of Fig. 1 implements a switching function. Assuming the positive logic give a sum of product expression for the output.

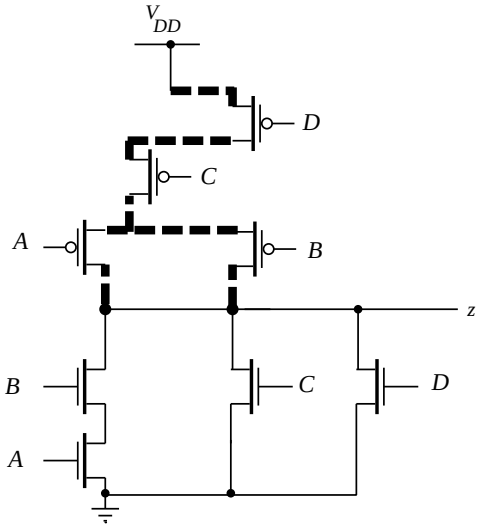


Fig. 1

NMOS switching function: $ab + c + d$

PMOS switching function: $(ab + c + d)' = (ab)'c'd' = (a' + b')c'd'$

Sum of products expression: $a'c'd' + b'c'd'$

Problem 3. (8 points)

a) With the help of Table 1, determine the worst case propagation delay of the network shown in Fig. 2. (Need to obtain Low to High and High to Low delays to determine the worst case.) Assume that each network output is connected to an input with load factor of 1.

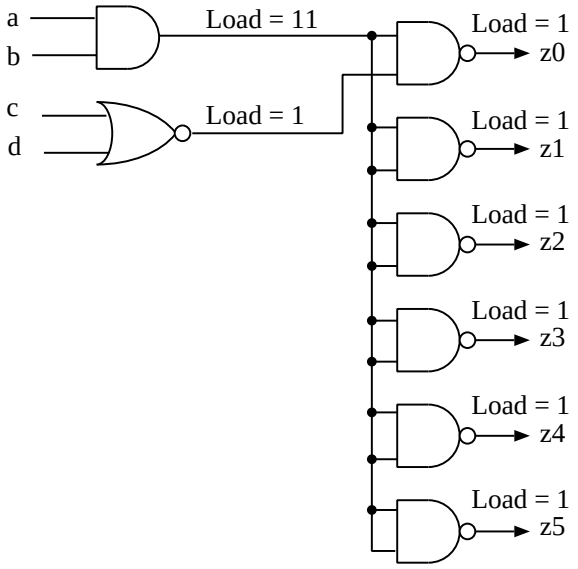


Table 1: Characteristics of CMOS gates

Gate type	Fan-in	Propagation delays		Load factor	Size
		t_{pLH} [ns]	t_{pHL} [ns]	[standard loads]	[equiv. gates]
AND	2	$0.15 + 0.039L$	$0.18 + 0.019L$	1.0	2
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0	1
NAND	2	$0.05 + 0.035L$	$0.08 + 0.027L$	1.0	1

The load on the AND gate is 11, the load on the NOR gate is 1, and the load on all NAND gates is 1.

When the signal ab rises, the NAND gate output (if it transitions) can only fall. When the signal ab falls, the NAND gate output (if it transitions) can only rise. For the path a → ab → z0 (or z1 to z5), the delay is:

AND ↑	0.15 + 0.429	=	0.579 ns
NAND ↓	0.08 + 0.027	=	0.107 ns
			0.686 ns

AND ↓	0.18 + 0.209	=	0.389 ns
NAND ↑	0.05 + 0.035	=	0.085 ns
			0.474 ns

Since the NOR gate delay with load 1 will always be less than the AND gate delay with load 11, the worst case propagation delay is either:

a↑ → ab↑ → {z0...z5}↓

or

b↑ → ab↑ → {z0...z5}↓

at 0.686 nanoseconds.

b) Determine the equivalent size of the network.

AND		NOR		NAND	
6 * 1	+	1*1	+	1*2	= 9 equivalent gates

c) Determine the minimum sum of products expression for z0.

$$\begin{aligned} z_0 &= [(ab)(c+d)']' \\ &= [(ab)(c'd')]' \\ &= [abc'd']' \\ &= a' + b' + c + d \end{aligned}$$

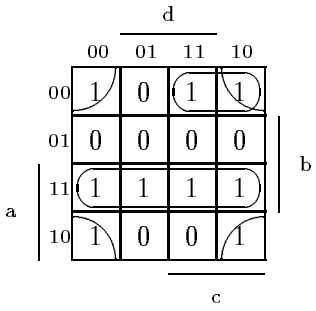
Problem 4. (5 points)

Find minimal sum of products and product of sums for the switching function specified as

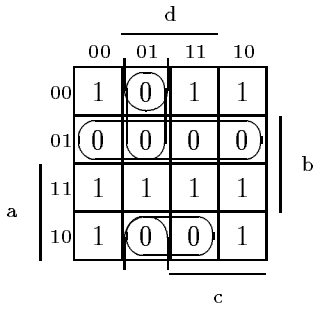
$E(a,b,c,d) = [(a'+b'+c')(b+d)]' + abc' + a'b'c$

Show all your work. Does the function have a unique minimal sum of products? A unique minimal product of sums?

Sum of Products:



Product of Sums:



Minimal sum of products:

$$\begin{aligned} E(a,b,c,d) &= [(a'+b'+c')(b+d)]' + abc' + a'b'c \\ &= (a'+b'+c')' + (b+d)' + abc' + a'b'c \\ &= abc + b'd' + abc' + a'b'c \\ &= (abc + abc') + b'd' + a'b'c \\ &= ab + b'd' + a'b'c \end{aligned}$$

The sum of products is unique.

Minimal product of sums:

$$\begin{aligned} E(a,b,c,d) &= (a+b')(a+c+d')(a'+b+d') \\ &\textit{or} \\ E(a,b,c,d) &= (a+b')(b+c+d')(a'+b+d') \end{aligned}$$

The product of sums is not unique.

Problem 5. (8 points)

Design a minimal NAND-NAND network to implement the following combinational system:

Input: $x, y \in \{0, 1, 2, 3\}$

Output: $z \in \{0, 1, 2, 3\}$

Function: $z = (3x - y + 3) mod 4$

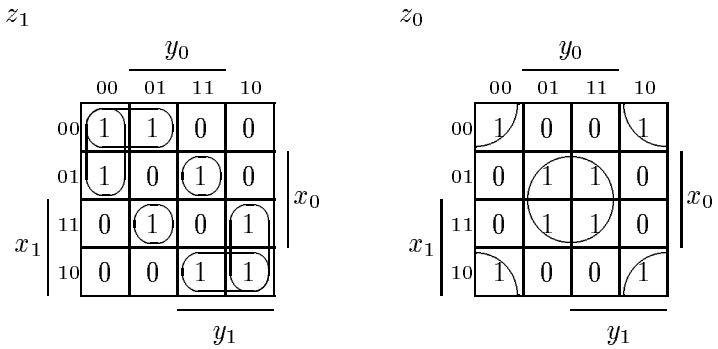
a) Show a table for z at the binary level.

x \ y	0	1	2	3
0	3	2	1	0
1	2	1	0	3
2	1	0	3	2
3	0	3	2	1

z

x_1	x_0	y_1	y_0	z_1	z_0
0	0	0	0	1	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	1

b) Derive minimal sums of products expressions for the outputs. Use the binary code to represent the inputs and the output. Show all your work.

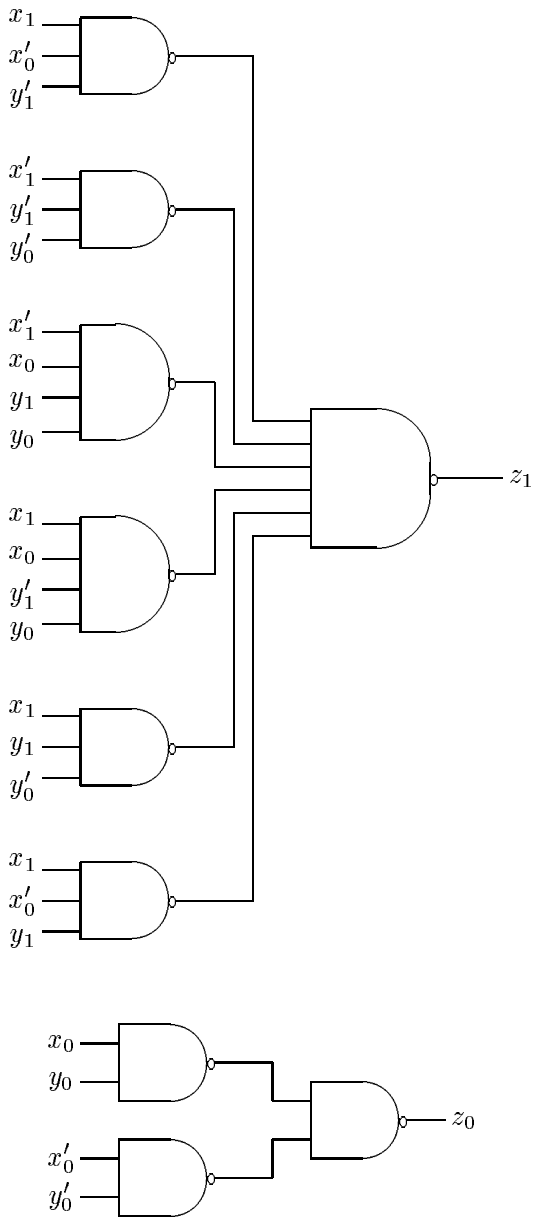


Minimal sum of products:

$$\begin{aligned} z_1 &= x_1'y_1'x_0' + x_1'y_1'y_0' \\ &\quad + x_1'x_0y_1y_0 + x_1x_0y_1'y_0 \\ &\quad x_1y_1x_0' + x_1y_1y_0' \end{aligned}$$

$$z_0 = x_0y_0 + x_0'y_0'$$

c) Show the corresponding NAND-NAND network.



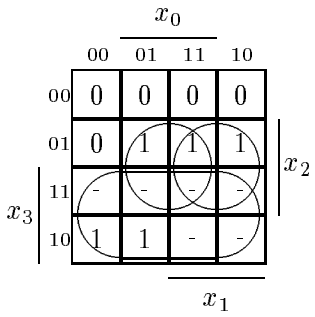
Problem 6. (8 points)

Design a network to convert $x = (x_3, x_2, x_1, x_0)$ in BCD code, i.e., $x \in \{0, ..., 9\}$ to $y = (y_3, y_2, y_1, y_0)$ in 2421 code shown in the following table.

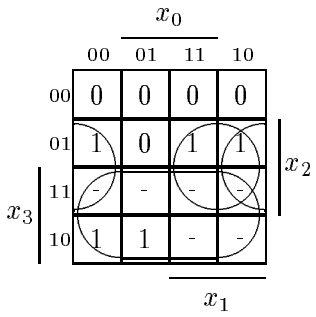
	BCD	2421
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	1011
6	0110	1100
7	0111	1101
8	1000	1110
9	1001	1111

a) Derive minimal sum of products expressions for the outputs. Note that $y_0 = x_0$. Show all your work

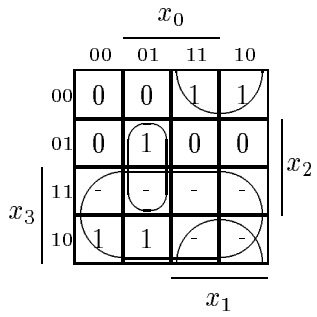
y_3



y_2



y_1



Minimal sum of products:

$$y_3 = x_3 + x_2x_1 + x_2x_0$$

$$y_2 = x_3 + x_2x_1 + x_2x_0'$$

$$y_1 = x_3 + x_2'x_1 + x_2x_1'x_0$$

$$y_0 = x_0$$

b) Implement your expressions from part a) by programming the PLA shown below.