| NAME | Type | OpCode | R1 | R2 | R3 | Shamt | Funct | Imm | 26-Bit | Description |
|------|------|--------|-----|-----|-----|-------|-------|-----|--------|-------------|
| add | R | 0 | R1 | R2 | RD | 0 | 32 | | | Addition |
| addi | I | 8 | RS | RD | | | | Imm | | AdditionImmediate |
| addu | R | 0 | R1 | R2 | RD | 0 | 33 | | | AdditionUnsigned(withoutoverflow) |
| addiu | I | 9 | RS | RD | | | | Imm | | AdditionImmediateUnsigned(withoutoverflow) |
| and | R | 0 | R1 | R2 | RD | 0 | 36 | | | AND |
| andi | I | 12 | RS | RD | | | | Imm | | ANDImmediate |
| beq | I | 4 | R1 | R2 | | | | Offset/4 | | BranchifEqual(ifR1=R2) |
| bgez | I2 | 1 | RS | 1 | | | | Offset/4 | | BranchifRSGreaterorEqualtoZero |
| bgezal | I2 | 1 | RS | 17 | | | | Offset/4 | | BranchandLinkifRSGreaterorEqualtoZero |
| bgtz | I2 | 7 | RS | 0 | | | | Offset/4 | | BranchifRSGreaterThanZero |
| blez | I2 | 6 | RS | 0 | | | | Offset/4 | | BranchifRSLessorEqualtoZero |
| bltz | I2 | 1 | RS | 0 | | | | Offset/4 | | BranchifRSLessThanZero |
| bltzal | I2 | 1 | RS | 16 | | | | Offset/4 | | BranchandLinkifRSLessThanZero |
| bne | I | 5 | R1 | R2 | | | | Offset/4 | | BranchifNotEqual(ifR1<>R2) |
| div | R6 | 0 | R1 | R2 | 0 | 0 | 26 | | | DivideR1/R2(HI-remainder,LO-quotient) |
| divu | R6 | 0 | R1 | R2 | 0 | 0 | 27 | | | DivideR1/R2Unsigned |
| j | J | 2 | | | | | | | Target | Jump |
| jal | J | 3 | | | | | | | Target | JumpAndLink |
| jalr | R5 | 0 | Addr | 0 | RD | 0 | 9 | | | JumpandLinkRegister |
| jr | R4 | 0 | Addr | 0 | 0 | 0 | 8 | | | JumpRegister |
| lb | I | 32 | Addr | RD | | | | Offset | | LoadByte |
| lbu | I | 36 | Addr | RD | | | | Offset | | LoadByteUnsigned |
| lh | I | 33 | Addr | RD | | | | Offset | | LoadHalfWord |
| lhu | I | 37 | Addr | RD | | | | Offset | | LoadHalfWordUnsigned |
| lui | I1 | 15 | 0 | RD | | | | Imm | | LoadUpperImmediate(Immediatex2^16) |
| lw | I | 35 | Addr | RD | | | | Offset | | LoadWord |
| lwl | I | 34 | Addr | RD | | | | Offset | | LoadWordLeft(4highbytesof8-byteword) |
| lwr | I | 38 | Addr | RD | | | | Offset | | LoadWordRight(4lowbytesof8-byteword) |
| mfhi | R1 | 0 | 0 | 0 | RD | 0 | 16 | | | MoveFromHI |
| mflo | R1 | 0 | 0 | 0 | RD | 0 | 18 | | | MoveFromLO |
| mthi | R4 | 0 | RS | 0 | 0 | 0 | 17 | | | MoveToHI |
| mtlo | R4 | 0 | RS | 0 | 0 | 0 | 19 | | | MoveToLO |
| mult | R6 | 0 | R1 | R2 | 0 | 0 | 24 | | | Multiply |
| multu | R6 | 0 | R1 | R2 | 0 | 0 | 25 | | | MultiplyUnsigned |
| nor | R | 0 | R1 | R2 | RD | 0 | 39 | | | NOR |
| or | R | 0 | R1 | R2 | RD | 0 | 37 | | | OR |
| ori | I | 13 | RS | RD | | | | Imm | | ORImmediate |
| sb | I | 40 | Addr | RS | | | | Offset | | StoreByte |
| sh | I | 41 | Addr | RS | | | | Offset | | StoreHalfWord |
| sll | R3 | 0 | - | RS | RD | SHAMT | 0 | | | ShiftLeftLogicalSHAMT |
| sllv | R | 0 | Shift | RS | RD | 0 | 4 | | | ShiftLeftLogicalVariable |
| slt | R | 0 | R1 | R2 | RD | 0 | 42 | | | SetifLessThan(RD=1ifR1<R2) |
| slti | I | 10 | RS | RD | | | | Imm | | SetifRSLessThanImmediate |
| sltiu | I | 11 | RS | RD | | | | Imm | | SetifRSLessThanImmediateUnsigned |
| sltu | R | 0 | R1 | R2 | RD | 0 | 43 | | | SetifLessThanUnsigned(RD=1ifR1<R2) |
| sra | R3 | 0 | - | RS | RD | SHAMT | 3 | | | ShiftRightArithmeticSHAMT |
| srav | R | 0 | Shift | RS | RD | 0 | 7 | | | ShiftRightArithmeticVariable |
| srl | R3 | 0 | - | RS | RD | SHAMT | 2 | | | ShiftRightLogicalSHAMT |
| srlv | R | 0 | Shift | RS | RD | 0 | 6 | | | ShiftRightLogicalVariable |
| sub | R | 0 | R1 | R2 | RD | 0 | 34 | | | SubtractR1-R2 |
| subu | R | 0 | R1 | R2 | RD | 0 | 35 | | | SubtractR1-R2Unsigned(withoutoverflow) |
| sw | I | 43 | Addr | RS | | | | Offset | | StoreWord |
| swl | I | 42 | Addr | RS | | | | Offset | | StoreWordLeft(4highbytesof8-byteword) |
| swr | I | 46 | Addr | RS | | | | Offset | | StoreWordRight(4lowbytesof8-byteword) |
| xor | R | 0 | R1 | R2 | RD | 0 | 38 | | | XOR |
| xori | I | 14 | RS | RD | | | | Imm | | XORImmediate |