LECTURE 11

LECTURE NOTES: FEBRUARY 12, 2003

OUTLINE

REVIEW

- Problem Solving Methods for Non-Ideal Operational Amplifier Circuits
- Problem Solving Methods for Ideal Operational Amplifier Circuits
- PSpice Simulation Methods for Operational Amplifier Circuits

DEFINITION

- We have been referring to our common reference potential as a "ground" potential. Here are some equivalent terms you may encounter that describe reference potentials:
- Common: The reference potential is common to all the node voltages, and is sometimes referred to as the common potential, or simply common.
- Ground: The earth is sometimes used as a reference potential for actual circuit systems. Thus, this most standard reference is referred to as Ground. It has become customary to refer to all reference potentials as ground potentials.
- Earth: Similar to ground, above.

OPERATIONAL AMPLIFIER CIRCUITS

- Inverting Current Amplifier for Photodiode Optical Communication Applications
  - Effective Input Resistance
  - Analytical Problem Solution
    - Ideal Operational Amplifier
    - Non-Ideal Operational Amplifier
  - PSpice Analysis
- High Gain Inverting Current Amplifier with Reduced Resistor Values
  - Design
  - PSpice Analysis
- Applications: Operational Voltage Adder
  - Analytical Problem Solution
    - Ideal Operational Amplifier
  - PSpice Analysis
- Applications: Differential Voltage Amplifier
  - Wireline Communication
  - Biomedical Instrumentation
  - Analytical Problem Solution
    - Ideal Operational Amplifier
    - Non-Ideal Operational Amplifier
    - PSpice Analysis
- Unity Gain Voltage Amplifier Application
  - Analytical Problem Solution
    - Ideal Operational Amplifier
    - Non-Ideal Operational Amplifier
  - Role of the Open Loop Input Resistance
  - Switching Inverting/NonInverting Amplifier Unity Gain Amplifier
    - PSpice Simulation
- The Operational Current Source
  - Analytical Problem Solution
    - Ideal Operational Amplifier
    - Non-Ideal Operational Amplifier
  - Output resistance – Thevenin equivalent

OPERATIONAL AMPLIFIER APPLICATION: PHOTODIODE DETECTORS FOR OPTICAL COMMUNICATION

- The combination of semiconductor diode laser and semiconductor photodiode detectors are essential components in fiber optic communication systems.

- The fiber optic communication system employs a high purity, glass optical fiber with a complex structure intended for guiding light waves over global distances.

- The figure below shows a semiconductor laser, photodiode detector and fiber system.

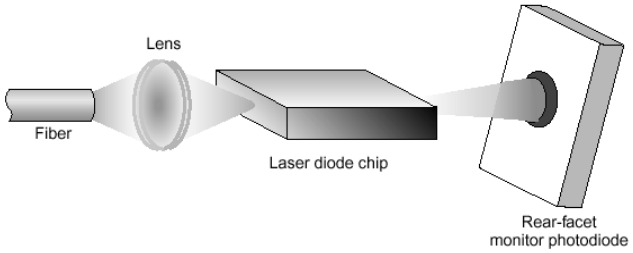

Figure 1. Fiber optic communication transmitter system with laser, photodiode laser power monitor, and fiber.

- Fiber optic elements are designed with core and cladding optical materials having differing indices of refraction. The discontinuity between cladding and core provides a lightwave guide, as shown below.

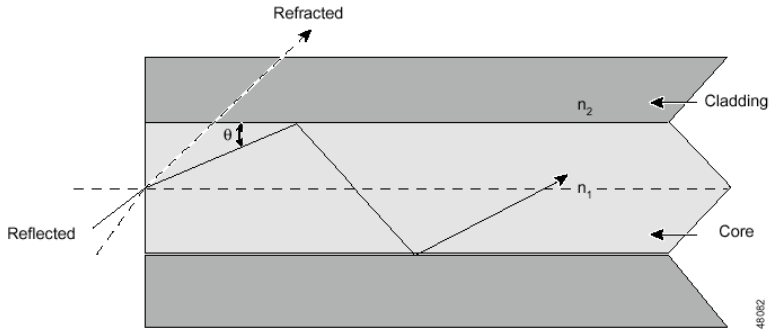

Figure 2. Fiber optic element cross-sectional view.

- Now, a fiber optic communication system is developed to inject many different optical signals, at differing wavelengths, into the fiber. Then, these waves propagate and exit at a receiver where the different signals, are separated and supplied to receivers. This method of wavelength division multiplexing (WDM) is shown below.

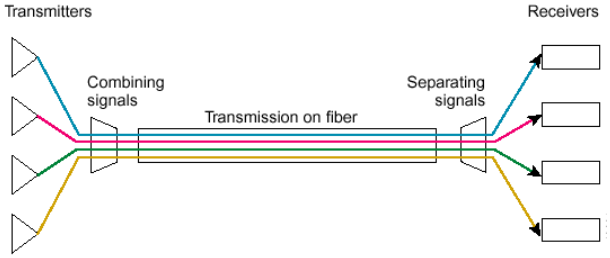

Figure 3. A fiber optic wavelength division (WDM) system

- Now, the optical signals at a receiver are captured by a photodiode detector.
- The photodiode captures photons within a semiconductor "diode" structure and creates electron-hole pairs. Two charges are liberated in the photodiode for each absorbed photon. Typical efficiencies lie in the range of 1 percent to 50 percent for the conversion of incoming photons to current-carrying charge. Typical current levels are 1 pA to 1 μA.
- Lets examine a photodiode circuit. The photodiode can be modeled as a time-dependent current source shunted by a "parasitic" impedance, Z_P. We will consider just a parasitic resistive shunt, R_P

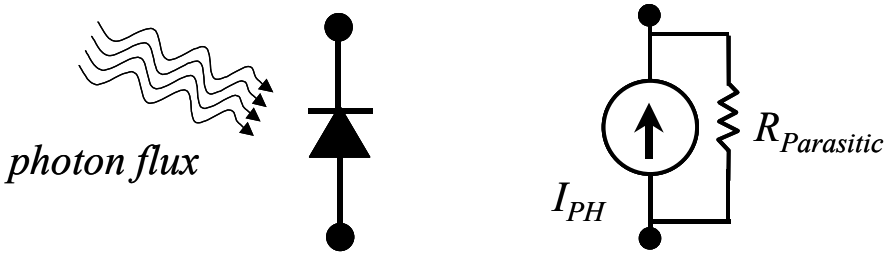

Figure 4. Semiconductor photodiode and its dc equivalent circuit consisting of a current source and a parallel parasistic resistance.

- Lets consider the output voltage of the photodiode system, shown above. We will consider the typical case where the photodiode current is 1 – 100nanoA.
- Now, the output voltage is just the product of the current and the parasitic resistance. Now, $R_{Parastic}$ may be a resistance of no greater than $10^5\Omega$. However, since the photon generated photodiode current is small, the voltage developed by this system is small, of the order of 0.1V – 10 mV for currents of 1 – 100nanoA.
- However, R_O is temperature dependent and variable in fabrication so that photodiode parasitic resistances vary and output voltages vary accordingly.
- Thus, we need a circuit that may measure the current from the photodiode and eliminated the effects of the parasitic resistance. This will be the Current to Voltage Amplifier.

INVERTING CURRENT TO VOLTAGE AMPLIFIER

- Lets consider the operational current amplifier.

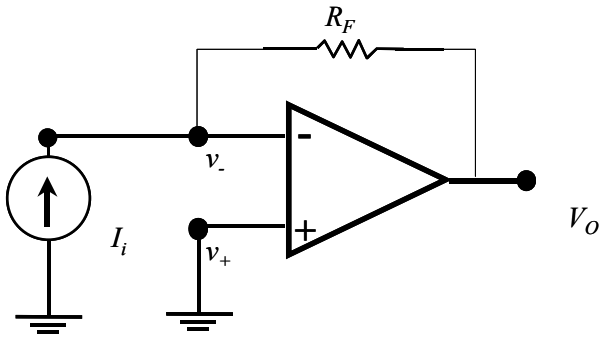

Figure 5. Inverting Current to Voltage Amplifier. Note that the feedback resistor and signal source are both connected to the Inverting Input.

- The inverting operational current amplifier is shown above.
- Now, lets consider a problem statement:

> *Compute the output voltage to input current ratio for an ideal operational amplifier*

- Lets use the ideal operational amplifier problem solving procedure.
- We will use the definitions that $v_+ = v_-$ and that the current into the input terminals is zero.
- Also, our procedure calls for us to note how the input terminals are connected within our circuit. We see that the non-inverting input is connected to the ground reference.
- Thus, the node voltage equation computed using KCL at the Inverting Input is:

$$I_i - \frac{v_- - V_O}{R_F} = 0$$

- But, $v_+ = v_-$ and the non-inverting input is directly coupled to the ground reference terminal. $v_+ = 0$. So, the node equation becomes:

$$I_i - \frac{-V_O}{R_F} = 0$$

- or

$$V_O = -I_i R_F$$

- Note the this is an inverting amplifier. Also, note that the input current is effectively multiplied by R_F.

- Now, this is the fundamental behavior, lets compute the effective Input Resistance for the case of a Non-Ideal Amplifier. Our problem statement will be:

- Compute the Input Resistance for the Inverting Current to Voltage Amplifier for a Non-Ideal Operational amplifier with finite open loop gain, A_V.

- So, following our *procedures*, we must redraw our circuit appropriately using the Non-Ideal model.

- This becomes:

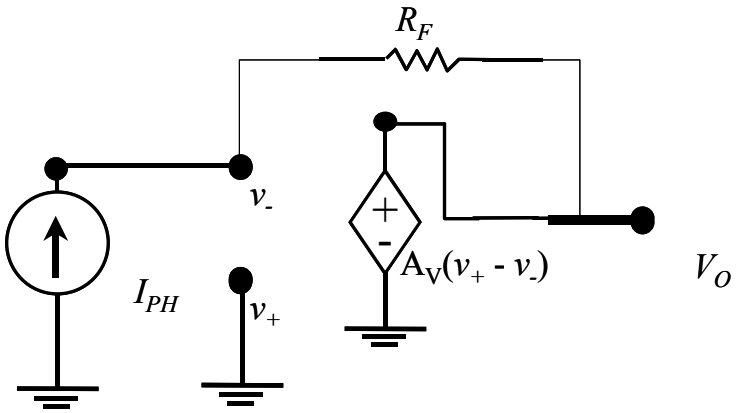

Figure 6. The Inverting Current to Voltage Amplifier using the Non-Ideal amplifier model with Open Loop Gain, A_V

- Carefully note the polarities of the Dependent Source! It matches the operational amplifier.

- Now, the node voltage equation remains as above:

$$I_i - \frac{v_- - V_O}{R_F} = 0$$

- But, the condition for the input terminal voltages becomes (according to our *procedures*)

$$V_O = A_V(v_+ - v_-)$$

- Also, recall that we always wish to examine closely to determine the connections at each terminal. We see that

$$v_+ = 0$$

- So, substituting these above two equations into the Node Voltage equation, we get

$$I_i - \frac{\left(-V_O / A_V\right) - V_O}{R_F} = 0$$

- or, manipulating

$$I_i = V_O \frac{\left(-1 / A_V\right) - 1}{R_F}$$

- and, we get the familiar form:

$$V_O = -I_i R_F \left(\frac{1}{1 + \frac{1}{A_F}} \right)$$

- Of course, in the limit of large gain, A_V, this equation for output voltage converges on that of the Ideal Operational Amplifier.

- Now, we wish to compute input resistance. This is simply the ratio of input voltage to input current. Input voltage is v_-. And, input current is I_i

- So, we return to the node voltage equation. But, now we make our substitutions to eliminate V_O and develop an equation in terms of I_i and v_-

$$I_i - \frac{v_- + A_V v_-}{R_F} = 0$$

- and, manipulating

$$I_i = v_- \frac{1 + A_V}{R_F}$$

- and the input resistance is

$$R_{Input} \equiv \frac{v_-}{I_i} = \frac{R_F}{1 + A_V}$$

- This is an important result, we can see that in the limit of large A_V, the input resistance at the Inverting Current Amplifier input is equal to the Feedback Resistance divided by the Open Loop Gain.

- Even for Feedback resistors of 10^7 with current to voltage gains of 10^7, with an open loop gain of 10^7, this yields an effective input resistance of only **1Ω**
- Negative Feedback has reduced input resistance (as desired) by a factor of 10^7
- Lets perform a PSpice analysis using the photodiode model with its parasitic resistance.
- This is shown below.

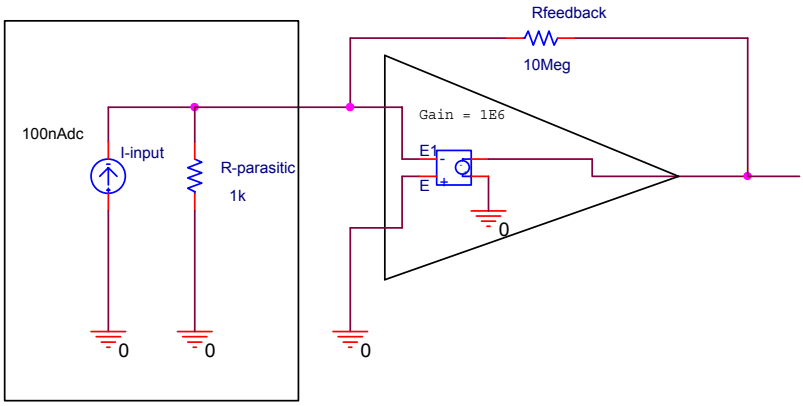

Figure 7. PSpice Schematic of the Inverting Current to Voltage Amplifier with an input system consisting of a 100nA current source in parallel with a parasitic resistance of 1kΩ. Note that the feedback resistor value is 10MΩ

- In PSpice, let us examine the system performance as a function of open loop gain. Let us also examine the effectiveness of this system in drawing current into the amplifier system and away from the parasitic resistance.
- This amplifier system has been essential for photodiode current measurement, for both avoiding the effects of input resistance on stealing current and the effects of input capacitance on reducing operating bandwidth.

HIGH GAIN INVERTING CURRENT AMPLIFIER WITH REDUCED RESISTOR VALUES

- Now, a drawback of the inverting current amplifier is the need to introduce very large resistance values in the feedback circuit, in order to achieve large gains.
- An improved circuit design is shown below.

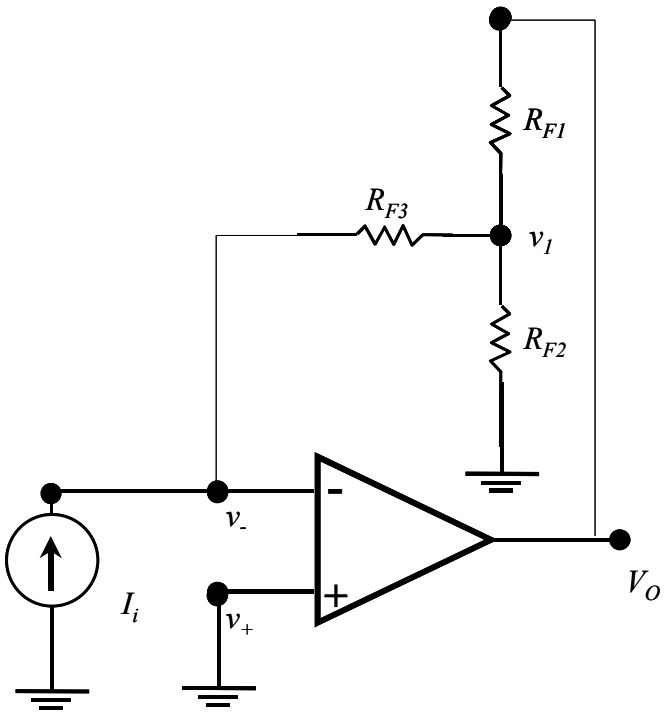

Figure 8. An improved Inverting Current to Voltage Amplifier. Note that the voltage divider system consisting of R_{F1} and R_{F2} reduce the output voltage before applying this to R_{F3}. We will find that we can achieve a gain equivalent to that of the Inverting Current Amplifier of the above circuit, with msall resistance values.

- Now, lets consider a problem statement:

> *Compute the output voltage to input current ratio for an ideal operational amplifier with the feedback network shown above..*

- Lets use the ideal operational amplifier problem solving procedure.
- We will use the definitions that $v_+ = v_-$ and that the current into the input terminals is zero.
- Also, our procedure calls for us to note how the input terminals are connected within our circuit. We see that the non-inverting input is connected to the ground reference.
- Thus, the node voltage equation computed using KCL at the Inverting Input is:

$$I_i - \frac{v_- - v_1}{R_{F3}} = 0$$

- And the node voltage equation computed using KCL at the node joining R_{F1} and R_{F2} is:

$$\frac{v_- - v_1}{R_{F3}} - \frac{v_1}{R_{F2}} + \frac{V_O - v_1}{R_{F1}} = 0$$

- But, $v_+ = v_-$ and the non-inverting input is directly coupled to the ground reference terminal. $v_+ = 0$. So, the node equations become:

$$I_i + \frac{v_1}{R_{F3}} = 0$$

- and

$$\frac{-v_1}{R_{F3}} - \frac{v_1}{R_{F2}} + \frac{V_O - v_1}{R_{F1}} = 0$$

- manipulating

$$-v_1\left(\frac{1}{R_{F3}} + \frac{1}{R_{F2}} + \frac{1}{R_{F1}}\right) + \frac{V_O}{R_{F1}} = 0$$

- and substituting for the v_1 in terms of I_i

$$I_i R_{F3}\left(\frac{1}{R_{F3}} + \frac{1}{R_{F2}} + \frac{1}{R_{F1}}\right) + \frac{V_O}{R_{F1}} = 0$$

- Finally,

$$\frac{V_O}{I_i} = -R_{F3}R_{F1}\left(\frac{1}{R_{F1}} + \frac{1}{R_{F2}} + \frac{1}{R_{F3}}\right)$$

- Note that with proper choices of resistors, the current to voltage gain may be much greater than R_{F3}.

- Now, consider limit where $R_{F3} >> R_{F2}$, and $R_{F3} >> R_{F1}$,

$$\frac{V_O}{I_i} \cong R_{F3}R_{F1}\left(\frac{1}{R_{F1}} + \frac{1}{R_{F2}}\right) = -R_{F3}\left(\frac{R_{F1} + R_{F2}}{R_{F2}}\right)$$

- We observe the voltage divider scale factor appearing here – why?

- This circuit provides a direct cost and performance benefit by reduced resistor size requirements by a factor of as large as 1000x

- Lets perform a PSpice simulation and examine directly the operation of this circuit.

OPERATIONAL VOLTAGE ADDER

- Frequent applications appear that require "mixing" of analog voltage or current signals. This may be required for precise control of combined audio signals, communication system signals, or signals within feedback control systems.

- We require a circuit that produces an output voltage that is equal to a weighted sum of input voltages.

- This is accomplished with operational amplifier circuits that may produce exact values for resistor voltage drops, thereby establishing exact currents and exact current weights.

- The Inverting Voltage Adder is shown below:

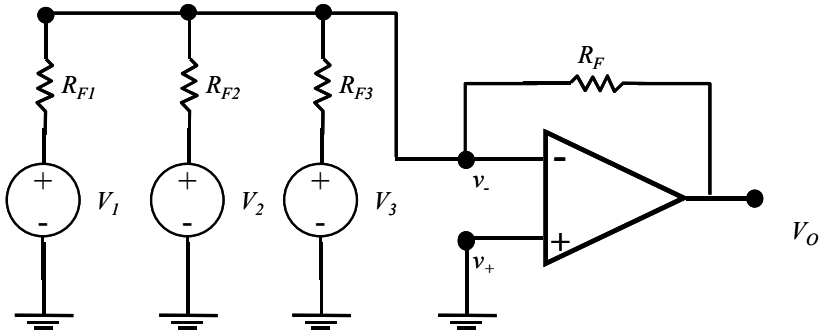

Figure 9. Inverting Voltage Adder

- Our problem statement will be:

> *Compute the output voltage in terms of the three input voltages for the voltage adder assuming an ideal operational amplifier.*

- Now, according to our procedure, we should proceed with Node Voltage analysis.

- We will write down the Node Voltage equation at one of the two Essential Nodes in our circuit (by the way, which are the essential nodes?)

- So, we have

$$\frac{V_1 - v_-}{R_{F1}} + \frac{V_2 - v_-}{R_{F2}} + \frac{V_3 - v_-}{R_{F3}} - \frac{v_- - V_O}{R_F} = 0$$

- But, we must use the rule that $v_- = v_+$
- Also, we must note that $v_+ = 0$.
- So, the Node Voltage equation becomes:

$$\frac{V_1}{R_{F1}} + \frac{V_2}{R_{F2}} + \frac{V_3}{R_{F3}} - \frac{-V_O}{R_F} = 0$$

- Or,

$$V_O = -\left(V_1\left(\frac{R_F}{R_{F1}}\right) + V_2\left(\frac{R_F}{R_{F2}}\right) + V_3\left(\frac{R_F}{R_{F3}}\right)\right)$$

- Note that the resistor ratios form weighting factors.
- In the event that $R_{F1} = R_{F2} = R_{F3} = R_F$ then, we have

$$V_O = -(V_1 + V_2 + V_3)$$

- Lets perform a PSpice analysis here and examine both voltage and current weighting.

INTRODUCING VOLTAGE SUPPLY SATURATION LIMITS FOR THE OPERATIONAL VOLTAGE ADDER

- Now, we must return to the topic of operational amplifier linear response. In particular, we must answer the question as to whether the amplifier output signal *computed assuming that the amplifier is ideal* is within the limits set by power supplies.

- Lets solve problem 5.10 as an example. This will be similar to problems you will encounter in homework.

- Here is our circuit:

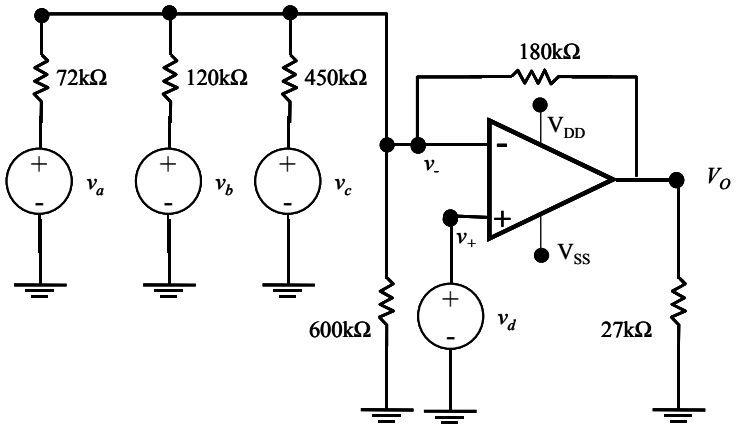

Figure 10 The circuit of Problem 5.10. Note that $V_{DD} = -V_{SS} = 16V$

- The problem statement is:

> *Find output voltage for* v_a = 18V, v_b = 6V, v_c = -15V, and v_d = 8V. Then, while all voltages other than v_c retain their values, specify the range of v_c such that the operational amplifier operates within its linear range.

- So, we will first assume *ideal* behavior and solve for output voltage.

- Lets review the procedures first:

1) Consider the problem statement and determine whether the problem requires a non-ideal or ideal operational amplifier.

2) If Ideal, we will follow this procedure

3) Then, draw the operational amplifier circuit according to the problem statement using the *simplified* operational amplifier symbol as in Figure 2, above.

4) Perform any available circuit simplifications with resistor equivalents.

5) Write down the Node Voltage equation using the Ground symbols as the common reference nodes. Note that *all Ground Symbols* ***are part of the same node***. As always, the Node Voltages are defined positive and defined relative to the Ground references.

6) Solve the Node Voltage equations.

7) If Ideal, then note that we will assume that

$$v_+ = v_-$$

8) Also, we set the current that flows into the Operational Amplifier at the Inverting and Non-Inverting inputs to zero.

9) Note very carefully the circuit components connected to the Non-Inverting (+) and Inverting (-) terminals.

10) Note very carefully how the *system* input voltage (V_i) or input current (I_i) is applied.

11) Solve for the requested values.

- First, before continuing, are there any components in this circuit that we may ignore? Why?
- Now, we again have two Essential Nodes. We should first identify these nodes.
- Lets write down the Node Voltage equation at the Inverting Input terminal:

$$\frac{v_a - v_-}{72} + \frac{v_b - v_-}{120} + \frac{v_c - v_-}{450} - \frac{v_-}{600} - \frac{v_- - V_O}{180} = 0$$

- Now, we know from our procedures that we should apply the equivalence of Inverting and Non-Inverting input terminals.
- Also, we review Step (10). We see that $v_+ = v_- = v_d$
- Thus, the Node Voltage equation becomes:

$$\frac{v_a - v_d}{72} + \frac{v_b - v_d}{120} + \frac{v_c - v_d}{450} - \frac{v_d}{600} - \frac{v_d - V_O}{180} = 0$$

- or,

$$V_o = -180\left(\frac{v_a - v_d}{72} + \frac{v_b - v_d}{120} + \frac{v_c - v_d}{450} - \frac{v_d}{600} - \frac{v_d}{180}\right)$$

- Now, we can just proceed to introduce the known values of the input voltages.

$$V_o = -180\left(\frac{10}{72} - \frac{2}{120} - \frac{23}{450} - \frac{8}{600} - \frac{8}{180}\right) = -2.4V$$

- We must know *compare* the output voltage with our supply bias values.
- Specifically, the operational amplifier circuit behaves in a linear fashion with

$$v_O = \mathrm{A_V}\,(\,v_+ - v_-\,)$$

  - But, if the output signal approaches one of the supply bias values, the output will "saturate" (remain fixed at and not exceed) this value.
  - Specifically, for

$$\mathrm{A_V}\,(\,v_+ - v_-\,) \;\le\; \mathrm{V_{SS}},\ \text{then } v_O \approx \mathrm{V_{SS}}$$

$$\mathrm{A_V}\,(\,v_+ - v_-\,) \;\ge\; \mathrm{V_{DD}},\ \text{then } v_O \approx \mathrm{V_{DD}}$$

- Now, lets compute the dependence of the output voltage on v_C with the other input signals fixed at their given values.

$$V_o = -180\left(\frac{10}{72} - \frac{2}{120} + \frac{v_c - 8}{450} - \frac{8}{600} - \frac{8}{180}\right) = -8.4 - 0.4v_c$$

- Now, to determine the maximum value of the input signal that allows linear operation, we may set this output equal to $\mathrm{V_{DD}}$, the maximum output excursion.

$$V_{Max} = -8.4 - 0.4v_c = 16V$$

- and the minimum output voltage is $\mathrm{V_{SS}}$. So, the minimum output excursion is:

$$V_{Min} = -8.4 - 0.4v_c = -16V$$

- Solving for v_C, we find that:

$$-61\mathrm{V} \le v_c \le 19\mathrm{V}$$

- Let us proceed to verify this with PSpice analysis

PSPICE IDEAL OPERATIONAL AMPLIFIER

- There is a convenient PSpice Ideal Operational Amplifier in the Analog Library of the Parts Menu.

- To access this, navigate to the Parts menu and select the Ideal OPAMP, as shown below:

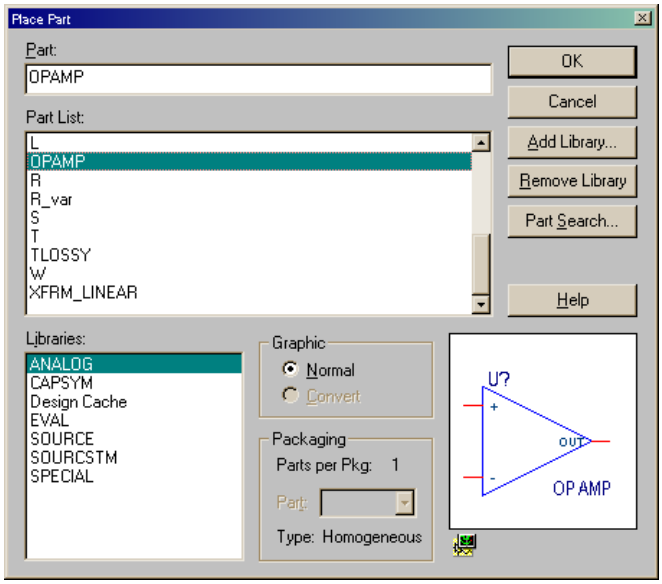

Figure 11. The Ideal OPAMP

- Now, place this part using care regarding the connectivity to the Inverting and Non-Inverting terminals ! You may "flip" the part by navigating to the Edit menu and selecting Mirror > Vertical

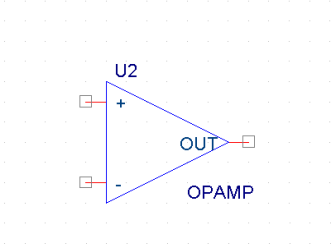

Figure 12. The Ideal OPAMP

- *Now, it is very important that this part contain the proper properties to match your problem.*

- These properties are set by the Property Editor. To reach this, double-click on the OPAMP and then view the Property Editor dialog box, shown below.

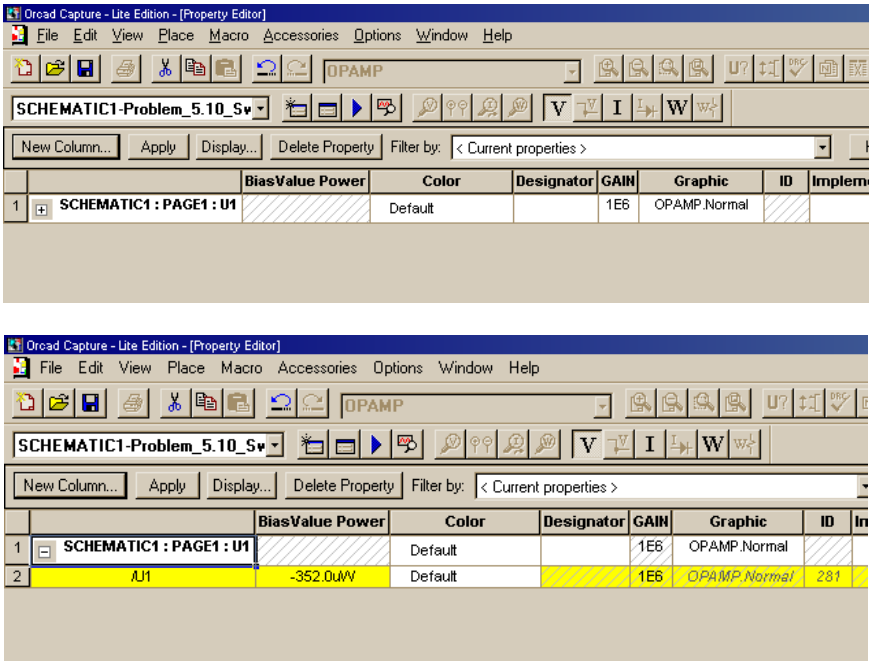

Figure 13. Two views of the Property Editor. IMPORTANT: when adjusting a parameter, collapse the two rows into one, as for the upper panel, by clicking on the +/- box just to the left of the word Schematic in the first row. Make chances in the collapsed row. This view focuses on the Gain column, which you can see is set to 1E6.

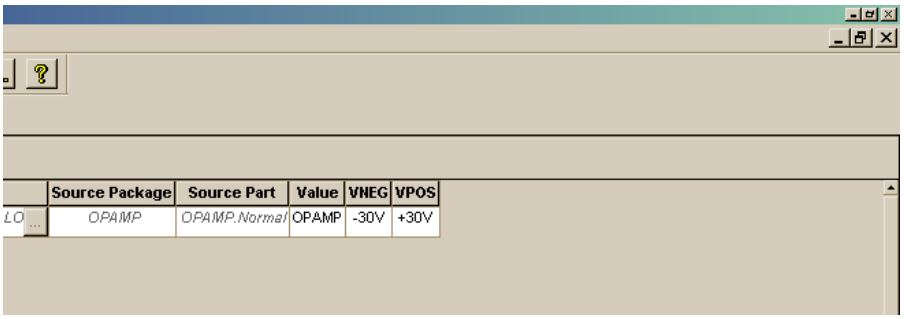

Figure 14. A view of the Property Editor with a focus on the V_{DD} and V_{SS} values. These are shown as VNEG and VPOS

- The critical properties to adjust are, Gain, VNEG (we define as V_{SS}), and VPOS (we define as V_{DD}).

- Procedures for setting these parameters are seen in the Figures above.

VOLTAGE SUPPLY SATURATION LIMITS FOR THE OPERATIONAL VOLTAGE ADDER: PROBLEM 5.10 PSPICE SIMULATION

- In EE10, we will be able to solve circuit problems using PSpice with the standard Bias Point analysis. However to illustrate an important capability, lets examine the DC Sweep method.
- We may automatically "sweep" a voltage or current signal and test the output voltage values for this circuit.
- Lets proceed, using the DC Sweep analysis method – selected from the PSpice menu:

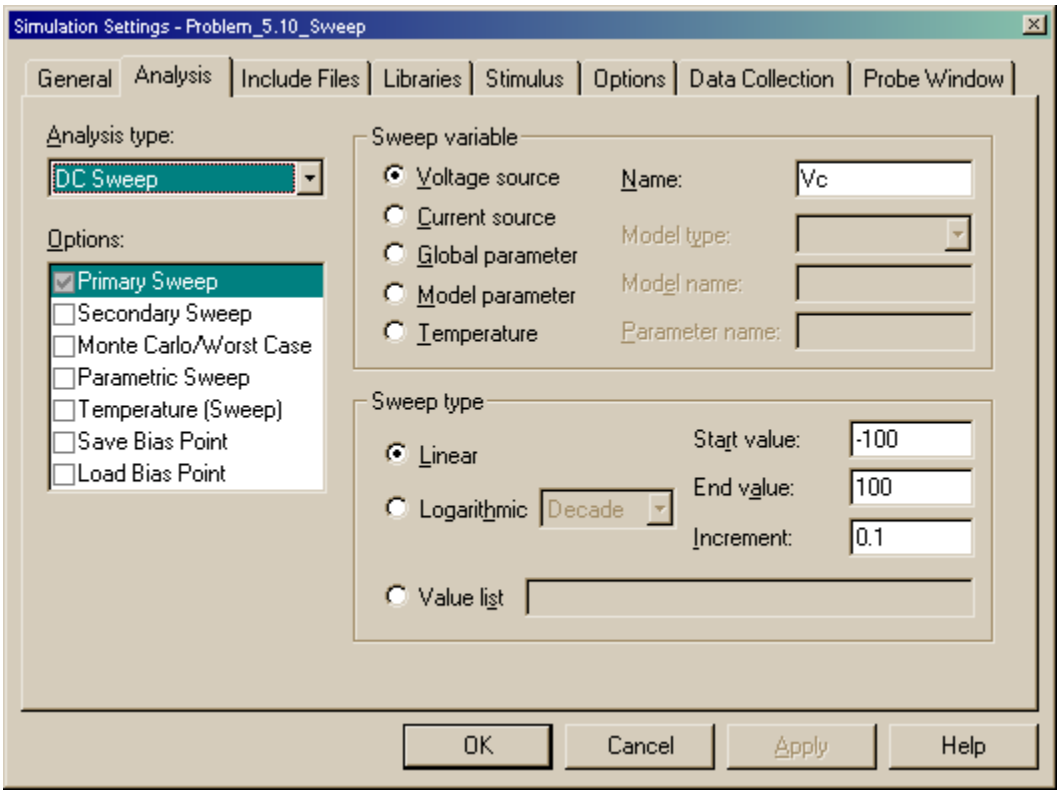

Figure 15. The DC Sweep Analysis method. Here, the voltage Vc of Problem 5.10 is being swept from -100 to 100V in 0.1V steps.

- Here is an example voltage sweep, below. The Operational Amplifier output is plotted on the vertical axis with the swept value, Vc, on the horizontal axis.
- Here we have two data sets. One corresponds to the case where the supply voltages for the Operational Amplifier are fixed at $V_{DD} = -V_{SS} = 30V$, and the other for $V_{DD} = -V_{SS} = 16V$. We can observe the saturation behavior here. Note that the linear operating region may be observed with $-61V \leq v_c \leq 19V$.

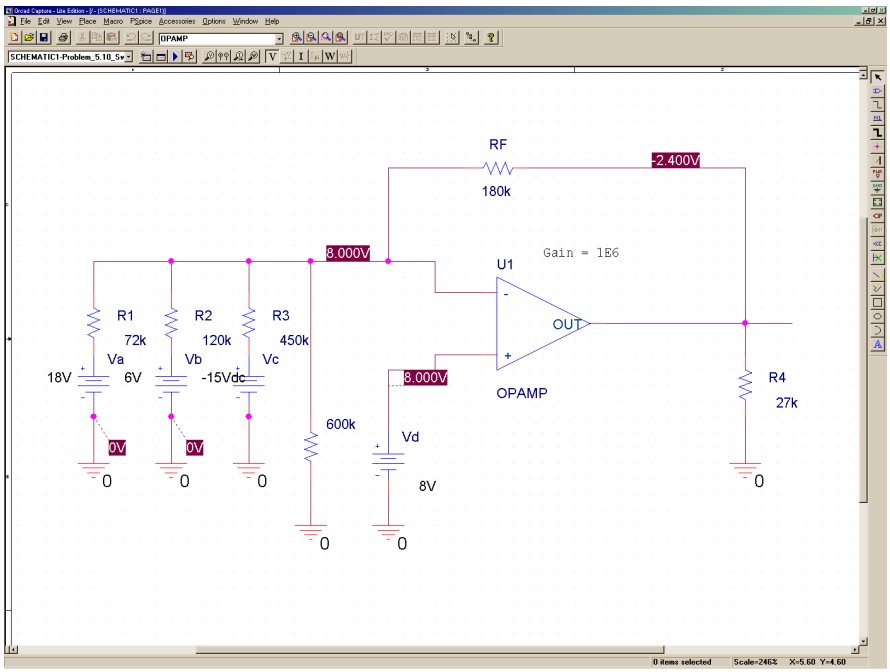

Figure 16. Schematic for Problem 5.10 using standard Bias Point analysis to obtain the voltages shown here.

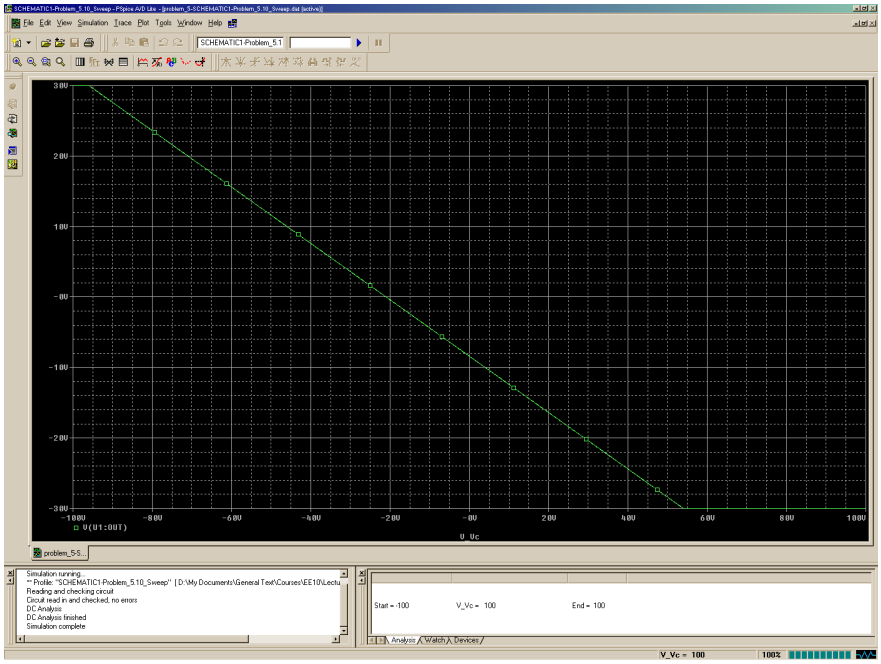

Figure 17. DC Sweep Analysis with $V_{DD} = -V_{SS} = 16V$

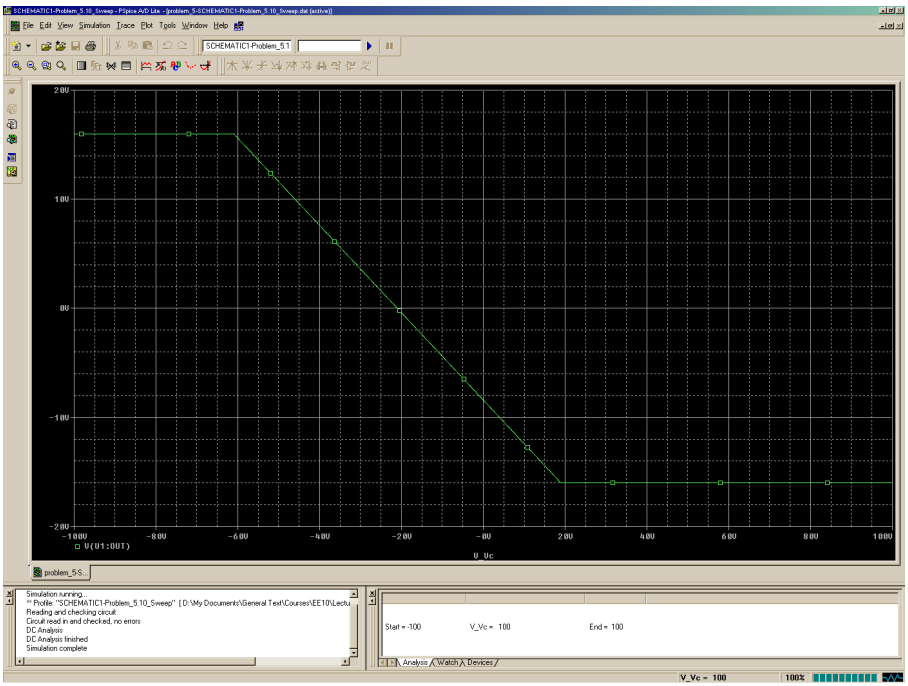

Figure 18. DC Sweep Analysis with $V_{DD} = -V_{SS} = 30V$