Chapter 8

Exercise 8.18

The expressions for the flip-flop inputs are

$$\begin{aligned} T_A &= Q_A + Q'_B \\ T_B &= Q_A + Q_B \end{aligned}$$

The flip-flops change state in every clock pulse depending only on the previous state. The transition table is

PS	FF inputs		NS
$Q_A(t)Q_B(t)$	$T_A(t)$	$T_B(t)$	$Q_A(t+1)Q_B(t+1)$
00	1	0	10
01	0	1	00
10	1	1	01
11	1	1	00

Let us define the following encoding:

Q_AQ_B	
00	S_0
01	S_2
10	S_1
11	S_3

The resulting state table is

PS	NS
S_0	S_1
S_1	S_2
S_2	S_0
S_3	S_0

The state diagram is presented in Figure **??**. It is an autonomous modulo-3 counter.

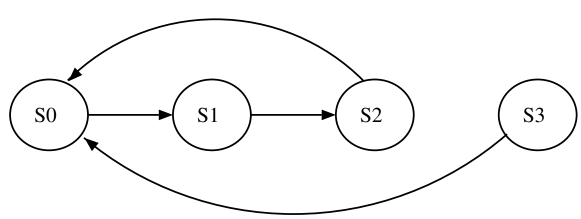

Figure 8.1: State diagram for Exercise 8.18

Exercise 8.20
The expressions for the flip-flop inputs are:

$$\begin{aligned} T_A &= Q_A + Q_B \\ T_B &= Q_A' + Q_B \end{aligned}$$

The transition table is

PS	FF inputs	NS
$Q_A(t)Q_B(t)$	$T_A(t)T_B(t)$	$Q_A(t+1)Q_B(t+1)$
00	01	01
01	11	10
10	10	00
11	11	00

Let us define the following encoding:

Q_AQ_B	
00	S_0
01	S_1
10	S_2
11	S_3

The resulting state table is

PS	NS
S_0	S_1
S_1	S_2
S_2	S_0
S_3	S_0

The state diagram is shown in Figure **??**. The network implements an autonomous modulo-3 counter.

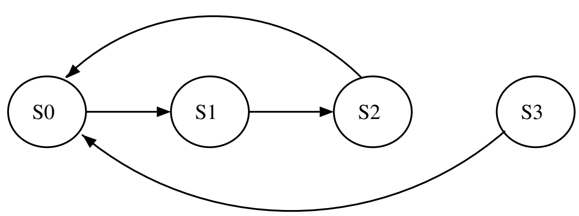

Figure 8.2: State diagram for Exercise 8.20

Exercise 8.24

Since the output at time t depends on the inputs at time $t-3, t-2, t-1$, it is necessary to store these in the state register. That is, the register consists of three flip-flops such that

$$\begin{aligned} Q_2(t) &= x(t-3) \\ Q_1(t) &= x(t-2) \\ Q_0(t) &= x(t-1) \end{aligned}$$

Consequently, the state description is

$$\begin{aligned} Q_2(t+1) &= Q_1(t) \\ Q_1(t+1) &= Q_0(t) \\ Q_0(t) &= x(t) \\ z &= x(t-3) \oplus x(t-2) \oplus x(t-1) \oplus x(t) = Q_2 \oplus Q_1 \oplus Q_0 \oplus x \end{aligned}$$

If we use D flip-flops, we get

$$\begin{aligned} D_2 &= Q_1 \\ D_1 &= Q_0 \\ D_0 &= x \end{aligned}$$

The sequential network is shown in Figure **??**.

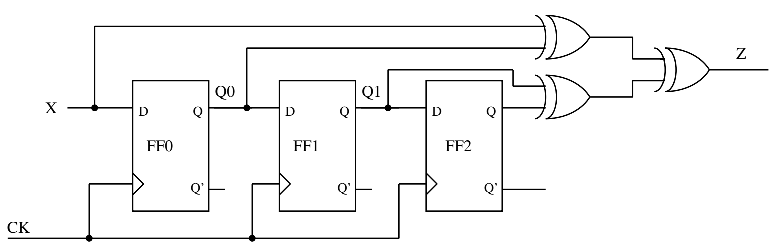

Figure 8.3: Network for Exercise 8.24

Exercise 8.26
The state corresponds to the count. That is,

$$s(t+1) = (s(t)+1) \bmod 3$$

Using a radix-2 representation for the count we get the following state table

PS	Input	
Q_2Q_1	$x=0$	$x=1$
00	00	01
01	01	10
10	10	00
	NS	

Since the excitation function of a SR flip-flop is

PS	NS	
	0	1
0	0-	10
1	01	-0
	SR	

we get the following switching expressions

$$S_2 = xQ_1 \qquad S_1 = xQ_2'Q_1'$$

$$R_2 = xQ_2 \qquad R_1 = xQ_1$$

The output is obtained directly from the state register. The sequential network is shown in Figure **??**.

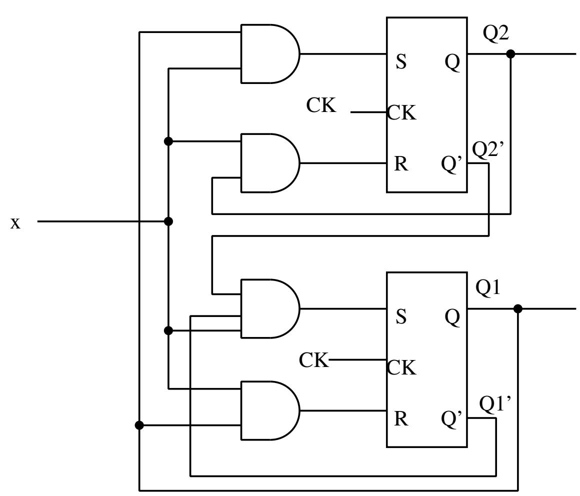

Figure 8.4: Network for Exercise 8.26

Exercise 8.32 Modulo-3 binary counter using "one flip-flop per state" approach.
The counter has 3 states $S \in \{0, 1, 2\}$, thus 3 flip-flops are required. The state codes are:

$y_2y_1y_0$	State
0 0 1	0
0 1 0	1
1 0 0	2

The counter changes state when the input $x = 1$. The state diagram for the counter is shown in Figure **??**. The switching expressions for the network can be obtained by inspection of the state diagram:

$$\begin{aligned}
Y_2 &= S_1x + S_2x' = y_1x + y_2x' \\
Y_1 &= y_0x + y_1x' \\
Y_0 &= y_2x + y_0x' \\
z_1 &= y_2 \\
z_0 &= y_1
\end{aligned}$$

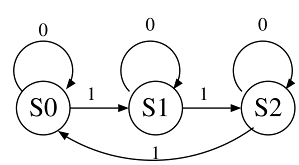

Figure 8.5: State Diagram for a Modulo-3 Counter

The corresponding network is shown in Figure **??**.

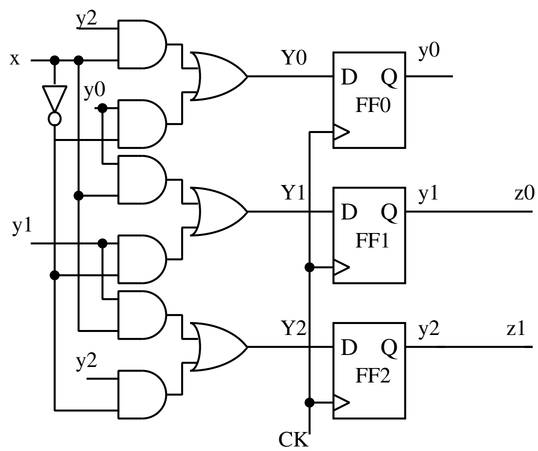

Figure 8.6: Modulo-3 counter - Exercise 8.32