Chapter 6

Exercise 6.8 The *complementer* is described by the expressions:

$$z_i = x_i \oplus c$$

The network that implements a 4-bit complementer using only XOR gates is presented in Figure **??**, on page **??**.

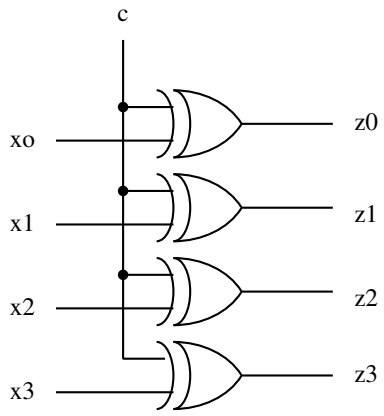

Figure 6.1: Complementer using XOR gates

Exercise 6.10 From the network in Figure 6.13 we can obtain the following expressions for the selection signal s (which controls the rightmost multiplexers), and the output signals z_1 and z_2:

$$\begin{aligned}
s &= ab + a'b' = (a \oplus b)' \\
z_1 &= cs + c's' \\
&= c \oplus s' \\
&= a \oplus b \oplus c \\
z_2 &= bs + cs' \\
&= b(ab + a'b') + c(ab' + a'b) \\
&= ab + ab'c + a'bc \\
&= a(b + b'c) + b(a + a'c) \\
&= a(b + c) + b(a + c) \\
&= ab + ac + bc
\end{aligned}$$

From the boolean expressions we can see that $z_1 = a \oplus b \oplus c$ corresponds to the high-level description:

$$z_1 = (a + b + c) \bmod 2$$

and $z_2 = 1$ when 2 or more inputs have the value 1. These equations correspond to sum and carry-out outputs of a one-bit adder, with inputs a, b, and c.