Chapter 5

(a) the K-map for $E(x,y,z)=\sum m(1,5,7)$ is:

		2	<u> </u>	
	0	1	0	0
x	0	1	1	0
		•		 /

(b)
$$E(w, x, y, z) = w'x'y + y'z + xz'$$

	Z						
	0	1	1	1			
	1	1	0	1	•		
117	1	1	0	1	X		
W	0	1	0	0	•		
				7	•		

(a)
$$E(w, x, y, z) = \prod M(1, 3, 4, 7, 10, 13, 14, 15) = \sum m(0, 2, 5, 6, 8, 9, 11, 12)$$

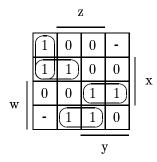
	Z					
•	1)	0	0	\bigcirc		
	0	(1)	0	1		
117	1	0	0	0	X	
W	1	$\boxed{1}$	1)	0		
				7		

minimal sum of products: wy'z' + wx'z + w'x'z' + w'yz' + w'xy'z

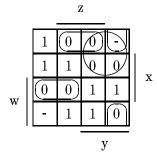
	,	3	ζ		
	1	0	0)	1	
	\bigcirc	1	\bigcirc	1	$\ _{\mathbf{w}}$
\mathbf{z}	1	0	0	\bigcirc	*`
2	1	1	1	0	
		•	7	7	•

minimal product of sums: (w+x+z')(w'+y'+z)(x'+y'+z')(w'+x'+z')(w+x'+y+z)

(b)
$$E(w,x,y,z) = \sum m(0,4,5,9,11,14,15), dc(w,x,y,z) = \sum m(2,8)$$



minimal SP: w'y'z' + w'y'x + wx'z + wxy



minimal PS:
$$(w+x+z')(w+y')(x+y'+z)(w'+x'+y)$$

(c) $E(x,y,z) = \sum m(0,1,4,6) = \prod M(2,3,5,7)$

		2	1	
	$\boxed{1}$	1)	0	0
X	1)	0	0	$\boxed{1}$
		•		7

minimal sum of products: x'y' + xz'

			9	
	1	1	$ \circ $	0
x	1	\bigcirc	0	1
			У	7

minimal product of sums: (x + y')(x' + z')

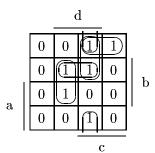
Input: (a, b, c, d), with $a, b, c, d \in \{0, 1\}$

Output: $y \in \{0, 1\}$

Function:

$$y = \begin{cases} 1 & \text{if } (8a + 4b + 2c + d) \text{ is prime} \\ 0 & \text{otherwise} \end{cases}$$

input value	abcd	у
0	0000	0
1	0001	0
2	0010	1
3	0011	1
4	0100	0
5	0101	1
6	0110	0
7	0111	1
8	1000	0
9	1001	0
10	1010	0
11	1011	1
12	1100	0
13	1101	1
14	1110	0
15	1111	0



From the Kmap we get the following prime implicants: a'bd, b'cd, a'b'c, a'cd, and bc'd. The essential prime implicants are: b'cd, a'b'c, and bc'd. A minimal sum of products for function y is:

$$y = b'cd + a'b'c + bc'd + a'cd$$

and the gate network that implements this expression is shown in Figure ??.

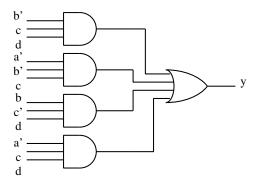
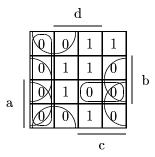


Figure 5.1: AND-OR gate network for "prime detector" (Exercise 5.8)



From the Kmap we get the following prime implicates: (b'+d), (a'+d), (b+c), (c+d) and (a'+b'+c'). Only the (c+d) prime implicate is not essential. So, the minimal product of sums in this case is:

$$y = (b' + d)(a' + d)(b + c)(a' + b' + c')$$

and the gate network that implements this expression is shown in Figure ??. Notice that the cost of the product of sums is lower.

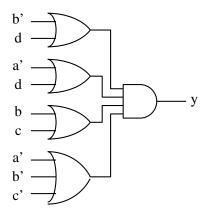


Figure 5.2: OR-AND gate network for "prime detector" (Exercise 5.8)

The multiplier is specified as follows:

Inputs: x, y where $x, y \in \{0, 1, 2, 3\}$

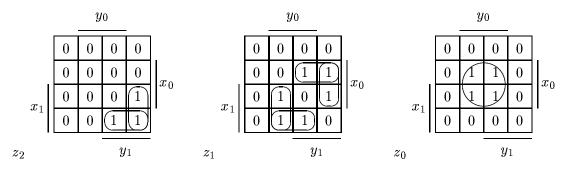
Output: $z \in \{0, 1, 2, 3, 4, 6, 9\}$

Function: $z = x \cdot y$

Coding the inputs and outputs in a binary code, produces the switching function of the following table:

2	X	7	y		2	Z	
x_1	x_0	y_1	y_0	z_3	z_2	z_1	z_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

From the table we get the following K-maps and expressions for the multiplier binary outputs:



 $z_0 = x_0 y_0$

 $z_1 = x_1 x_0' y_0 + x_0 y_1 y_0' + x_1' x_0 y_1 + x_1 y_1' y_0$

 $z_2 = x_1 x_0' y_1 + x_1 y_1 y_0'$

Output z_3 corresponds to only one minterm (no Kmap is needed in this case):

 $z_3 = x_1 x_0 y_1 y_0$

The NAND-NAND network is obtained directly from the sum of products. The correspoding network is presented in Figure ??.

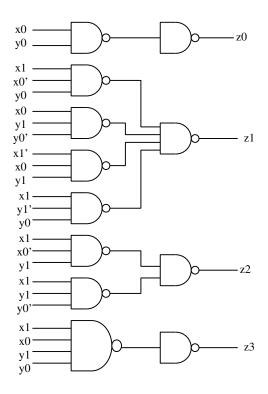


Figure 5.3: Network for a 2x2 bit multiplier. Exercise 5.14

Exercise 5.18 A high-level specification for the system is:

Input: x is a decimal digit, represented in BCD

Output: y is an unsigned integer represented in binary

Function: $y = x^2$

The switching functions for this exercise are given as:

x (BCD)	$y = x^2$ (Binary)
0000	0000000
0001	0000001
0010	0000100
0011	0001001
0100	0010000
0101	0011001
0110	0100100
0111	0110001
1000	1000000
1001	1010001

Using K-maps we obtain:

$$y_0 = x_0$$

$$y_1 = 0$$

$$y_2 = x_1 x_2'$$

$$y_{3} = x'_{2}x_{1}x_{0} + x_{2}x'_{1}x_{0}$$

$$y_{4} = x_{2}x'_{1} + x_{2}x_{0}$$

$$y_{5} = x_{2}x_{1}$$

$$y_{6} = x_{3}$$

The PLA implementation of this system is shown in figure ??.

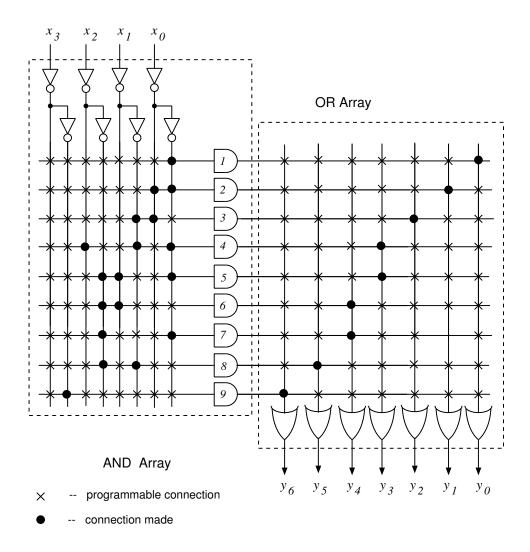


Figure 5.4: PLA implementation for Exercise 5.18