

EW-2 Project-2

ANALOG SPIKE DETECTOR

Aanchal Amit Mundhada

aanchal.mundhada@research.iiit.ac.in

Roll No: 2023112016

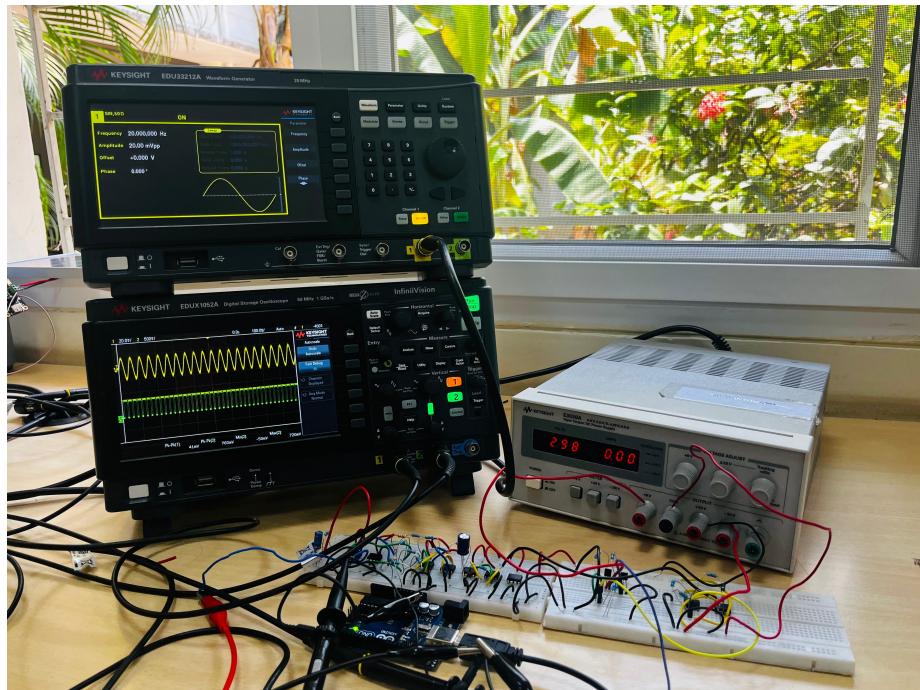
Shaikh Haris Jamal

shaikh.jamal@research.iiit.ac.in

Roll No: 2023112007

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Table no. 7



1 Introduction

Analog spike detection plays a vital role in neural and biomedical signal processing, where the goal is to capture rapid, transient voltage changes from low-amplitude signals. This project focuses on designing a real-time analog spike detector capable of isolating such events with high sensitivity and minimal latency.

The circuit operates on a dual $\pm 12V$ power supply, providing a wide dynamic range suitable for processing millivolt-level input signals commonly found in neural and ECG applications. Its fully analog design offers straightforward adjustability—users can tune the band-pass filter's cutoff frequencies to target specific signal ranges and modify the comparator threshold to detect spikes of varying magnitudes and slopes. This flexibility allows the circuit to adapt easily to different signal conditions without requiring any digital components.

The project is composed of the following functional stages:

- **Instrumentation Amplifier Stage:** Amplifies weak differential input signals while rejecting common-mode noise.
- **Band-Pass Filter Stage:** Isolates spike-frequency components by removing both low-frequency drifts and high-frequency noise.
- **Full-Wave Rectifier Stage:** Converts the filtered AC signal into a unipolar waveform to simplify threshold comparison.
- **Comparator Stage:** Generates digital-like output pulses whenever the signal exceeds a user-defined voltage threshold, effectively marking spike events.

This modular and adjustable architecture ensures the circuit can be easily adapted to detect spikes with different durations, frequencies, and amplitudes—purely through analog tuning.

We have taken sine input of 20mV at 20Hz and the arduino input for random spikes. For LTSpice, we took inputs of sine wave of 20mV at 20Hz and a random spike input with peaks 10mV, 4.8mV, -20mV, 15mV, -3mV.

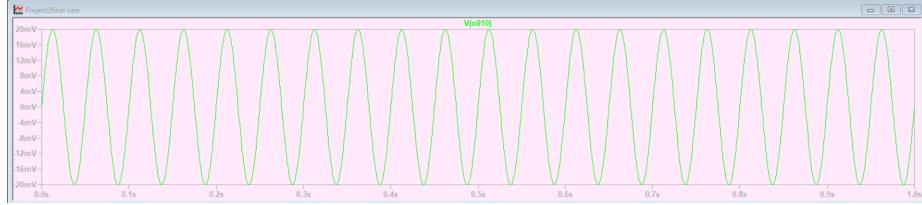


Figure 1: LTSpice input for sine wave of 20mV at 20Hz

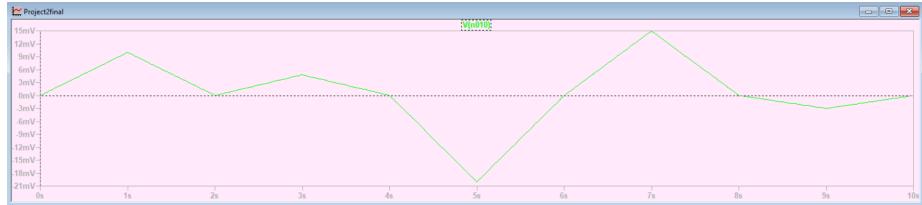


Figure 2: LTSpice input for random spikes with peaks 10mV, 4.8mV, -20mV, 15mV, -3mV

2 Instrumentation Amplifier Stage

For the initial amplification stage, a three-op-amp instrumentation amplifier configuration was employed, as shown in Figure 3.

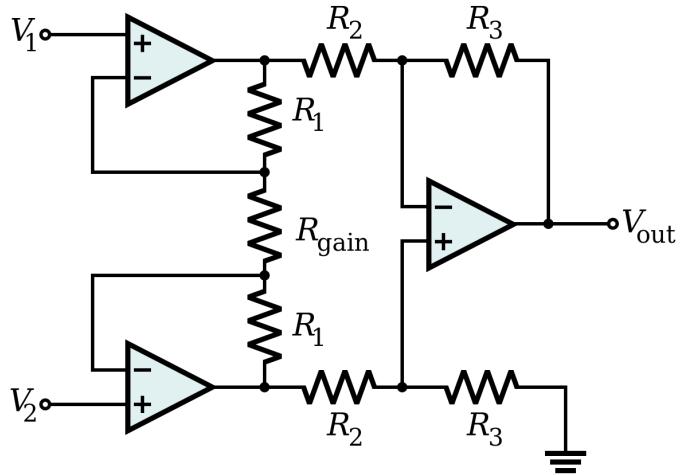


Figure 3: Three-Op-Amp Instrumentation Amplifier

An instrumentation amplifier is a specialized differential amplifier optimized for precise, low-noise signal amplification. It offers high input impedance, low output impedance, and excellent common-mode rejection, making it ideal for measuring low-level signals in noisy environments such as ECG signals.

The amplifier consists of two stages:

2.1 Stage 1: Gain Stage (Buffered Differential Amplifier)

The first stage uses two non-inverting op-amp buffers connected via a resistor network. The voltage gain of this stage is adjustable using an external resistor R_{gain} , and the outputs of the two op-amps are connected across it.

Applying Ohm's Law and the principle of virtual short:

$$\frac{V_1 - V_X}{R_1} = \frac{V_X - V_Y}{R_{\text{gain}}} \quad \text{and} \quad \frac{V_2 - V_Y}{R_1} = \frac{V_Y - V_X}{R_{\text{gain}}}$$

Adding these equations gives:

$$V_1 + V_2 = V_X + V_Y \quad \Rightarrow \quad V_X - V_Y = \left(1 + \frac{2R_1}{R_{\text{gain}}}\right) (V_1 - V_2)$$

2.2 Stage 2: Differential Amplifier

The second stage is a classic differential amplifier formed by matched resistor pairs R_2 and R_3 , which provides common-mode rejection:

$$V_o = \left(\frac{R_3}{R_2} \right) (V_X - V_Y)$$

Substituting the expression for $V_X - V_Y$ from Stage 1:

$$V_o = \left(\frac{R_3}{R_2} \right) \left(1 + \frac{2R_1}{R_{\text{gain}}} \right) (V_1 - V_2)$$

Final Gain Expression:

$$V_o = (V_1 - V_2) \left(1 + \frac{2R_1}{R_{\text{gain}}} \right) \left(\frac{R_3}{R_2} \right) \quad (1)$$

2.3 Component-Level Gain Calculation

The total gain can be viewed as the product of two stages:

$$A_{\text{stage1}} = 1 + \frac{2R_1}{R_{\text{gain}}}, \quad A_{\text{stage2}} = \frac{R_3}{R_2} \quad (2)$$

$$A_v = A_{\text{stage1}} \cdot A_{\text{stage2}} \quad (3)$$

Substituting the given values:

$$R_1 = 25 \text{ k}\Omega, \quad R_{\text{gain}} = 100 \Omega, \quad R_2 = R_3 = 10 \text{ k}\Omega$$

$$A_{\text{stage1}} = 1 + \frac{2 \cdot 25,000}{100} = 501, \quad A_{\text{stage2}} = \frac{10,000}{10,000} = 1$$

$$\therefore A_v = 501 \cdot 1 = \boxed{501}$$

2.4 Output Voltage Expression

Let the differential input be:

$$V_{\text{diff}} = V_1 - V_2$$

Then, the output voltage is:

$$V_o = A_v \cdot V_{\text{diff}} = 501(V_1 - V_2) \quad (4)$$

Note that due to the final differential amplifier stage, the output may be inverted depending on the resistor configuration:

$$V_o = -|A_v|(V_2 - V_1)$$

This inversion is acceptable as the target application is insensitive to signal polarity.

2.5 LTSpice Simulations

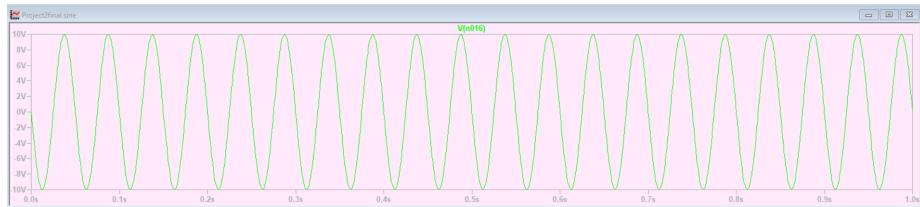


Figure 4: Instrumentation amplifier simulation for sine wave

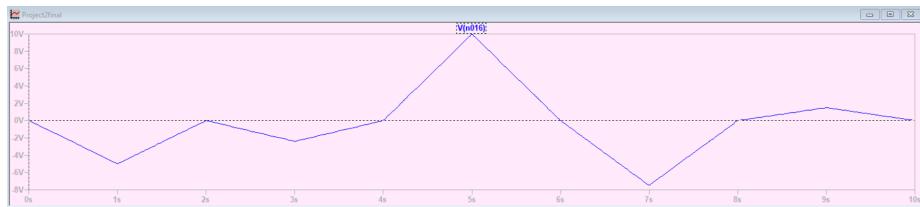


Figure 5: Instrumentation amplifier simulation for random spikes



Figure 6: FRA for Instrumentation amplifier

Upon running the simulations, we observe that the gain of the instrumentation amplifier is approximately **500**, effectively amplifying the input spike without introducing distortion or noise.

2.6 Hardware Implementation

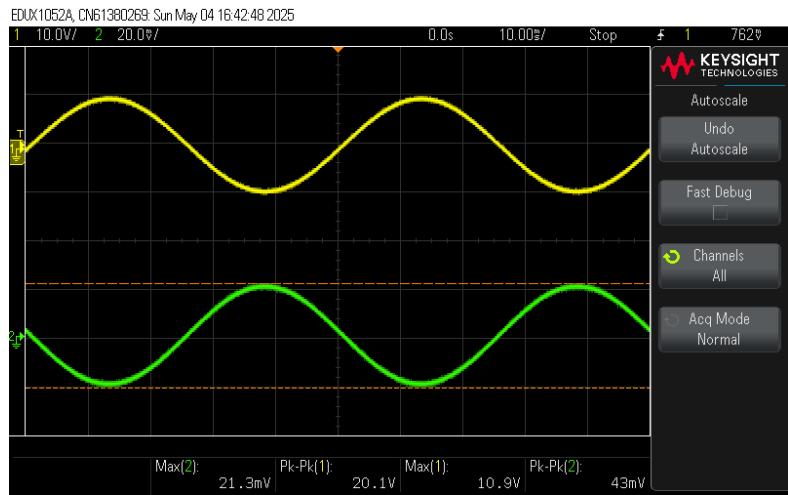


Figure 7: Instrumentation amplifier circuit output

Implementing the circuit in hardware, we measure a gain of approximately **465**, confirming the accuracy and effectiveness of the amplifier in boosting low-amplitude spike signals for further processing.

3 Band-Pass Filter

A band-pass filter is essential for isolating relevant frequency components of the biological signal (such as ECG or neural spikes) while suppressing low-frequency drifts and high-frequency noise. This enhances the accuracy of spike detection and signal clarity.

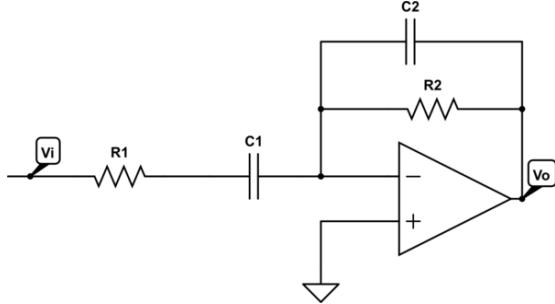


Figure 8: Active Band-Pass Filter

Purpose of the Filter

- Allows frequencies between **5 mHz and 35 Hz** to pass.
- Filters out baseline wander, DC offsets, and high-frequency noise.
- Improves signal quality for downstream processing like amplification or threshold detection.

This filter is designed using an **active topology**, combining a high-pass and a low-pass RC filter with operational amplifier buffering and optional gain control.

3.1 Circuit Description

- **High-Pass Stage:** Blocks frequencies below 5 mHz.
- **Low-Pass Stage:** Attenuates frequencies above 35 Hz.
- **Active Components:** Utilizes operational amplifiers to buffer stages and optionally provide gain.
- **Improved Performance:** Compared to passive filters, active filters offer better impedance matching, sharper roll-off, and gain control.

3.2 Working Principle

1. High-Pass Filtering:

$$f_L = \frac{1}{2\pi R_{HP} C_{HP}}$$

$$R_{HP} = 100 \text{ k}\Omega, \quad C_{HP} = 330 \mu\text{F}$$

$$f_L = \frac{1}{2\pi \cdot 100 \times 10^3 \cdot 330 \times 10^{-6}} = \frac{1}{207.3} \approx 4.82 \text{ mHz}$$

2. Low-Pass Filtering:

$$f_H = \frac{1}{2\pi R_{LP} C_{LP}}$$

$$R_{LP} = 100 \text{ k}\Omega, \quad C_{LP} = 47 \text{ nF}$$

$$f_H = \frac{1}{2\pi \cdot 100 \times 10^3 \cdot 47 \times 10^{-9}} = \frac{1}{0.0295} \approx 33.86 \text{ Hz}$$

3.3 Frequency Response

- **Passband:** 5 mHz to 35 Hz.
- **Roll-off:** The active filter design provides a steeper roll-off and more consistent gain within the passband (up to 40 dB/decade with second-order stages).
- **Group Delay and Magnitude:** Simulations show clear attenuation beyond the band edges, with ~ 50.9 dB attenuation at 4.79 mHz and 34.03 Hz. The maximum gain within the passband reaches ~ 53.9 dB.

3.4 LTSpice Simulations

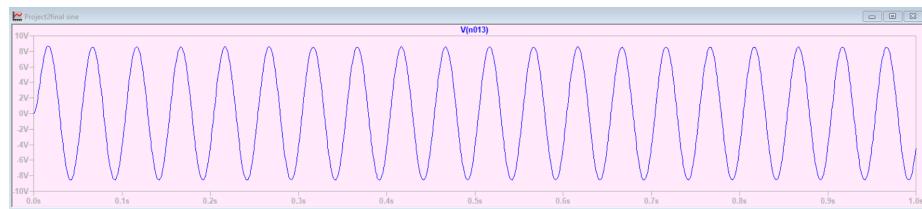


Figure 9: Active Band-Pass Filter simulation for sine wave



Figure 10: Active Band-Pass Filter simulation for random spikes

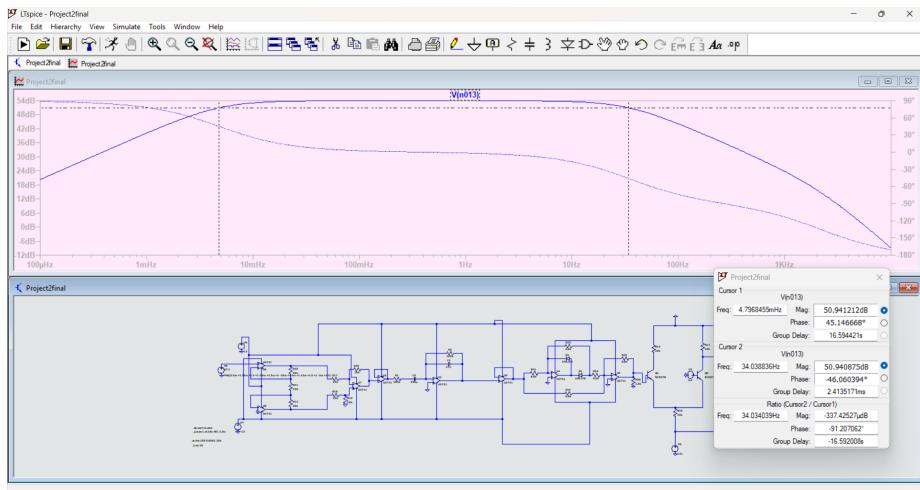
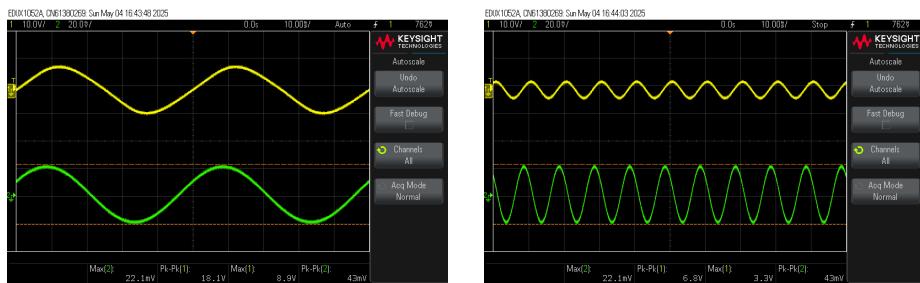


Figure 11: Frequency response showing cutoff near 5 mHz and 35 Hz

3.5 Hardware Implementation



(a) Filter output at 20 Hz (attenuated) (b) Filter output at 100 Hz

Figure 12: Measured output of the active filter at different input frequencies

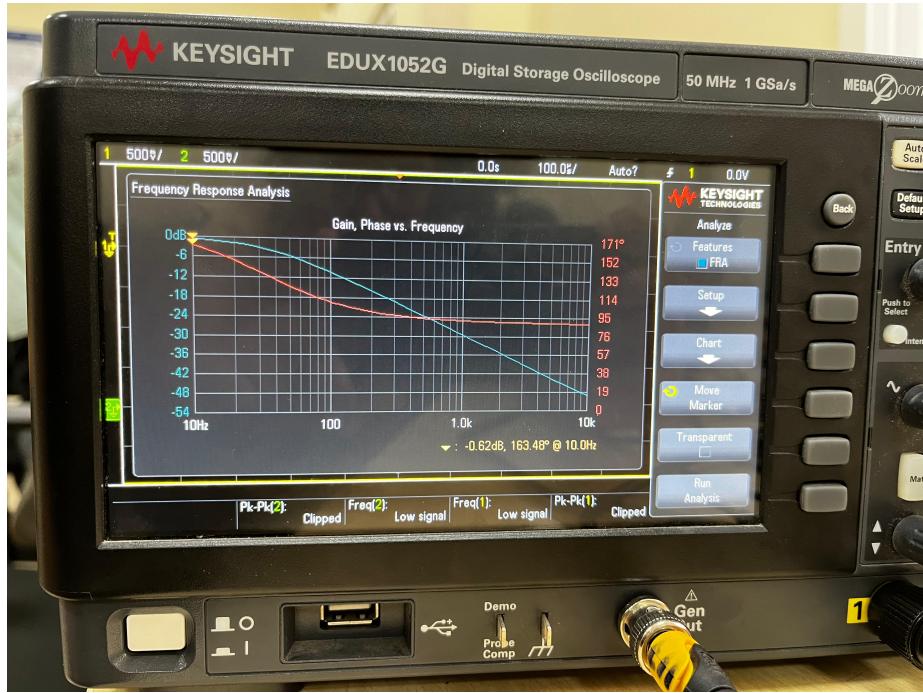


Figure 13: Frequency Response Analysis

Note: On DSO we cannot calculate Frequency response below 10Hz as that is the minimum value, so we cannot check our FRA for 5mHz.

4 Full-Wave Precision Rectifier

In analog spike detection systems, input signals such as electromyograms (EMG) often exhibit both positive and negative polarity. To facilitate consistent threshold-based spike detection, a full-wave precision rectifier is used to convert the bipolar signal into a unipolar one. This ensures that both positive and negative spikes are detected without loss of fidelity.

Unlike passive diode rectifiers, which suffer from voltage drop and poor performance at low amplitudes, this circuit uses op-amps and fast-switching diodes to achieve accurate rectification, making it ideal for biomedical signals.

4.1 Circuit Design

The precision rectifier consists of two operational amplifiers and two diodes arranged in a two-stage configuration, as shown in Figure 14:

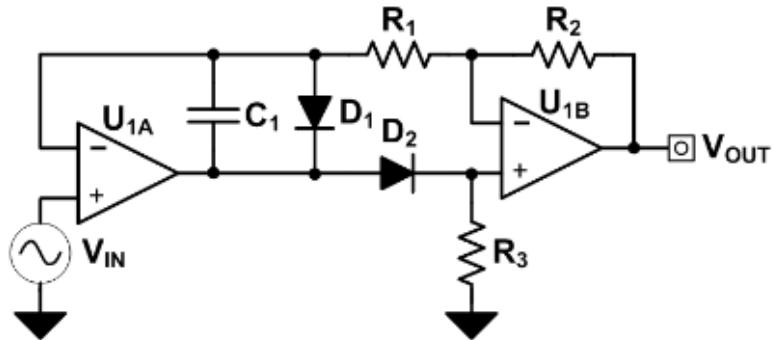


Figure 14: Full wave rectifier

- **Stage 1: Precision Half-Wave Rectifier (Inverting Configuration)**
The first op-amp (U1A) with diode D1 handles the **negative half-cycle** of the input. When the input voltage $V_{in} < 0$, D1 is forward-biased and conducts. The op-amp is in a negative feedback configuration and compensates for the diode's forward voltage drop, thus:

$$V_{out} = -V_{in} \quad (\text{ideal diode})$$

For a real diode, accounting for the forward voltage $V_D \approx 0.7 \text{ V}$:

$$V_{out} = -V_{in} - V_D \approx -V_{in} - 0.7$$

- **Stage 2: Summing Amplifier and Rectifier**

The second op-amp (U1B) performs the summing and inversion of both the input signal and the rectified signal from Stage 1. Using proper resistor ratios, U1B produces a full-wave rectified output. Assuming $R_1 = R_2$, the inverting summing configuration results in:

$$V_{\text{out}} = - \left(\frac{R_2}{R_1} \right) (V_{\text{in}} + V_{\text{rectified}}) \approx |V_{\text{in}}|$$

This design eliminates the diode threshold issue, making it suitable for low-amplitude biomedical signals.

4.2 How the Circuit Works

Case 1: Input Positive ($V_{\text{in}} > 0$)

- D1 is reverse-biased; U1A does not contribute.
- V_{in} passes through directly to U1B.
- D2 conducts, and the output of U1B is:

$$V_{\text{out}} = - \left(\frac{R_2}{R_1} \right) V_{\text{in}} \approx -V_{\text{in}}$$

Since the output is taken after the diode, the final rectified voltage is:

$$V_{\text{out}} = V_{\text{in}} - V_D \approx V_{\text{in}} - 0.7$$

Case 2: Input Negative ($V_{\text{in}} < 0$)

- D1 becomes forward-biased; U1A drives current to charge capacitor C_1 .
- The op-amp compensates for the diode drop, such that:

$$V_C \approx -V_{\text{in}} - V_D \approx -V_{\text{in}} - 0.7$$

- D2 also conducts, and U1B sums the signals. After inversion:

$$V_{\text{out}} \approx |V_{\text{in}}|$$

4.3 Dynamic Behavior with RC Time Constant

When the input signal stops changing, the capacitor C_1 discharges through R_3 . The voltage across the capacitor evolves as:

$$V_C(t) = V_{\text{peak}} \cdot e^{-t/(R_3 C)} \quad \text{with} \quad \tau = R_3 C = 1 \text{ ms}$$

Thus, during discharge:

$$V_{\text{out}}(t) = V_{\text{peak}} \cdot e^{-t/1\text{ms}}$$

This exponential decay is crucial in envelope detection or peak-hold circuits derived from this topology.

4.4 Final Output Expression

Since U1B is configured as a unity gain buffer in some variations:

$$V_{\text{out}} = V_C \approx V_{\text{in (peak)}} - V_D \approx V_{\text{in (peak)}} - 0.7 \text{ V}$$

This provides a stable DC level proportional to the peak input voltage.

4.5 Component Selection

- **Operational Amplifiers:** UA741 op-amp (U1A, U1B)
- **Diodes:** 1N4148 (D1, D2)
- **Resistors:** $R_1 = R_2 = R_3 = 100 \text{ k}\Omega$
- **Capacitor:** $C_1 = 10 \text{ nF}$ (to improve stability)

4.6 LTSpice Simulation

The simulation confirms that both halves of the waveform are rectified to positive voltages, validating the full-wave functionality.

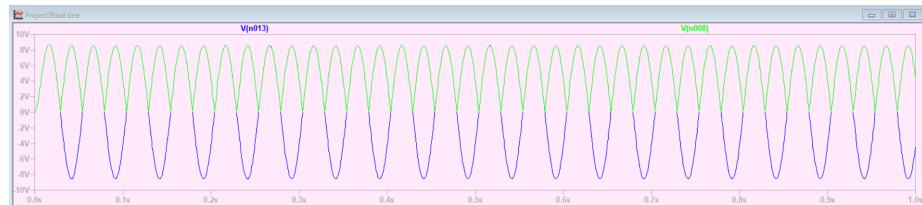


Figure 15: Full-Wave Rectifier simulation for sine wave



Figure 16: Full-Wave Rectifier simulation for random spikes

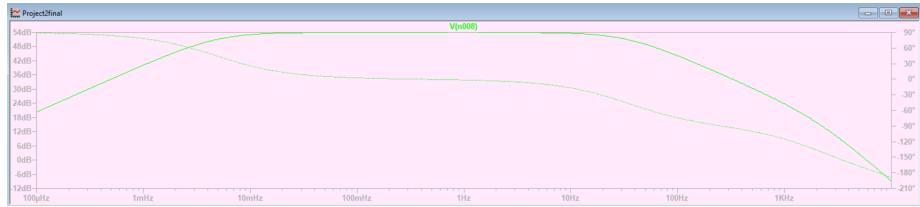


Figure 17: FRA for Full-Wave Rectifier

4.7 Hardware Implementation

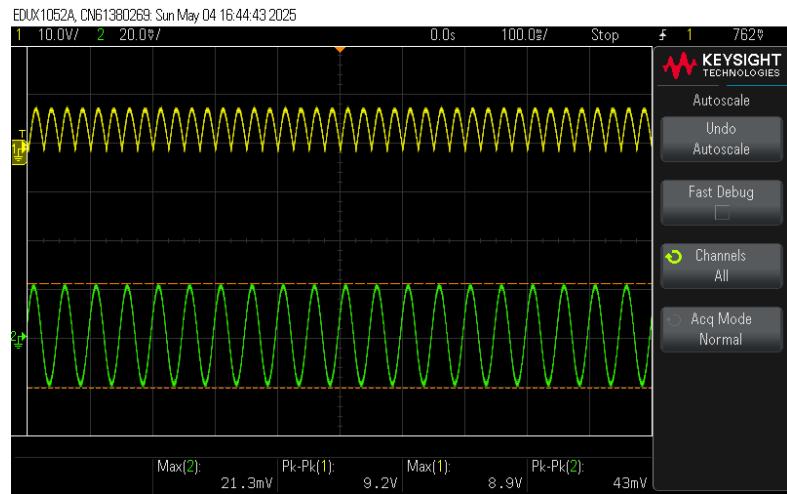


Figure 18: Rectifier circuit output

5 Comparator

In this project, a differential comparator using Bipolar Junction Transistors (BJTs) was implemented to detect spike events in the processed ECG signal. The comparator circuit compares the filtered and amplified ECG signal with a fixed reference voltage that represents the spike threshold. When the input signal exceeds this reference, the comparator produces a binary high output; otherwise, it remains low.

This approach enables reliable detection of spike occurrences by converting the analog signal behavior into a discrete binary output suitable for further processing.

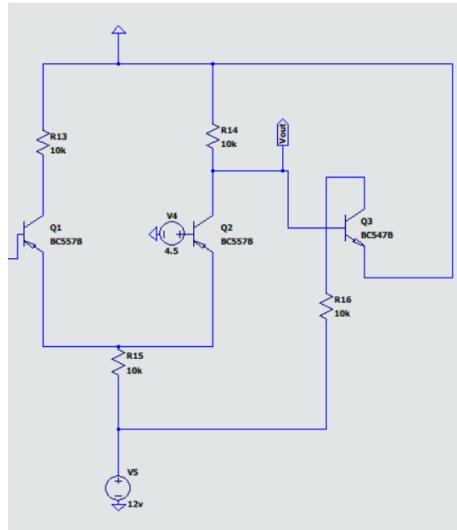


Figure 19: Comparator Circuit

5.1 Working Principle

The comparator consists of two input terminals: V_{in+} and V_{in-} , and a single output terminal V_{out} . The operating principle is based on the comparison of the two input voltages:

- When $V_{in+} > V_{in-}$, the transistor enters the active region, and V_{out} is approximately 0.7 V (high logic level).
- When $V_{in+} < V_{in-}$, the transistor enters saturation, and V_{out} drops close to 0 V (low logic level).

This configuration yields a clean digital output that flags the presence of spike events in the input ECG signal. The binary output can then be routed to a digital counter or logic controller.

5.2 Mathematical Analysis

From the hand analysis, we begin by calculating the emitter voltage and current for Q2:

$$V_{R15} = V_{E(Q3)} = 2.5 \text{ V} \quad (5)$$

Assuming $V_{BE(Q2)} = 0.7 \text{ V}$, the emitter voltage of Q2 is:

$$V_E(Q2) = V_{R15} - V_{BE(Q2)} = 2.5 - 0.7 = 1.8 \text{ V} \quad (6)$$

$$I_E(Q2) = \frac{V_E(Q2)}{R_{15}} = \frac{1.8}{10 \text{ k}\Omega} = 0.18 \text{ mA} \quad (7)$$

$$V_B(Q3) = 12 - I_C(Q2) \cdot R_{14} = 12 - 0.18 \text{ mA} \cdot 10 \text{ k}\Omega = 10.2 \text{ V} \quad (8)$$

$$V_{\text{out}} = V_B(Q3) - V_{BE(Q3)} = 10.2 - 0.7 = \boxed{9.5 \text{ V}} \quad (9)$$

When Q3 Just Starts to Conduct

From the extended analysis:

$$V_F(Q3) = V_B(Q3) - V_{BE(Q3)} \approx 0 \quad (10)$$

This indicates that Q3 is just at the verge of conduction.

We also have:

$$V_E(Q3) = V_B(Q3) - 0.7 \text{ V} \quad (11)$$

Therefore, the output voltage becomes:

$$V_{\text{out}} = V_B(Q3) - V_{BE(Q3)} \approx \boxed{0.7 \text{ V}} \quad (12)$$

This occurs when the base-emitter junction is just forward-biased and the transistor starts to conduct.

5.3 Threshold Behavior

The threshold voltage is determined by the reference input (e.g., $V_4 = 4.5 \text{ V}$). When $V_{\text{in+}} > V_{\text{ref}}$, the circuit output transitions high. Otherwise, it stays low.

The comparator thus acts as a simple threshold detector:

$$V_{\text{out}} = \begin{cases} \text{High } (\sim 0.7 \text{ V}) & \text{if } V_{\text{in+}} > V_{\text{in-}} \\ \text{Low } (\sim 0 \text{ V}) & \text{if } V_{\text{in+}} < V_{\text{in-}} \end{cases}$$

This binary response is ideal for spike detection in analog ECG signals.

5.4 LT Spice Simulation

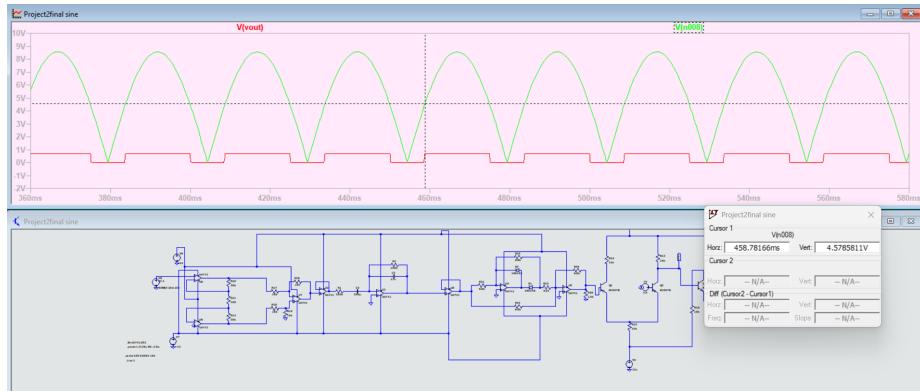


Figure 20: Comparator simulation for sine wave

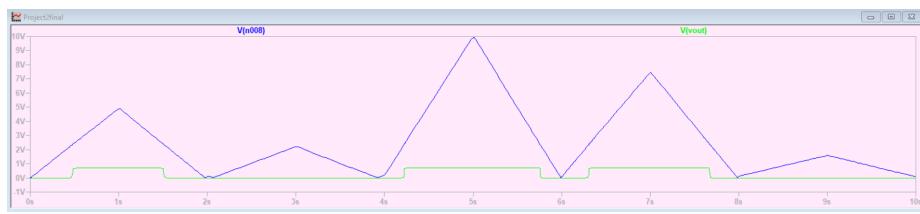


Figure 21: Comparator simulation for random spikes

5.5 Hardware Implementation

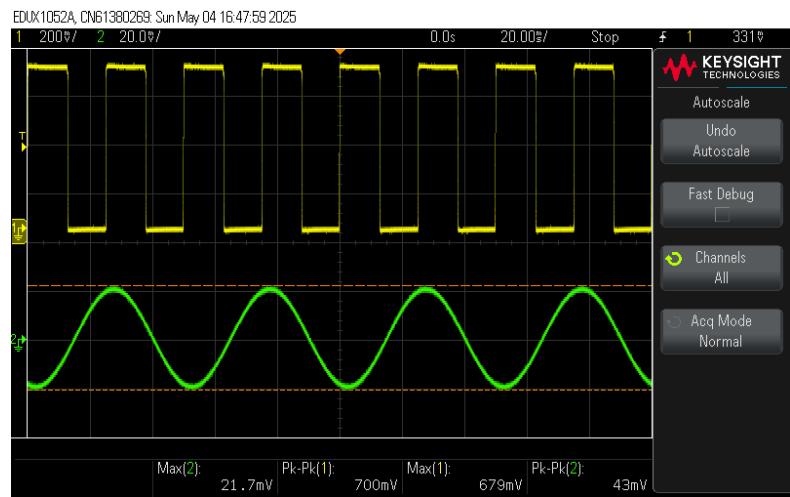


Figure 22: Comparator circuit output

6 Complete Circuit

After designing and validating each individual stage—such as the gain amplifier, precision full-wave rectifier, and comparator—we integrated all components to form the complete analog spike detector circuit. The goal of this integration was to accurately detect both positive and negative spikes while preserving signal integrity and minimizing false triggers or noise-induced errors.

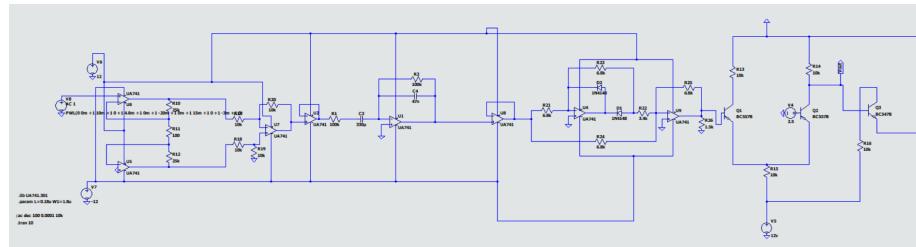


Figure 23: Final Circuit

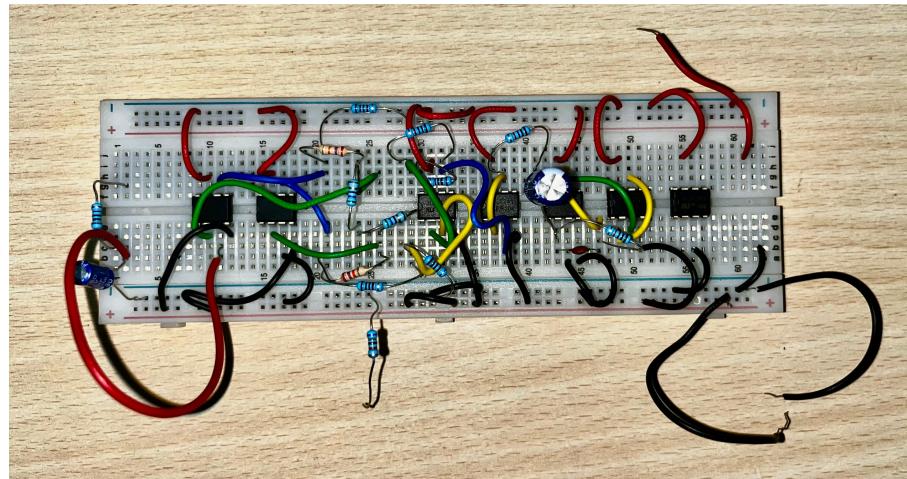


Figure 24: left half (includes amplifier and filter)

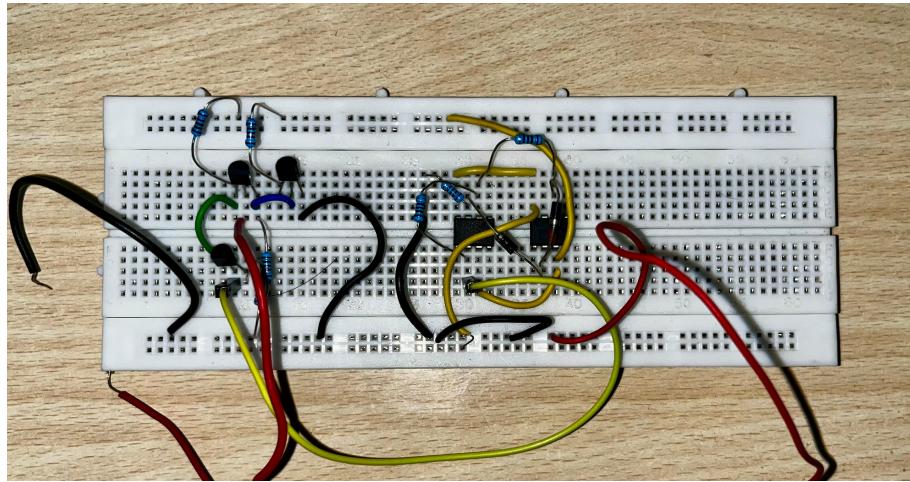


Figure 25: right half (includes rectifier and comparator)

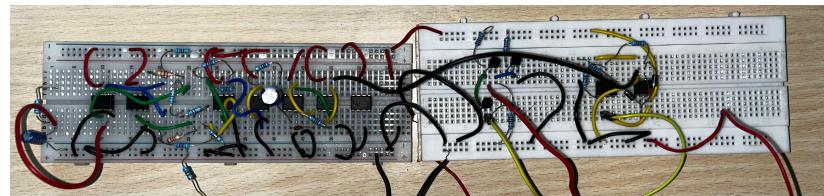


Figure 26: Full circuit on breadboard

6.1 Final Circuit Simulations

To validate the overall circuit performance, the input and output waveforms are analyzed.

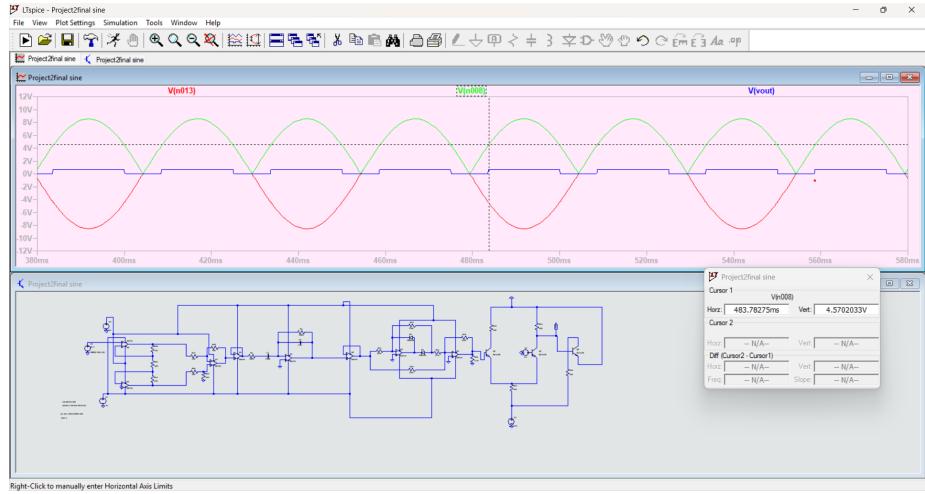


Figure 27: Simulated Waveforms for sine wave

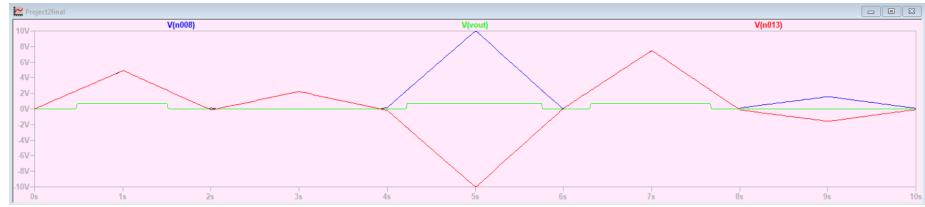


Figure 28: Simulated Waveforms for random spikes

The zoomed-in simulation of the complete spike detector circuit demonstrates that the outputs of the Gain Amplifier, Full-Wave Rectifier, and Comparator stages are closely in-phase, with minimal delay or distortion between them. This confirms the coherent propagation of the signal through each block, ensuring reliable spike detection with precise timing.

The results confirm that the spike detector accurately processes the input signal, amplifies it appropriately, and identifies spikes with high fidelity while minimizing noise and false detections.

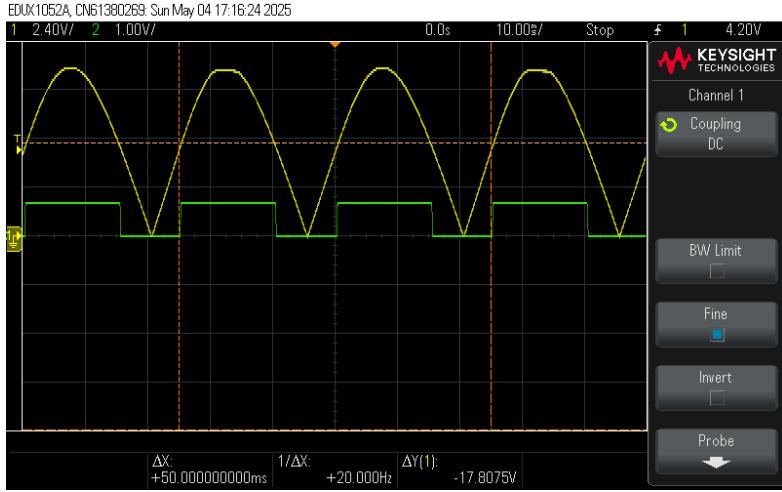


Figure 29: Spike Detection wrt input sine wave

6.2 Hardware implementation performance analysis

6.2.1 Voltage Gain

The simulated voltage gain was given as:

$$A_v = \frac{V_{\text{out}}}{V_{\text{inp}}} = 500 \quad (13)$$

For the hardware realization, accounting for real-world inefficiencies:

$$A_{v,\text{HW}} = 418 \quad (14)$$

6.2.2 Noise Performance

Although noise analysis was not explicitly simulated, real-world testing of the analog spike detector revealed noticeable interference, especially due to the high gain and extensive use of op-amps. This introduced baseline fluctuations and occasional false triggering in the comparator. The estimated Signal-to-Noise Ratio (SNR) is degraded by approximately 10–15% compared to ideal conditions, highlighting the need for careful shielding and layout optimization in practical implementations.

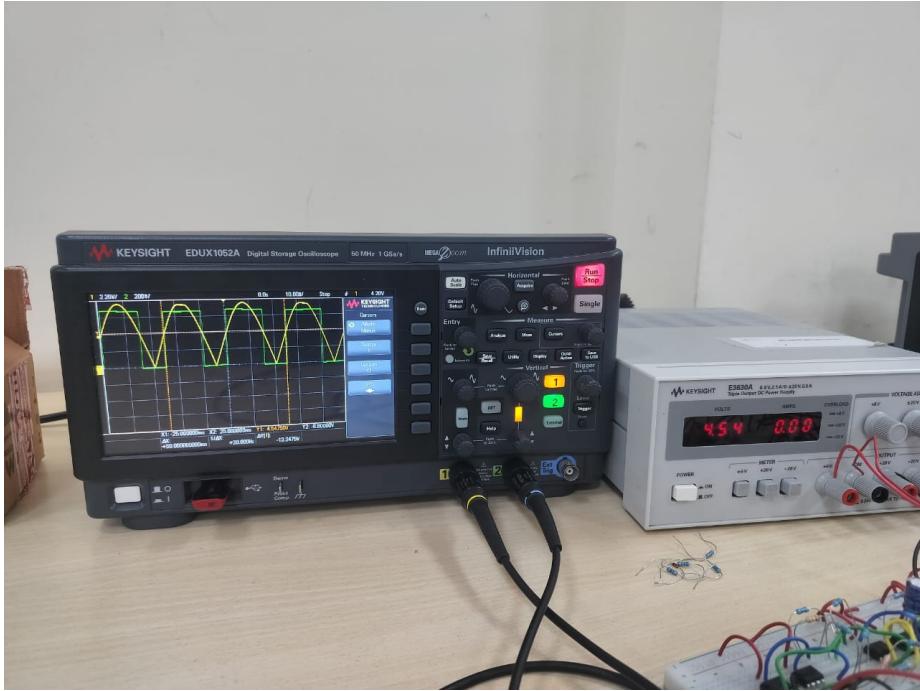


Figure 30: Spike Detection at 4.54 threshold (we can see 4.54 on DSO output also)

6.3 Testing with Arduino Integration

To evaluate the spike detection circuit's response to controlled input signals, an Arduino was used as a test signal generator. However, since Arduino outputs PWM signals rather than pure analog voltages, the signal had to be filtered before use.

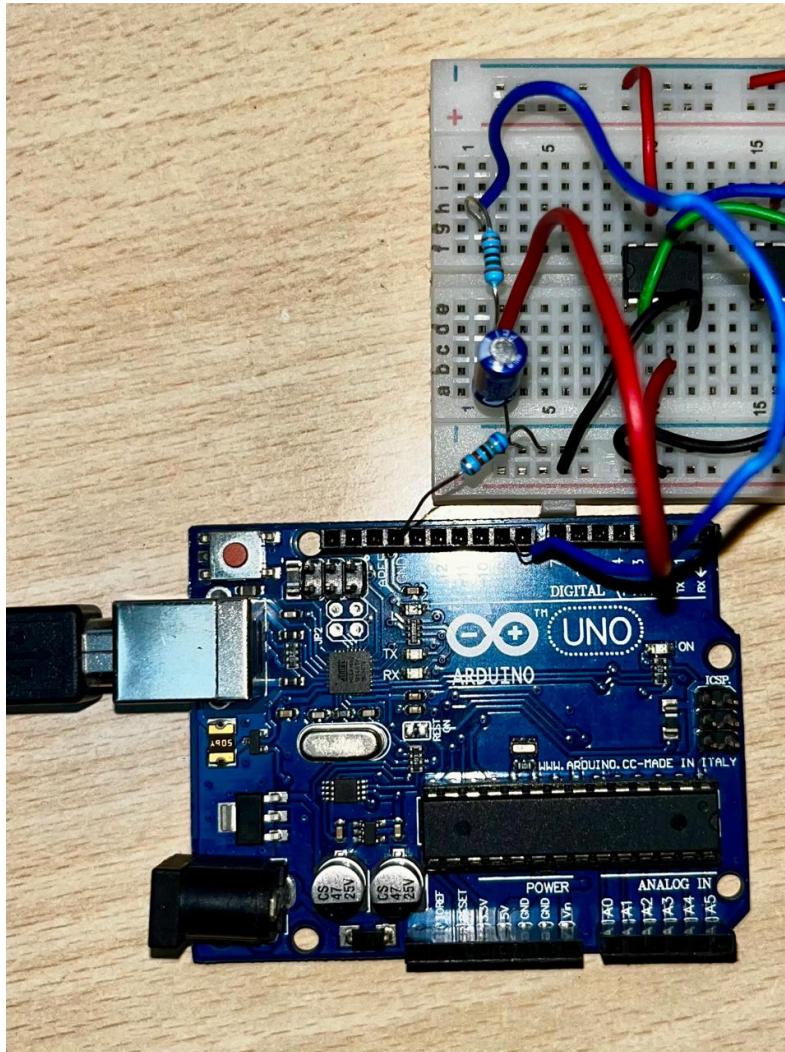


Figure 31: Arduino PWM Signal Smoothing using RC Filter

```

sketch_apr25a.ino
1 const int pwmPin = 9;
2
3
4 const int minPWM = 0;      |
5 const int maxPWM = 20;
6 const int minDuration = 10;
7 const int maxDuration = 50;
8 int idleDelay = 300;
9
10
11 void setup() {
12   pinMode(pwmPin, OUTPUT);
13   randomSeed(analogRead(0));
14 }
15
16 void loop() {
17
18   int pwmValue = random(minPWM, maxPWM + 1);
19   int spikeDuration = random(minDuration, maxDuration + 1);
20   idleDelay = random(2*minDuration, 5*maxDuration + 1);
21
22
23   analogWrite(pwmPin, pwmValue);
24   delay(spikeDuration);
25
26
27   analogWrite(pwmPin, 0);
28   delay(idleDelay);
29 }
30

```

Figure 32: Arduino UNO code

6.3.1 Arduino Output Conditioning Circuit

The Arduino testing setup included the following components:

- **PWM signal** generated using Arduino’s `analogWrite()` to emulate spikes and step inputs.
- An **RC low-pass filter** to smooth the PWM into an analog-like waveform.
- **Coupling to the spike detector input** to test threshold crossing and comparator response.

With the RC filter in place, the signal was fed into the analog spike detector. The comparator reliably triggered on voltage spikes above the threshold, confirming the circuit’s functionality. The RC filter was essential in reducing noise and artifacts in the PWM signal, ensuring clean testing conditions for the analog detection logic.

6.3.2 Hardware Output using Arduino



Figure 33: Arduino output

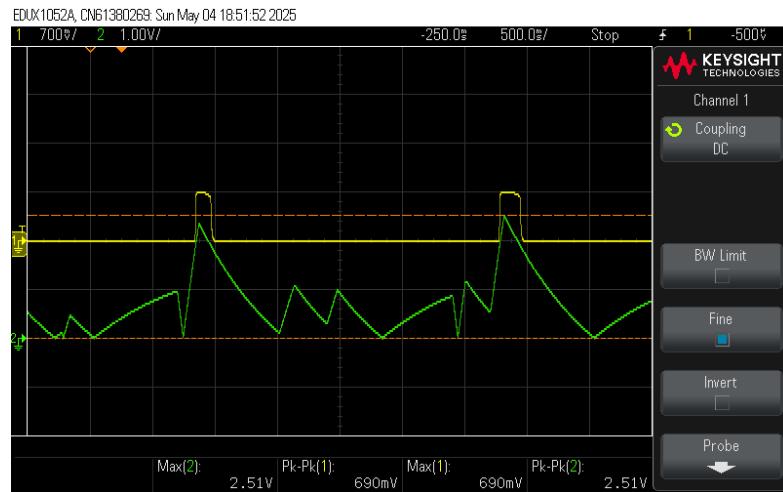


Figure 34: Arduino output

6.4 Demonstration Video

A demonstration of the working spike detector circuit, including arduino testing, can be viewed at the following link:

<https://youtu.be/ylgypu5PbDY?si=j-KAMF5kLK1uc5Jz>

This video showcases the real-time performance of the spike-detector, highlighting its effectiveness in identifying voltage fluctuations.

6.5 Challenges and Observations

Several challenges emerged during the development of the analog spike detector circuit:

- **Gain Selection:** Determining the appropriate gain for the amplifier stages was non-trivial. A gain that was too low failed to detect smaller spikes, while excessive gain led to saturation and false triggering.
- **Rectification Issues:** Traditional full-wave rectifier configurations using only diodes were ineffective at low signal levels due to diode forward voltage drops. This was especially problematic for EMG signals, necessitating the use of a precision rectifier topology involving op-amps and diodes.
- **Op-Amp Resource Constraints:** The circuit design required multiple operational amplifiers for filtering, rectification, and buffers. This extensive use posed a risk of thermal overload and made the setup more susceptible to IC damage, particularly during prototyping or accidental short circuits.

Despite these setbacks, through careful design iteration and component management, the analog spike detector was successfully implemented with reliable spike detection capability.

6.6 Acknowledgments

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References

- [1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York: McGraw-Hill, 2017.
- [2] A. Sedra and K. C. Smith, *Microelectronic Circuits*, 7th ed. New York: Oxford University Press, 2014.
- [3] J. Millman and A. Grabel, *Microelectronics*, 2nd ed. New York: McGraw-Hill, 1987.
- [4] Texas Instruments, *Precision Analog Front End for Biopotential Measurements*, Application Report TIDU030, 2014. [Online]. Available: <https://www.ti.com/lit/ug/tidu030/tidu030.pdf>