ECEN 325 Project - Final Report

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Sections: 512, 507

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Specifications and Background:

The main idea behind this project was to design a multistage amplifier that meets the following specifications given in the project prompt:

- $R_L = 20\Omega,\ Z_i > 20k\Omega$
- No more than 3 stages
- Bandwidth covering audio range 100 Hz to 10 kHz
- Maximum input signal 20 mV
- Gain of 30 dB

Our group decided to approach the design by using a two stage amplifier. Initially, a three stage bipolar junction transistor amplifier was considered, but a realization was made that by using a pair of one bipolar junction and one NMOS transistor, the same functionality could be realized. Additionally, the transistor for each stage served each of the two following purposes: creating gain and preserving gain. The fundamentals ideas for each stage are discussed below.

The first stage makes use of a bipolar junction transistor in the common-emitter configuration with a relatively high output impedance. In the common-emitter configuration, the signal is amplified; consequently, this stage is labelled the gain stage. The input impedance was designed to be above the design requirement of 20kΩ. The output impedance will have to be matched to the input impedance of the second stage in order to maximize gain and minimize distortion and clipping. This idea is discussed further in the calculations.

The second stage makes use of a NMOS transistor in the common-drain configuration with a high input impedance. In the common-drain configuration, there is essentially no gain, but it serves as a buffer stage in order to deliver the gain signal to the load without attenuation. In this stage, large resistors were used in order to evenly distribute current to the load and the source resistor. Doing this ensured that no voltage would be lost across the load resistor, and the effective gain from the first stage would be present in the signal at the load in the second stage.

The two stages do not necessarily work independently of each other, because the common-emitter at the first stage was designed to deliver the proper gain for the input signal when the input impedance of the second stage is connected as the load for the first stage. The two stages are coupled through use of a capacitor in order for the DC biasing of each individual transistor to be maintained. This in essence only allows AC signals to flow through the capacitors, while keeping the DC signals with the corresponding configurations.

Calculations:

To begin, the common-emitter stage was designed. We first assume

$$V_{RE} = 1.25V$$

Next, to determine a value for V_{RC}, we have

$$V_{CC} - \hat{V}_o - V_{RE} - 0.5 \geq V_{RC}$$

$$V_{RC} \leq 2.25V = 2.25V$$

This value was maximized in order to have as much gain as possible.

Next, the collector current was calculated with a β of 100

$$I_C \leq \frac{\beta}{R_i} * \frac{1}{\frac{10}{V_{RE} + V_{BE}} + \frac{10}{V_{CC} - V_{RE} - V_{BE}} + \frac{|A_v|}{V_{RE}}} \leq 96\mu A = 95\mu A$$

Where

$$|A_v| = \frac{V_{RC}}{V_T}$$

From here, the collector, emitter, and gain resistor values were calculated using the above parameters. The base resistors were found using the below equation, where N, the parameter for beta-insensitivity was taken to be 10.

$$R_{B1} = \frac{\beta(V_{CC} - V_{RE} - 0.7)}{NI_C}$$

$$R_{B2} = \frac{\beta(V_{RE} + 0.7)}{NI_C}$$

Next, the second common-drain stage was designed. V_{RS} was first assumed to be 1V, and V_{GS} was taken to be 2.1V, reflecting the typical values contained in the datasheet for the 2N7000G transistor. Next, the values for the gate resistors were found using the following pair of equations:

$$R_{O,Stage\,1} = 25k\Omega = R_{i,Stage2} = R_{G1}//R_{G2}$$

$$V_G = V_{CC}\frac{R_{G2}}{R_{G1} + R_{G2}}$$

The first equation is necessary to match the impedances of the stages in order to have minimal gain loss and distortion. The second equation is a simple voltage divider reflecting the gate voltage assumed prior.

From here, the gain of the common-drain can be obtained from the equation:

$$|A_v| = \frac{R_S}{\frac{1}{g_m} + R_S}$$

From this equation it is clear that R_S should be maximized in order to provide as much gain as possible to the output. The value of R_H was chosen to match R_S in order to maximize the voltage over the load resistor and therefore the output voltage.

All capacitors were chosen as 10μF to strongly isolate the DC component while keeping the bandwidth of the circuit between 100Hz – 10KHz as required.

Justification of Architecture:

All of the components included in our multistage amplifier serve a specific design purpose in order to achieve or be very close to the design specifications given for the project. The first stage provided gain to the input AC sinusoidal voltage signal. The second stage acts as a buffer for the gain stage, maintaining the gain of the stage for the amplified signal to be delivered to the load, the speaker. Specifically, the common-emitter configuration is the best way to provide maximum gain to a load. The common-drain was chosen for the buffer stage due to the fact that no current flows through the gate of the transistor. This makes the input impedance much easier to calculate and match to the first stage, and simplifies the gain of the circuit, making it dependent on only the source resistor.

As seen in *Figure 2*, the magnitude of the gain is approximately -36.3 mdB for the first stage. This value is very close to 0 dB, which corresponds to a gain of one. This is as expected, because the second stage makes use of a NMOS transistor in the common-drain configuration to act as a buffer for the first stage. In *Figure 3*, the magnitude of the gain is approximately 30.2 dB. This value corresponds to a gain of 32.4 with an appreciable bandwidth from around 100Hz to 100kHz. The values fall within the design constraints and indicate that the design can satisfy the requirements needed to drive the speaker with an amplified audio signal.

Design, Simulations, and Measurements:

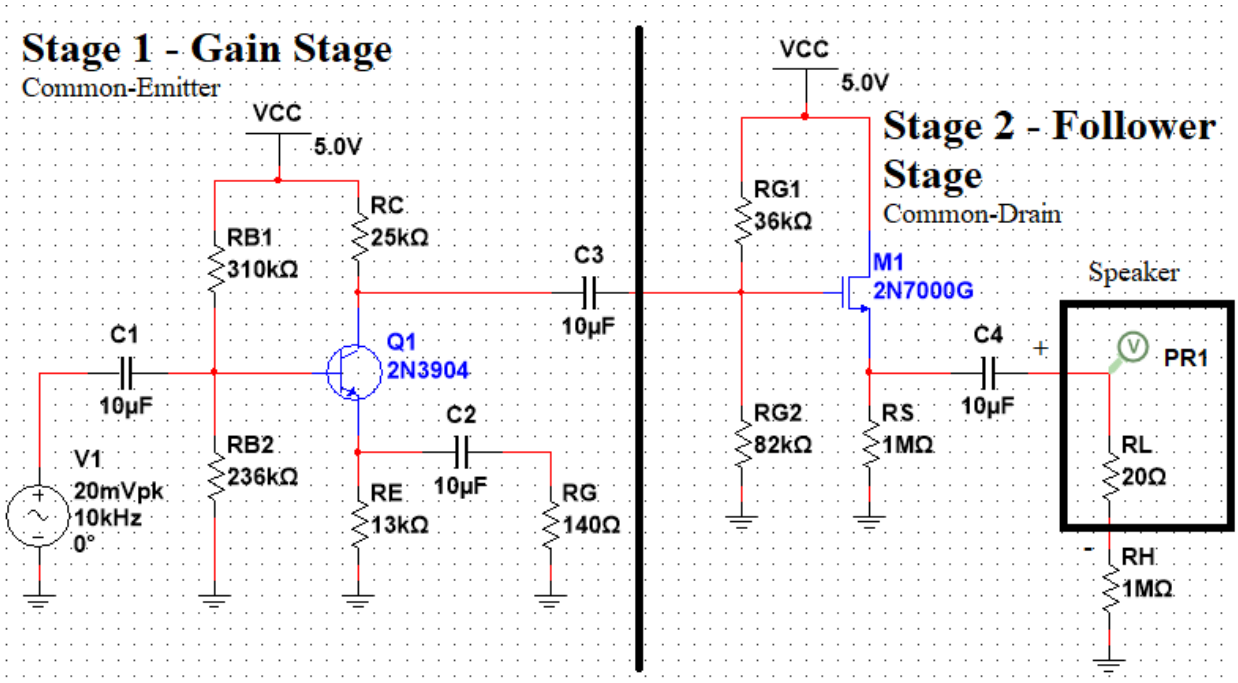

Figure 1: 2-stage amplifier Multisim schematic

Table 1: Component Values										
First Stage - Common-Emitter					Second Stage - Common-Drain					Coupling Caps
R_{B1}	R_{B2}	R_C	R_E	R_G	R_{G1}	R_{G2}	R_S	R_L	R_H	C_1, C_2, C_3, C_4
310kΩ	236kΩ	25kΩ	13kΩ	140Ω	36kΩ	82kΩ	1MΩ	20Ω	1MΩ	10 µF

Table 2: Measured and Simulated Results				
First Stage - Common-Emitter			Overall Results	
	Gain	THD	Gain	THD
Simulation	-36.28mdB	2.72%	30.161dB	4.936%
Measurement	N/A	N/A	28.851dB	6.8%

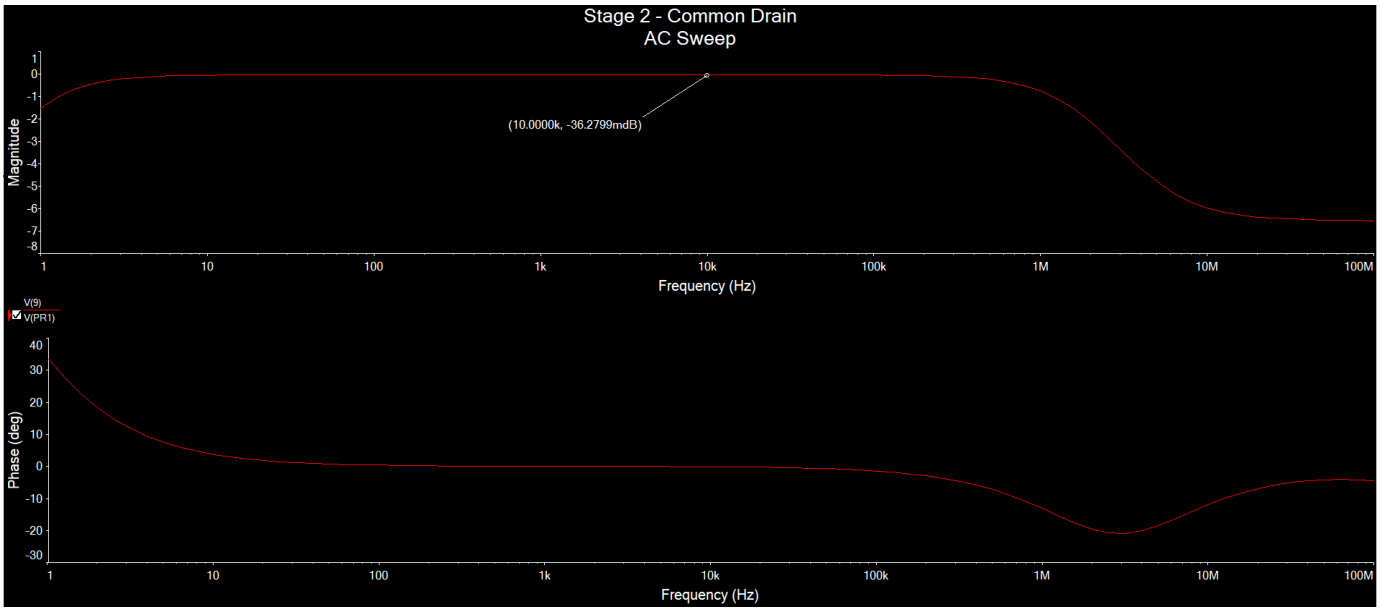

Figure 2: Simulation Bode Plot for the second (common-drain) stage

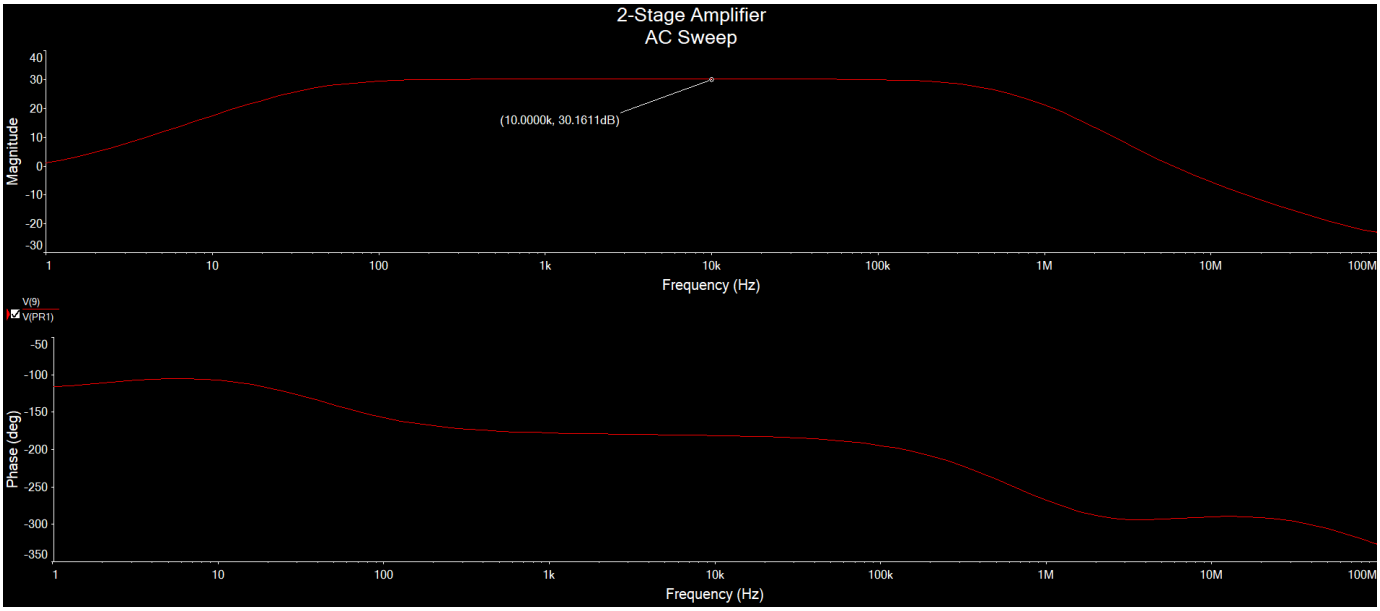

Figure 3: Simulation Bode Plot for both stages

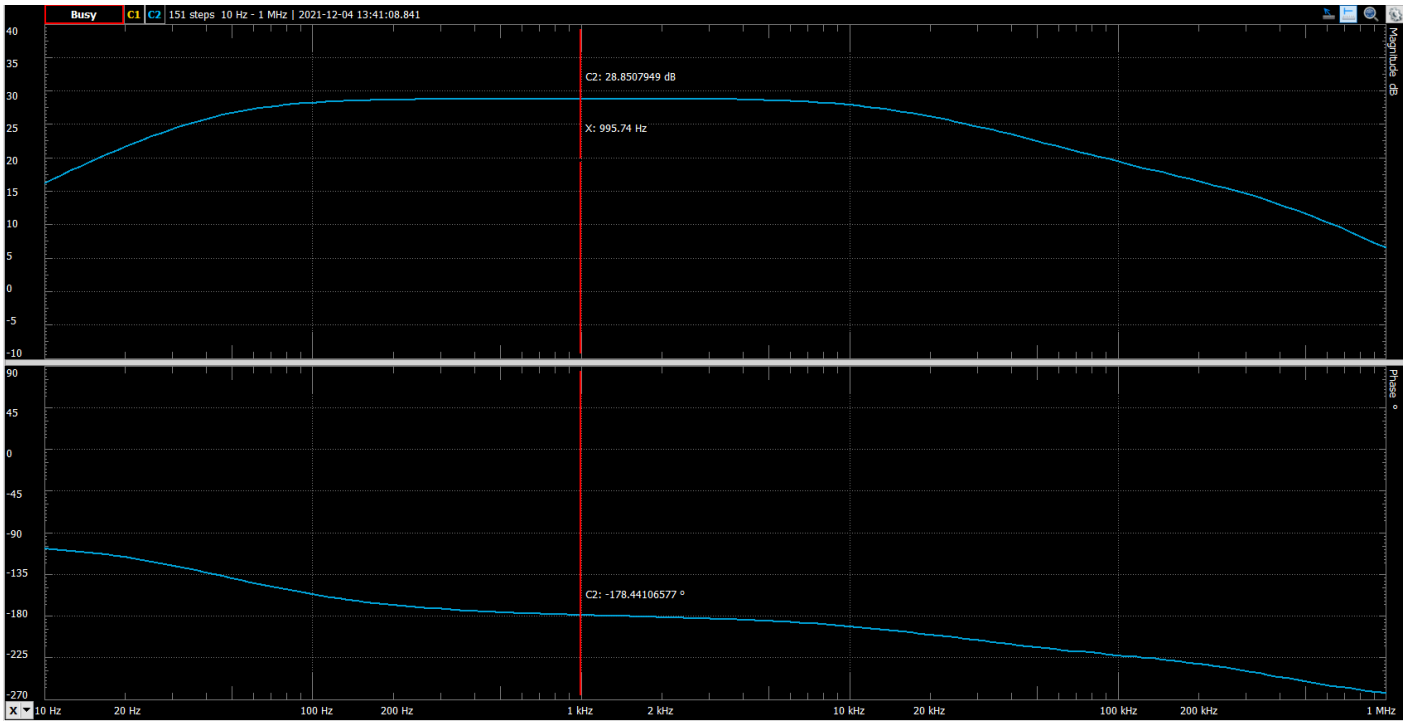

Figure 4: Measurement Bode Plot for 2-stage amplifier

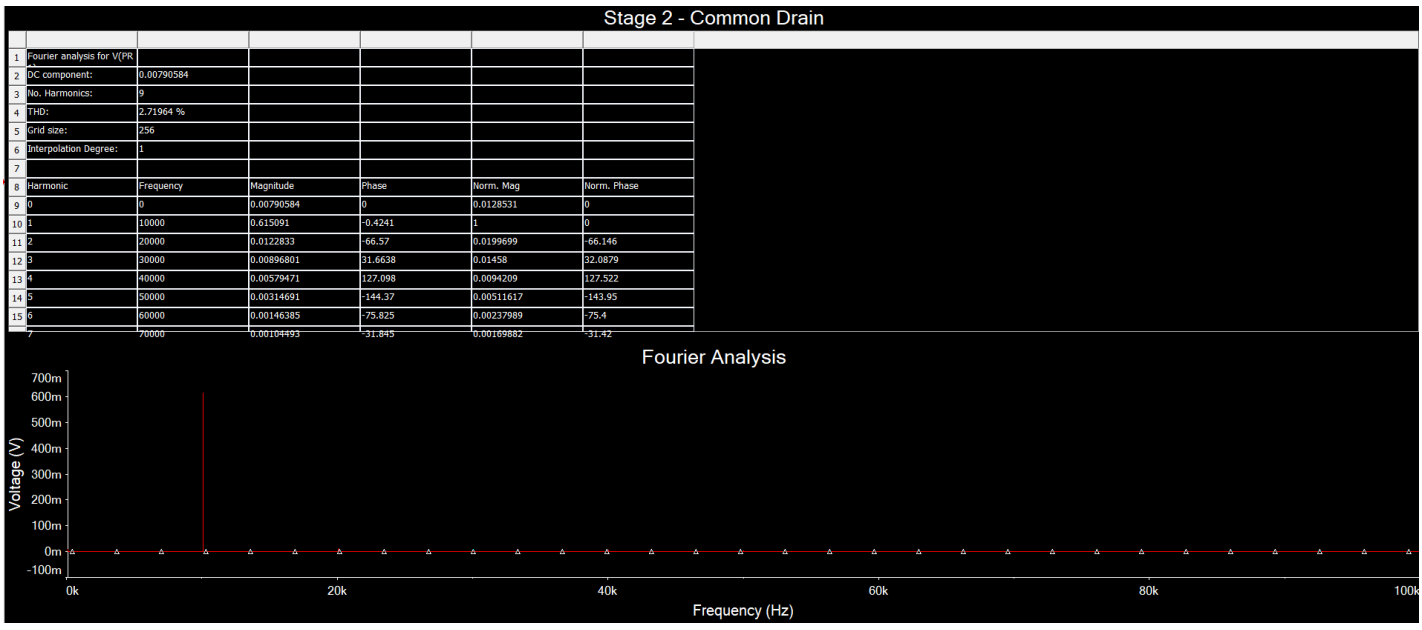

Figure 5: Simulated THD for the second (common-drain) stage

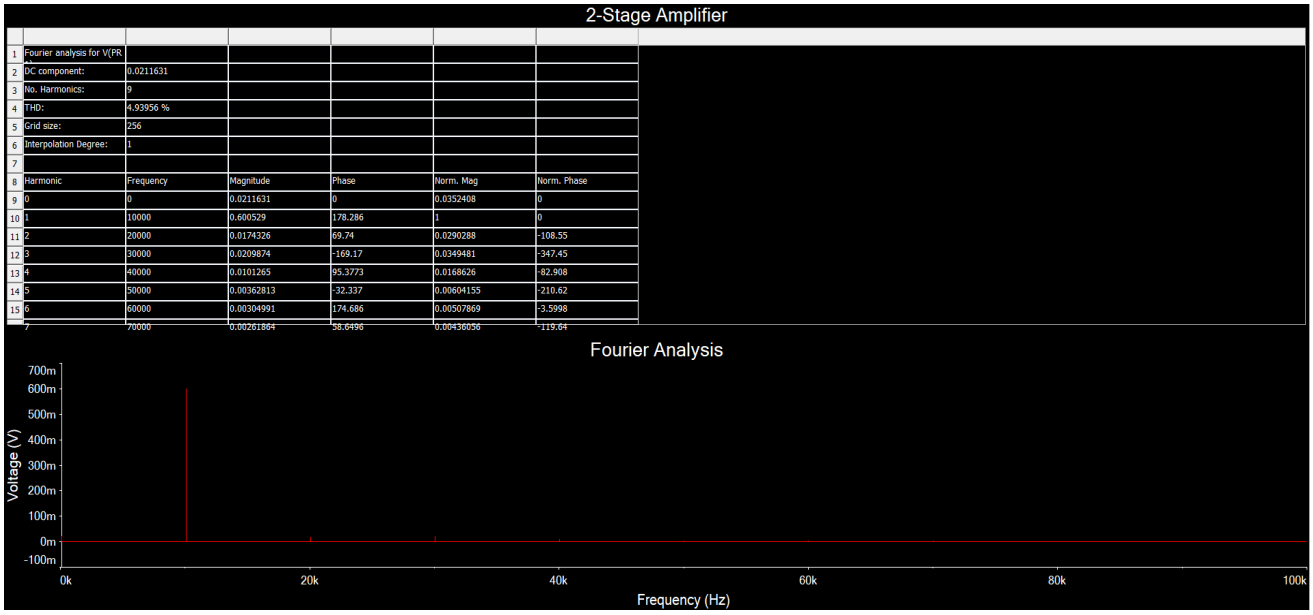

Figure 6: Simulated THD for 2-Stage Amplifier

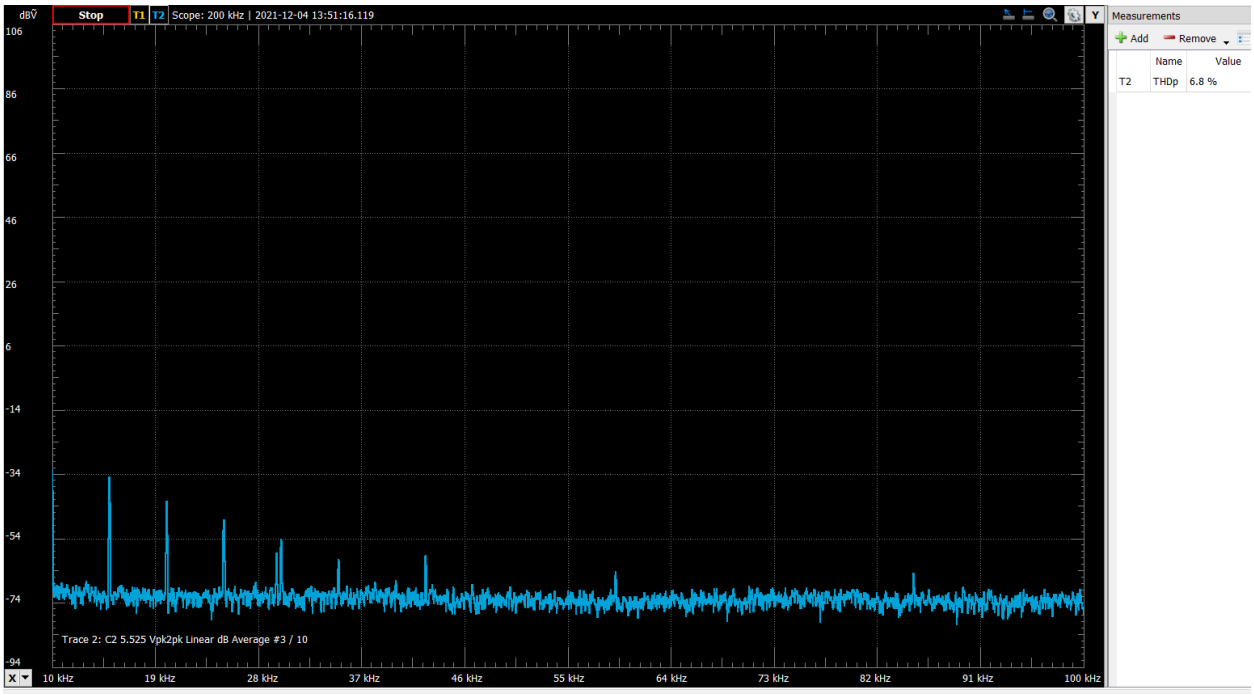

Figure 7: Measured THD for 2-Stage Amplifier

Comparison of Results:

This section draws comparisons between our simulation and measurement results. When physically constructing the circuit, a voltmeter was used to get the measurements for all the resistors to ensure that the values for resistance manifested on the board were the same as those in the intended simulated design.

A straight comparison of the figures for the Bode plots of the multistage amplifier shows that the gain in measurements was a little bit lower than the gain seen in the simulation. The gain in the measurements was approximately 28.9 dB as seen in *Figure 4,* and the gain in the simulation was 30.2 dB as seen in *Figure 3.* Fundamentally, there is a difference of around 1 dB between the simulation and the actual measurement, which may be attributed to variations in beta based on the temperature in the room and possibly some differences in the actual value for the resistor values. The differences in individual resistor values with a gold band level of tolerance is typically +/- 5%, however when multiple resistors are used to achieve certain resistor values, the error propagates and can create more differences from expectation as seen in the simulation.

In the simulation, the THD of the 2-Stage Amplifier (*Figure 6*) was around 4.93% and in the measurement (*Figure 7*) was 6.8%. The difference between simulation and measurement was very minor. Slight variation may be attributed to the differences in resistor values explained above. Additionally, an observation was made that there was a potential grounding issue when the physical circuit was constructed. The grounding issue was observed at the peak of the sinusoidal output wave for the transient response. The peak of the signal appeared to have an instability that was adversely affecting the distortion present in the signal.

Experimental Results:

The results of the experiment were similar to what was expected from the simulation. We noticed that the gain for the amplifier was a little lower than initially designed and that the THD was a little bit worse as detailed above. In the end, the multistage amplifier served its purpose of amplifying the signal with a sufficient maximum output swing for the maximum input signal with an amplitude of 20 mV. When the load resistor was replaced with the speaker, some minor adjustments had to be made to the buffer stage, but in the end everything worked as intended with sufficient gain and minimal distortion.

Conclusions:

The experiment was very successful except for some minor adjustments that had to be made in the final demo. The resistors values were slightly changed in the buffer stage so that the voltage was large enough across the speaker in order to have an audible output. After the adjustments, we were able to make the speaker work and output good quality audio.