Lab 6: Design and Characterization of a Flip-Flop

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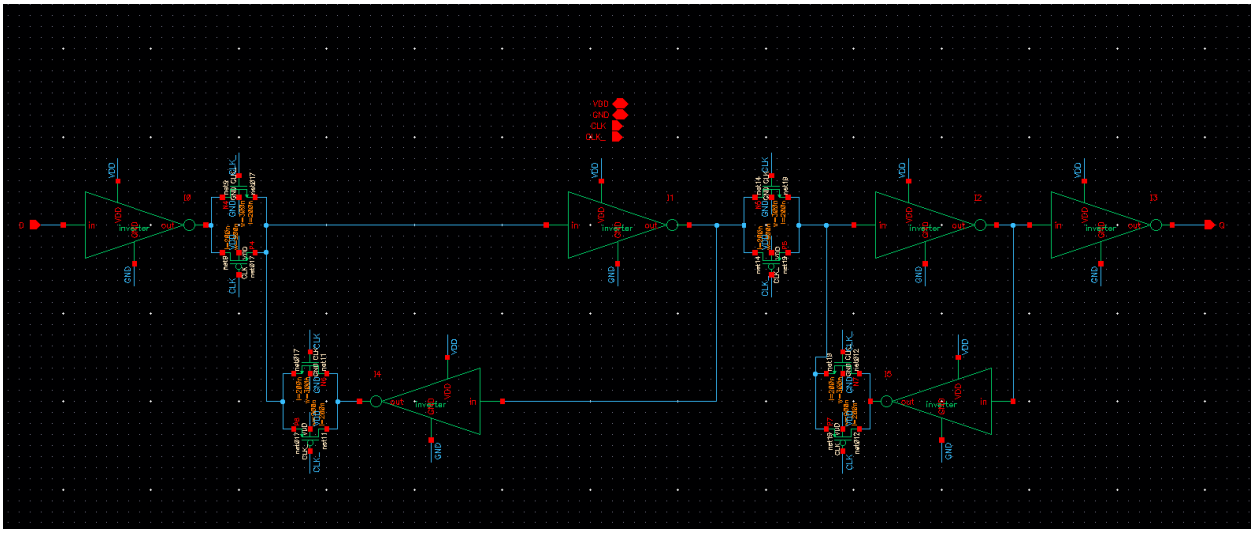

Figure 1: Schematic

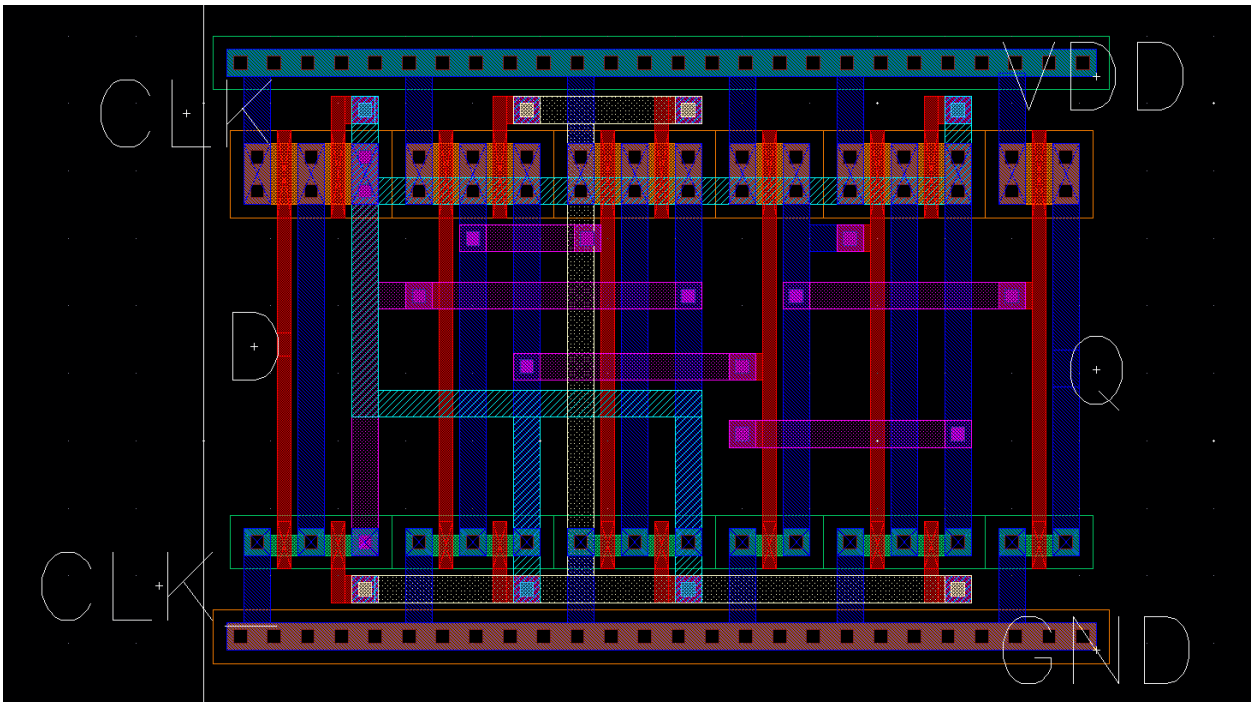

Figure 2: Layout

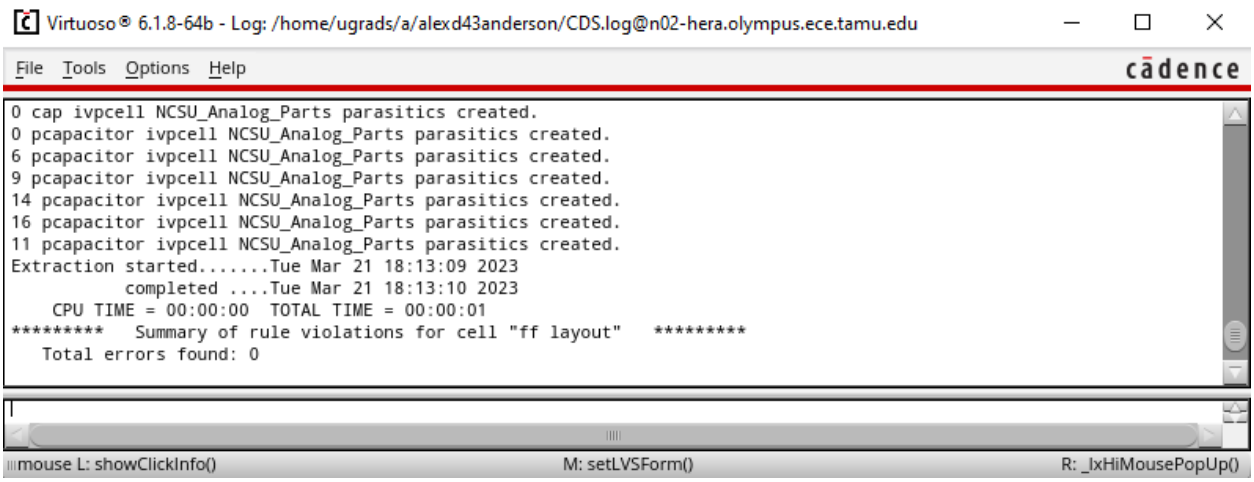

Figure 3: DRC

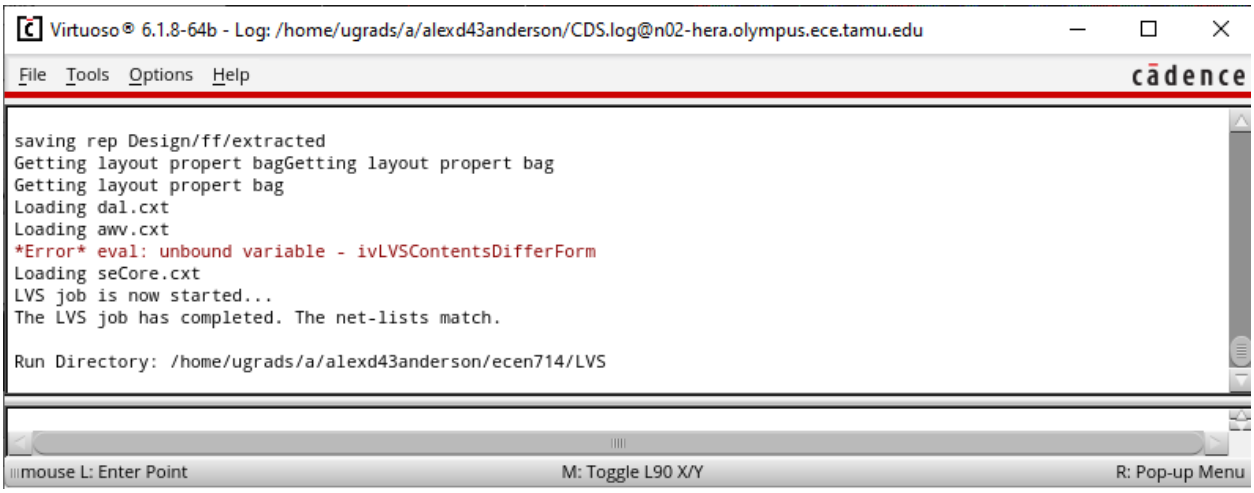

Figure 4: LVS

A test bench was used to verify the necessary specifications:

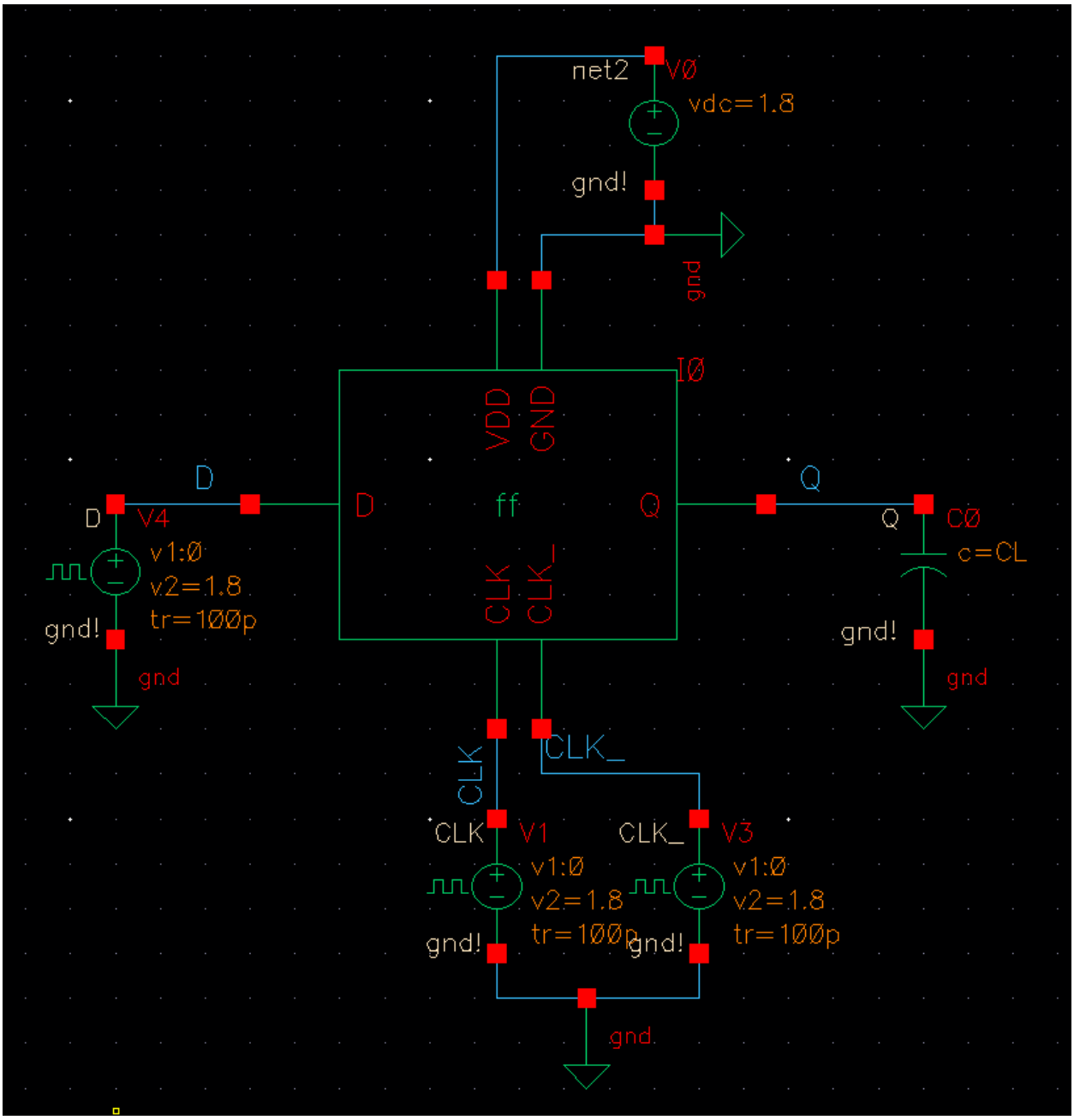

Figure 5: Test Bench

The design was verified for some set of inputs:

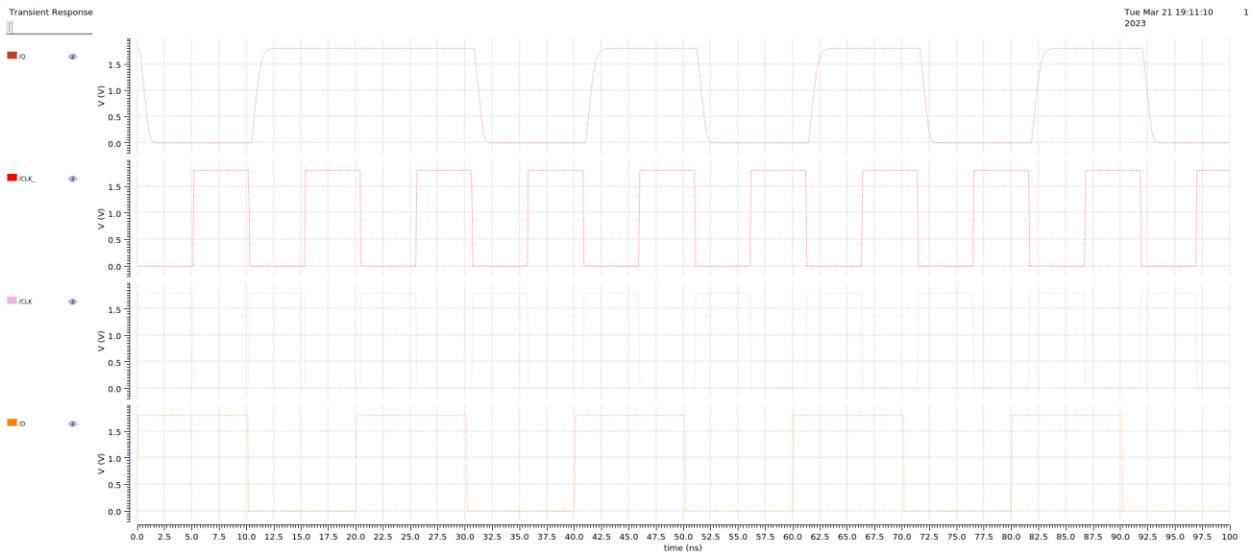

Figure 6: Transient Response

Next, the delays for various output capacitance were measured:

Table 1: Output Capacitance Delay Table

Output Capacitance (fF)	Rising Time (ps)	Falling Time (ps)
1	206.27	175.13
12	263.7	235.9
23	313.2	286
34	362	334.7
45	410.5	383
56	458.7	431.4
67	507.2	479.6
78	555.4	527.9
89	603.8	576.2
100	652.1	624.3

Next, the input sink capacitance was measured over 1-1GHz and was averaged to determine a value of **3.15fF (see below).**

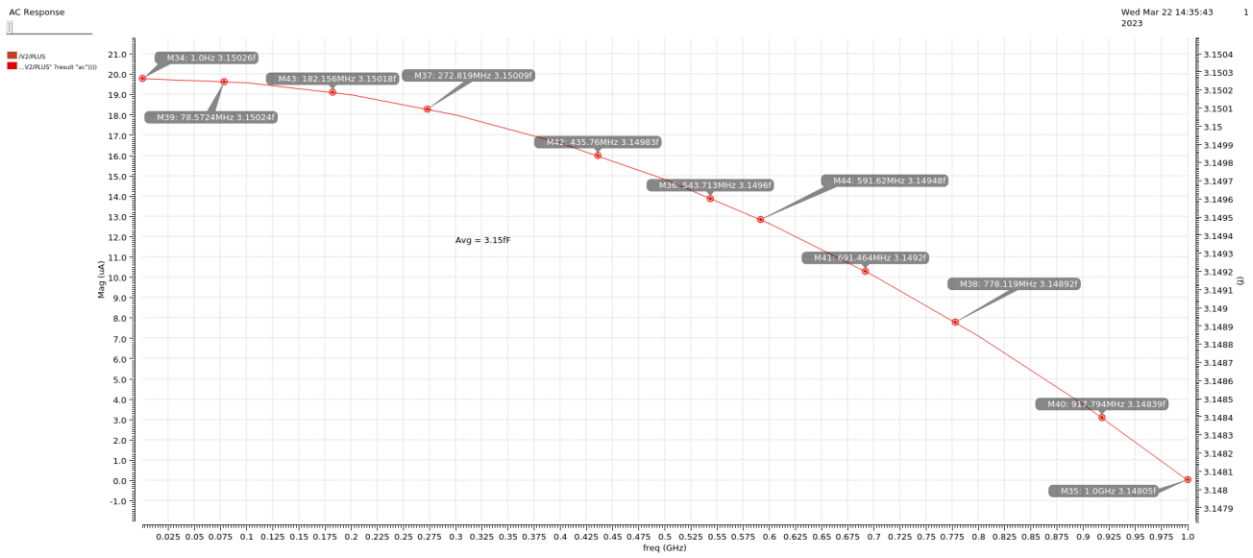

Figure 7: Sink Capacitance AC Response

Next the setup time was recorded by observing the rising edge of D relative to Q. The fall time stays the same since it is unaffected for further inputs.

Table 2: Setup Time Delay Table

Input (D) Delay (ns)	Rise Time Delay (ns)	Fall Time Delay (ps)
9.98	0.666	624
9.988	0.6709	624
9.996	0.6783	624
10	0.7065	624
10.012	0.7266	624
10.02	21.05	624
10.036	21.05	624
10.044	21.05	624
10.052	21.05	624
10.06	21.05	624

Thus, since the lowest possible input delay without error is 10.02ns, with a clock period of 10ns, this means the worst-case setup time is 0.02ns or **20ps**.