Lab 4: Advanced Layout Design Techniques

ECEN 704-601
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Description

In this lab, the layout of a two stage op amp was performed using previously explored layout techniques: dummy elements and common centroid, as well as of guard rings to reduce substrate noise, isolate devices, and prevent latch-up.

Design

The two stage op amp was designed using a transistor length of 180nm and unit width of 720nm. Dummy elements were included to support common centroid layout and the NMOS and PMOS devices were separated and isolated by guard rings. The below floorplan was used in planning and executing the layout.

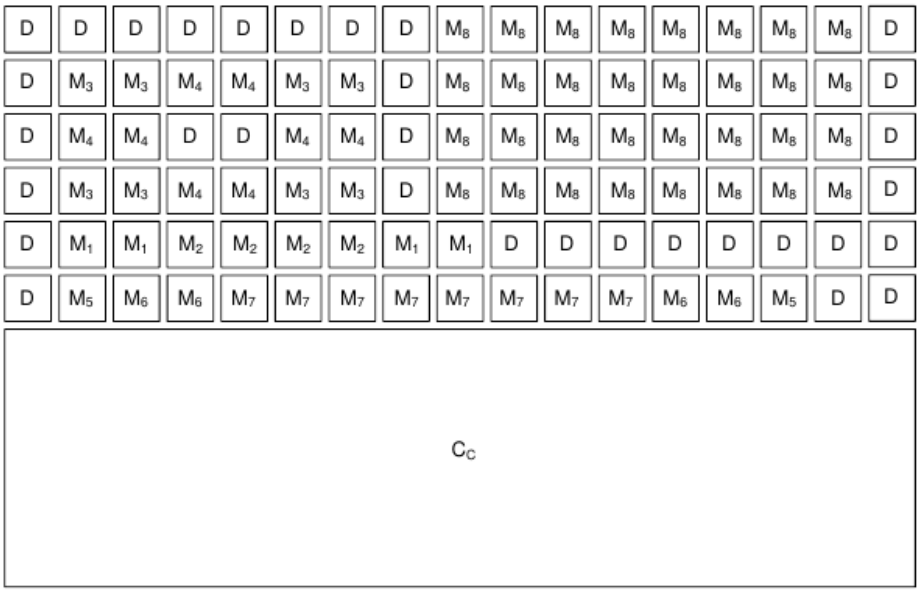

Figure 1: Floorplan

To prevent latch-up and reduce substrate noise, both the NMOS and PMOS devices were surrounded by a guard ring of vias from the substrate to metal 1. In addition, an inner ring of vias from n-well to metal 1 was placed around the PMOS devices. This helps to prevent the possibility of latch-up between the n-well and substrate.

The capacitor was implemented as a plate capacitor from metal 1 to top metal, with dimensions 120um x 123.44um, to equal 10pF. The capacitor was also surrounded by a guard ring between metal 1 and the substrate.

Results

The schematic of the two stage op amp is shown below in Figure 2. Dummies are included in the schematic.

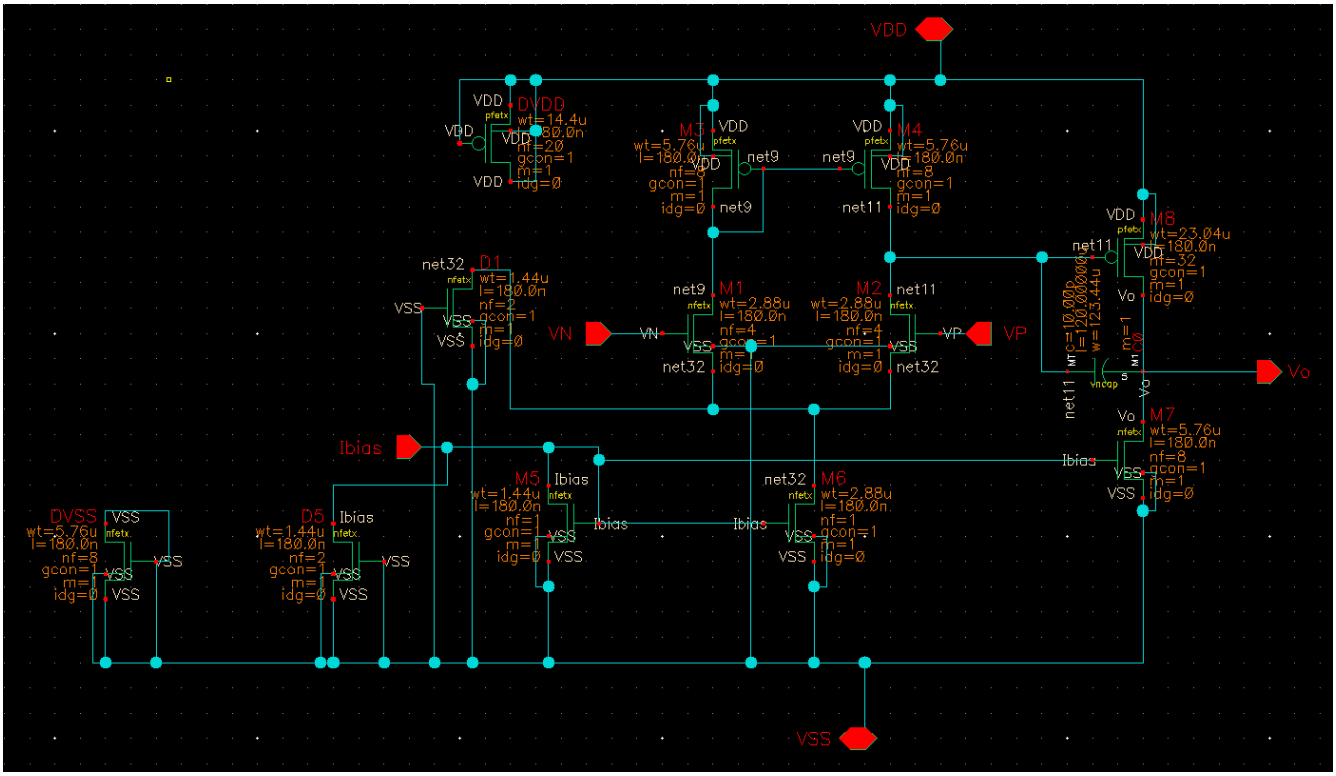

Figure 2: Schematic

From here, the layout of the PMOS devices was completed (Figure 3). The source of the devices was routed on metal 1, while the drains were routed on metal 2. The two guard rings as discussed previously were also implemented.

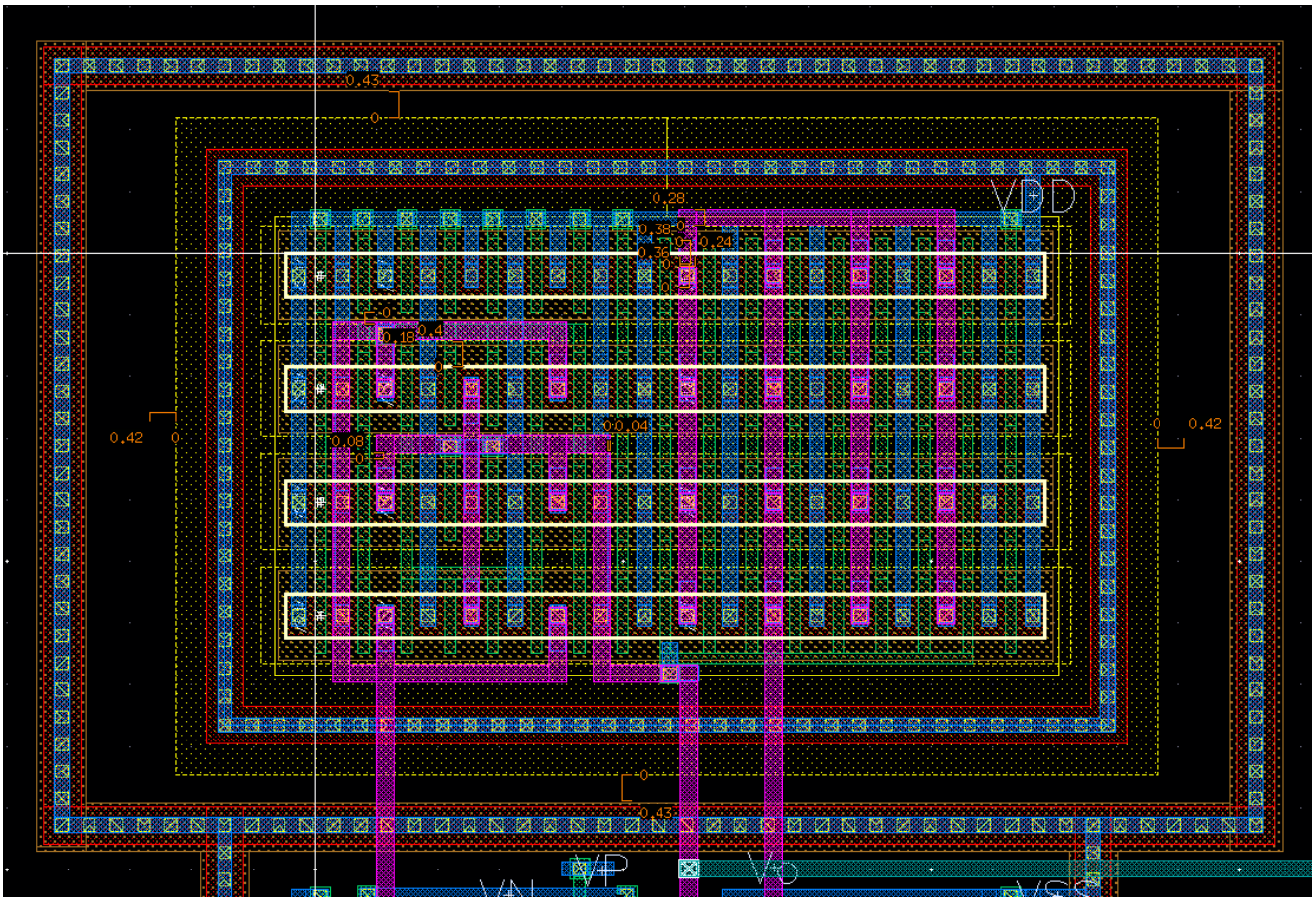

Figure 3: PMOS Devices

Next, the layout of the NMOS devices was completed (Figure 4). Three levels of metal were used, where metal 1 was primarily connected to the sources of the devices, and metals 2 and 3 were used as interconnects. Connections to the PMOS devices and capacitor were completed on metal 2 and metal 3.

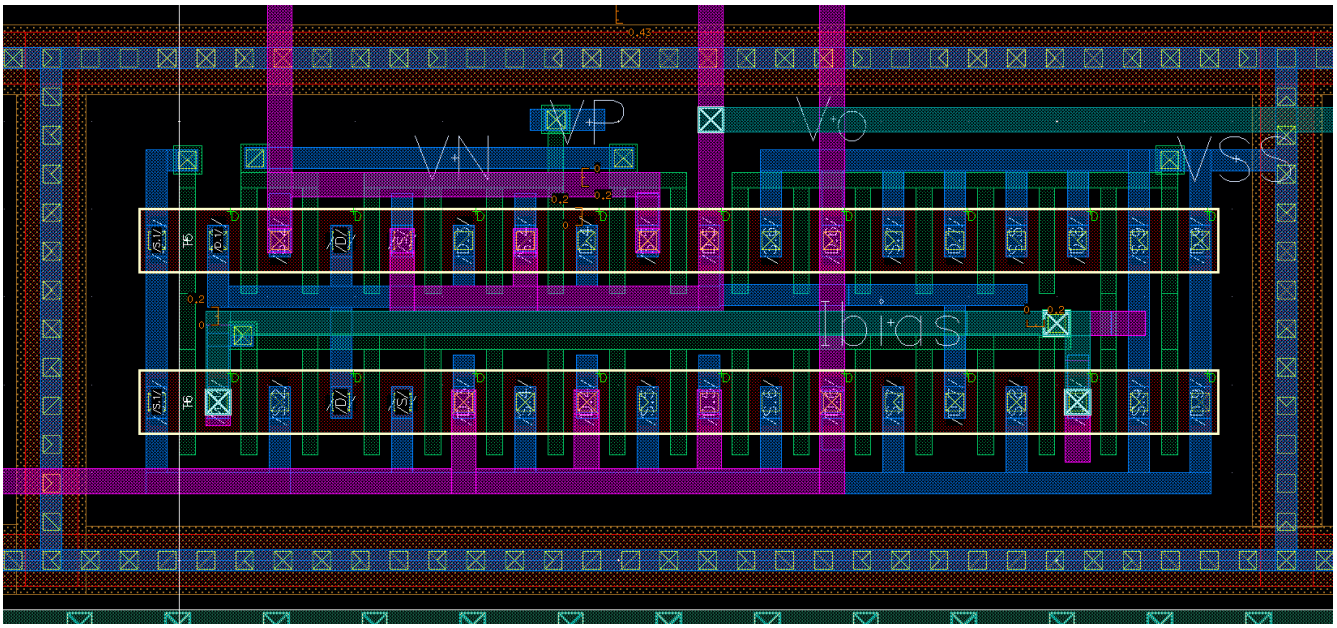

Figure 4: NMOS Devices

Next, the capacitor was placed below the transistors and encapsulated with a guard ring from metal 1 to substrate. The guard ring was connected to the outer ring around the transistors (Figure 5). The layout including the capacitor is shown in Figure 6.

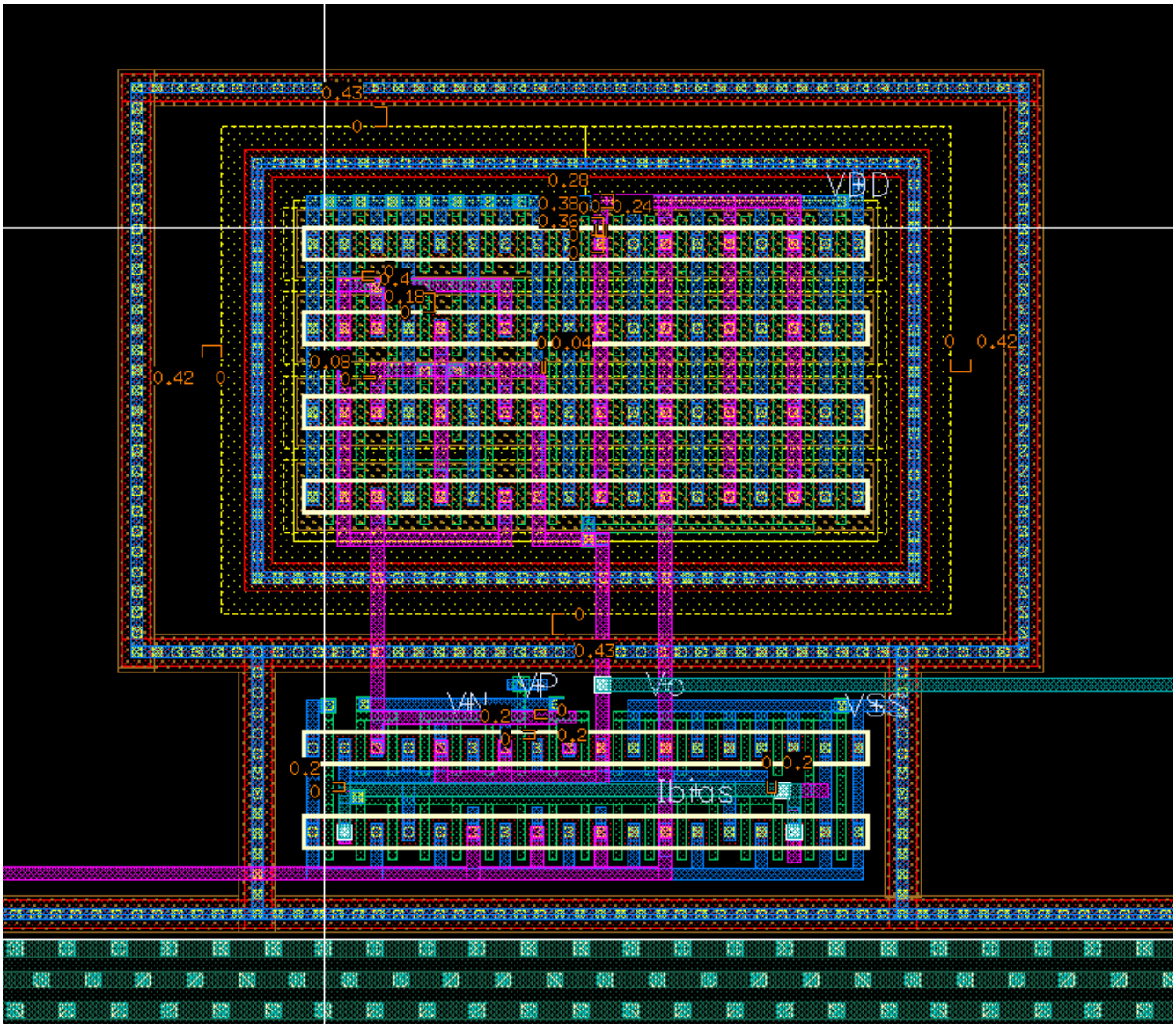

Figure 5: Transistor Block

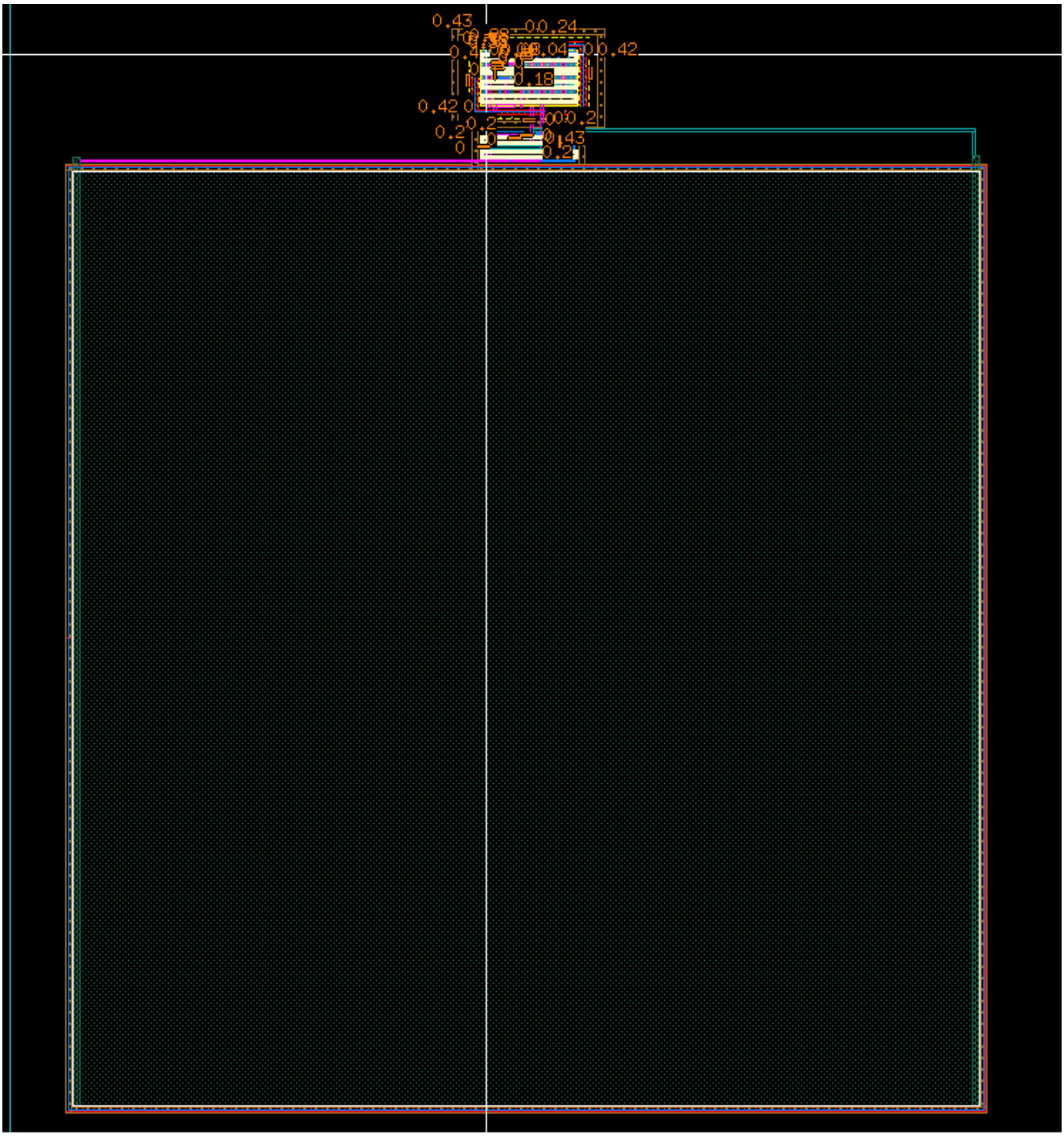

Figure 6: Full Layout

Finally, with the layout done and labels created for each pin, a final DRC and LVS check was completed successfully (Figure 7, 8).

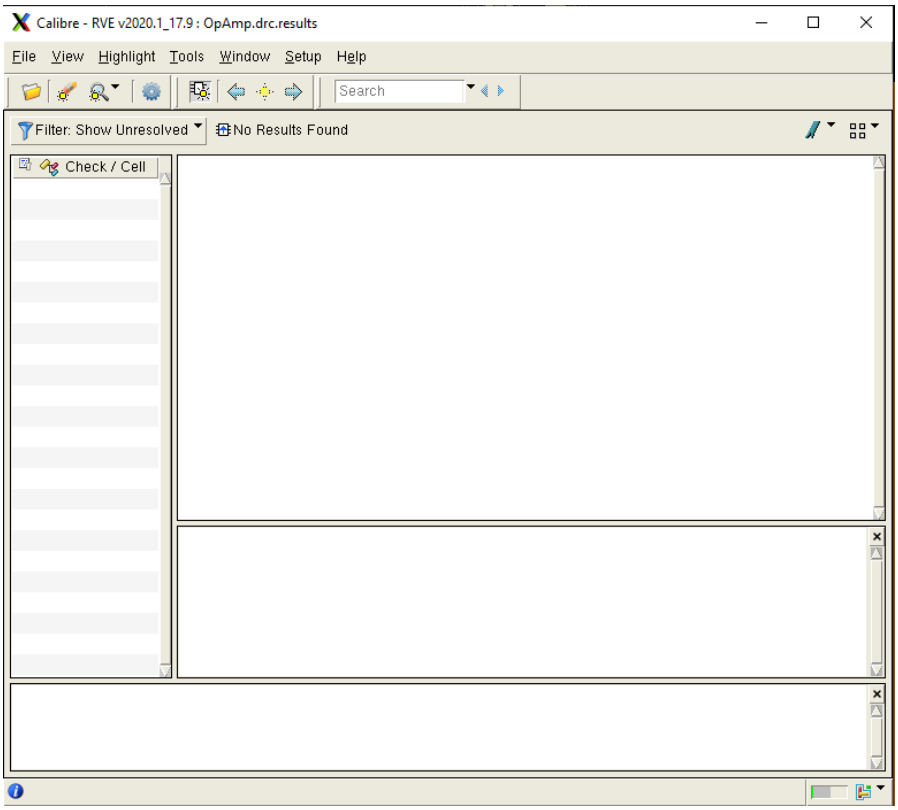

Figure 7: DRC

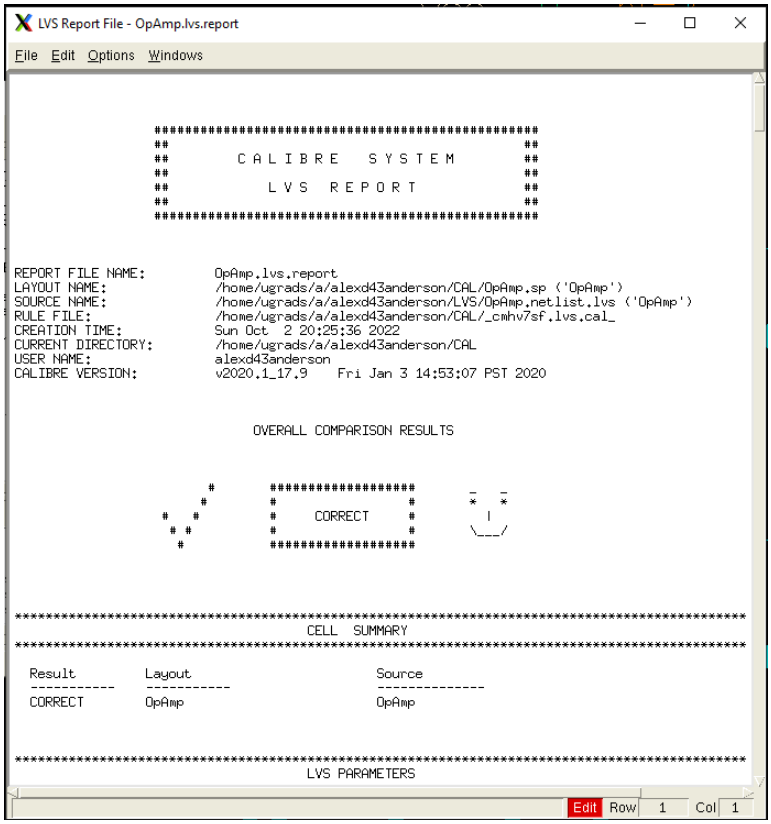

Figure 8: LVS Check

Discussion

The use of guard rings is very important to prevent unwanted substrate noise, especially in extremely sensitive analog blocks. By surrounding transistors with a ring of vias connected to the low supply of the circuit, substrate noise can be prevented by providing a low impedance path to low potential.

The use of two types of guard rings for PMOS devices both reduces substrate noise and ensures that latch-up will not occur between the n-well and substrate.

Conclusion

In this lab, guard ring layout techniques were applied to a two stage op amp. Previously discussed techniques including common centroid design and dummy elements were also used.