Lab 1: Introduction to Cadence and MOS Device Characterization

ECEN 704-601
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Description

In this lab, characterization of fundamental MOS devices was performed. The intrinsic properties and parameters were determined using simulation tools within Cadence. A fundamental PMOS and NMOS device was characterized for various different transistor lengths and widths. The use of these parameters will be vital in hand calculations for future designs.

Design

For each MOS device, a variety of parameters were extracted from the I-V curves. First, from the I_D - V_{GS} curve, μC_{ox} , V_t , and θ were extracted from the curve. All of the mentioned parameters can be extracted from the curve of the transconductance, g_m , versus the gate-source voltage. The transconductance can be found using its fundamental relation to the drain current

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Extraction of the above parameters can be obtained using the relations summarized below in Figure 1.

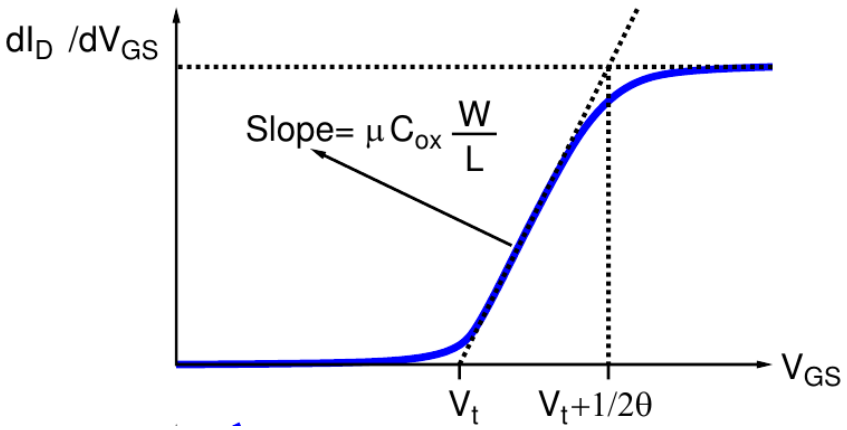


Figure 1: ID vs. VGS Parameter Extraction

Next, from the I_D - V_{DS} curve, the channel modulation parameter λ can be extracted from the active region as

$$\lambda \simeq \frac{\partial I_D}{\partial V_{DS}} / I_D \Big|_{V_{DS}=V_{DS,sat}}$$

In this case, we will take $V_{DS,sat}=1V$.

Finally, to extract the intrinsic gain A_i and the unity-gain frequency f_t , the AC output in a common-drain configuration with sufficient drain current bias is measured with respect to the AC input magnitude. The bias voltages are set as

$$V_{GS}=V_t+50mV+\frac{1}{4\theta}$$

$$V_{DS}=1V$$

and the drain current is set accordingly as determined from the previously found I-V plots. The schematic used to characterize each device is included below for both NMOS (Figure 2) and PMOS (Figure 3).

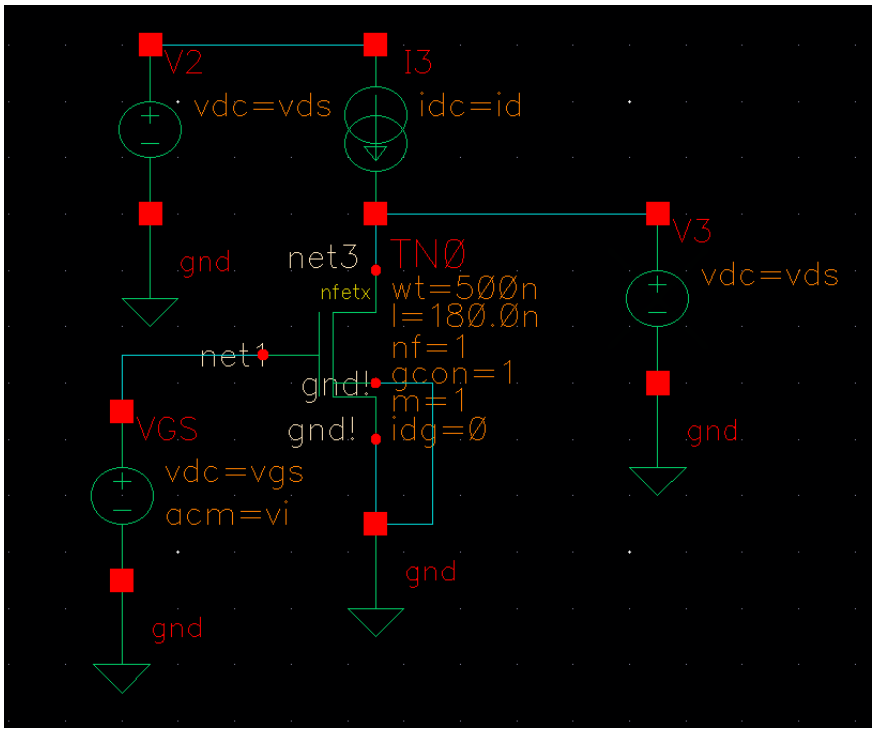


Figure 2: NMOS Characterization Schematic

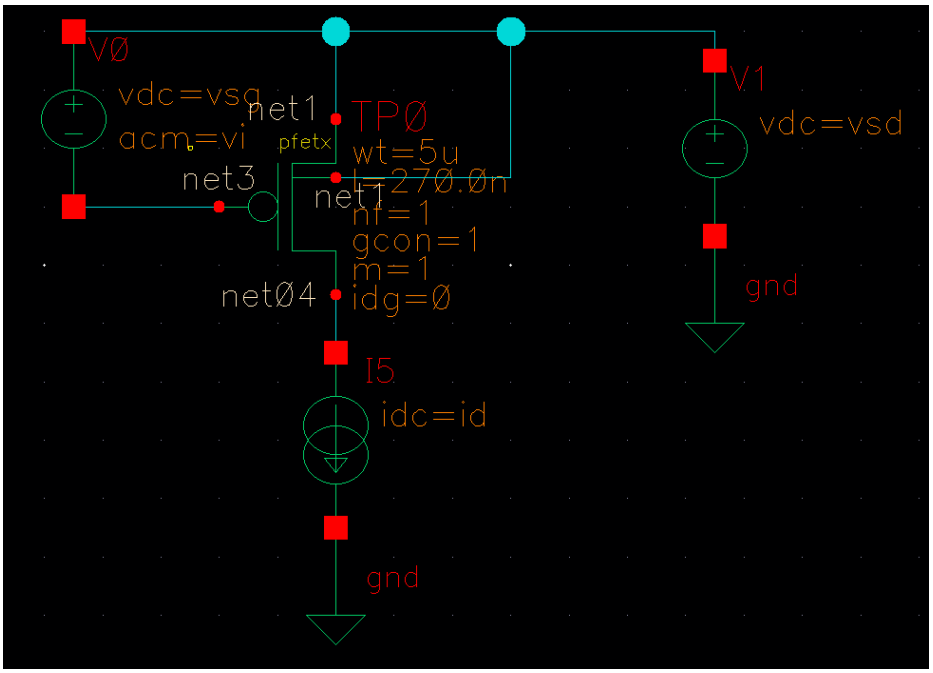


Figure 3: PMOS Characterization Schematic

Results

The summary of parameters collected is summarized below in Table 1 for the NMOS device and Table 2 for the PMOS device.

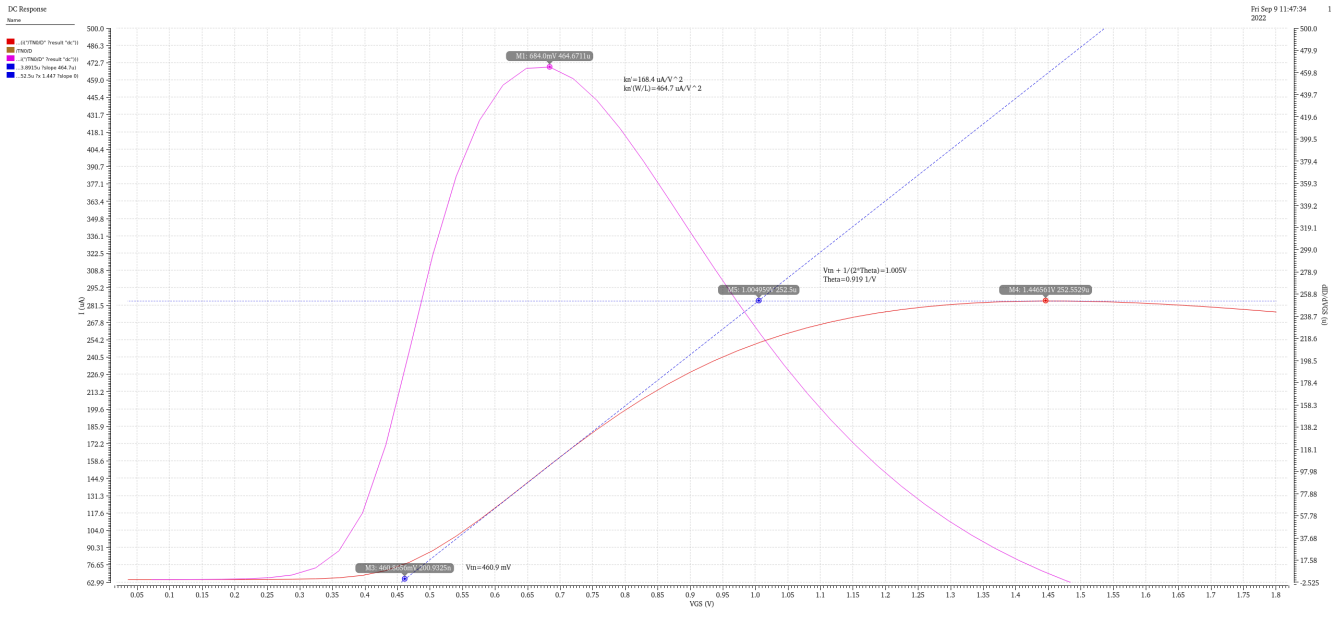
Table 1: NMOS Device Parameters

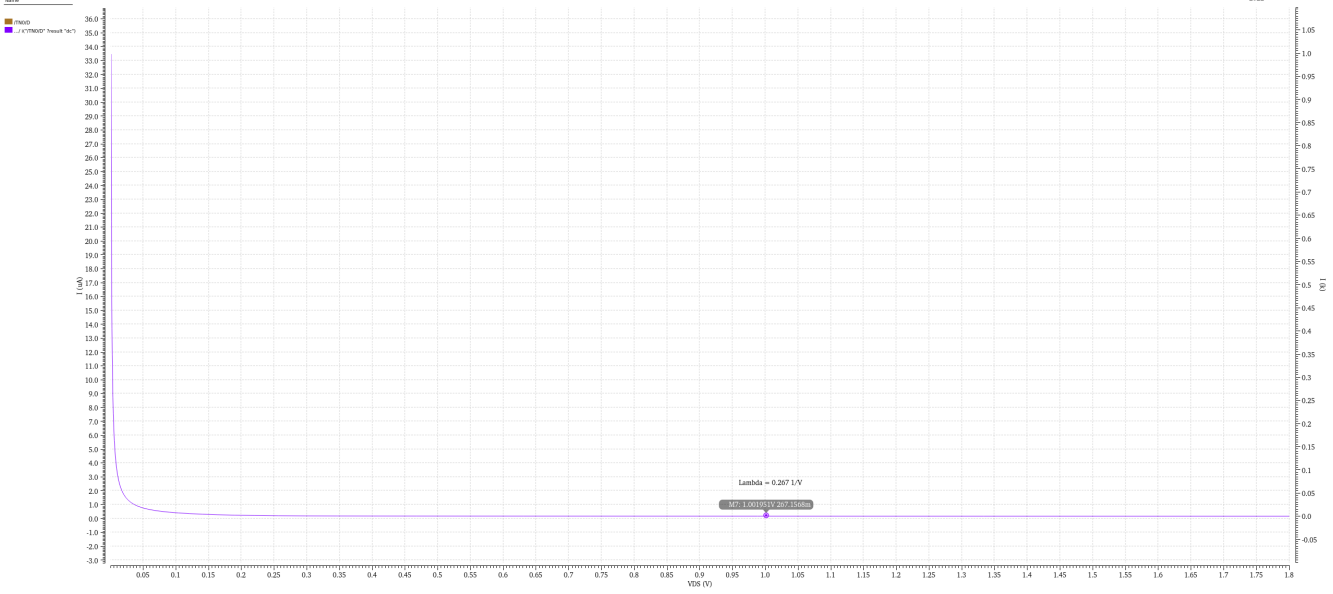
Parameter	W/L = 0.5µ / 0.18µ	W/L = 5µ / 0.18µ	W/L = 5µ / 0.27µ
V_{tn}	460.9 mV	460.6 mV	451.4 mV
$\mu_n C_{ox}$	168.4 $\mu A/V^2$	217.2 $\mu A/V^2$	214.33 $\mu A/V^2$
θ	0.919 1/V	1.293 1/V	0.998 1/V
λ	0.267 1/V	0.611 1/V	0.188 1/V
A_i	21.012 V/V	29.713 V/V	46.202 V/V
f_t	50.48 GHz	51.12 GHz	48.66 GHz

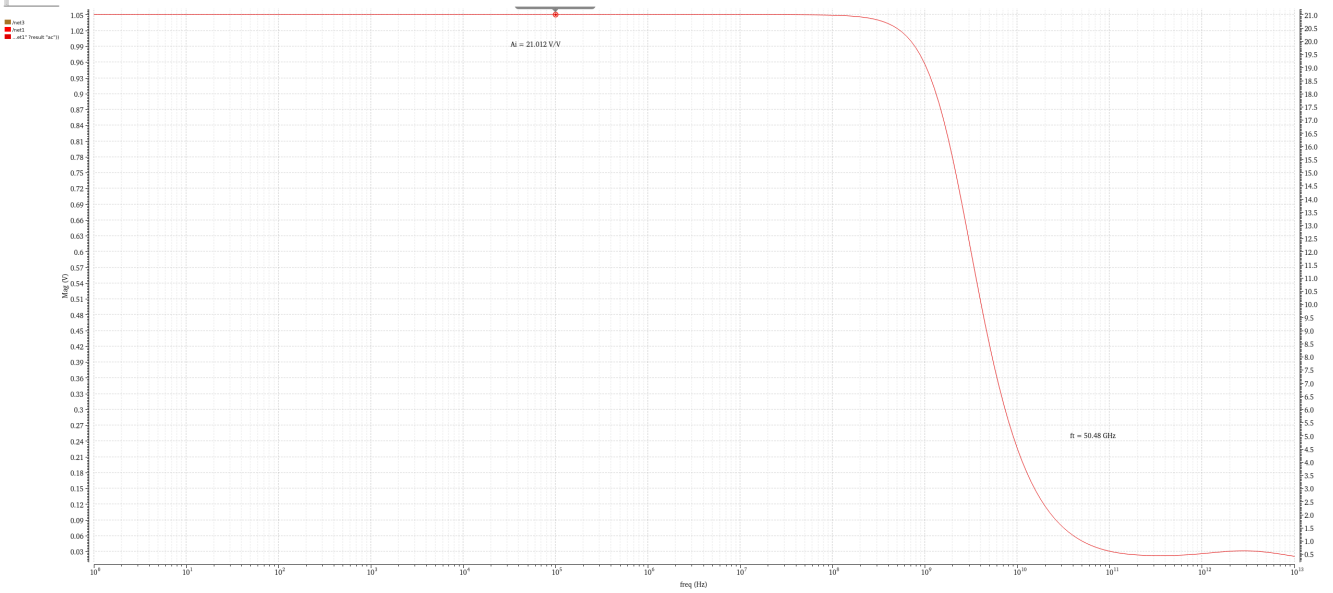
Table 2: PMOS Device Parameters

Parameter	W/L = 0.5µ / 0.18µ	W/L = 5µ / 0.18µ	W/L = 5µ / 0.27µ
V_{tp}	-433.1 mV	-414.1 mV	-421.6 mV
$\mu_p C_{ox}$	47.37 $\mu A/V^2$	56.495 $\mu A/V^2$	47.528 $\mu A/V^2$
θ	0.747 1/V	0.775 1/V	0.653 1/V
λ	0.295 1/V	0.298 1/V	0.164 1/V
A_i	18.687 V/V	16.958 V/V	27.4154 V/V
f_t	58.64 GHz	49.48 GHz	115.8 GHz

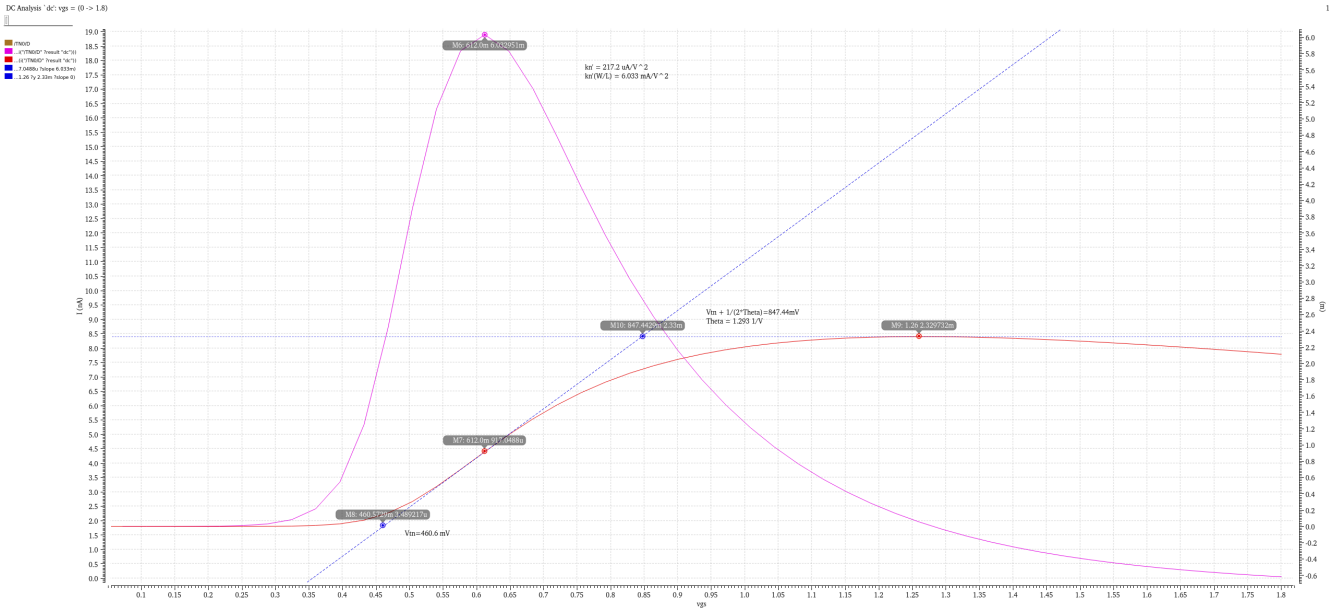
In addition, the simulation plot schematics for each of the above measurements is included below. For the NMOS device with W/L = 0.5µ / 0.18µ:

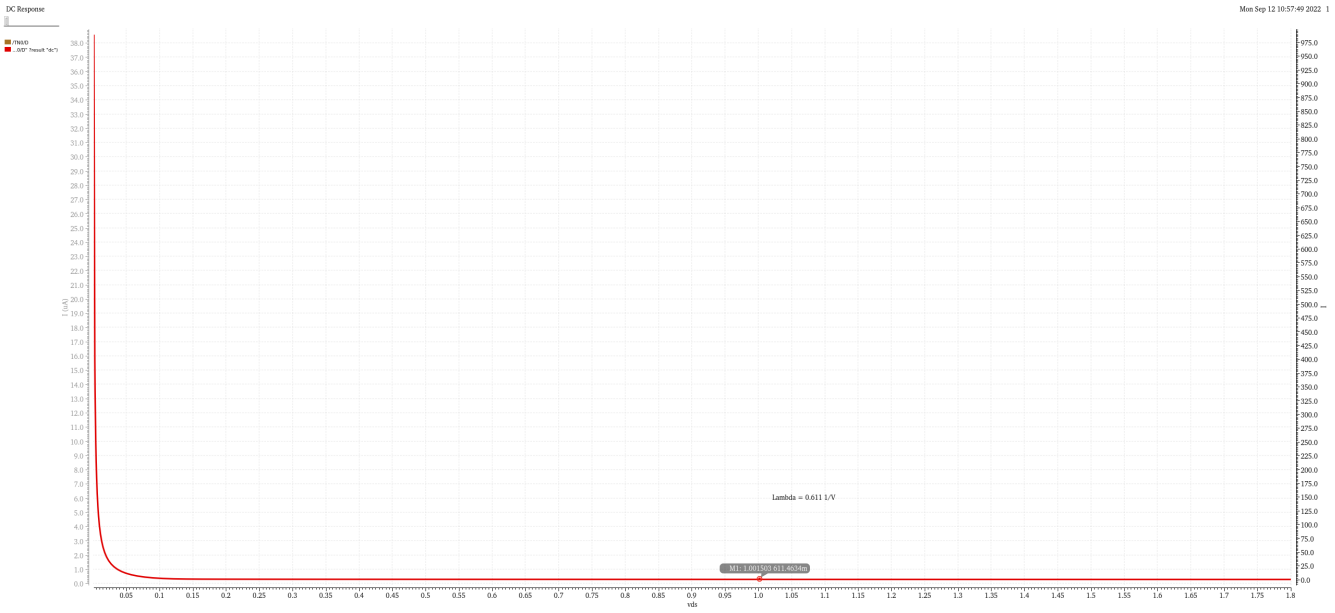


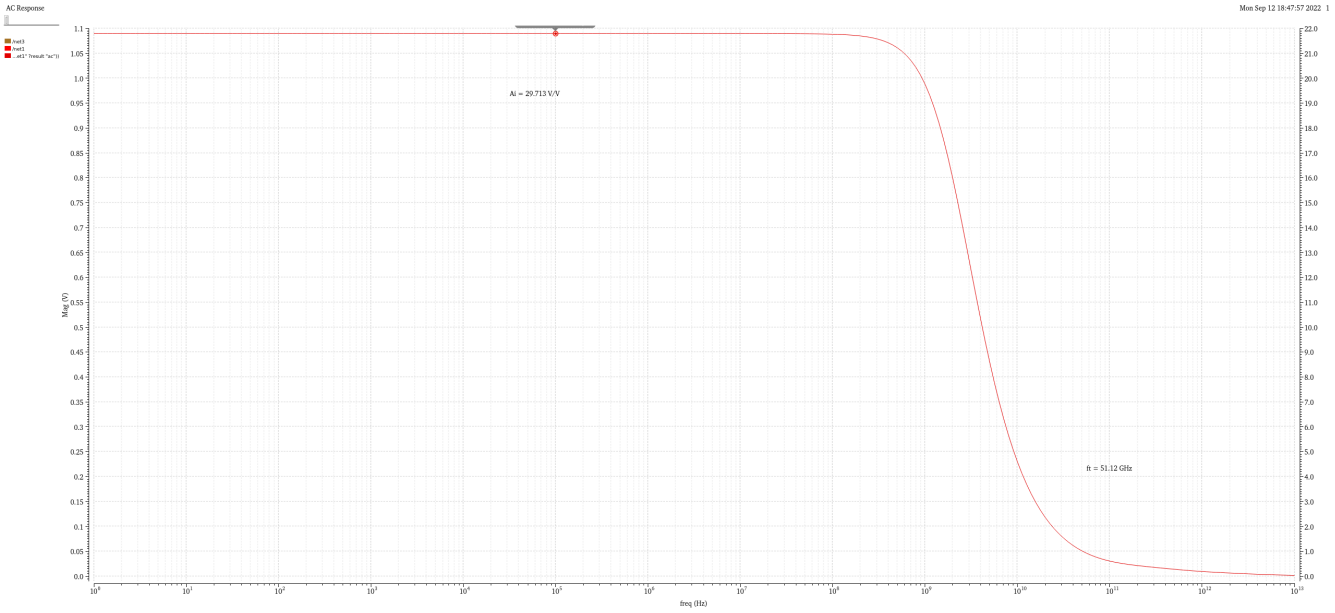

Name
/MN0/D
./ :"/"/MN0/D" ?result "dc")
I (uA)
I (D)
VDS (V)
Lambda = 0.267 1/V
M7: 1.0010810/267.1568m


/out3
/out3
../ac1" ?result "ac")
Ai = 21.012 V/V
ft = 50.48 GHz
Mag (V)
freq (Hz)

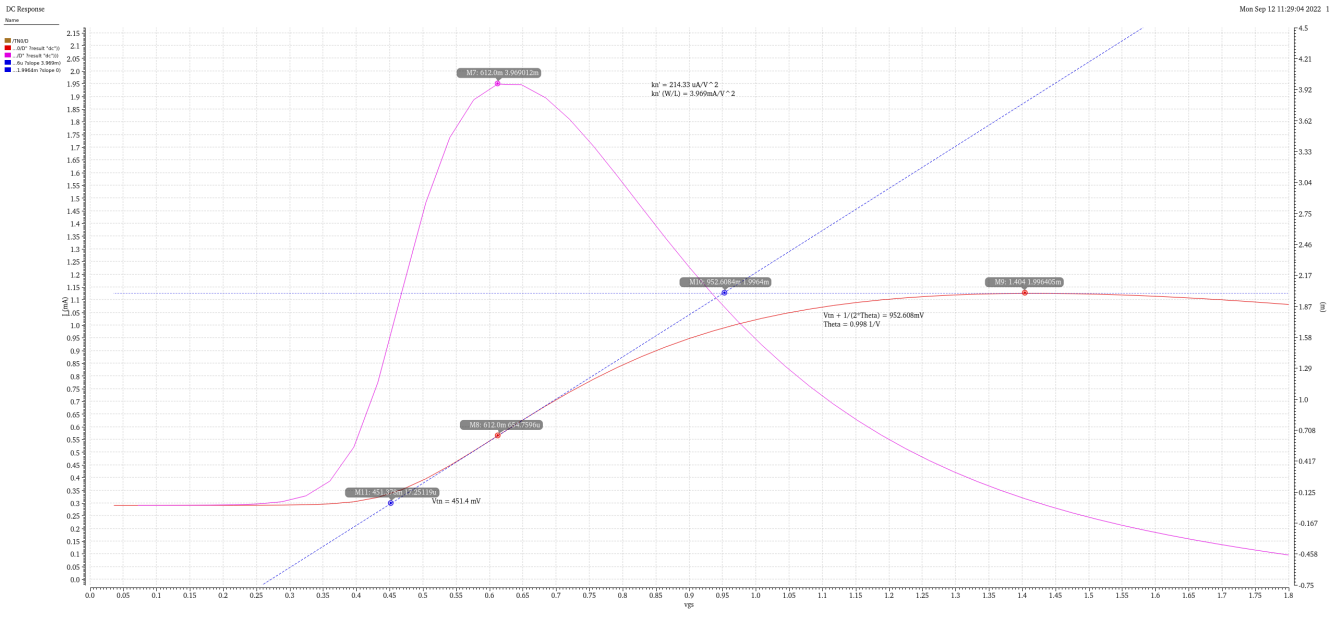
Next, for the NMOS device with W/L = 5µ / 0.18µ:



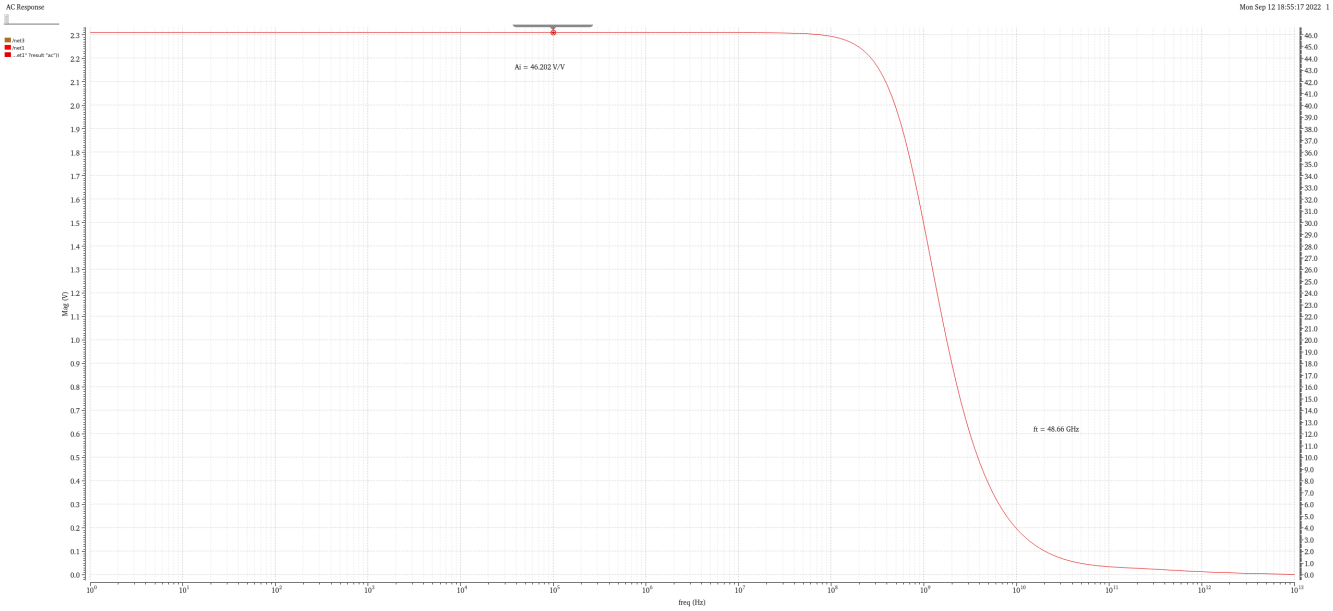




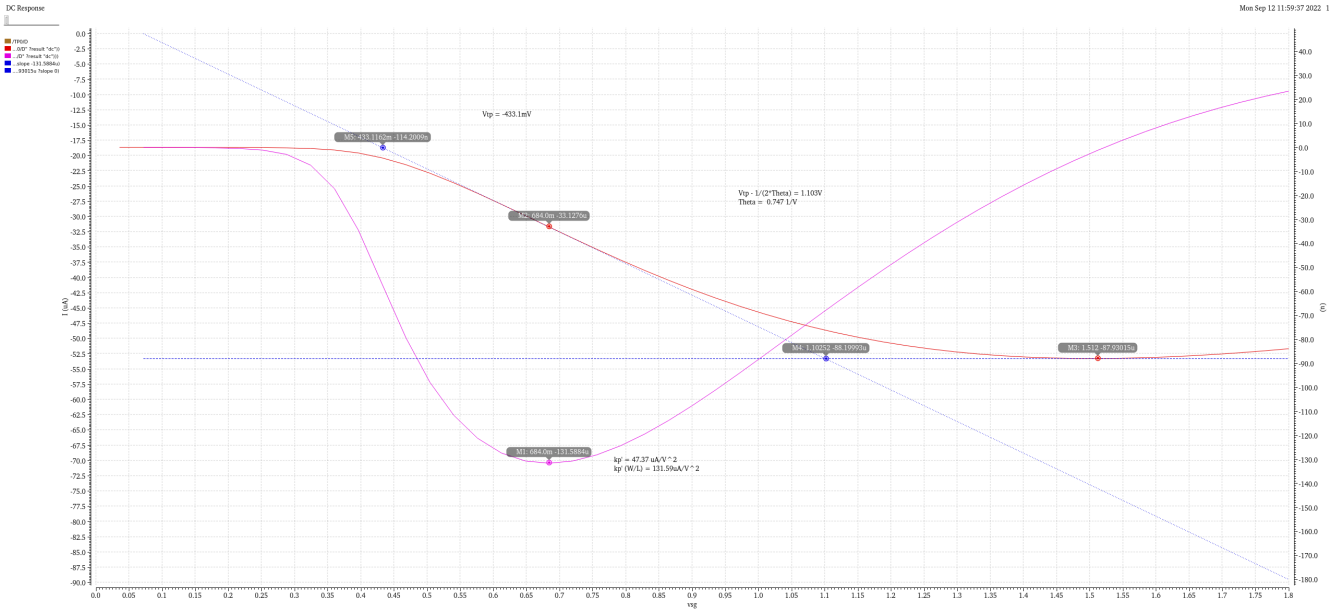
For the NMOS device with W/L = 5µ / 0.27µ:

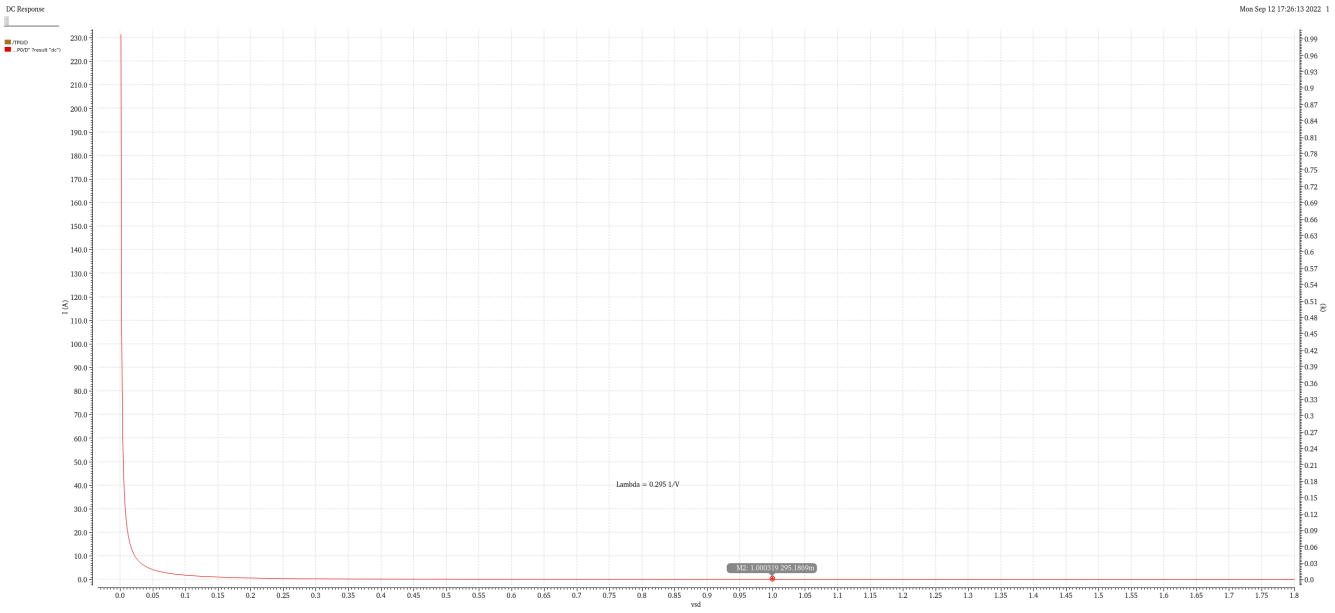


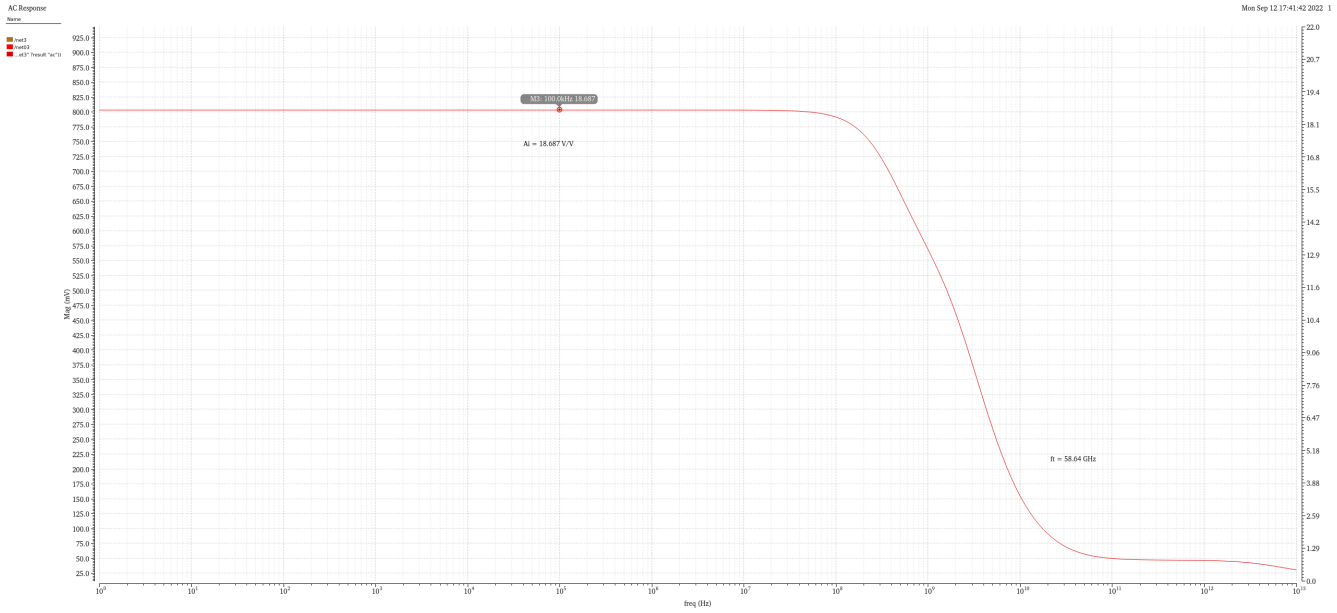

DC Response
Mon Sep 12 11:43:58 2022 1
Name
/M9/D
../0/0" ?result "dc")
I (uA)
(S)
Lambda = 0.188 1/V
M13: 1.000004468 187.8719084m
0.001
0.665754
1.33051
1.99526
vds


AC Response
Mon Sep 12 18:55:17 2022 1
/out3
/out3
../ac1" ?result "ac")
Ai = 46.202 V/V
ft = 48.66 GHz
Mag (V)
freq (Hz)

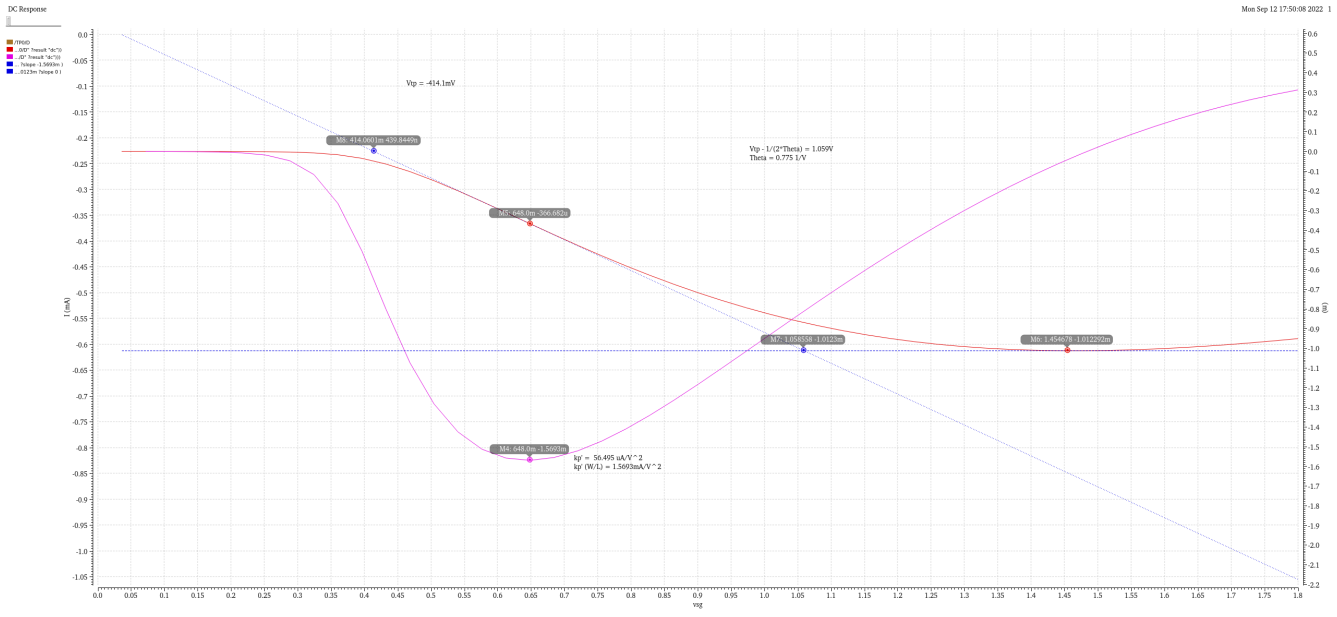
Next, for the PMOS device with W/L = 0.5µ / 0.18µ:

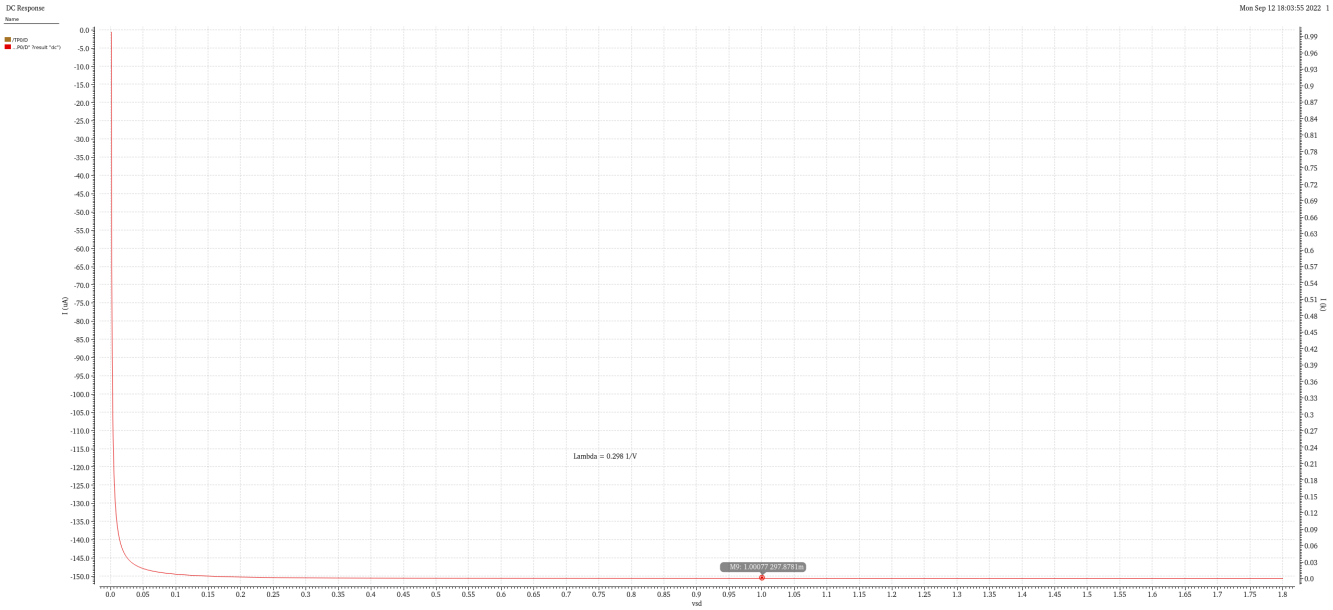


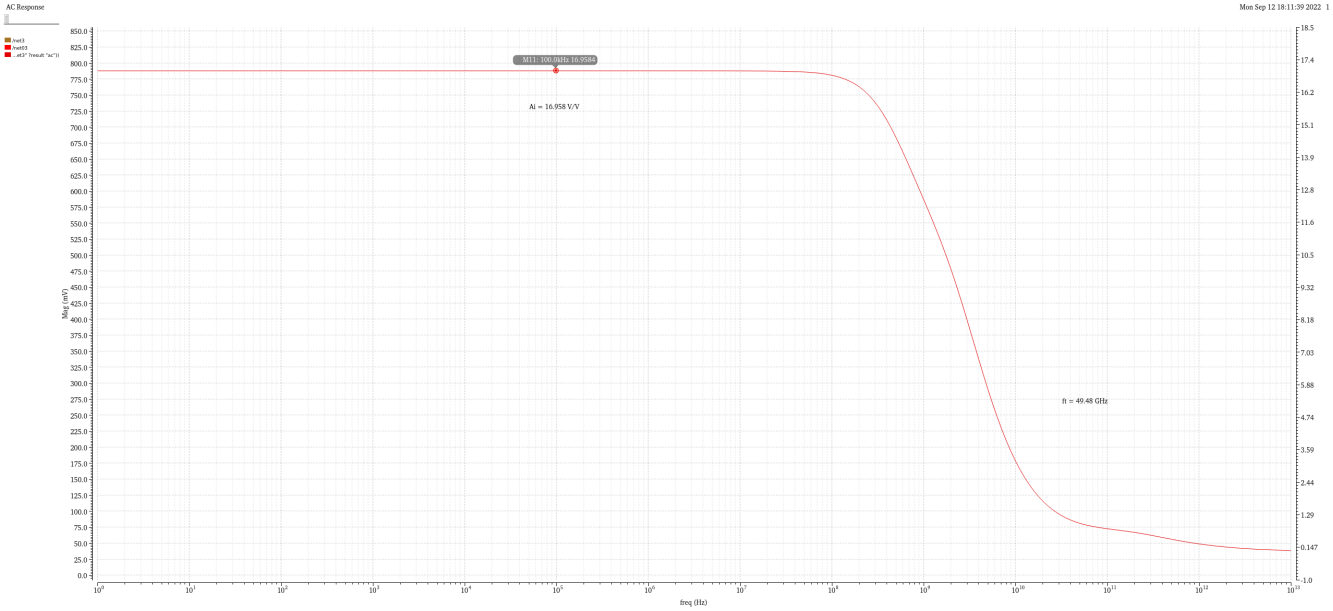




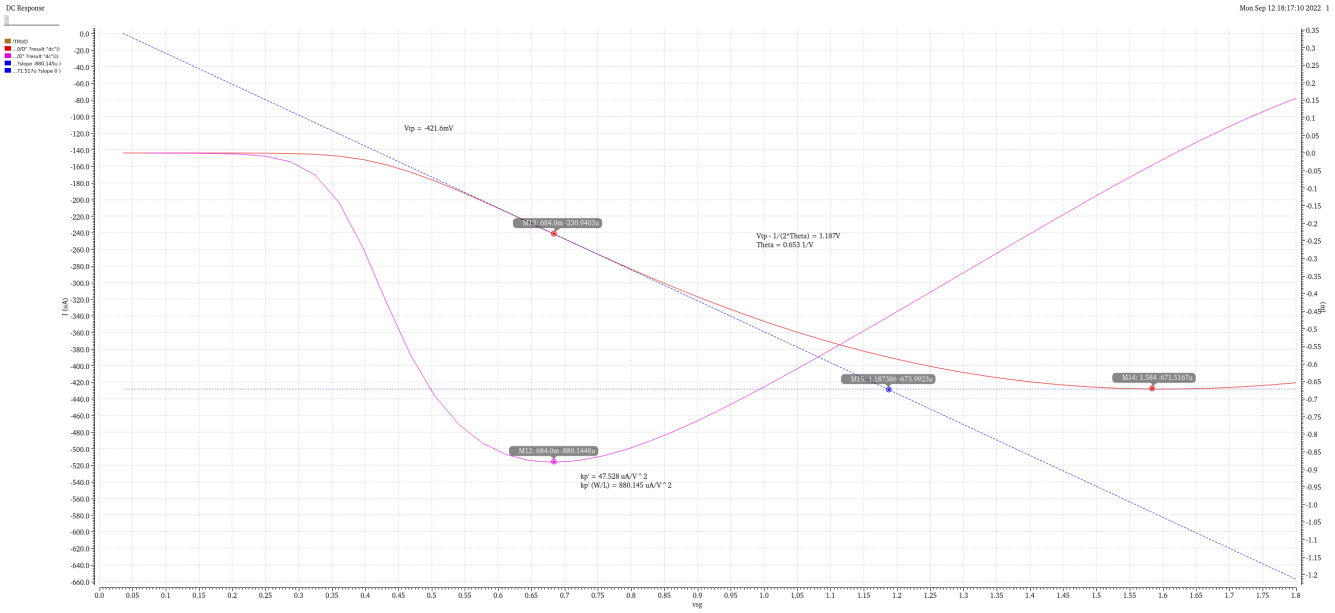
For the PMOS device with W/L = 5µ / 0.18µ:

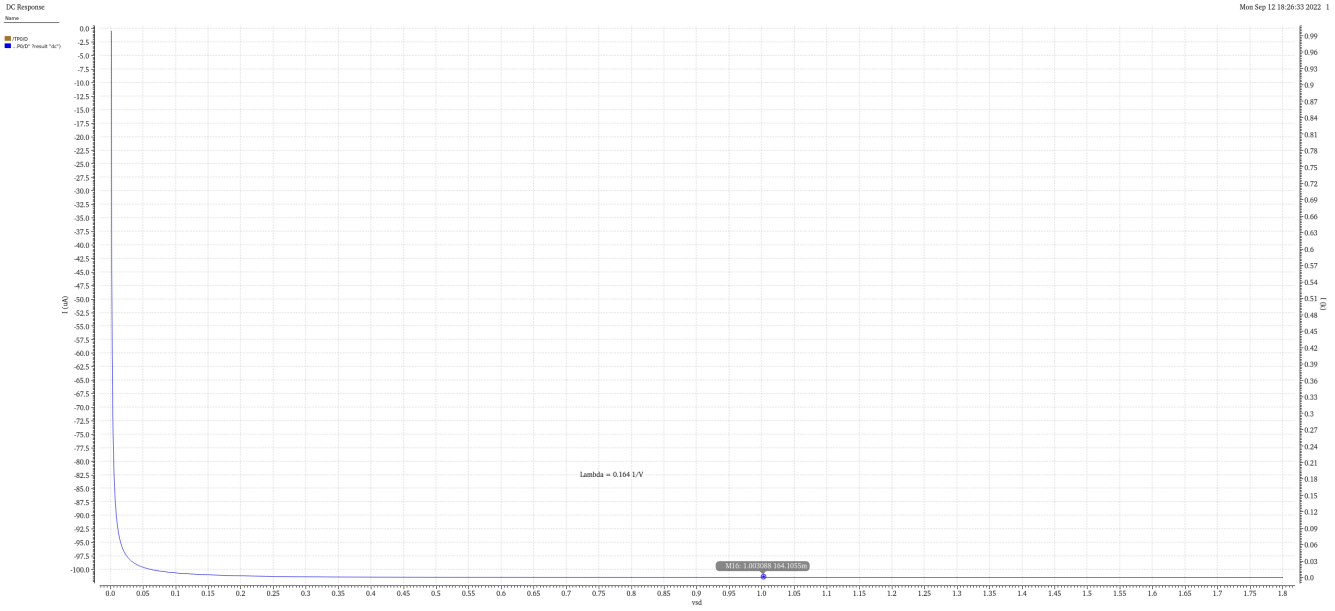


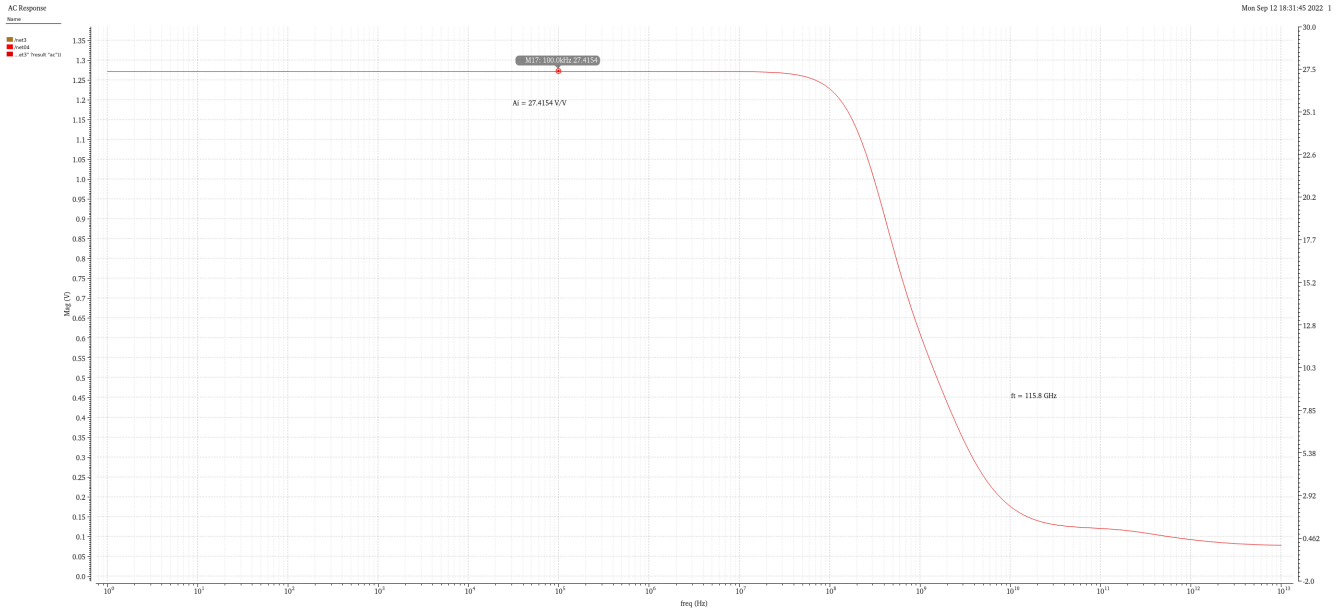

DC Response
Mon Sep 12 18:03:55 2022 1
Name
/TPOD
/PO/D" ?result "dc")
I (uA)
Lambda = 0.298 1/V
M9: 1.00077 297.878 n
vsd
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
-45.0
-50.0
-55.0
-60.0
-65.0
-70.0
-75.0
-80.0
-85.0
-90.0
-95.0
-100.0
-105.0
-110.0
-115.0
-120.0
-125.0
-130.0
-135.0
-140.0
-145.0
-150.0
0.99
0.96
0.93
0.9
0.87
0.84
0.81
0.78
0.75
0.72
0.69
0.66
0.63
0.6
0.57
0.54
0.51
0.48
0.45
0.42
0.39
0.36
0.33
0.3
0.27
0.24
0.21
0.18
0.15
0.12
0.09
0.06
0.03
0.0
0.0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.65
0.7
0.75
0.8
0.85
0.9
0.95
1.0
1.05
1.1
1.15
1.2
1.25
1.3
1.35
1.4
1.45
1.5
1.55
1.6
1.65
1.7
1.75
1.8


AC Response
Mon Sep 12 18:11:39 2022 1
/out3
/out03
...st2" ?result "ac")
Mag (mV)
M11: 100.0 Hz 16.9584
Ai = 16.958 V/V
ft = 49.48 GHz
freq (Hz)
850.0
825.0
800.0
775.0
750.0
725.0
700.0
675.0
650.0
625.0
600.0
575.0
550.0
525.0
500.0
475.0
450.0
425.0
400.0
375.0
350.0
325.0
300.0
275.0
250.0
225.0
200.0
175.0
150.0
125.0
100.0
75.0
50.0
25.0
0.0
18.5
17.4
16.2
15.1
13.9
12.8
11.6
10.5
9.32
8.18
7.03
5.88
4.74
3.59
2.44
1.29
0.147
-1.0
10^{9}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
10^{7}
10^{8}
10^{9}
10^{10}
10^{11}
10^{12}
10^{13}

And finally, for the PMOS device with W/L = 5µ / 0.27µ:







Discussion

For both the NMOS and PMOS devices of various lengths, the threshold voltage stayed relatively consistent, around 460mV for the NMOS devices and -425mV for the PMOS devices. This is expected as the threshold voltage is relatively independent of transistor size and dependent on transistor material properties such as the dielectric constant or doping density.

Similarly, the value of μC_{ox} stayed relatively consistent over transistor size variations, about 200 $\mu A/V^2$ for the NMOS devices and 50 $\mu A/V^2$ for the PMOS devices. This consistency is once again expected since both the permeability oxide capacitance are material parameters independent of transistor size. There was some variations that can be attributed to simulation errors or imperfect approximations for determining the value.

Theta, another material property, was approximately constant over transistor size variations as well, about 1 1/V for the NMOS devices and 0.7 1/V for the PMOS devices.

In contrast, the value of lambda varied with a change in the transistor length. With an increased length, the value of lambda decreased, which is expected given its inverse relation to L.

As expected, the intrinsic gain increased significantly as L was increased and remained relatively the same with increased W. The unity-gain frequency decreased as L increased for the NMOS device as expected, but due to some sort of simulation or calculation error, appears to be higher for the PMOS device. Despite this outlier, the frequency behaves as expected.

Conclusion

In this lab, the fundamental parameters of NMOS and PMOS devices at various transistor areas were extracted for the 180nm IBM process. The use of these parameters will be vital in future hand calculations of circuits and is necessary to understand the operation of devices in this design kit.