Lab 4: Design & Simulation of 1-bit Adder

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ECEN 714-603

Post layout verification was first done for the inverter, NAND2, and XOR cells. Changes were made to all gates to optimize the delay.

Inverter:

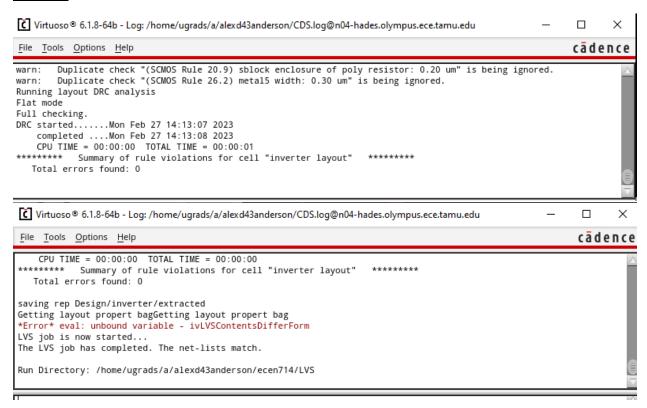


Figure 1: Inverter DRC and LVS

■ FALLING RISING POWER ×						
time (s)	FALLING (s)	time (s)	RISING (s)	Expression	Value	
3.050E-9	256.2E-12	8.150E-9	263.2E-12	POWER	11.37E-6	
15.05E-9	256.2E-12	20.15E-9	263.2E-12			
27.05E-9	256.2E-12					

Figure 2: Inverter Transient Data

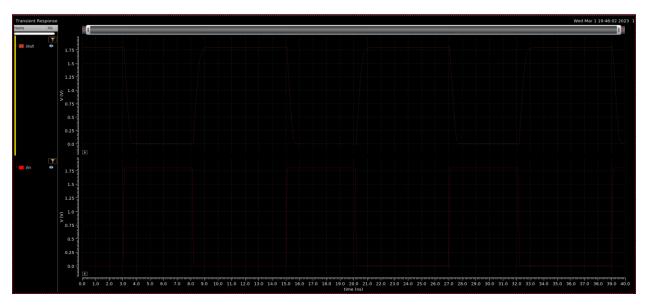


Figure 3: Inverter Waveform

NAND2:

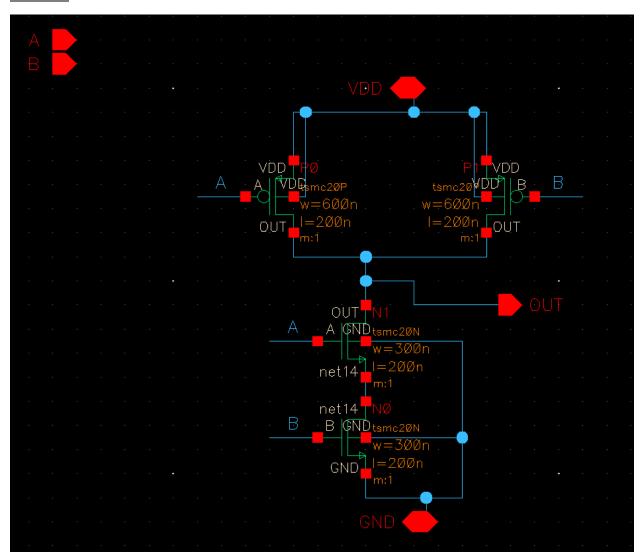


Figure 4: NAND2 Schematic

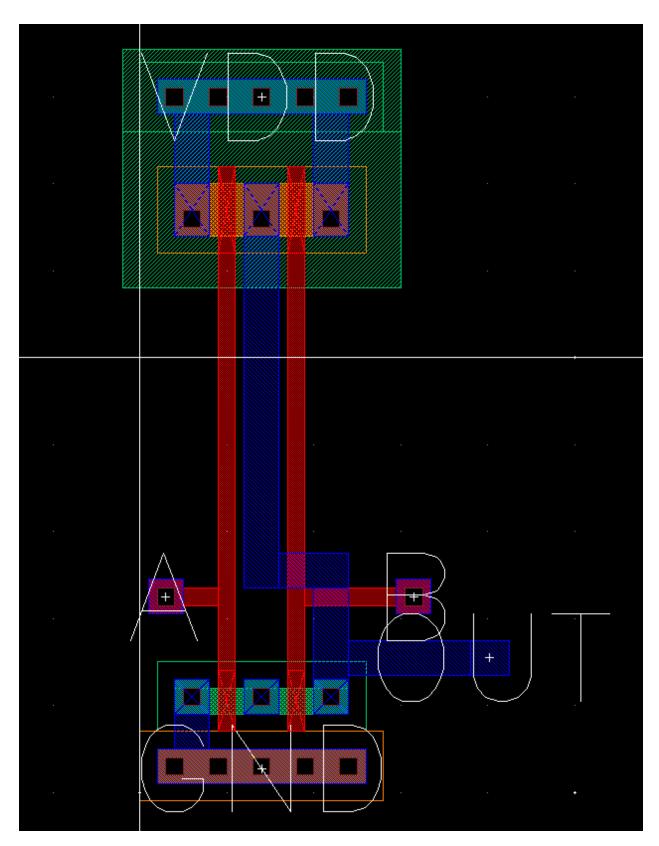


Figure 5: NAND2 Layout

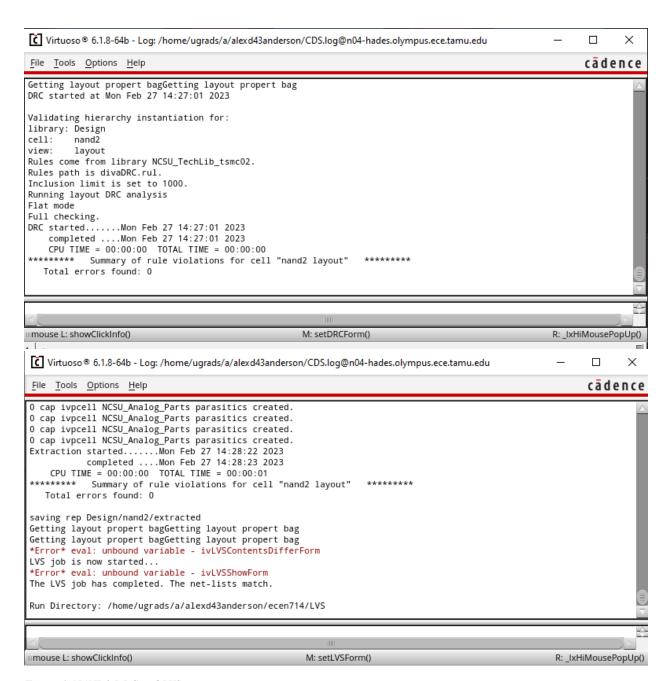


Figure 6: NAND2 DRC and LVS

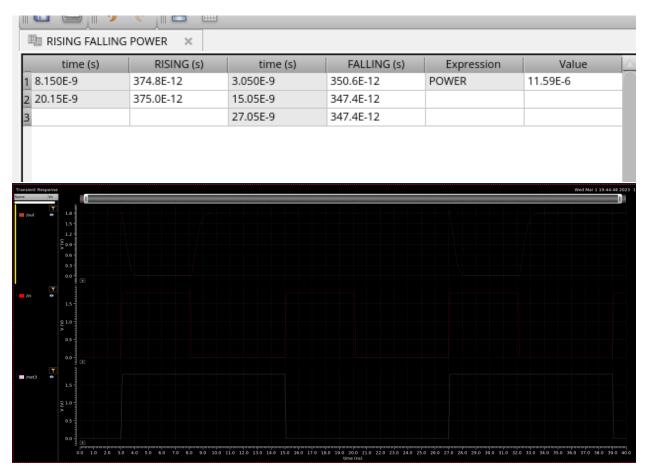


Figure 7: NAND2 Transient Data and Waveform

XOR2:

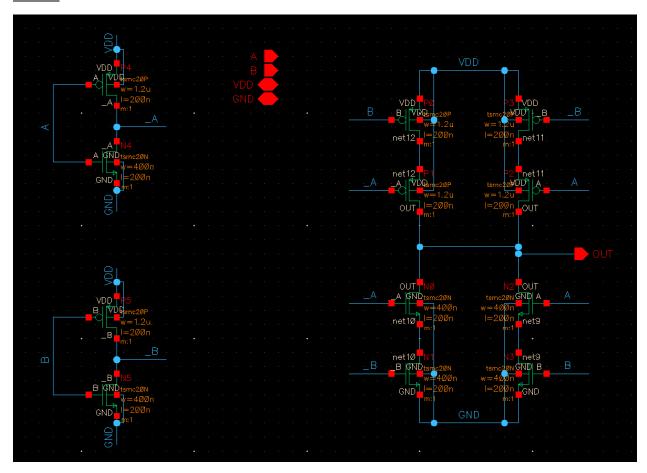


Figure 8: XOR2 Schematic

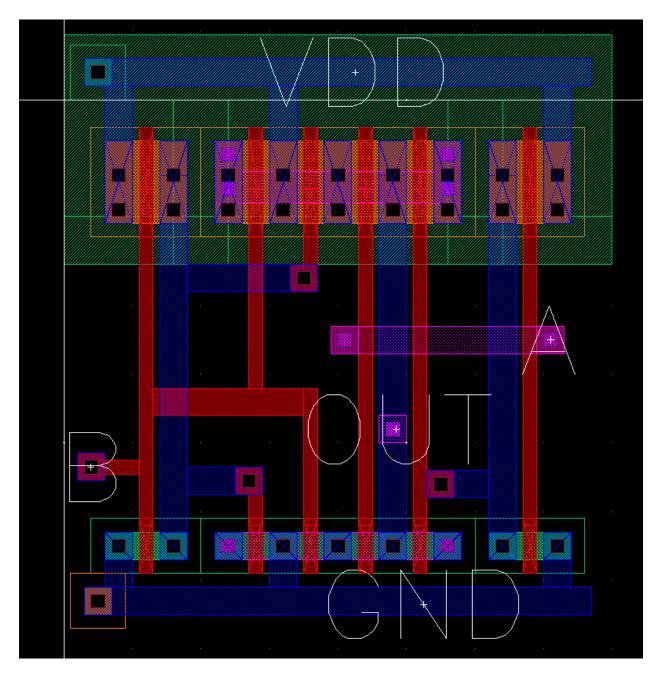


Figure 9: XOR2 Layout

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(Virtuoso® 6.1.8-64b - Log: /home/ugrads/a/alexd43anderson/CDS.log@n04-hades.olympus.ece.tamu.edu
                                                                                                                              Х
 File Tools Options Help
                                                                                                                             cādence
 Getting layout propert bagGetting layout propert bag
 DRC started at Mon Feb 27 14:59:44 2023
 Validating hierarchy instantiation for:
 library: Design
 cell:
           xor2
 view:
           layout
 Rules come from library NCSU_TechLib_tsmc02.
 Rules path is divaDRC.rul.
 Inclusion limit is set to 1000.
 Running layout DRC analysis
 Flat mode
 Full checking.
 DRC started......Mon Feb 27 14:59:44 2023
     completed ....Mon Feb 27 14:59:44 2023
      CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
  ******** Summary of rule violations for cell "xor2 layout"
    Total errors found: 0
                                                              M: setDRCForm()
                                                                                                                      R: _lxHiMousePopUp()
 mouse L: showClickInfo()
                                                                                                                                     \times
 (Virtuoso® 6.1.8-64b - Log: /home/ugrads/a/alexd43anderson/CDS.log@n04-hades.olympus.ece.tamu.edu
                                                                                                                             File Tools Options Help
                                                                                                                             cādence
nmos4 (instance "N3", library "NCSU_Analog_Parts")
 pmos4 (instance "P1", library "NCSU_Analog_Parts")
 pmos4 (instance "P2", library "NCSU_Analog_Parts")
 pmos4 (instance "PO", library "NCSU_Analog_Parts")
pmos4 (instance "P3", library "NCSU_Analog_Parts")
INFO (SCH-1170): Extracting "xor2 schematic"
INFO (SCH-1426): Schematic check completed with no errors.
Getting schematic propert bagGetting schematic propert bagINFO (SCH-1181): "Design xor2 schematic" saved. INFO (SCH-1170): Extracting "xor2 schematic" INFO (SCH-1426): Schematic check completed with no errors.
 Getting schematic propert bagGetting schematic propert bagINFO (SCH-1181): "Design xor2 schematic" saved.
 LVS job is now started...
 The LVS job has completed. The net-lists match.
 Run Directory: /home/ugrads/a/alexd43anderson/ecen714/LVS
mouse L: showClickInfo()
                                                                                                                     R: schHiMousePopUp()
                                                           M: schHiMousePopUp()
1 >
```

Figure 10: XOR2 DRC and LVS

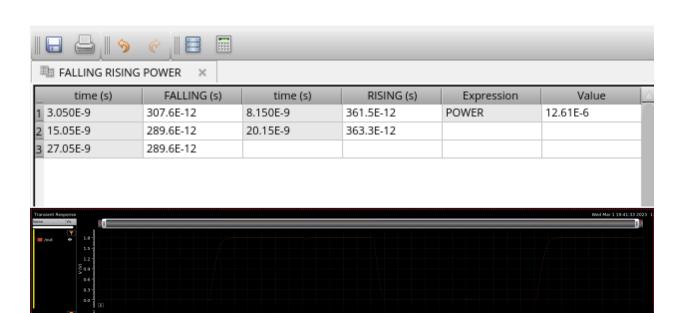


Figure 11: XOR2 Data and Waveform

Now, the 1-bit adder was assembled and tested using all the above blocks. Due to a problem with Cadence, hierarchical design could not be used, so the individual transistors had to be copied into the top cell view (see my post on Piazza for more info).

1-bit adder:

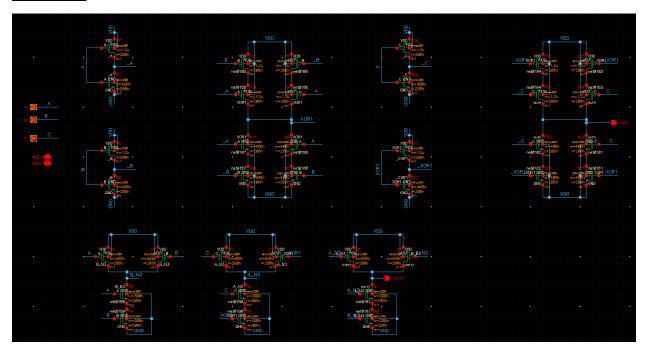


Figure 12: 1-bit Adder Schematic

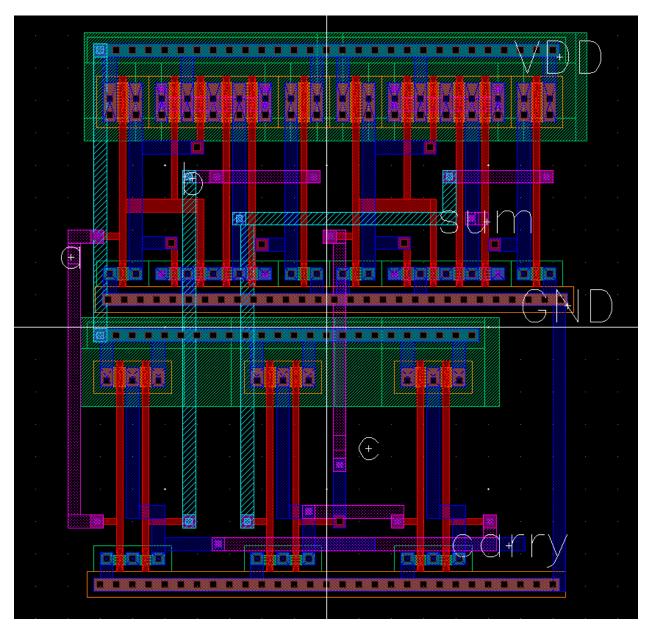


Figure 13: 1-bit Adder Layout

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Virtuoso® 6.1.8-64b - Log: /home/ugrads/a/alexd43anderson/CDS.log@n01-zeus.olympus.ece.tamu.edu
                                                                                                                     cādence
File Tools Options Help
            (SCMOS_SUBM Rule 9.2.b) metal2 spacing: 0.30 um
        1 Total errors found
metal2 drawing -> net: "a" height: 0.50 width: 0.40
Getting layout propert bagGetting layout propert bag
DRC started at Mon Feb 27 22:21:28 2023
Validating hierarchy instantiation for:
library: Design
cell:
         fulladder
view:
         layout
Rules come from library NCSU_TechLib_tsmc02.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started......Mon Feb 27 22:21:28 2023
    completed ....Mon Feb 27 22:21:28 2023
    CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
******* Summary of rule violations for cell "fulladder layout"
   Total errors found: 0
mouse L: showClickInfo()
                                                         M: setDRCForm()
                                                                                                             R: _IxHiMousePopUp()
(home/ugrads/a/alexd43anderson/ecen714/LVS/si.out@n01-zeus.olympus.ece.tamu.edu
                                                                                                                      X
File Edit View Help
                                                                                                                      cādence
@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexd43anderson/ecen714/LVS -l -s -t /home/ug
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...
    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/layout/netlist
      count
       25
                       nets
                       terminals
       18
                       pmos
       18
   Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/schematic/netlist
      count
       25
                       terminals
       18
                       pmos
       18
                       nmos
   Terminal correspondence points
             N13
                       GND
   N21
                       VDD
   N20
             N23
   N19
             N24
                       b
   N18
             N11
                       C
   N23
             N3
                       carry
Devices in the netlist but not in the rules:
       pcapacitor
Devices in the rules but not in the netlist:
       cap nfet pfet nmos4 pmos4
The net-lists match.
                           layout schematic
```

Figure 14: 1-bit Adder DRC and LVS

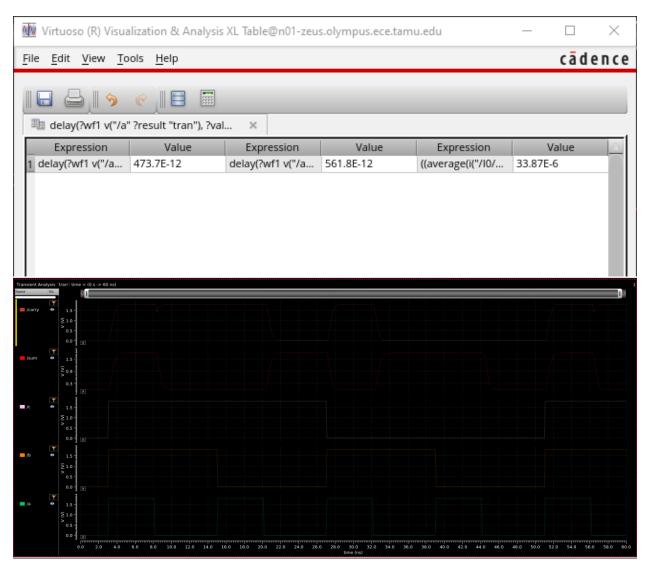


Figure 15: 1-bit Adder Data and Waveform

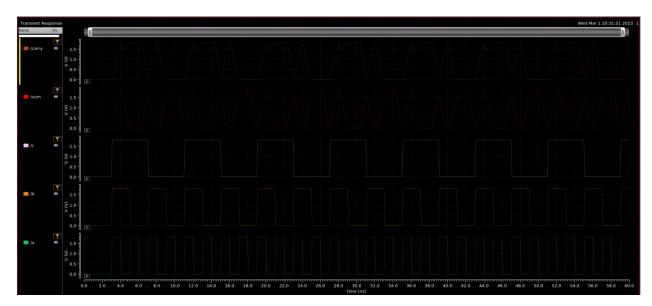


Figure 16: 1-bit Adder Max Frequency

The minimum period for the 1-bit adder was found to be 1ns, thus the max frequency is **0.5 GHz.**