# Lab 3: Cell Characterization using Spectre

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ECEN 714-603

Inverter:

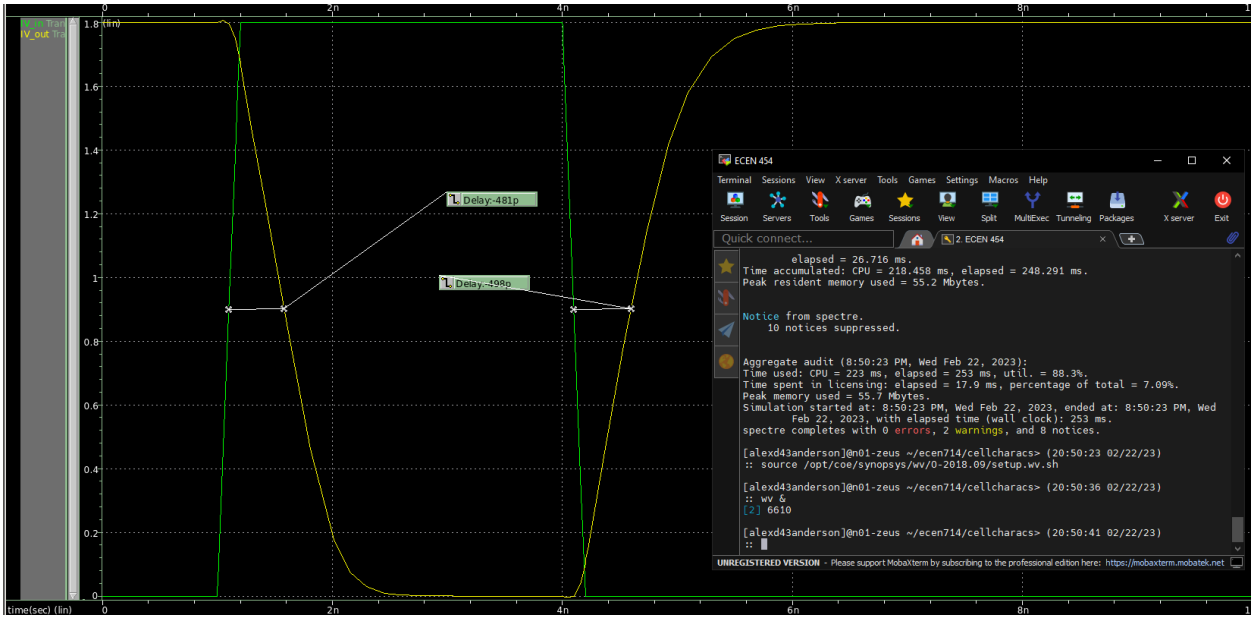


*Figure 1: Inverter Transient Sim*

Table 1: Inverter Delay Table

| Capacitance | Rise (ps) | Fall (ps) | Error |
|---|---|---|---|
| 1f | 45.2 | 27.1 | 40.0% |
| 5f | 74.5 | 57.7 | 22.6% |
| 10f | 101 | 85.8 | 15.0% |
| 20f | 144 | 131 | 9.0% |
| 25f | 166 | 153 | 7.8% |
| 30f | 188 | 175 | 6.9% |
| 40f | 232 | 219 | 5.6% |
| 45f | 255 | 240 | 5.9% |
| 50f | 277 | 262 | 5.4% |
| 60f | 321 | 306 | 4.7% |
| 65f | 345 | 329 | 4.6% |
| 70f | 368 | 351 | 4.6% |
| 80f | 410 | 393 | 4.1% |
| 90f | 451 | 439 | 2.7% |
| 100f | 498 | 481 | 3.4% |

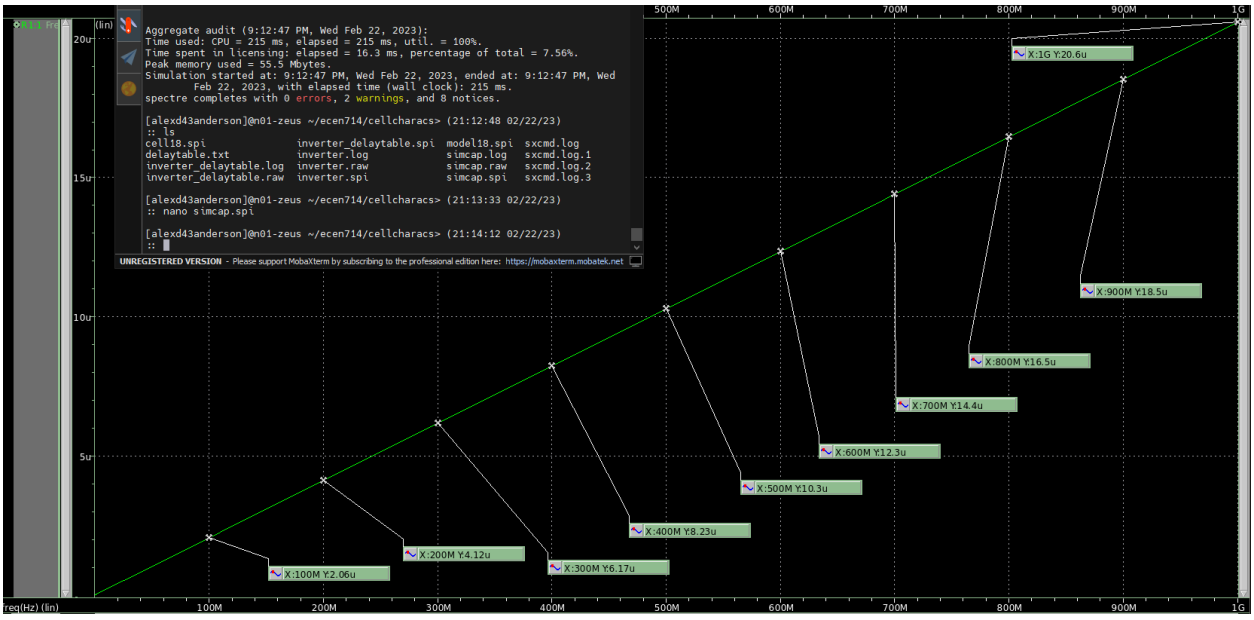


*Figure 2: Inverter AC Sim*

Table 2: Inverter Sink Capacitance

| Frequency (MHz) | Current (uA) | Sink capacitance (fF) |
|---|---|---|
| 100 | 2.06 | 3.279 |
| 200 | 4.12 | 3.279 |
| 300 | 6.17 | 3.273 |
| 400 | 8.23 | 3.275 |
| 500 | 10.3 | 3.279 |
| 600 | 12.3 | 3.263 |
| 700 | 14.4 | 3.274 |
| 800 | 16.5 | 3.283 |
| 900 | 18.5 | 3.272 |
| 1000 | 20.6 | 3.279 |

From these values, the average sink capacitance is 3.275fF.

NAND:

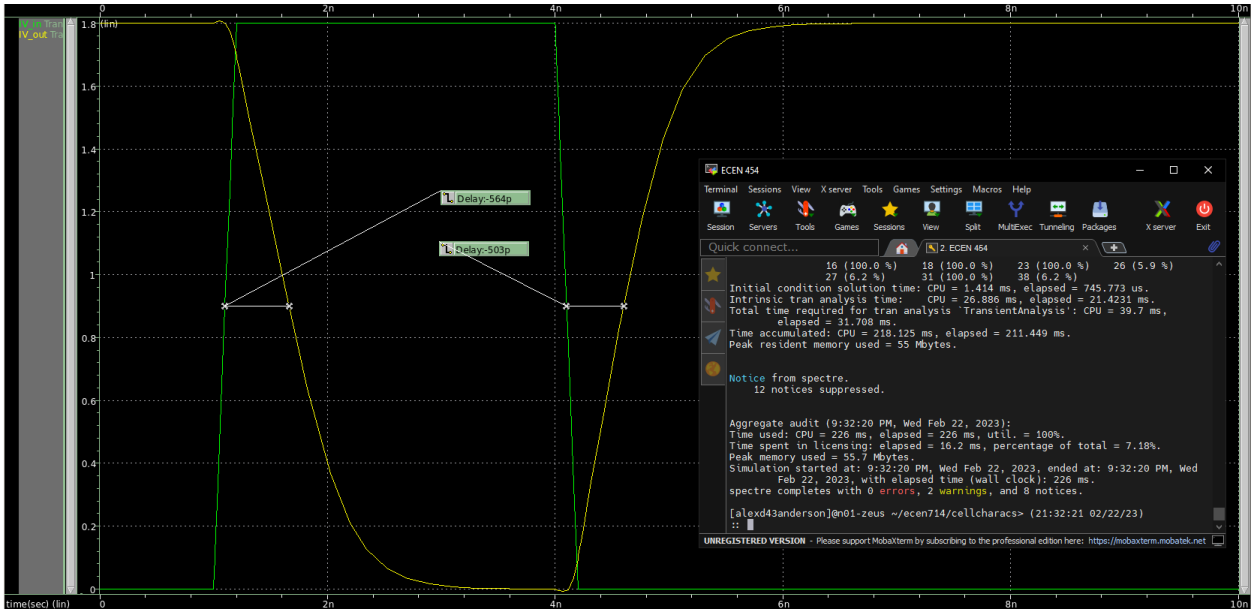


*Figure 3: NAND Transient Sim*

Table 3: NAND Delay Table

| Capacitance | Rise (ps) | Fall (ps) | Error |
|---|---|---|---|
| 1f | 52.5 | 40.3 | 23.2% |
| 5f | 79.8 | 71 | 11.0% |
| 10f | 105 | 101 | 3.8% |
| 20f | 149 | 153 | 2.7% |
| 25f | 171 | 179 | 4.7% |
| 30f | 193 | 204 | 5.7% |
| 40f | 237 | 257 | 8.4% |
| 45f | 260 | 282 | 8.5% |
| 50f | 282 | 307 | 8.9% |
| 60f | 326 | 359 | 10.1% |
| 65f | 349 | 387 | 10.9% |
| 70f | 372 | 412 | 10.8% |
| 80f | 414 | 462 | 11.6% |
| 90f | 457 | 512 | 12.0% |
| 100f | 503 | 564 | 12.1% |

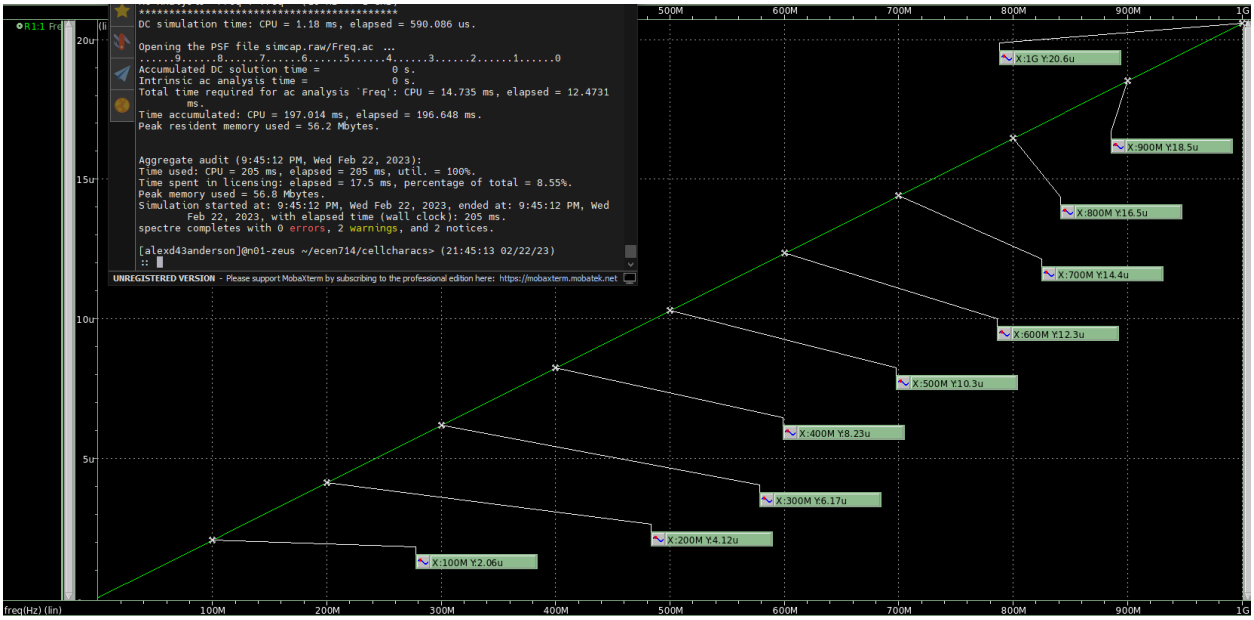


*Figure 4: NAND AC Sim*

Table 4: NAND Sink Capacitance

| Frequency (MHz) | Current (uA) | Sink capacitance (fF) |
|---|---|---|
| 100 | 2.06 | 3.279 |
| 200 | 4.12 | 3.279 |
| 300 | 6.17 | 3.273 |
| 400 | 8.23 | 3.275 |
| 500 | 10.3 | 3.279 |
| 600 | 12.3 | 3.263 |
| 700 | 14.4 | 3.274 |
| 800 | 16.5 | 3.283 |
| 900 | 18.5 | 3.272 |
| 1000 | 20.6 | 3.279 |

From these values, the average sink capacitance is 3.275fF.

XOR:

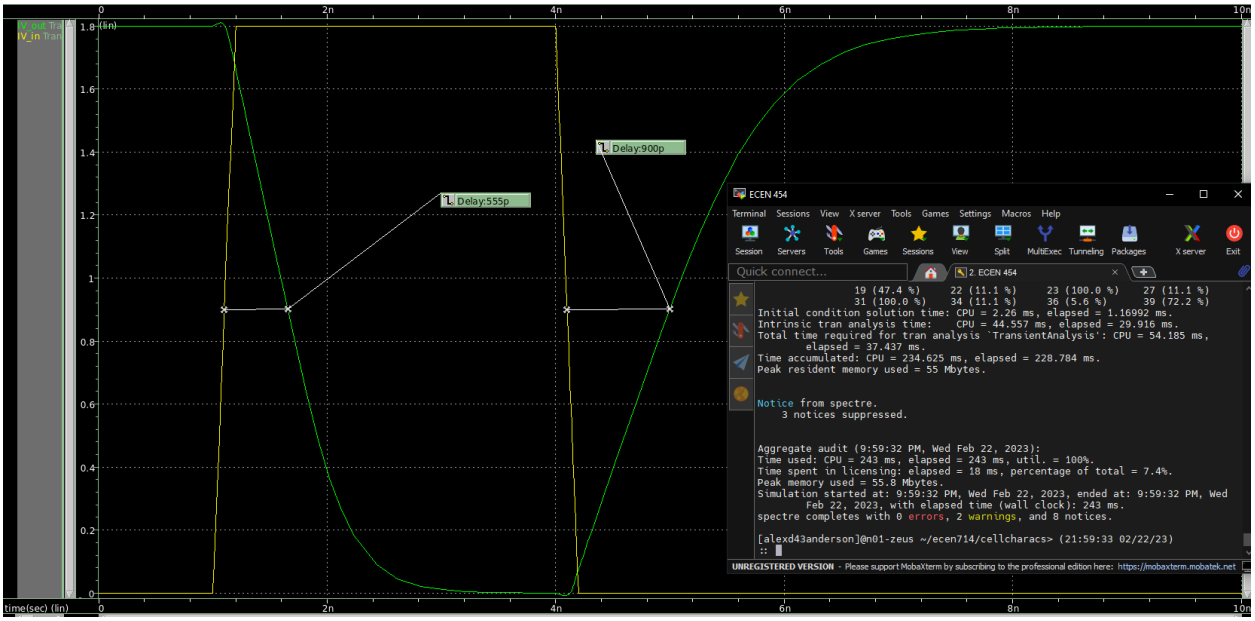


*Figure 5: XOR Transient Sim*

Table 5: XOR Delay Table

| Capacitance | Rise (ps) | Fall (ps) | Error |
|---|---|---|---|
| 1f | 59.3 | 30.3 | 48.9% |
| 5f | 95 | 58.8 | 38.1% |
| 10f | 137 | 90.6 | 33.9% |
| 20f | 223 | 144 | 35.4% |
| 25f | 266 | 170 | 36.1% |
| 30f | 310 | 196 | 36.8% |
| 40f | 394 | 247 | 37.3% |
| 45f | 438 | 273 | 37.7% |
| 50f | 478 | 299 | 37.4% |
| 60f | 563 | 350 | 37.8% |
| 65f | 604 | 376 | 37.7% |
| 70f | 649 | 401 | 38.2% |
| 80f | 732 | 453 | 38.1% |
| 90f | 815 | 504 | 38.2% |
| 100f | 900 | 555 | 38.3% |

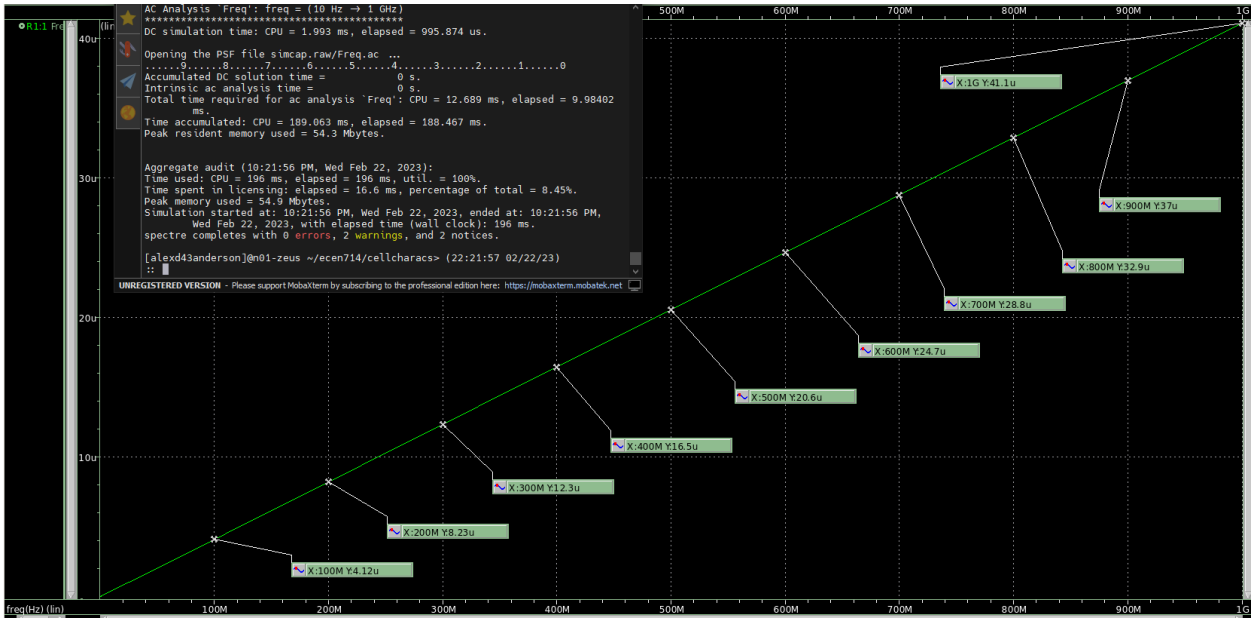


*Figure 6: XOR AC Sim*

Table 6: XOR Sink Capacitance

| Frequency (MHz) | Current (uA) | Sink capacitance (fF) |
|---|---|---|
| 100 | 4.12 | 6.557 |
| 200 | 8.23 | 6.549 |
| 300 | 12.3 | 6.525 |
| 400 | 16.5 | 6.565 |
| 500 | 20.6 | 6.557 |
| 600 | 24.7 | 6.552 |
| 700 | 28.8 | 6.548 |
| 800 | 32.9 | 6.545 |
| 900 | 37 | 6.543 |
| 1000 | 41.1 | 6.541 |

From these values, the average sink capacitance is 6.548fF.

```
[alexd43anderson]@n01-zeus ~/ecen714/cellcharacs> (22:21:57 02/22/23)
:: cat cell18.spi
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

subckt NAND (A B output VDD VSS)
        parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u
        P0 output A VDD VDD tsmc18P w=wp l=lp
        P1 output B VDD VDD tsmc18P w=wp l=lp
        N0 c B VSS VSS tsmc18N w=wn l=ln
        N1 output A c VSS tsmc18N w=wn l=ln
ends NAND

subckt XOR (A B output VDD VSS)
        parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u
        I1 A _A VDD VSS IV wp=wp wn=wn lp=lp ln=ln
        I2 B _B VDD VSS IV wp=wp wn=wn lp=lp ln=ln
        P0 net12 B VDD VDD tsmc18P w=wp l=lp
        P1 output _A net12 VDD tsmc18P w=wp l=lp
        P3 net11 _B VDD VDD tsmc18P w=wp l=lp
        P2 output A net11 VDD tsmc18P w=wp l=lp
        N0 output _A net10 VSS tsmc18N w=wn l=ln
        N1 net10 _B VSS VSS tsmc18N w=wn l=ln
        N2 output A net9 VSS tsmc18N w=wn l=ln
        N3 net9 B VSS VSS tsmc18N w=wn l=ln
ends XOR


[alexd43anderson]@n01-zeus ~/ecen714/cellcharacs> (22:48:30 02/22/23)
::
```

*Figure 7: cell18.spi File*

```
[alexd43anderson]@n01-zeus ~/ecen714/cellcharacs> (22:49:18 02/22/23)
:: cat inverter.spi
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen714/cellcharacs/model18.spi"
include "~/ecen714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

*Figure 8: inverter.spi File*

```
[alexd43anderson]@n01-zeus ~/ecen714/cellcharacs> (22:49:21 02/22/23)
:: cat nand.spi
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen714/cellcharacs/model18.spi"
include "~/ecen714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in vdd IV_out vdd gnd) NAND wp=0.9u lp=0.2u wn=0.4u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

*Figure 9: nand.spi File*

```
[alexd43anderson]@n01-zeus ~/ecen714/cellcharacs> (22:50:00 02/22/23)
:: cat xor.spi
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen714/cellcharacs/model18.spi"
include "~/ecen714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in vdd IV_out vdd gnd) XOR wp=0.9u lp=0.2u wn=0.4u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

*Figure 10: xor.spi File*