Lab 6: Differential Pairs

ECEN 704-601

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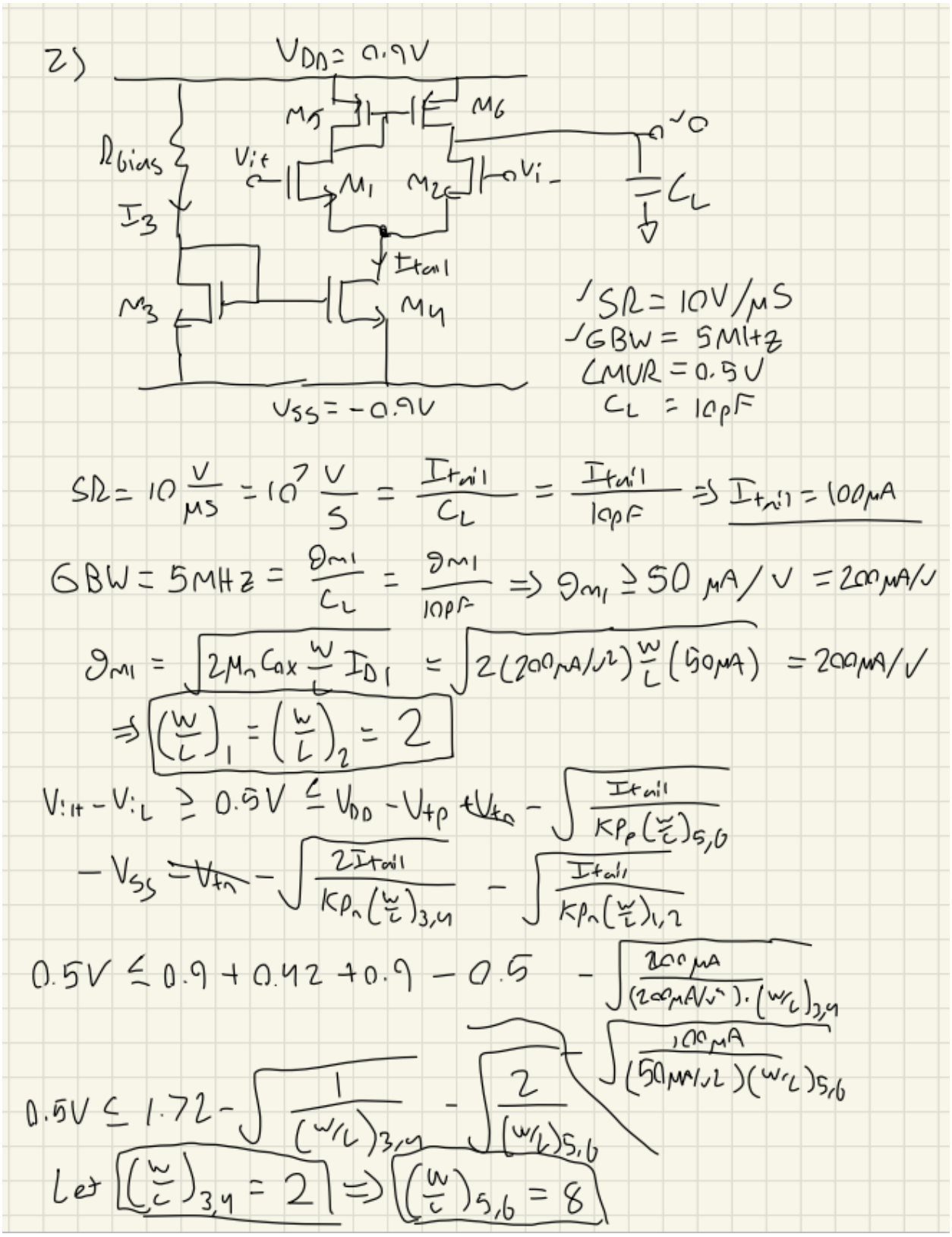
Description

In this lab, the design of differential pairs was explored. Differential pairs have vast applications, including OTAs and differential amplifiers. Two primary circuits were analyzed: a simple differential amplifier and a differential amplifier with low voltage cascode current mirrors. As always, good practice layout techniques were used such as common centroid, dummy elements, and guard rings.

Design

For the simple differential amplifier, the tail current was first determined from the given slew rate specification and load capacitance. From here, using the gain-bandwidth product spec, a value for gm1 was calculated. Using this and the value for the tail current, aspect ratios for both M1 and M2 were determined. Next, a size for M3 and M4 were assigned and from the common mode voltage range spec, the sizing of M5 and M6 was determined. Finally, Rbias was determined using known currents and voltages to set the bias current as desired. The calculations are shown below in Figure 1.



$$SR = 10\frac{V}{\mu s} = 10^7\frac{V}{s} = \frac{I_{tail}}{C_L} = \frac{I_{tail}}{10pF} \Rightarrow I_{tail} = 100\mu A$$

$$GBW = 5MHz = \frac{g_{m1}}{C_L} = \frac{g_{m1}}{10pF} \Rightarrow g_{m1} \geq 50\ \mu A/V = 200\mu A/V$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_{D1}} = \sqrt{2(200\mu A/V^2)\frac{W}{L}(50\mu A)} = 200\mu A/V$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 2}$$

$$V_{i1} - V_{iL} \geq 0.5V \leq V_{DD} - V_{tp} + V_{to} - \sqrt{\frac{I_{tail}}{KP_p\left(\frac{W}{L}\right)_{5,6}}}$$

$$- V_{SS} = V_{tn} - \sqrt{\frac{2I_{tail}}{KP_n\left(\frac{W}{L}\right)_{3,4}}} - \sqrt{\frac{I_{tail}}{KP_n\left(\frac{W}{L}\right)_{1,2}}}$$

$$0.5V \leq 0.9 + 0.42 + 0.9 - 0.5 - \sqrt{\frac{200\mu A}{(200\mu A/V^2)\cdot\left(\frac{W}{L}\right)_{3,4}}}$$

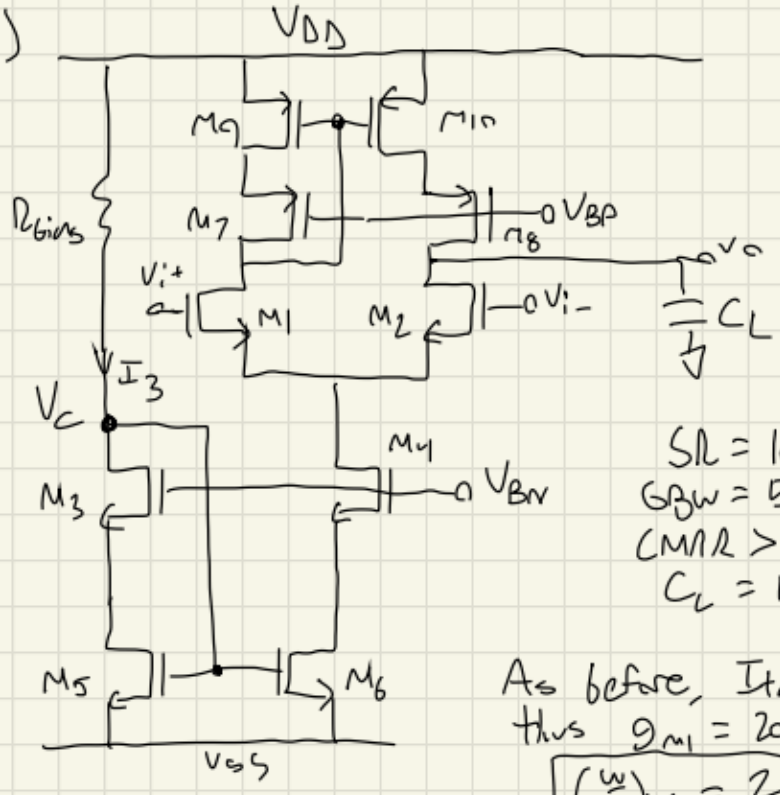
$$0.5V \leq 1.72 - \sqrt{\frac{1}{\left(\frac{W}{L}\right)_{3,4}}} - \sqrt{\frac{2}{\left(\frac{W}{L}\right)_{5,6}}} - \sqrt{\frac{100\mu A}{(50\mu A/V^2)\left(\frac{W}{L}\right)_{5,6}}}$$

Let $\boxed{\left(\frac{W}{L}\right)_{3,4} = 2} \Rightarrow \boxed{\left(\frac{W}{L}\right)_{5,6} = 8}$

Figure 1: Simple Differential Amplifier Calculations

Next, the topology with cascode current mirrors was designed. As before, the tail current and gm1 were set from the given quantities. Next, using the desired common mode rejection ratio and calculated value for differential mode gain, a maximum common mode gain was derived. From this expression, the sizing of M3, M4, M5, and M6 was calculated and the remaining transistors were matched to their differential counterparts. Finally, Rbias was derived using known voltages and the desired current mirror reference. The calculations are shown below in Figure 2.

3)



$SR = 10^7\ V/s$
$GBW = 5MHz$
$CMRR > 60dB$
$C_L = 10pF$

As before, $I_{tail} = 100\mu A$ and thus $g_{m1} = 200\mu A/V$ @

$$\boxed{\left(\frac{W}{L}\right)_{1,2} = 2}$$

$$A_{DM} = g_{m1} r_{o2} = (200\mu A/V)\left(\frac{1}{0.3 \cdot 50\mu A}\right) = 13.33$$

$$CMRR > 60dB = 20\log_{10}\left[\left|\frac{A_{DM}}{A_{CM}}\right|\right] \Rightarrow A_{CM} \leq 0.0133$$

$$0.0133 \geq \frac{1}{2(r_{o4} + r_{o6} + g_{m4} r_{o4} r_{o6}) g_{m9}}$$

Let $\boxed{\left(\frac{W}{L}\right)_{9,10} = 4}$ $\Rightarrow$ $g_{m9} = \sqrt{2\mu_n C_{ox} \frac{W}{L} \frac{I_{tail}}{2}} = \sqrt{(50\mu A/V^2)(4)(50\mu)}$

$g_{m9} = 141.42\mu A/V$, $r_{o4} = r_{o6} = \frac{1}{\lambda_n I_{tail}} = \frac{1}{0.3 \cdot 100\mu A} = 33.33k\Omega$

$$\Rightarrow 0.0133 \geq \frac{1}{2(2 \cdot 33.33k + (33.33k)^2\left[\sqrt{2(20\mu)\left(\frac{W}{L}\right)_1(100\mu)}\right](141.42\mu)}$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_{1,5,6,3} = 2}$$ For matching $\boxed{\left(\frac{W}{L}\right)_{2,8} = 4}$

$$I_3 = I_{tail} = 100\mu A$$

$$\Rightarrow V_{eff,5} = \frac{2I_3}{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_3 I_3}} = \frac{2(100\mu A)}{\sqrt{2(200\mu A/V^2)(2)(100\mu A)}}$$

$$V_{eff,5} = 0.707\,V \Rightarrow V_{GS5} = V_{eff,5} - V_{tn} = 0.257\,V$$

$$\Rightarrow V_{GS5} = 0.257 = V_G - V_{SS} \Rightarrow V_G = -0.643\,V$$

$$R_{bias} = \frac{V_{DD} - V_G}{I_{tail}} = \frac{0.9 - (-0.643)}{100\mu A} = 15.43\,K\Omega$$

Figure 2: Cascode Differential Amp Calculations

Results

The schematic for the simple differential amplifier is shown below in Figure 3, including dummy elements.

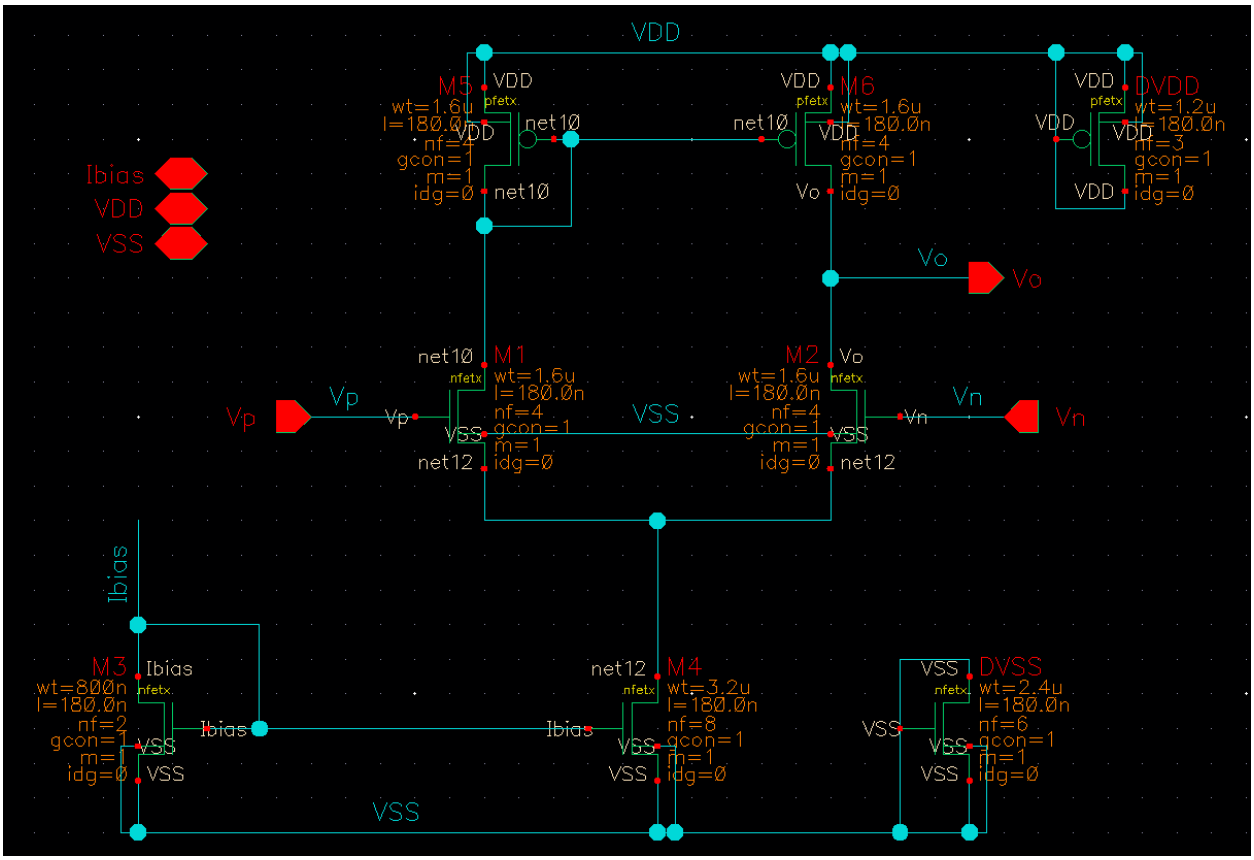


Figure 3: Simple Schematic

From here, a test bench for the system was created (Figure 4).

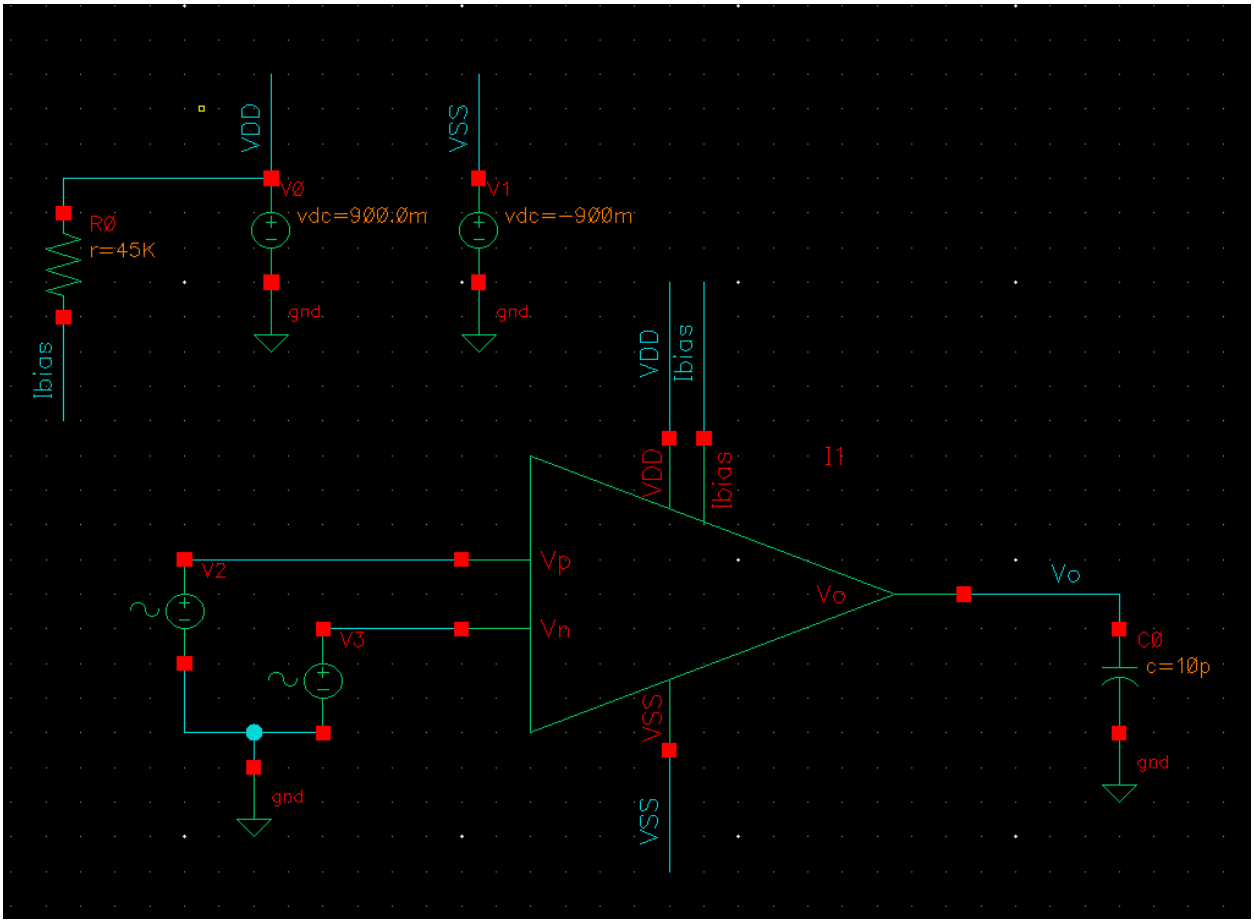


Figure 4: Simple Test Bench

From here, the necessary simulations were completed for the common mode voltage range, differential gain, common mode gain, common mode rejection ratio, dominant pole location, gain-bandwidth product, and slew rate.

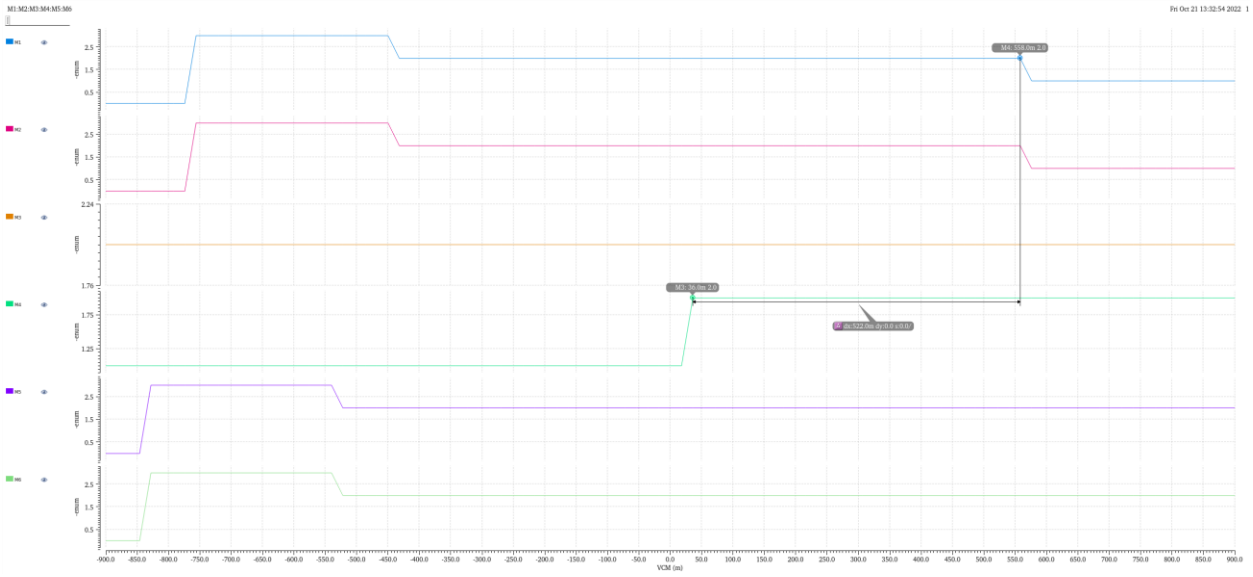


Figure 5: Simple CMVR

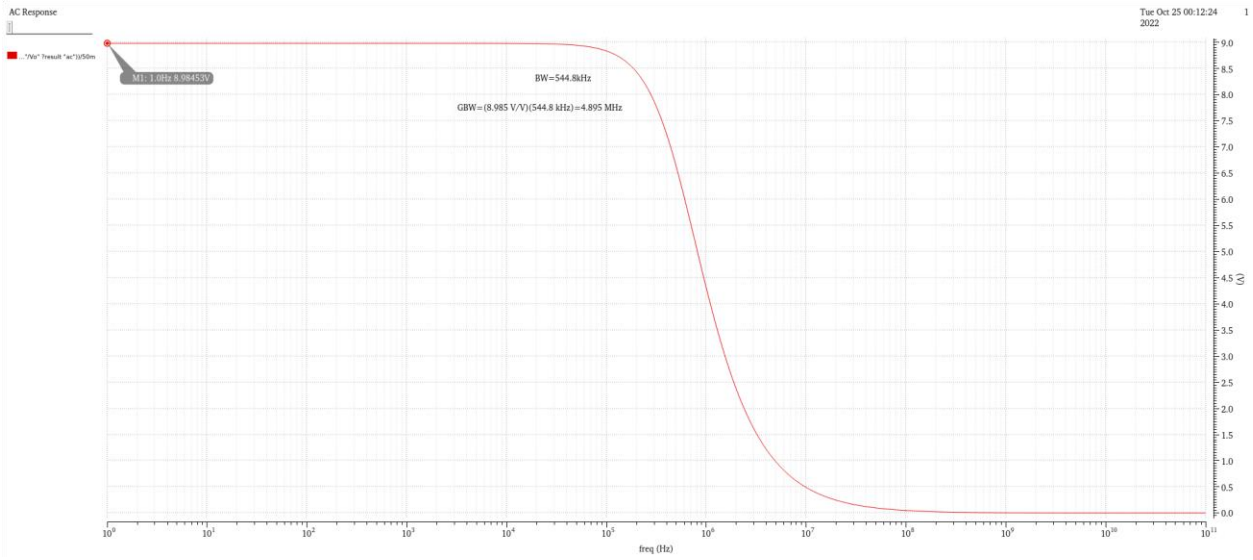


Figure 6: Simple ADM and GBW

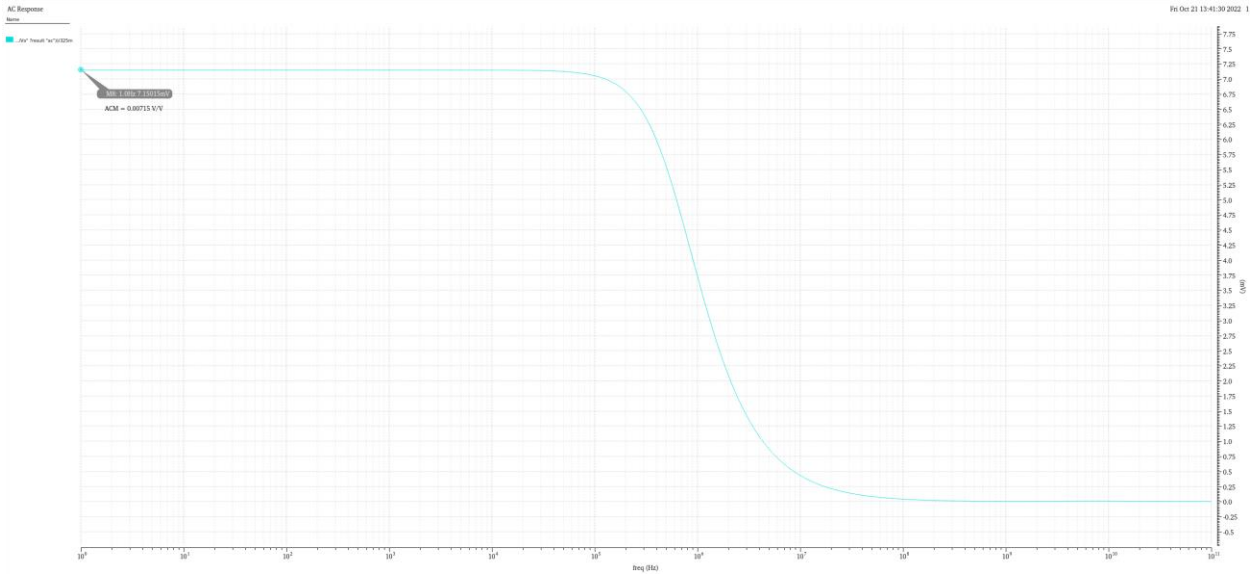


Figure 7: Simple ACM

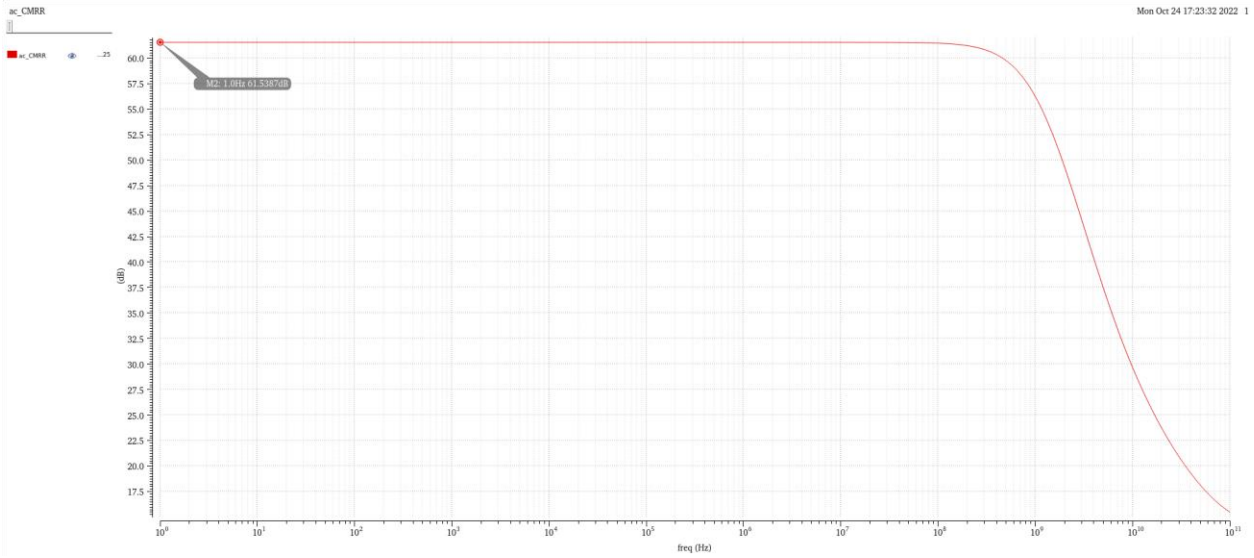


Figure 8: Simple CMRR

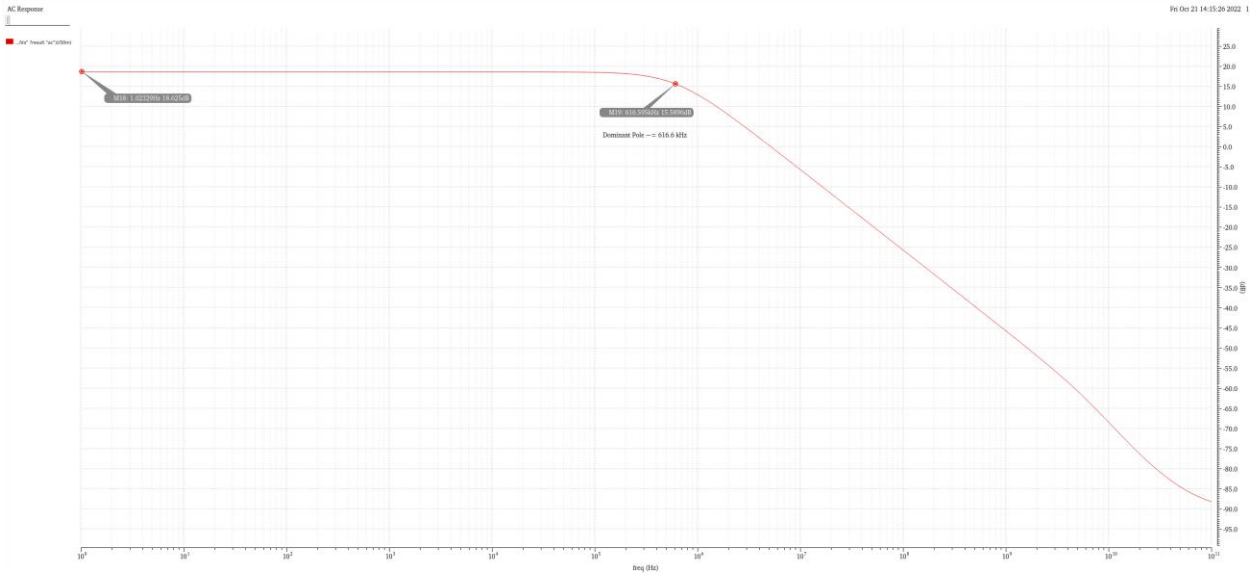


Figure 9: Simple Pole

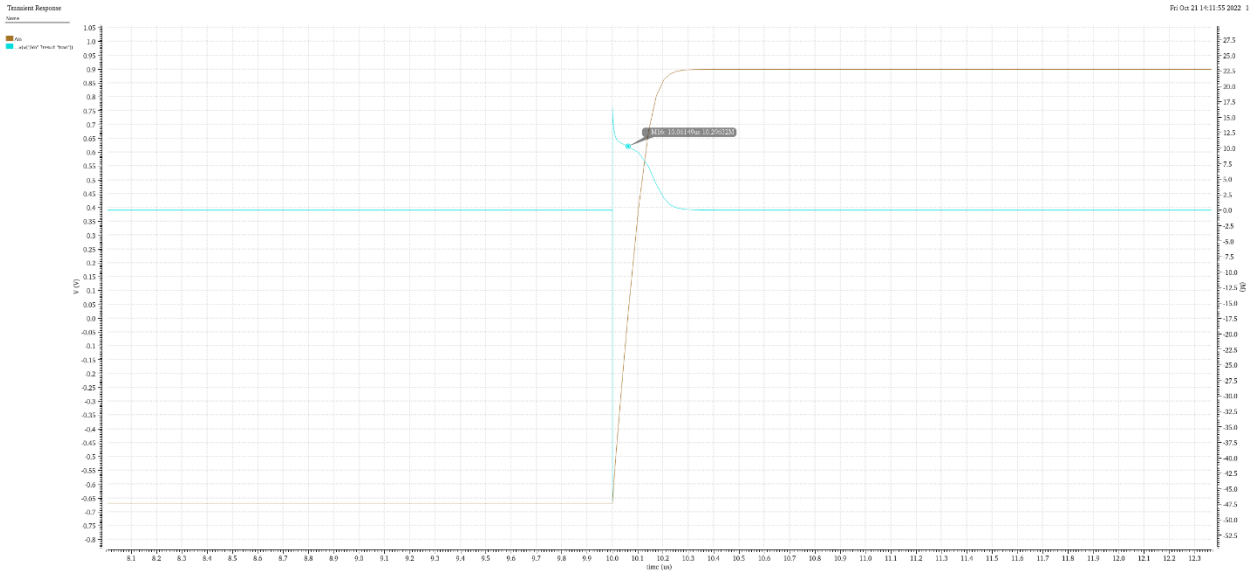


Figure 10: Simple Slew Rate

Next, the layout was completed. The design was verified successfully using DRC and LVS.

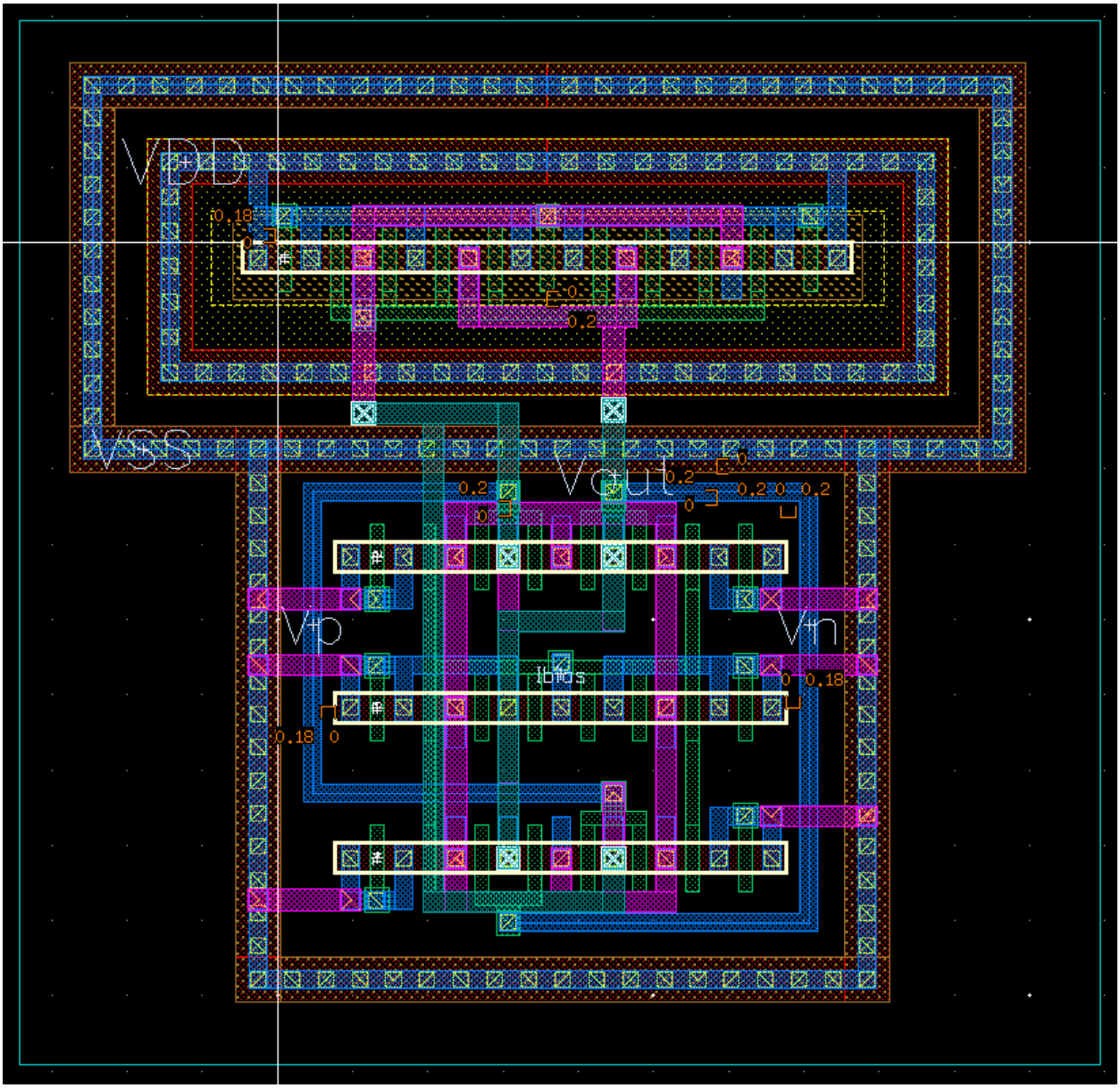


Figure 11: Simple Layout

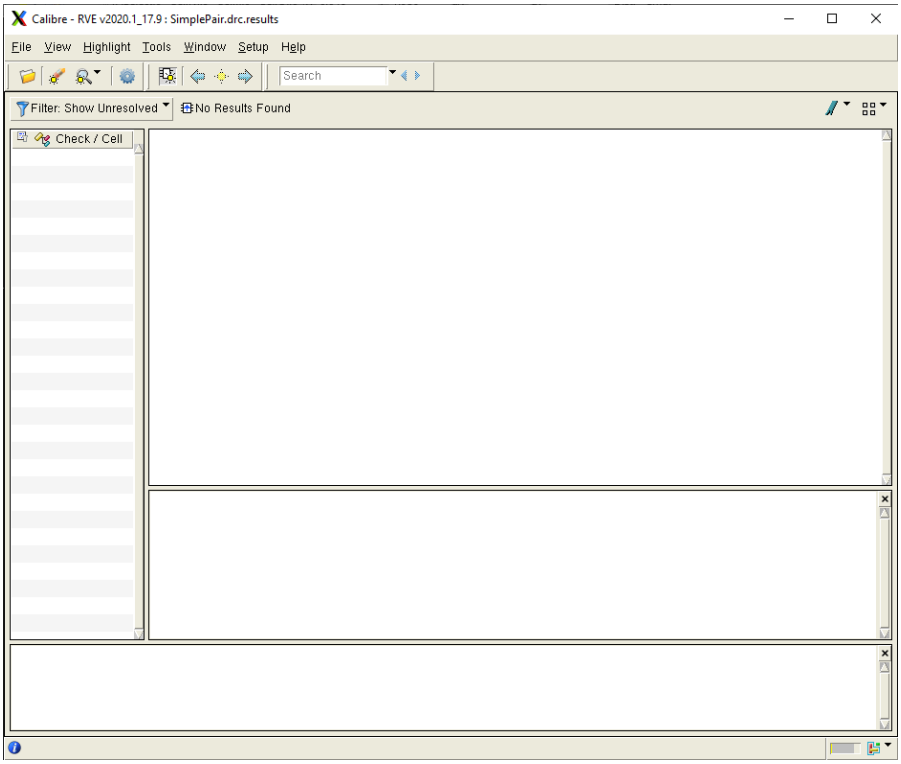


Figure 12: Simple DRC

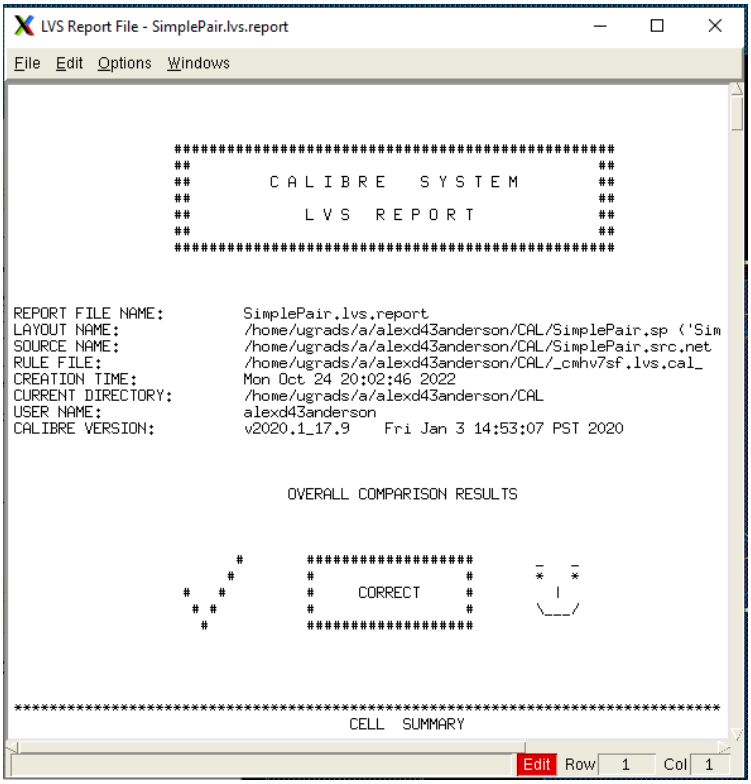


Figure 13: Simple LVS

Finally, with the layout complete and checked, the parasitic capacitances and resistances were extracted and used to perform post layout simulations for all the desired quantities.

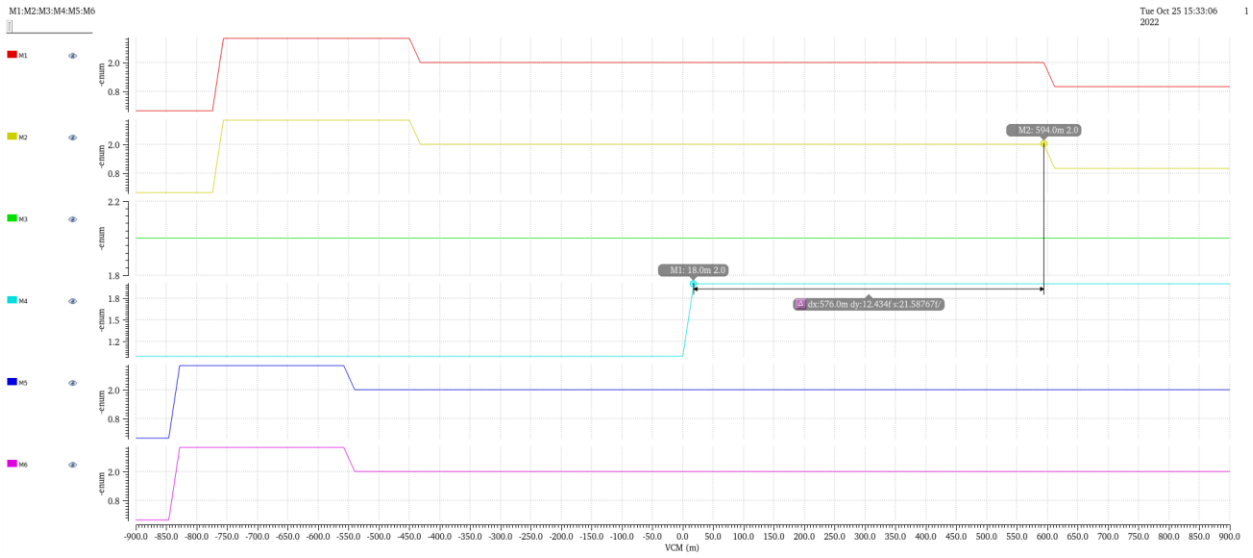


Figure 14: Simple CMVR – Post

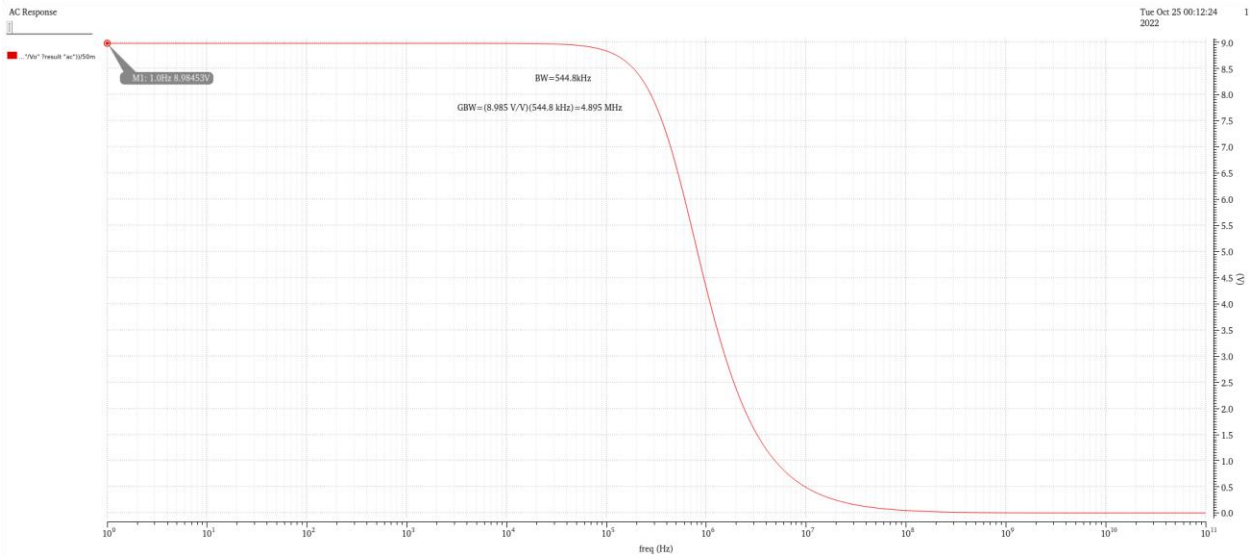


Figure 15: Simple ADM and GBW – Post

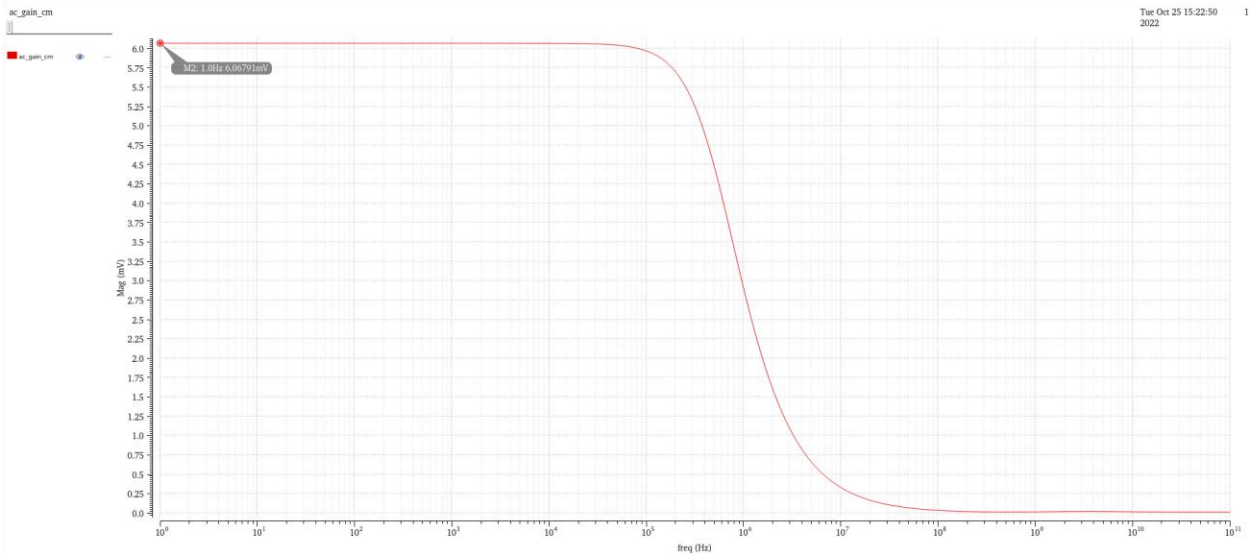


Figure 16: Simple ACM – Post

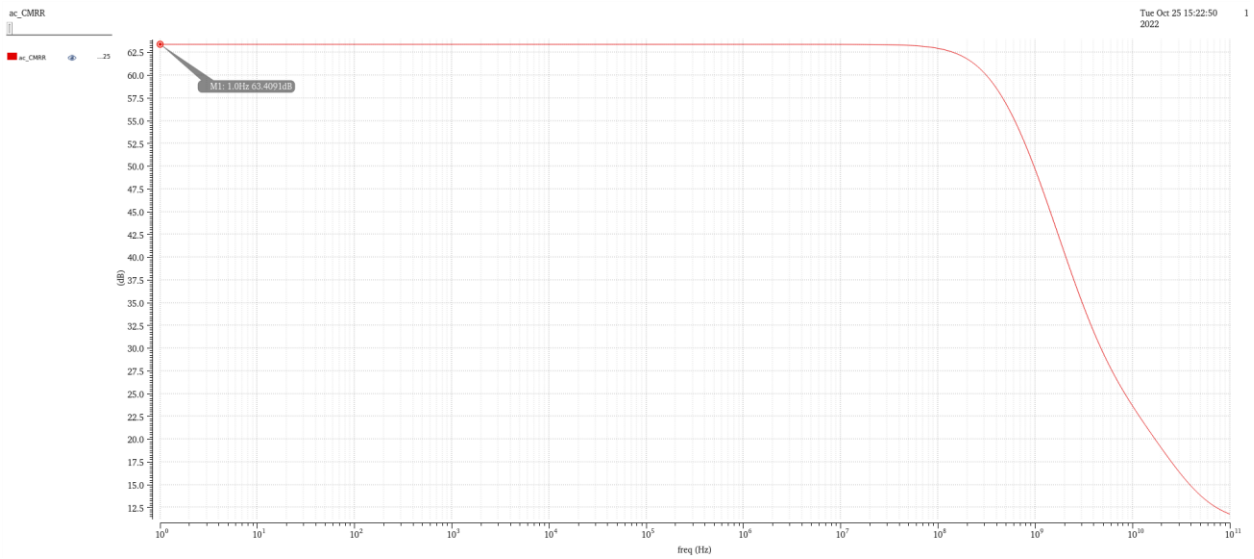


Figure 17: Simple CMRR – Post

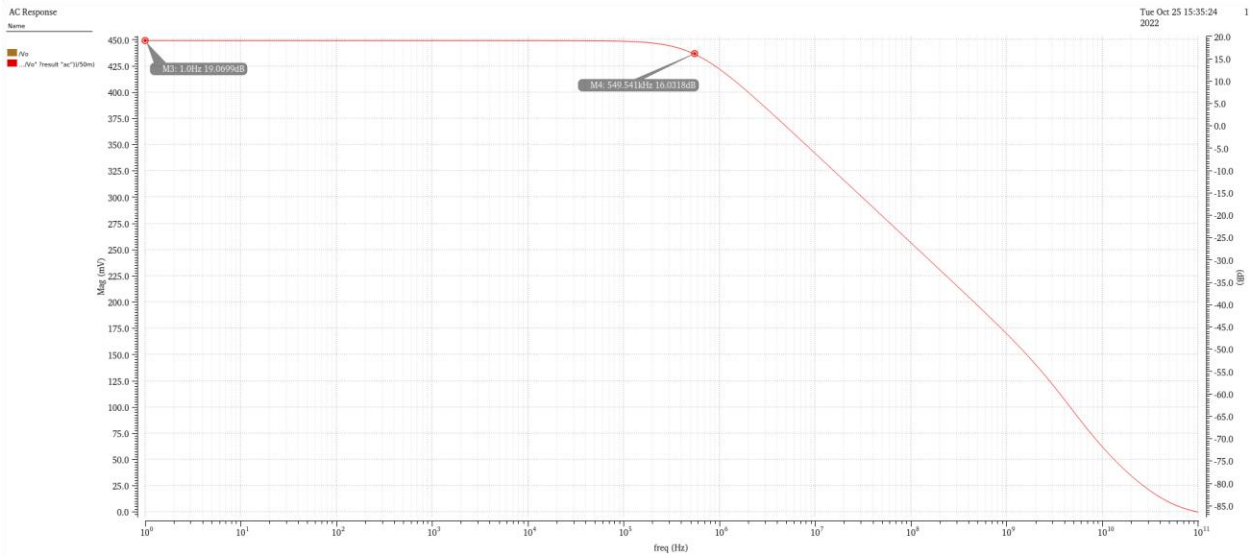


Figure 18: Simple Pole – Post

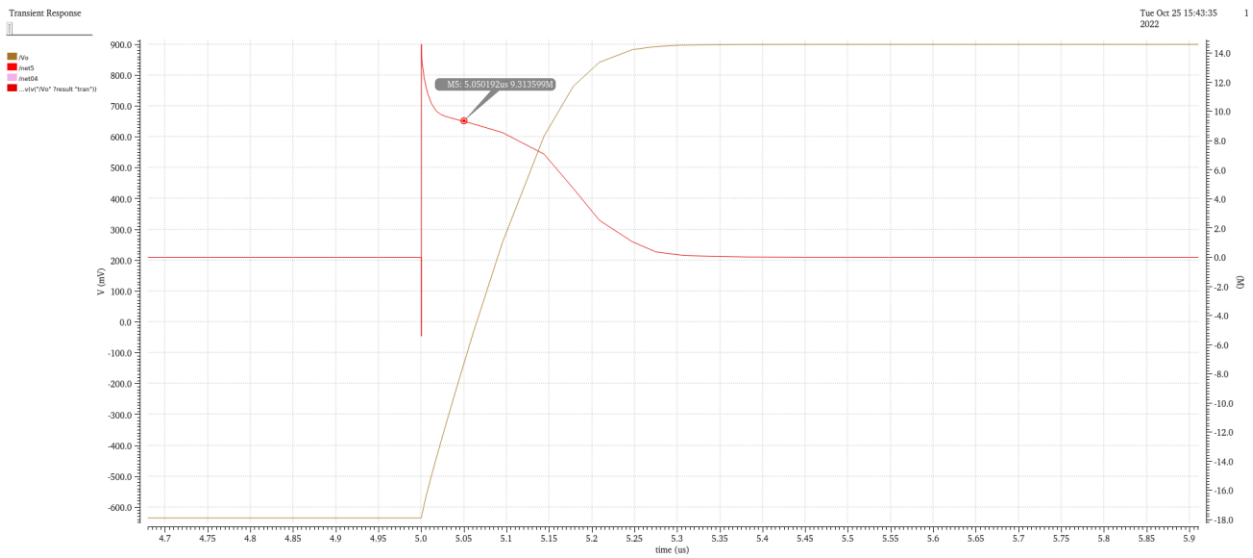


Figure 19: Simple Slew Rate - Post

The schematic for the differential amplifier with cascode current mirrors is shown below in Figure 20, including dummy elements that were added post-layout.

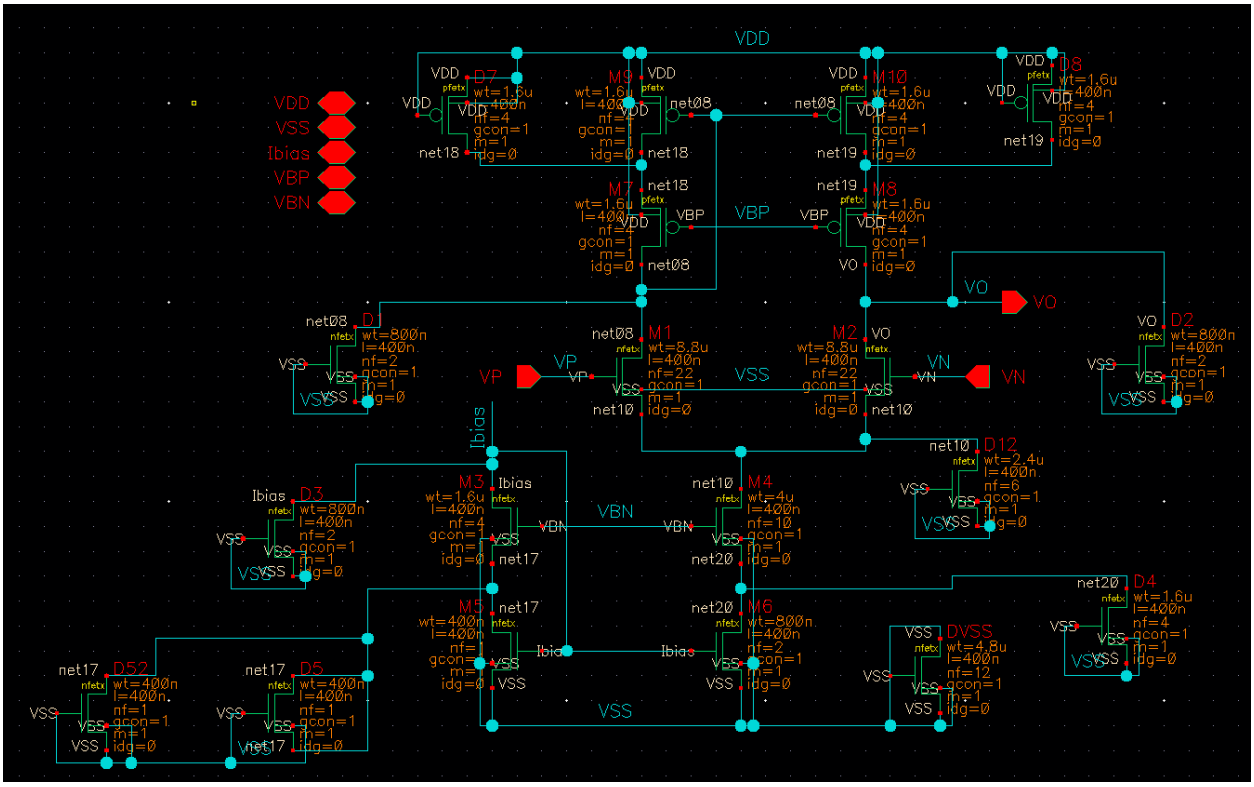


Figure 20: Cascode Schematic

From here, a test bench for the system was created and simulations for the desired parameters were performed.

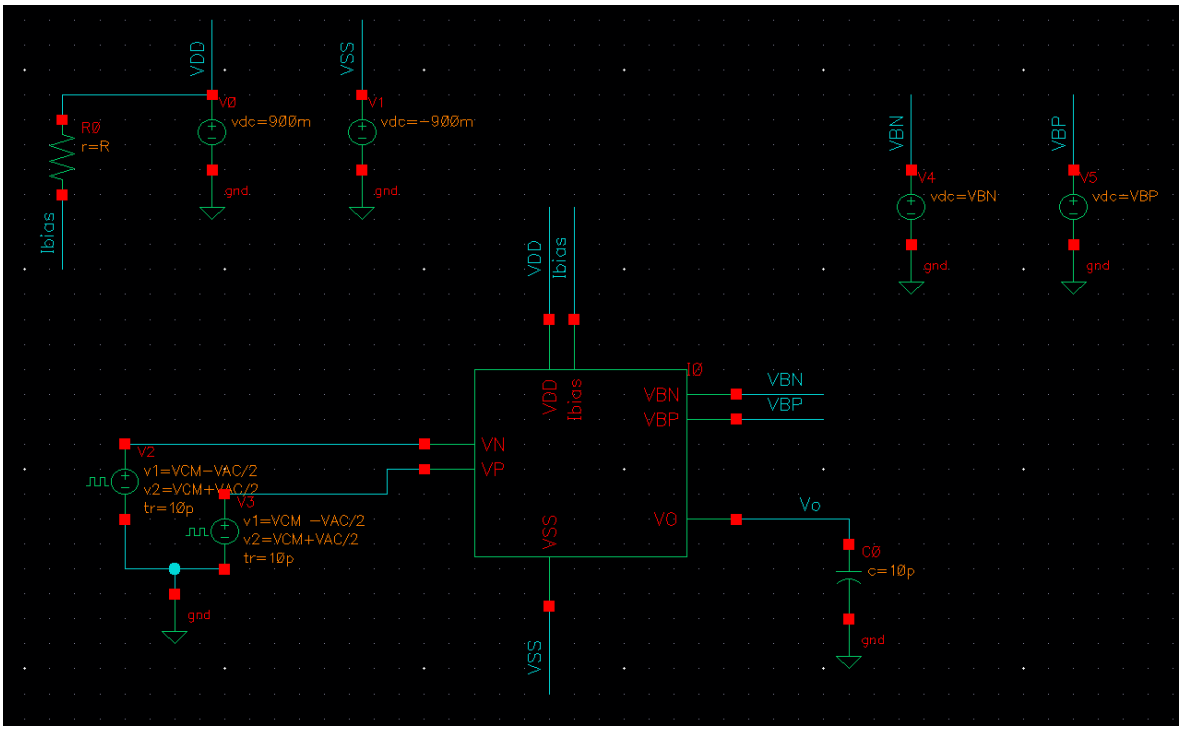


Figure 21: Cascode Test Bench

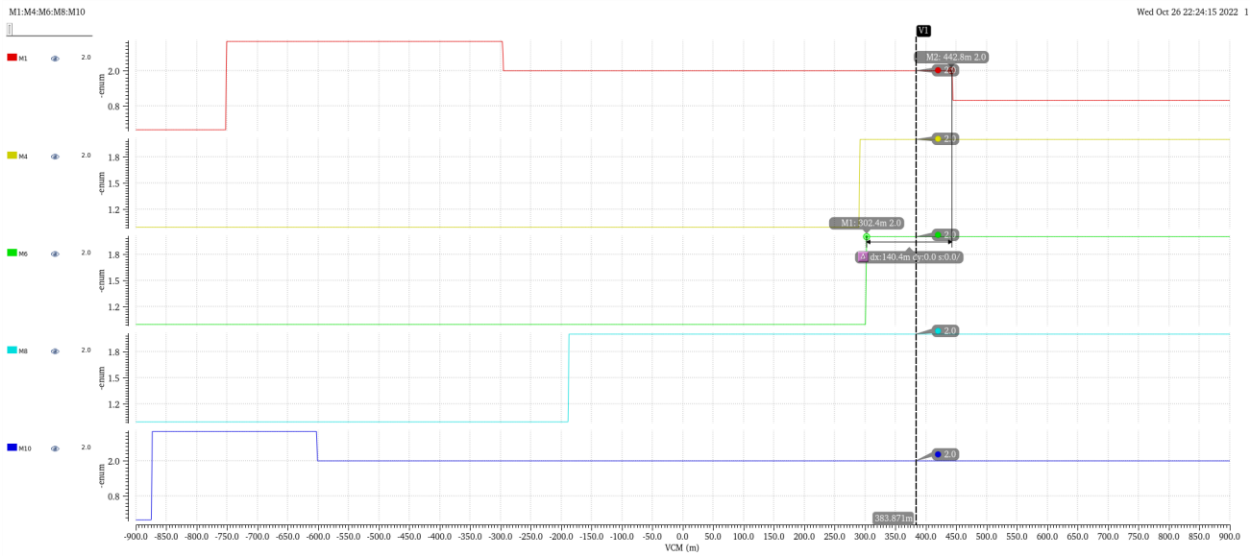


Figure 22: Cascode CMVR

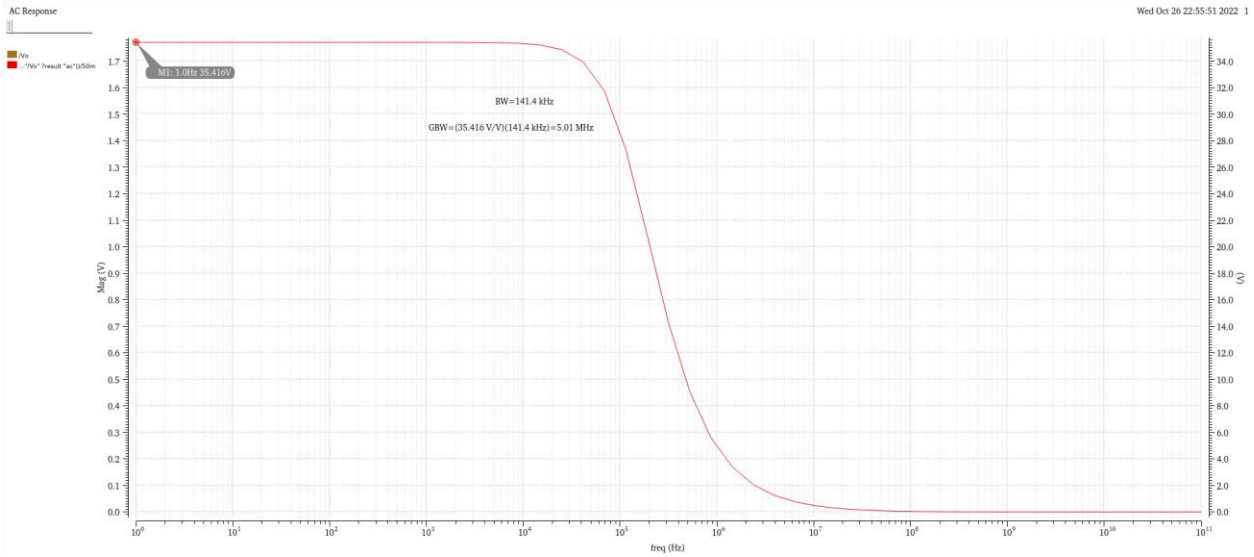


Figure 23: Cascode ADM and GBW

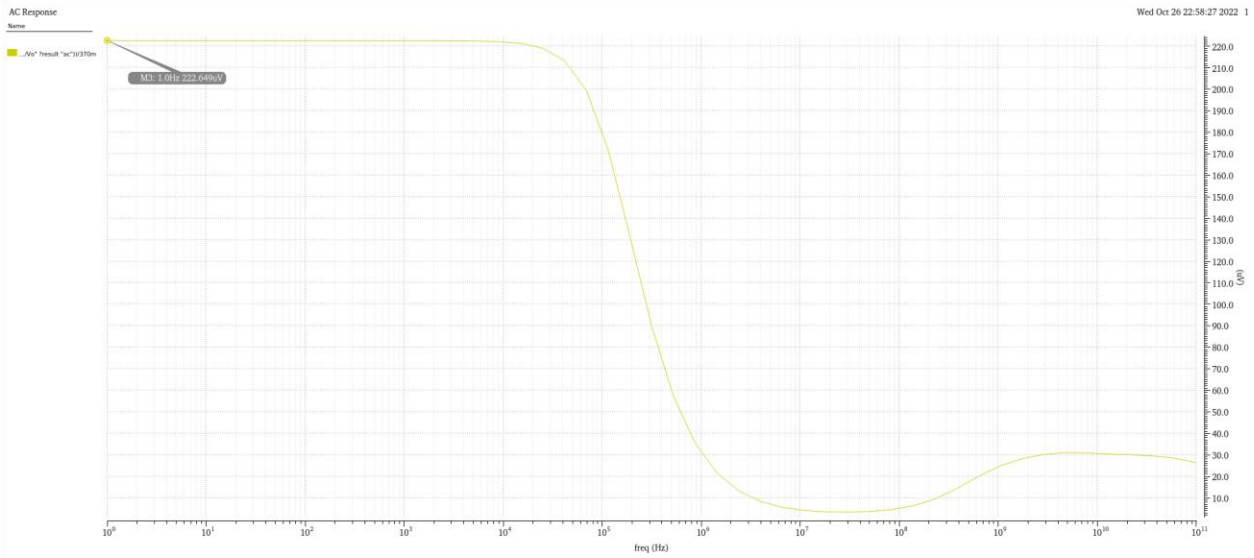


Figure 24: Cascode ACM

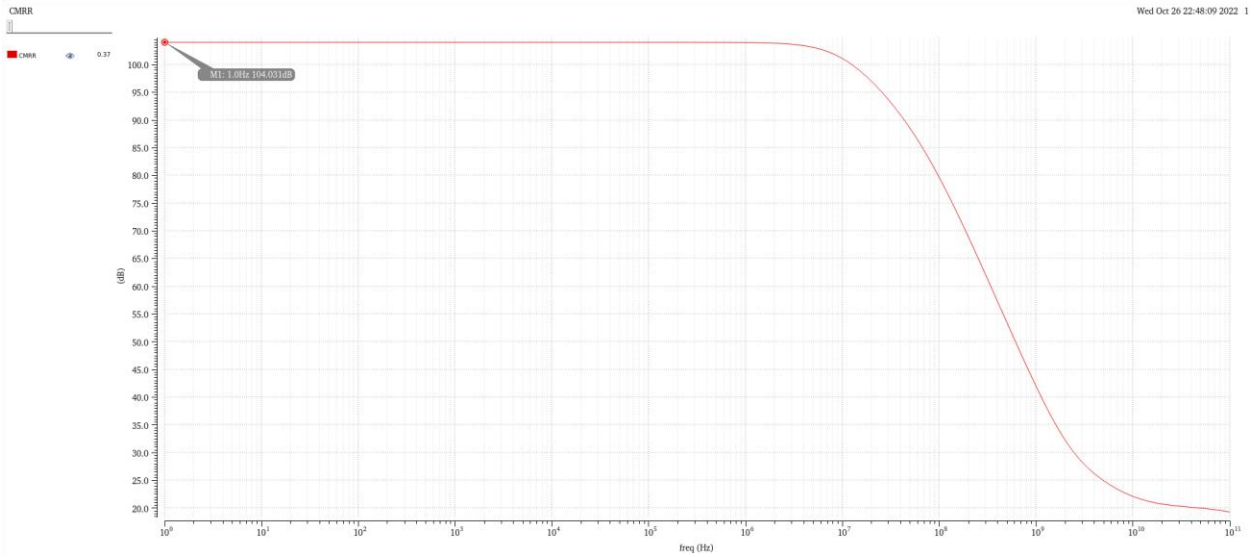


Figure 25: Cascode CMRR

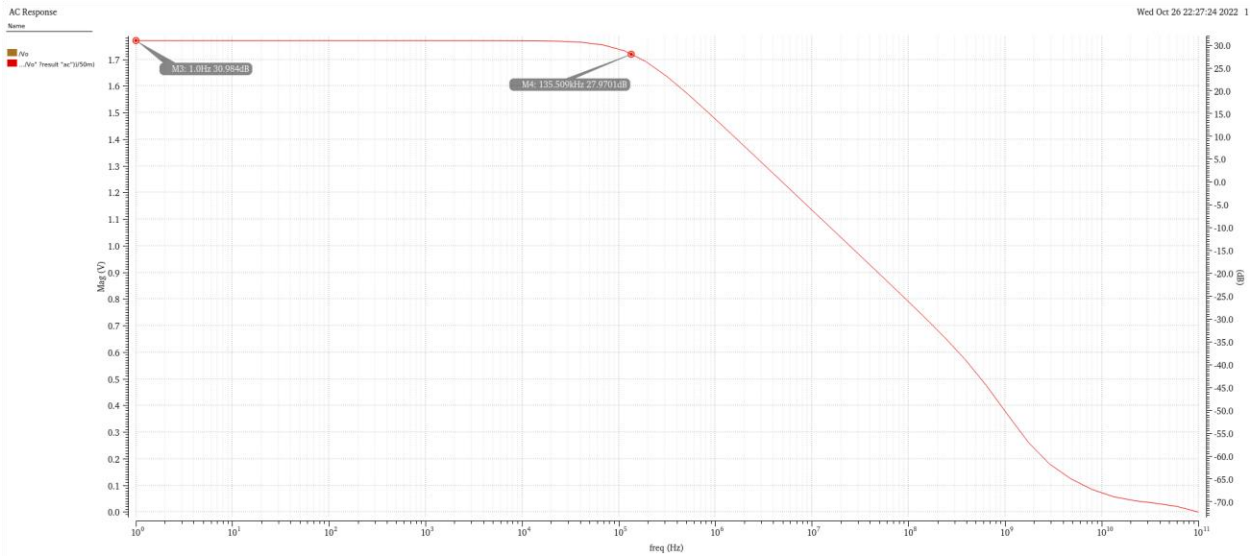


Figure 26: Cascode Pole

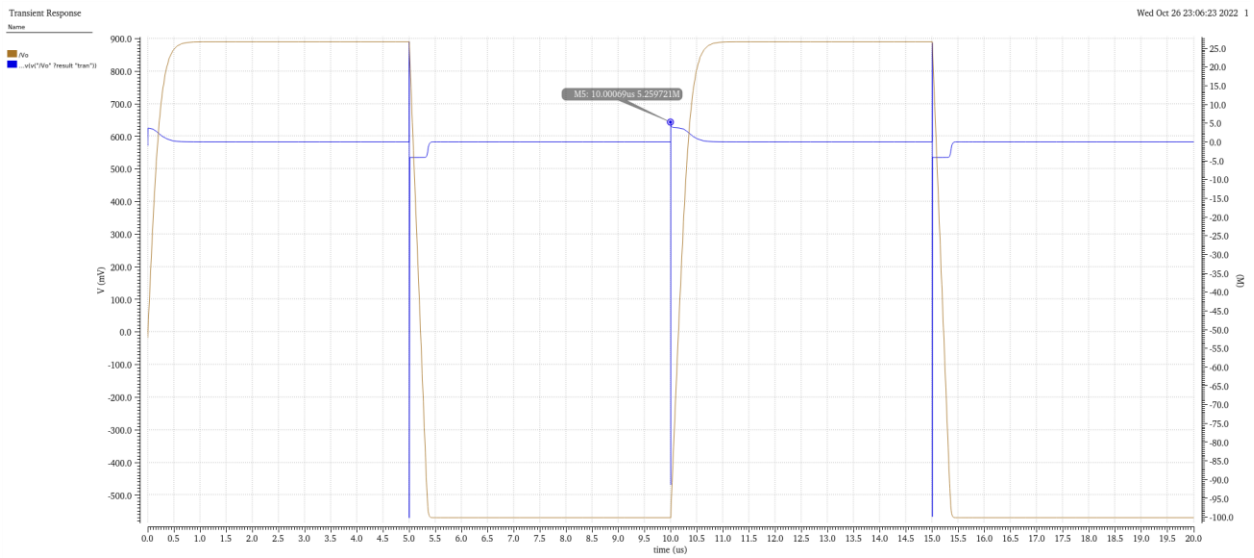


Figure 27: Cascode Slew Rate

Next, the layout was completed. The design was verified successfully using DRC and LVS.

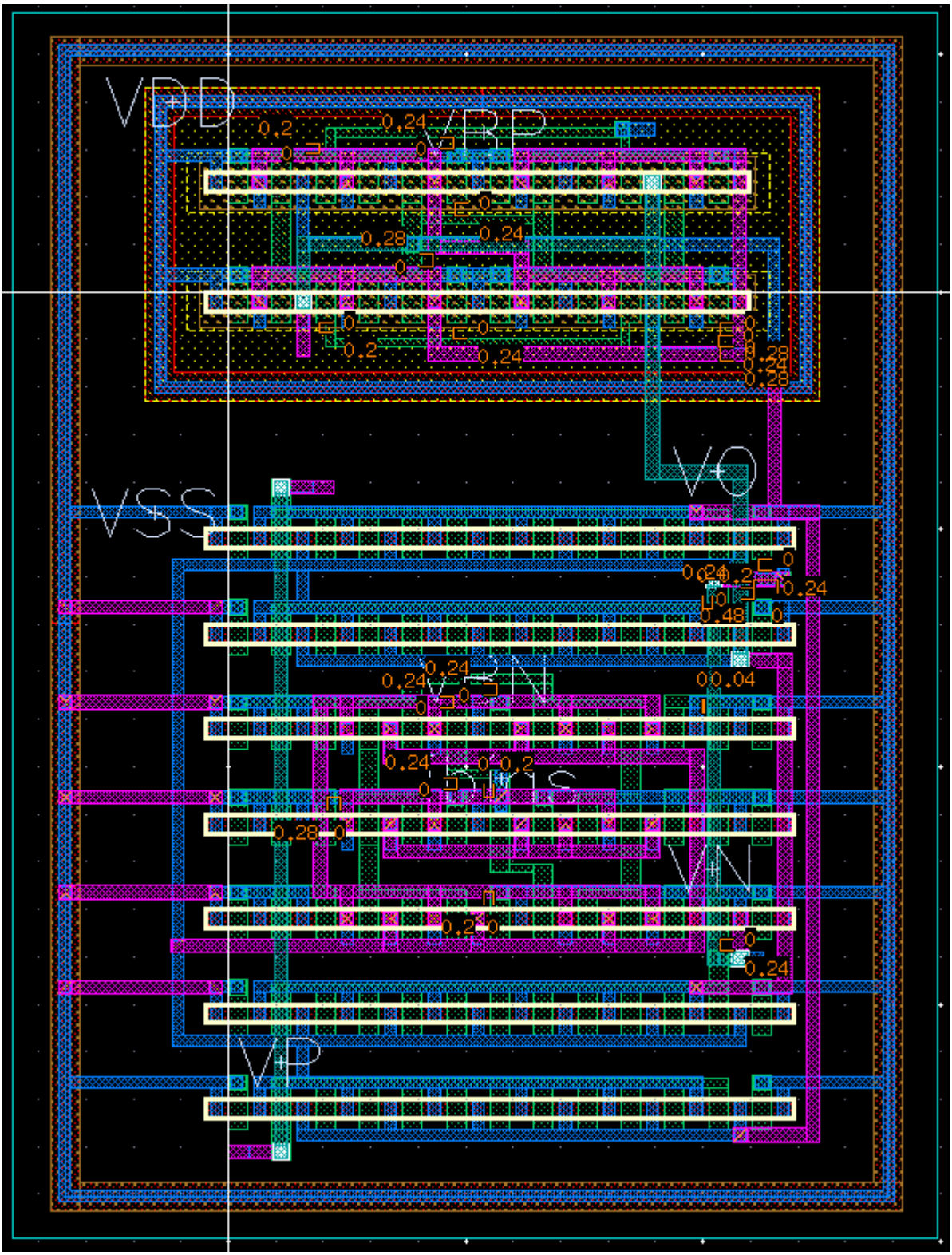


Figure 28: Cascode Layout

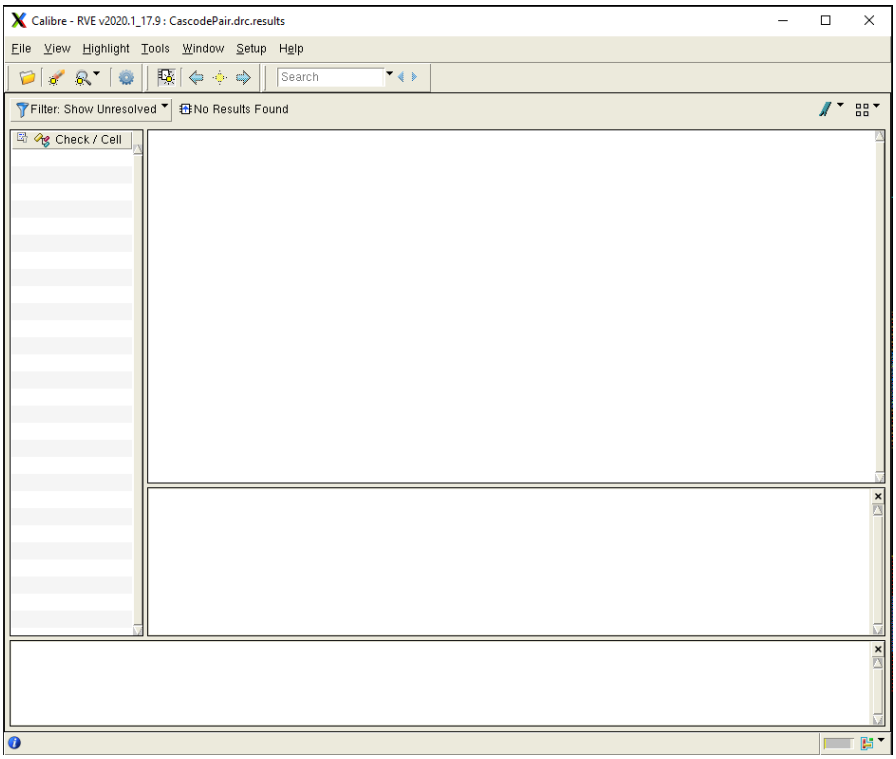


Figure 29: Cascode DRC

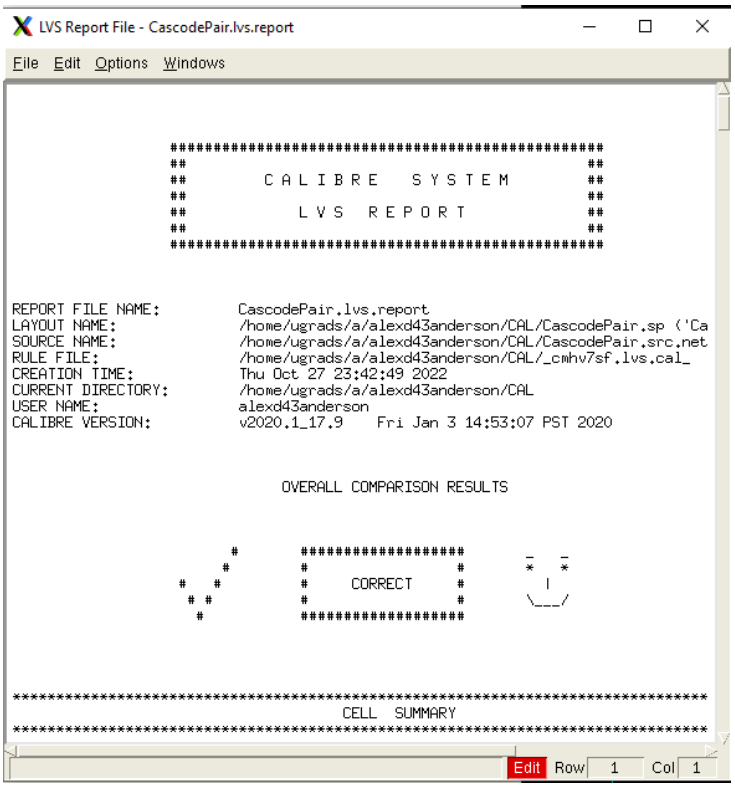


Figure 30: Cascode LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations.

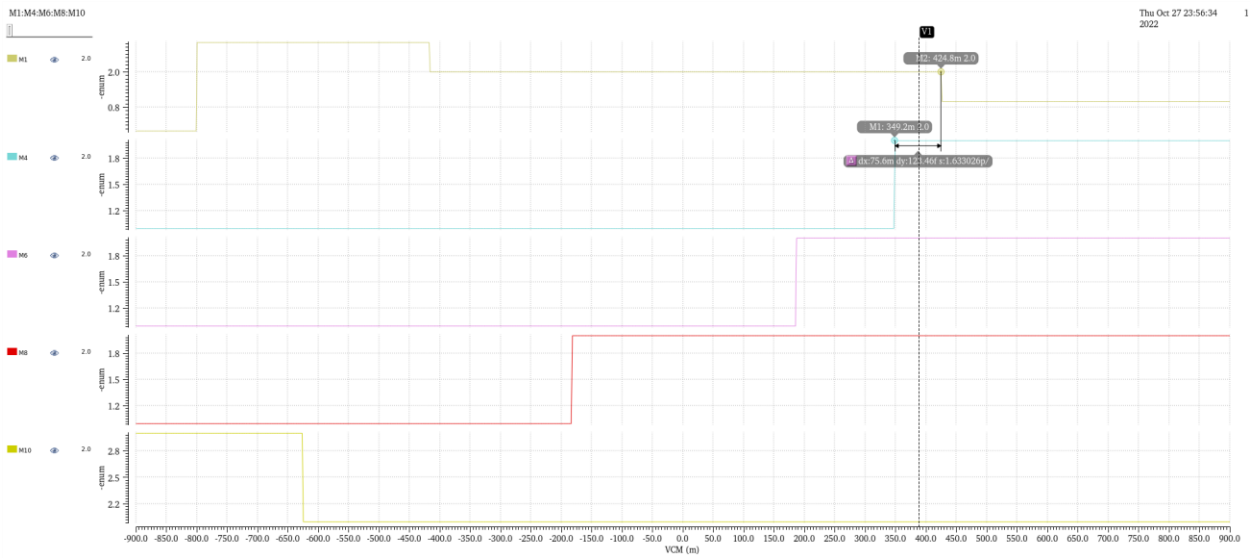


Figure 31: Cascode CMVR – Post

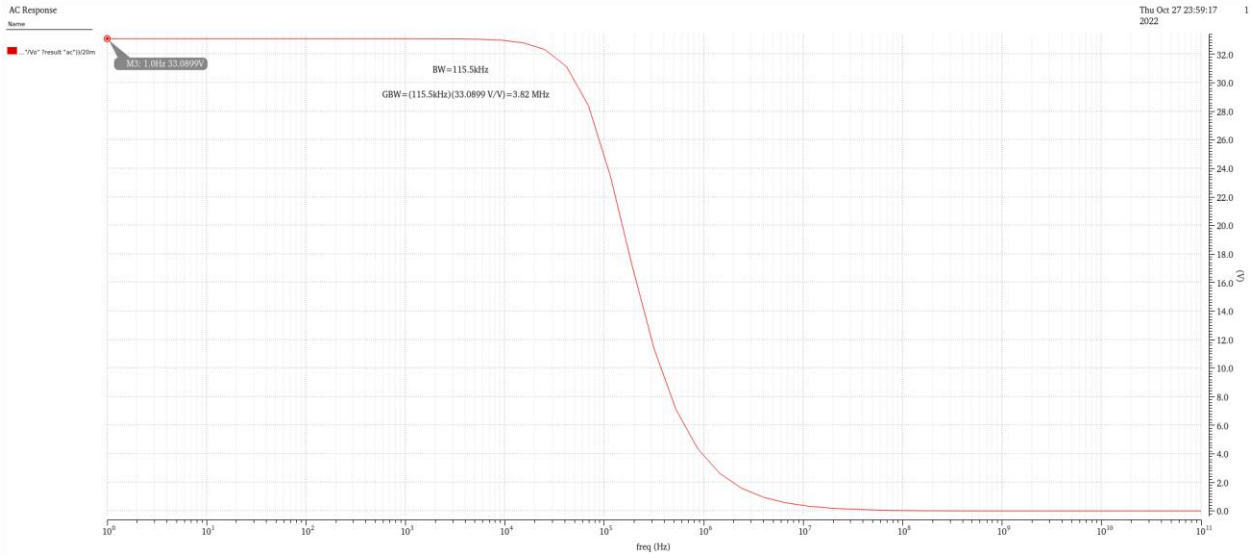


Figure 32: Cascode ADM and GBW – Post

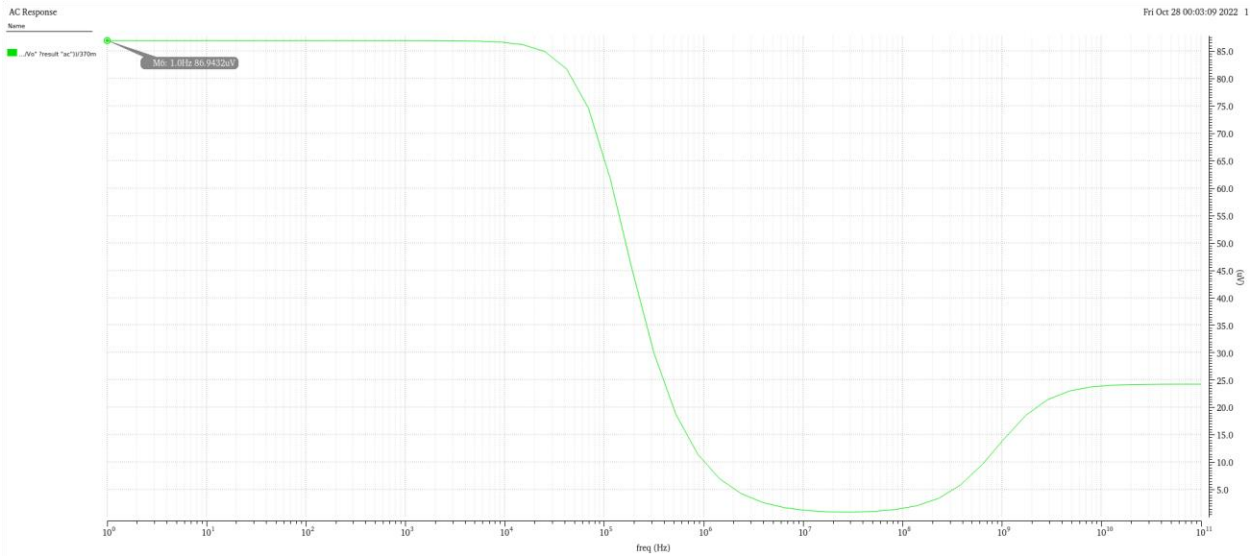


Figure 33: Cascode ACM – Post

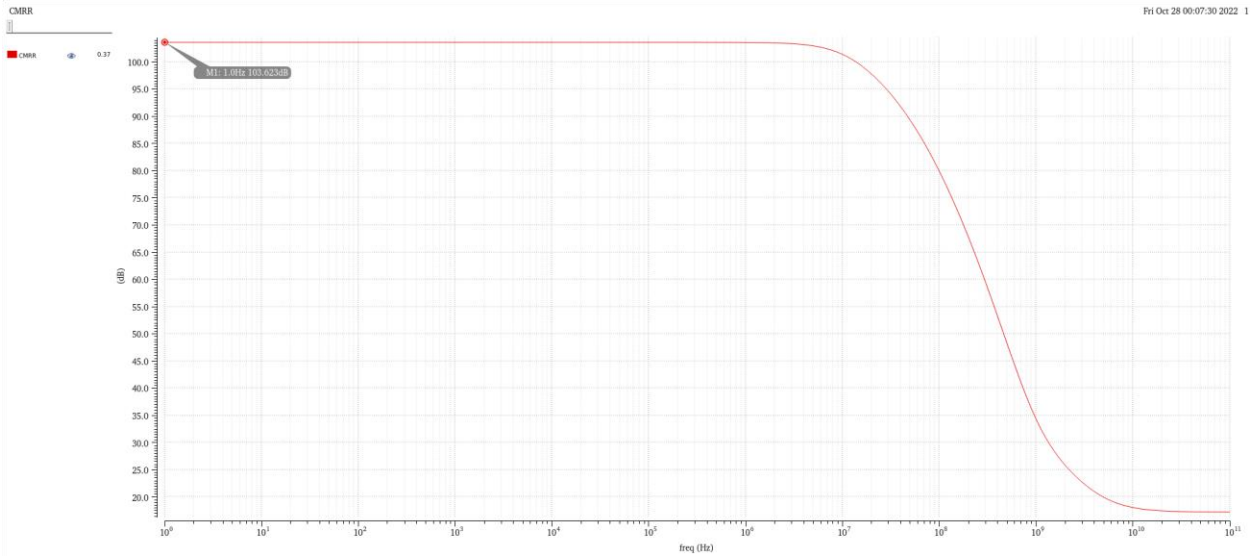


Figure 34: Cascode CMRR – Post

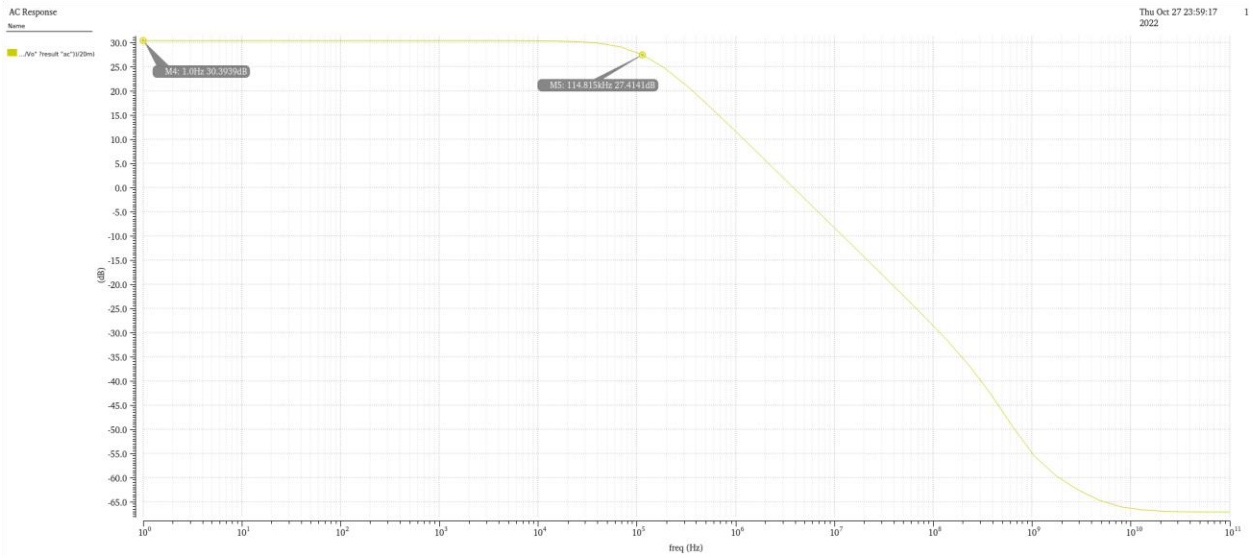


Figure 35: Cascode Pole – Post

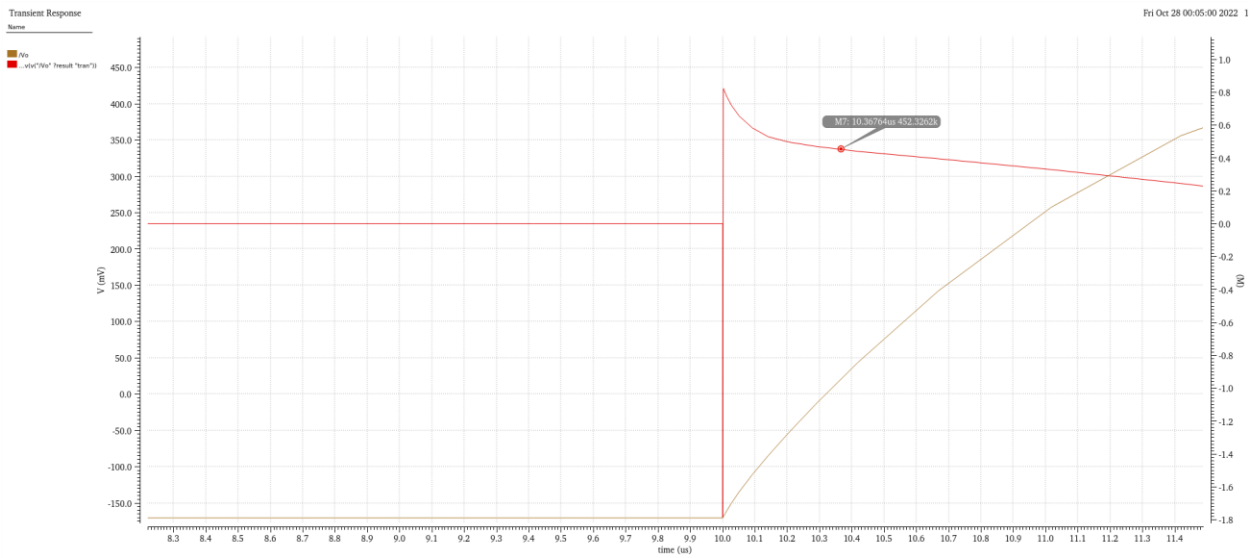


Figure 36: Cascode Slew Rate – Post

Discussion

Comparing the two topologies, the simple differential amplifier displays a far lower ADM and far higher ACM than the cascode amplifier. For this reason, the common mode rejection ratio is far superior on the cascode amplifier, 104dB vs. 61dB. However, this improved performance comes at the cost of common mode voltage range. The cascode amplifier has a very small common mode range, 140mV compared to the simple amplifier's 522mV. The cascode amplifier's bandwidth is slightly worse, which makes sense considering the large devices required in order to keep all devices active.

Post layout, the common mode voltage range decreased in both cases, enough for the cascode to cause one of the transistors to fall out of saturation. To solve this, VBN had to be slightly altered.

In the case of the simple amplifier, both the ADM and ACM improved. However, due to the added capacitances, the bandwidth lowered considerably. For the cascode amplifier, ACM improved significantly while ADM decreased slightly. Again, the bandwidth was much worse due to layout parasitic capacitances. The slew rate was also vastly decreased, likely due to the added output capacitances.

Conclusion

In this lab, two differential amplifier topologies were designed and compared. Post layout simulations were used to compare the behavior of the systems when considering layout parasitics. As always, good design practices were used in the layout such as common centroid, dummy elements, and guard rings.