Lab 2: Layout Design, Simulation, and Verification in Cadence

ECEN 704-601
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Description

In this lab, the design, layout, and simulation of a simple CMOS inverter was performed. Various simulation and verification tools in Cadence were used such as Design Rule Check (DRC), Layout Versus Schematic (LVS), and post layout extraction simulations.

Design

To begin, a simple CMOS inverter was designed in the schematic editor. The inverter consists of a NMOS and PMOS device and off page net connectors. The NMOS device size was set to W/L=0.5u/0.18u and the PMOS device size was set to double this, W/L=1u/0.18u. The schematic is shown below in Figure 1.

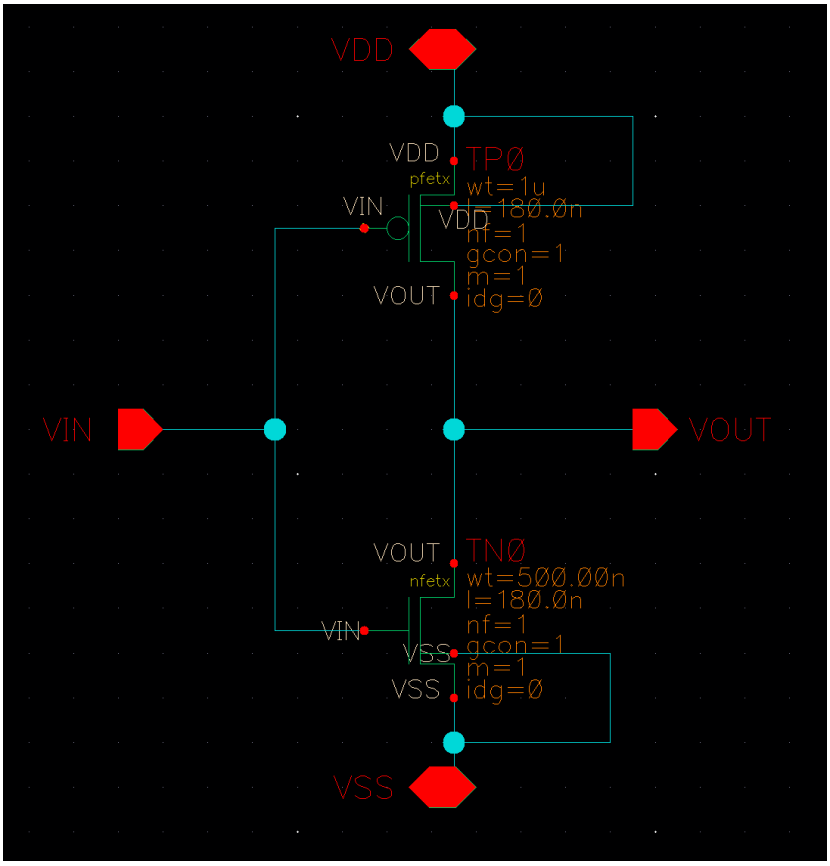

Figure 1: Inverter Schematic

Next, a symbol was created for simplicity of use in the test bench. The symbol is shown below in Figure 2.

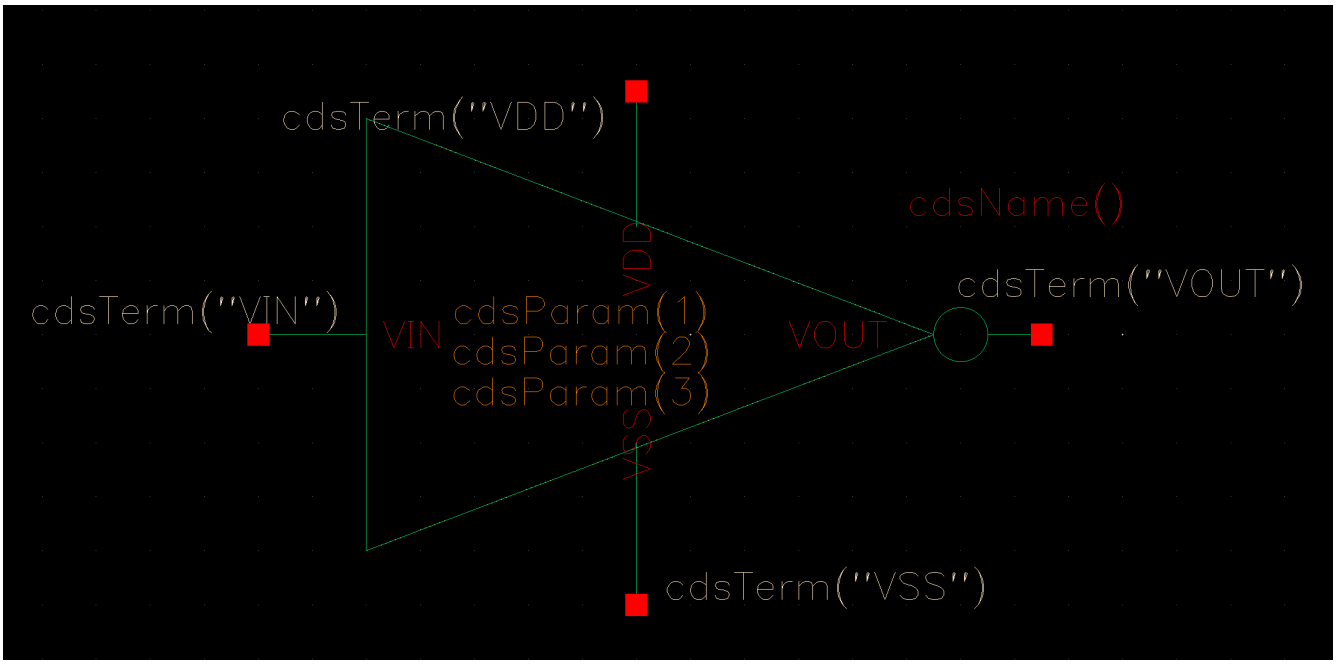

Figure 2: Inverter Symbol

Next, a test bench was created in order to perform DC simulations. The supply voltage VDD was set to be 1.8V and VSS was set to ground. A DC voltage source was placed on the input side, and a 100kΩ resistor was used on the output side as a load. The test bench is shown below in Figure 3.

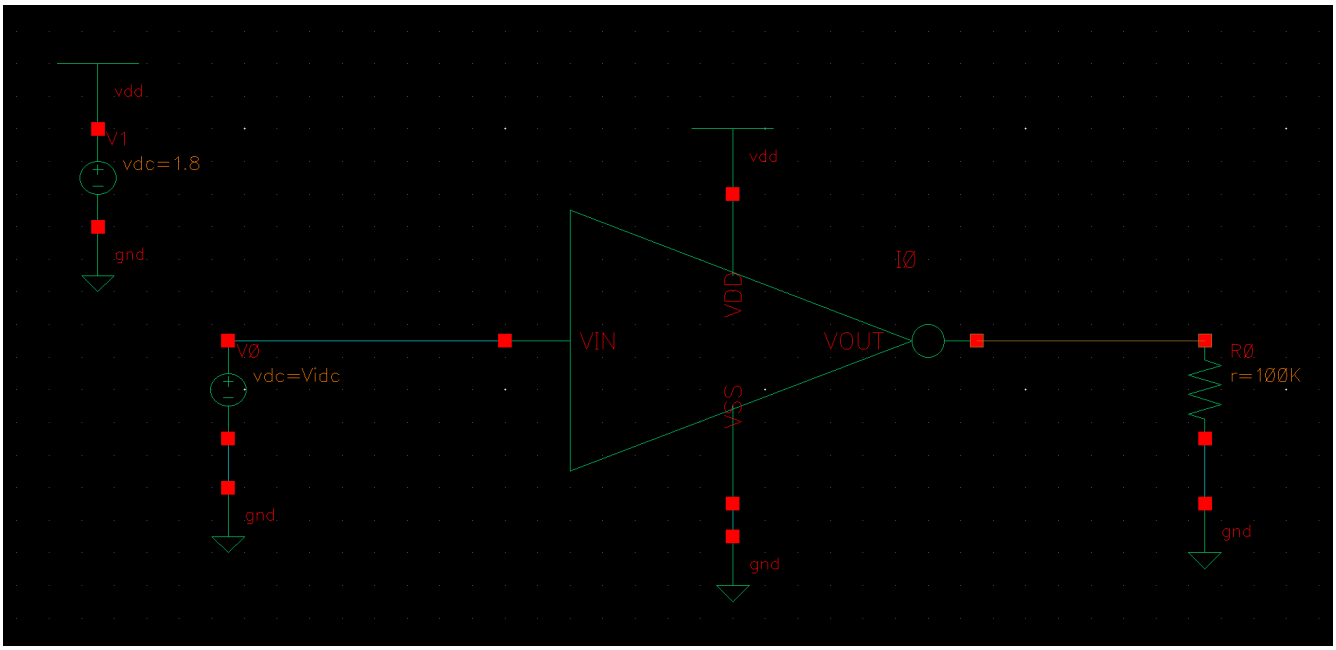

Figure 3: Test Bench Schematic

Next, the layout for the inverter block was performed. A set of 2x5 vias was used for the external connection to both VDD and VSS. The VIN pin was placed on the connection between transistor gates. Lastly, the VOUT pin was placed on the connection between transistor drains. The completed layout is shown below in Figure 4.

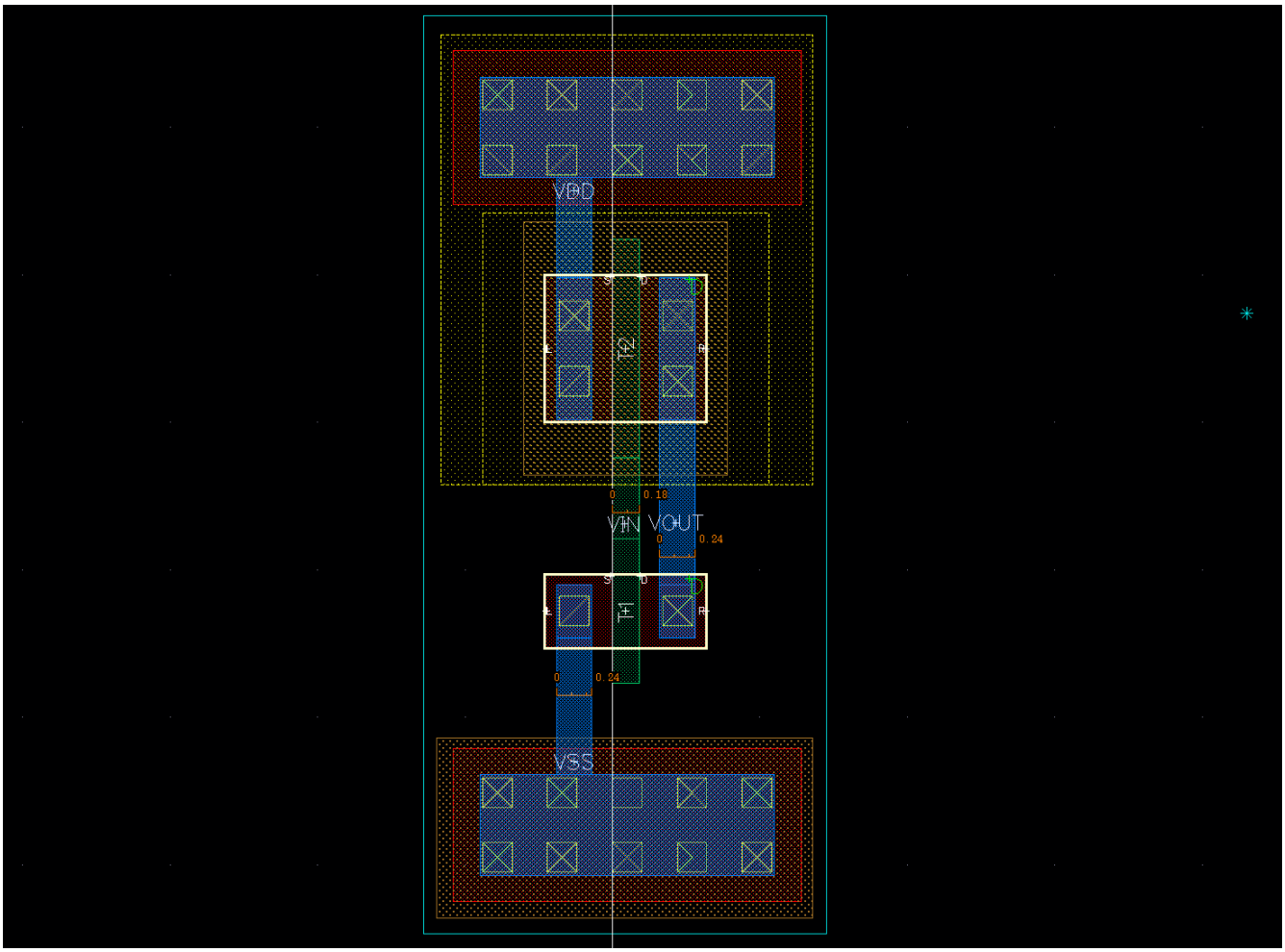

Figure 4: Inverter Layout

From here, various simulation and verification steps were taken.

Results

Once the initial schematic design was completed, a DC sweep was performed over Vin, plotting Vout to demonstrate the functionality of the inverter. The plot is shown below in Figure 5.

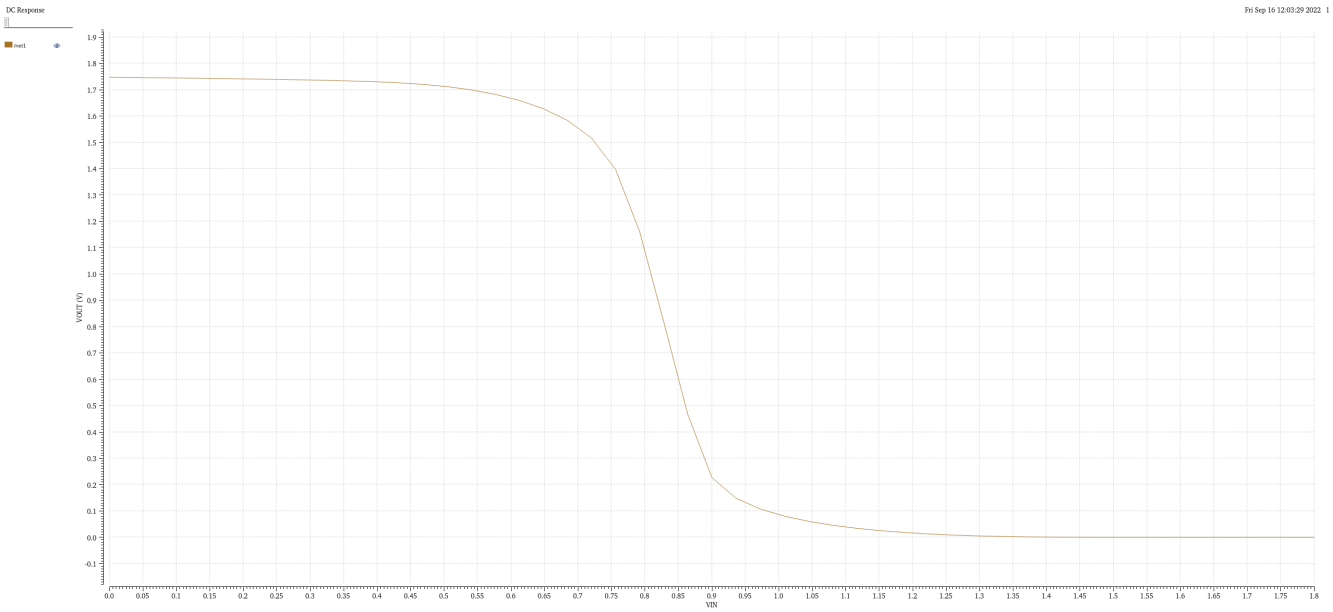

Figure 5: Vout vs. Vin DC Sweep (Pre-Layout)

Next, the layout for the inverter was completed. The DRC check (Figure 6) yielded no errors except for a density warning, which is not a consideration for the scope of this course, but is important for fabrication. Finally, a LVS check (Figure 7) was completed successfully for the design.

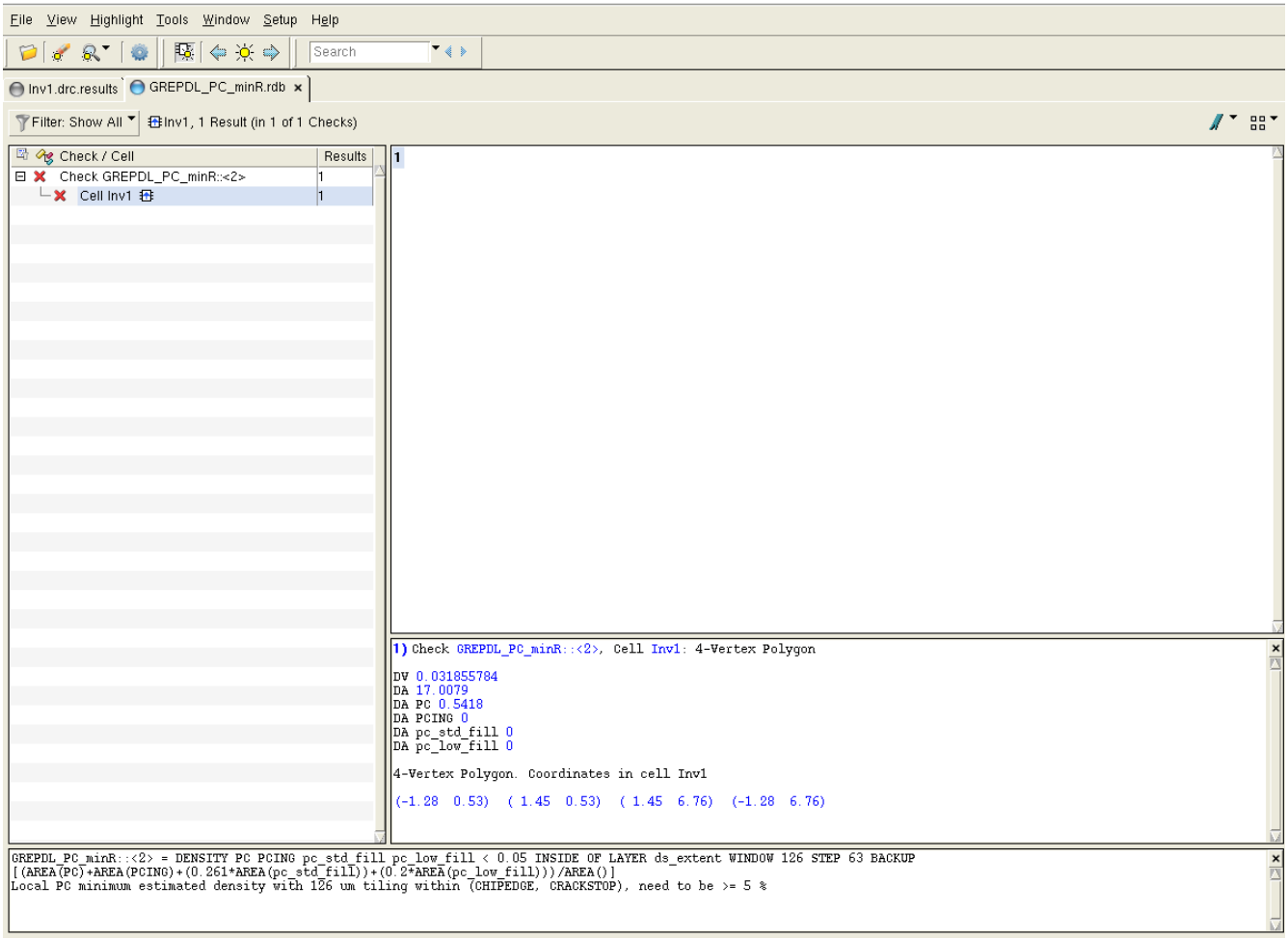

Figure 6: DRC Check

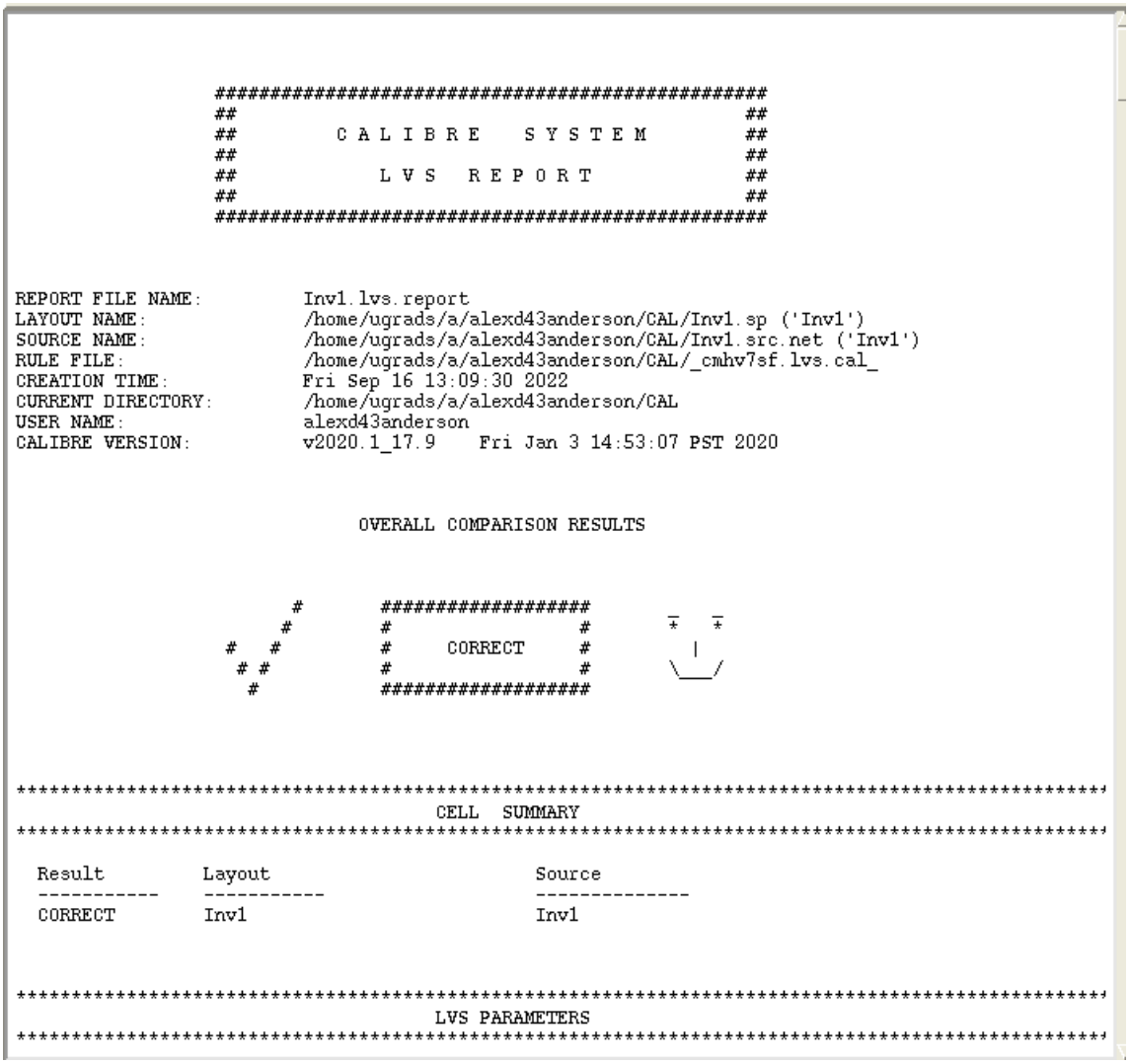

Figure 7: LVS Check

Next, with the completed and verified layout, the parasitics were extracted from the layout and used to complete another DC sweep simulation, this time considering these effects (Figure 8).

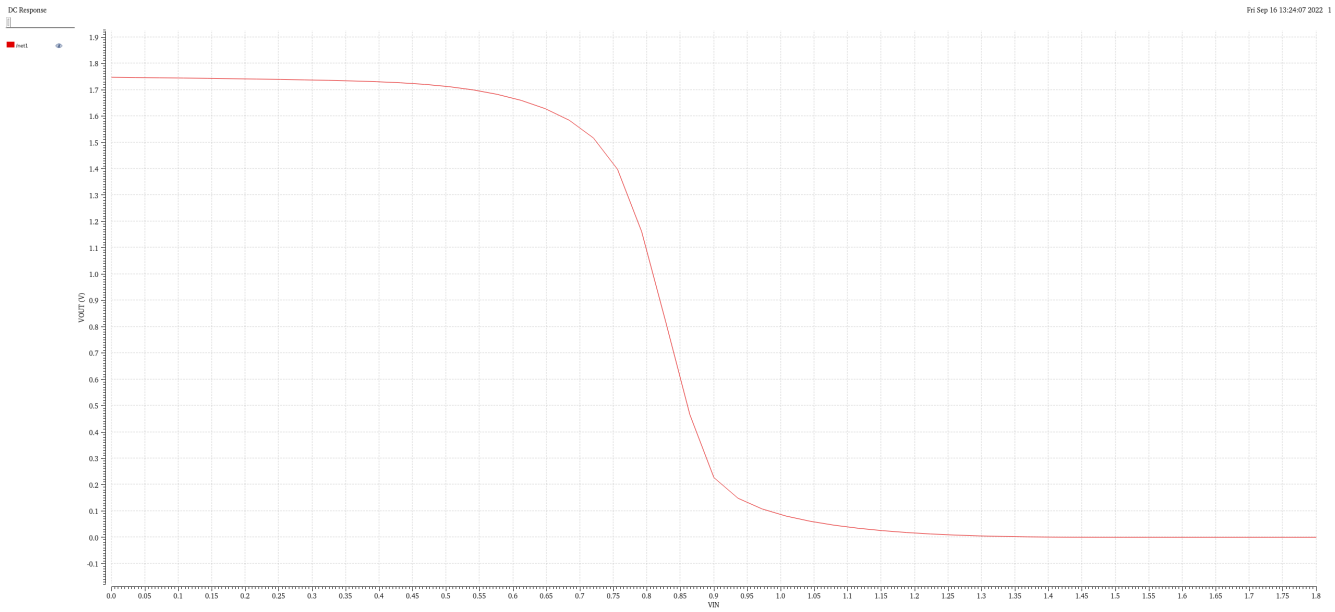

Figure 8: Vout vs. Vin DC Sweep (Post-Layout)

Discussion

No noticeable difference is seen in the post-layout simulation compared to the pre-layout simulation, however this is expected due to the fact it is a DC sweep. The effects of parasitics such as capacitances or inductances will only be realized for high-frequency signals or components, such as the rising edge of a transient signal. If a transient simulation was performed, the waveform would display a slower rise/fall time and perhaps more overshoot/undershoot compared to the pre-layout simulation.

Conclusion

In this lab, the basic layout and verification of a CMOS inverter was completed. Various simulation tools available in Cadence for layout verification such as DRC and LVS were used to check the design. Finally, a DC simulation was performed both pre and post layout to verify the DC characteristics of the circuit.