Lab 3: Layout Design Techniques

ECEN 704-601
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Description

In this lab, the design and layout of a simple current mirror, capacitor array, and matched resistors was performed. Layout techniques such as inter-digitization, common centroid, and dummy elements were used to ensure effective device matching.

Design

To start, a floorplan for the current mirror was created (Figure 1). To achieve the desired width of 16um, the two devices were split each into 32 smaller transistors of size W/L=0.5u/0.18u. A layout of 16 elements per row for a total of 4 rows, and 8 total dummy elements was used.

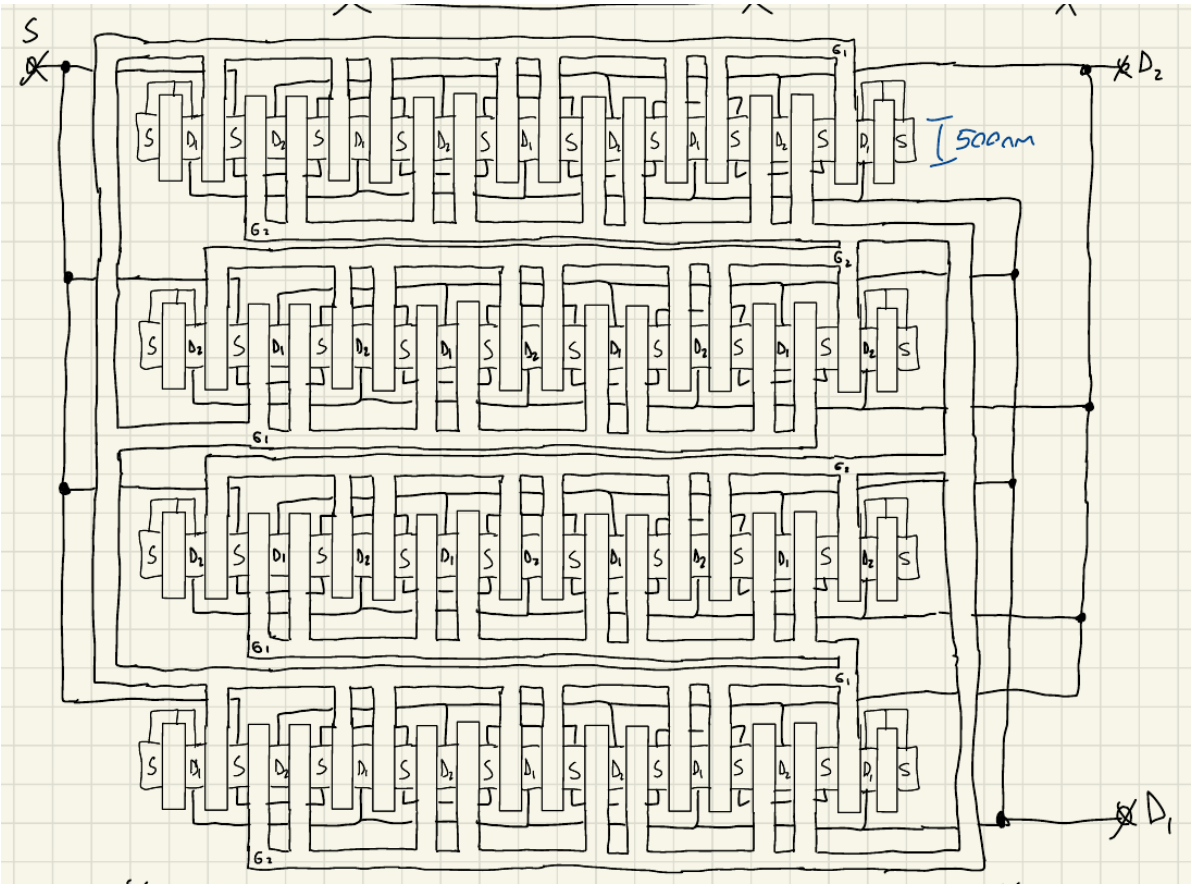

Figure 1: Current Mirror Floorplan

Next, a capacitor array of two capacitors was designed. The array consists of 8 unit capacitors and 1 non-unit. The capacitor ratio was set to be 1.3:1 and the unit capacitor size used was 10.56um x 10.56um. To find the multiplier for the non-unit capacitor, N, the following equation can be used:

$$\frac{C_1}{C_2}=\frac{I_1 C_u}{I_2 C_u + N C_u}$$

where I_1 is the number of unit capacitors for C_1 and I_2 is the number of unit capacitors for C_2. In this case, for $I_1=I_2=4$, we find that N=1.2. To find the non-unit capacitor width and length, we simply use the following set of equations:

$$L_{nu}=L_0\left(N+\sqrt{N(N-1)}\right)$$

$$W_{nu} = N \frac{L_0^2}{L_{nu}}$$

For this set of values, we find that L=17.845um and W=8.124um. Lastly, a floorplan was created for the layout (Figure 2), including 16 dummy elements on the outside edge.

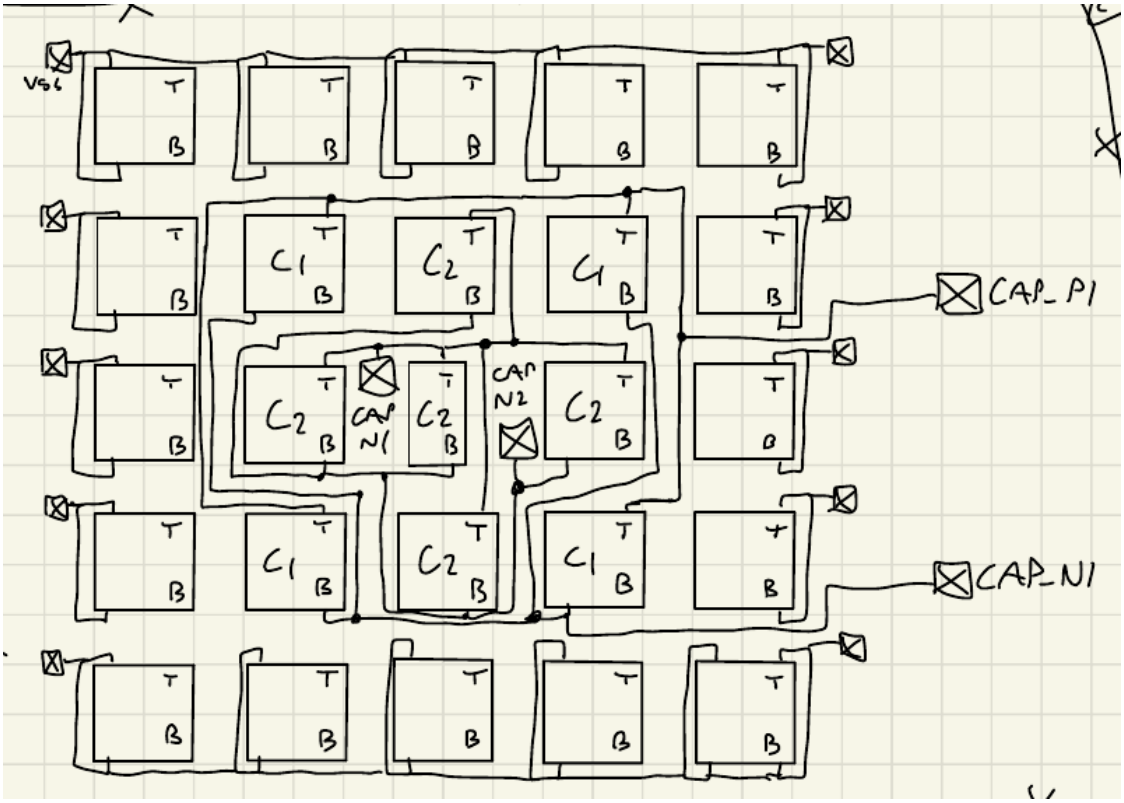

Figure 2: Capacitor Array Floorplan

Next, two matched 12kΩ resistors were designed. To calculate the resistance, including contact resistance, the following formula can be applied:

$$R_{nom} = R_s \frac{L}{W} + 2 \frac{R_{con}}{W}$$

The process parameters R_s and R_{con} equal 0.165 kΩ/sq and 0.015 kΩ-um respectively (nominal values). From here, W was taken to be 0.32um, the minimum possible. Solving for L using the desired resistance and other parameters, a value of 3.967um is obtained. A floorplan was drawn for the elements (Figure 3), including inter-digitization and two dummy elements on either side of the array.

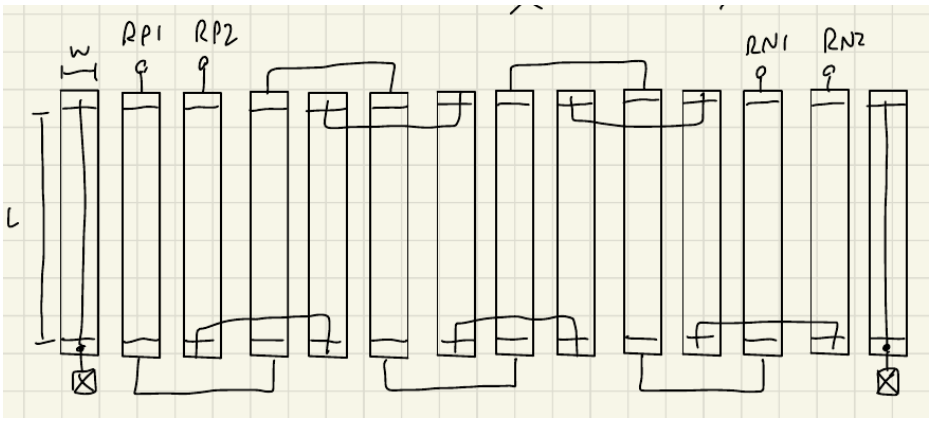

Figure 3: Matched Resistors Floorplan

Results

First, the simple current mirror was created in the schematic editor, including dummy elements.

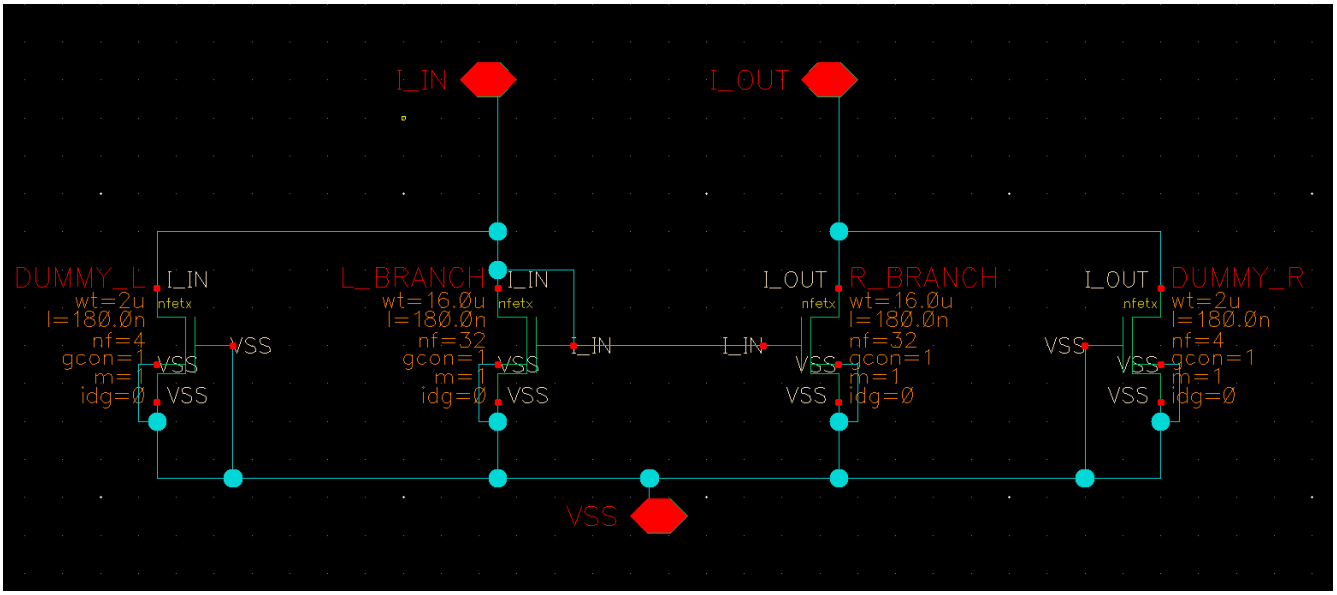

Figure 4: Current Mirror Schematic

Next, the layout was performed. The sources of both transistors were routed on metal 1. The drains of the left and right transistors were routed on metal 2 and 3 respectively. The gate and source of the dummy elements were shorted and connected to VSS to ensure they will remain off.

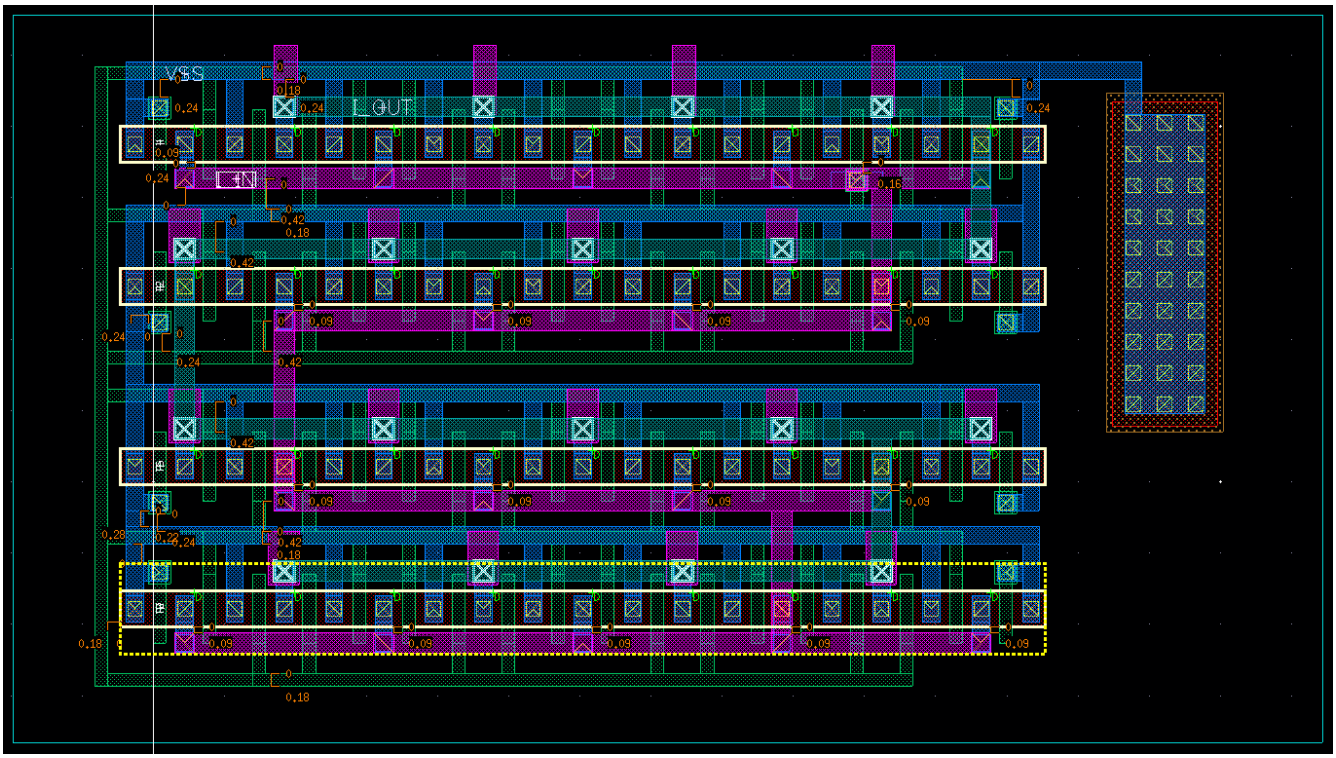

Figure 5: Current Mirror Layout

Next, verification of the design was completed using DRC and LVS. Both were successful with the exception of density errors in DRC as expected.

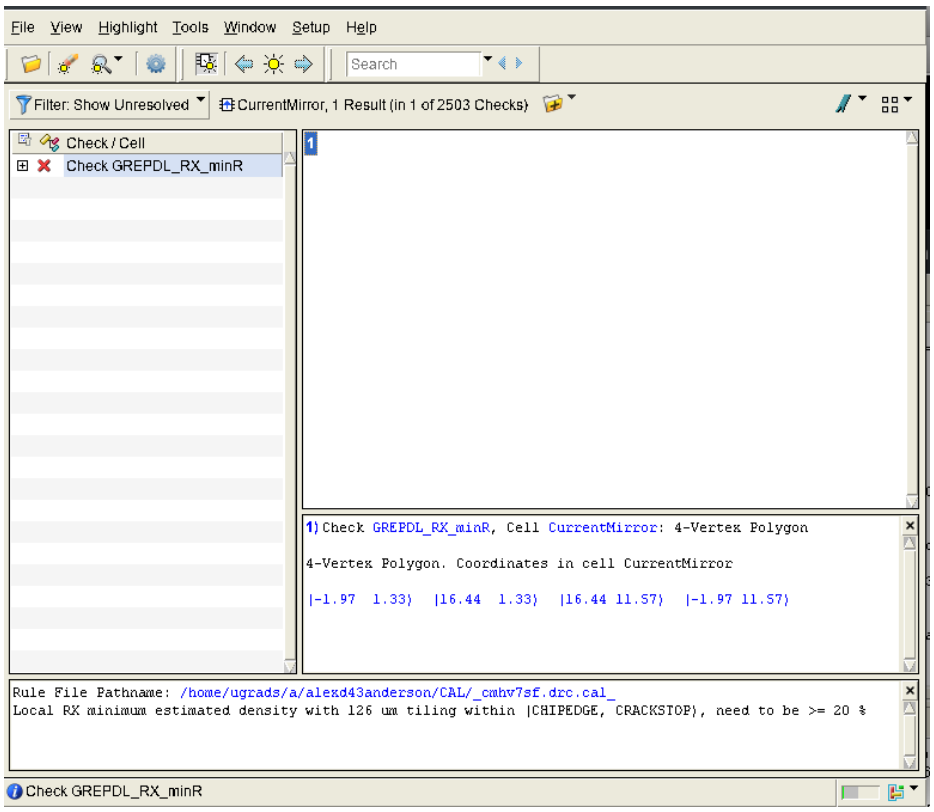

Figure 6: Current Mirror DRC

```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################


REPORT FILE NAME:         CurrentMirror.lvs.report
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SOURCE NAME:              /home/ugrads/a/alexd43anderson/CAL/CurrentMirror.src.net |'CurrentMirror'}
RULE FILE:                /home/ugrads/a/alexd43anderson/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Fri Sep 23 16:08:04 2022
CURRENT DIRECTORY:        /home/ugrads/a/alexd43anderson/CAL
USER NAME:                alexd43anderson
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                        OVERALL COMPARISON RESULTS


                      #       ####################       _   _
                     #        #                  #       *   *
                #   #         #     CORRECT      #         |
                 # #          #                  #       \___/
                  #           ####################


********************************************************************************************************
                                    CELL  SUMMARY
********************************************************************************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        CurrentMirror               CurrentMirror
```

Figure 7: Current Mirror LVS

Next, the capacitor array was created in the schematic editor, including dummy elements.

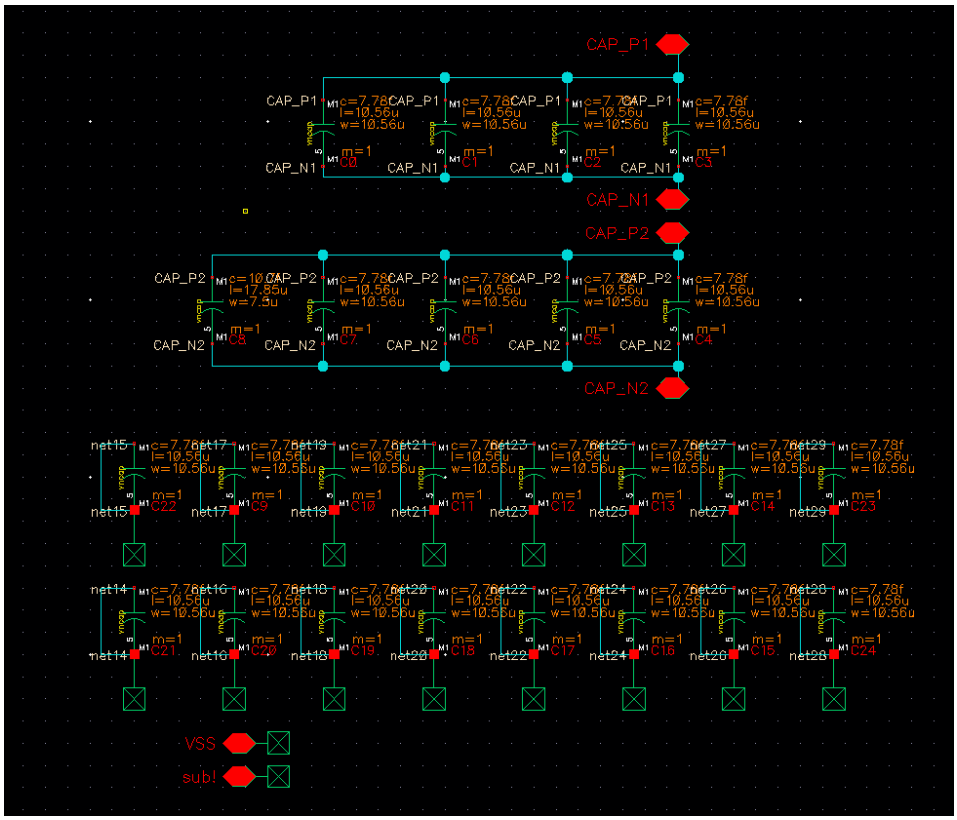


Figure 8: Capacitor Array Schematic

Next, the layout was performed. The terminals of C1 were connected using metal 2, and the terminals of C2 were connected using metal 3. The dummy elements were shorted together using metal 1.

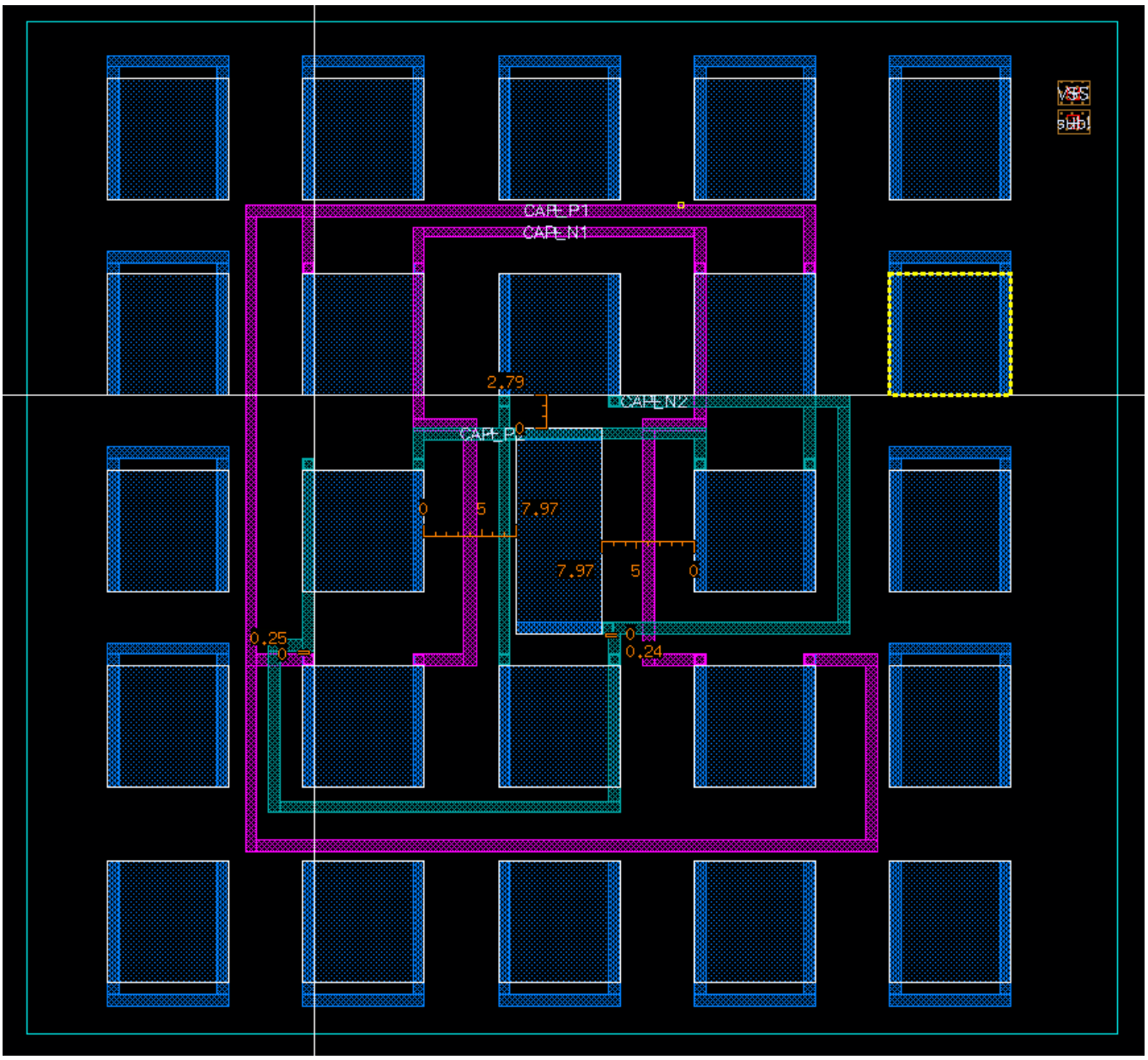


Figure 9: Capacitor Array Layout

Verification of the array was completed using DRC and LVS. Both were successful with no errors.

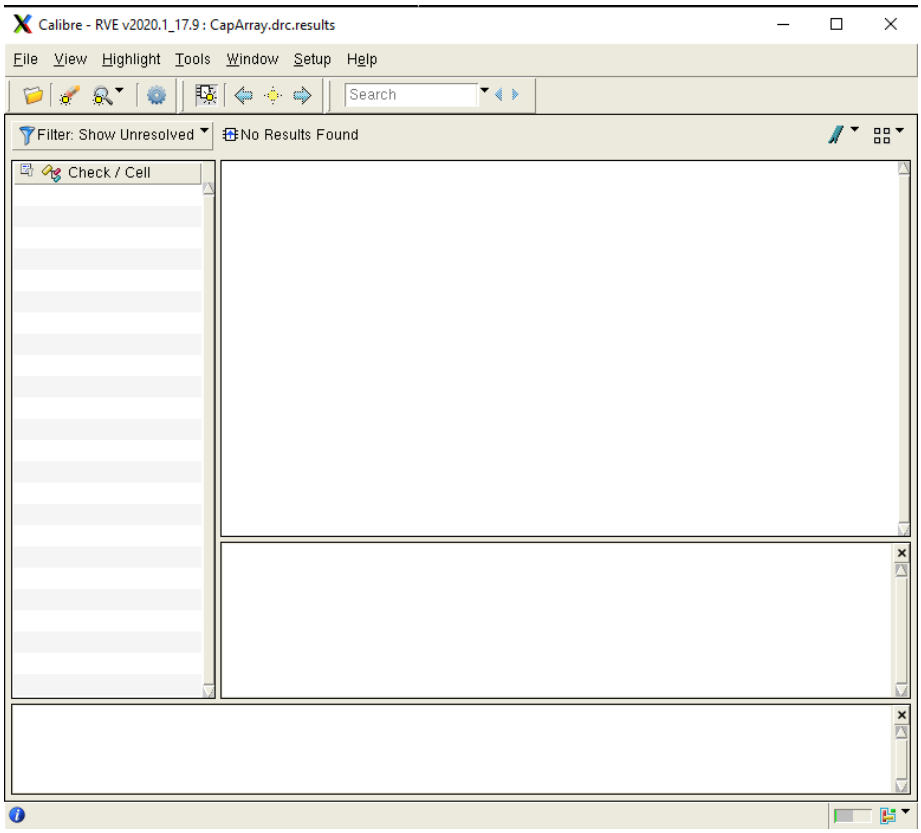
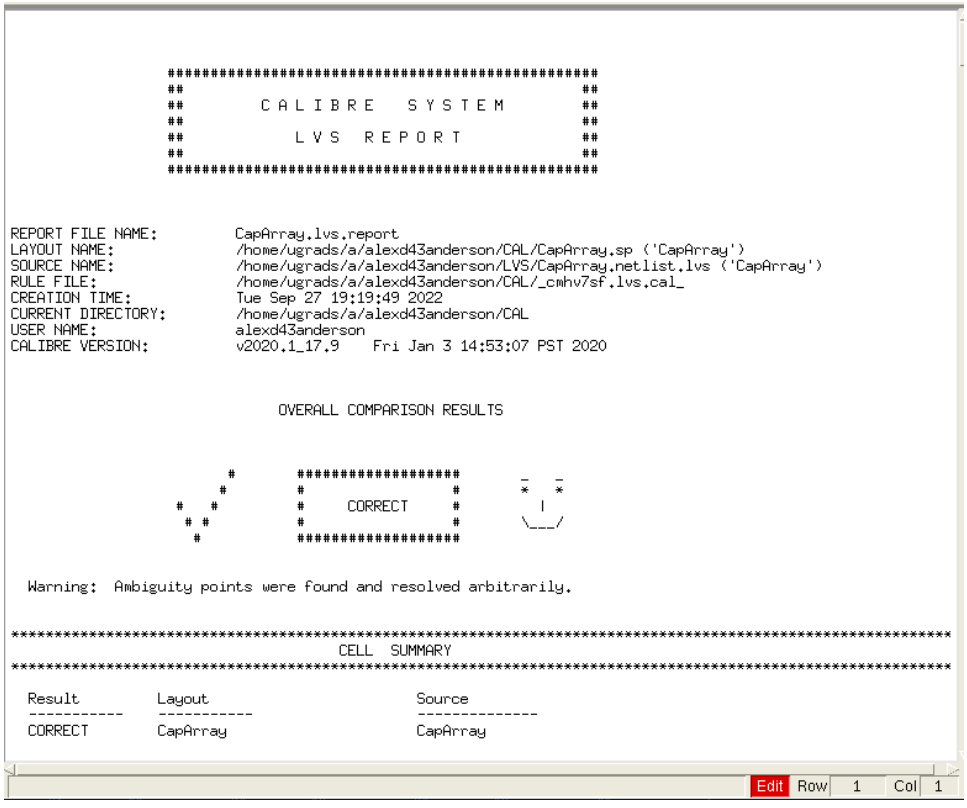


Figure 10: Capacitor Array DRC



```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##           L V S   R E P O R T              ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         CapArray.lvs.report
LAYOUT NAME:              /home/ugrads/a/alexd43anderson/CAL/CapArray.sp ('CapArray')
SOURCE NAME:              /home/ugrads/a/alexd43anderson/LVS/CapArray.netlist.lvs ('CapArray')
RULE FILE:                /home/ugrads/a/alexd43anderson/CAL/_cmhv7sf.lvs.cal_
CREATION TIME:            Tue Sep 27 19:19:49 2022
CURRENT DIRECTORY:        /home/ugrads/a/alexd43anderson/CAL
USER NAME:                alexd43anderson
CALIBRE VERSION:          v2020.1_17.9    Fri Jan 3 14:53:07 PST 2020


                          OVERALL COMPARISON RESULTS


                      #       ##################       _   _
                    #         #                #       *   *
                  #   #       #    CORRECT     #         |
                   # #        #                #       \___/
                    #         ##################


  Warning:  Ambiguity points were found and resolved arbitrarily.


*****************************************************************************************************************
                                    CELL  SUMMARY
*****************************************************************************************************************

  Result          Layout                    Source
  -----------     -----------               --------------
  CORRECT         CapArray                  CapArray
```

Figure 11: Capacitor Array LVS

Lastly, the matched resistors were created in the schematic editor, including dummy elements.

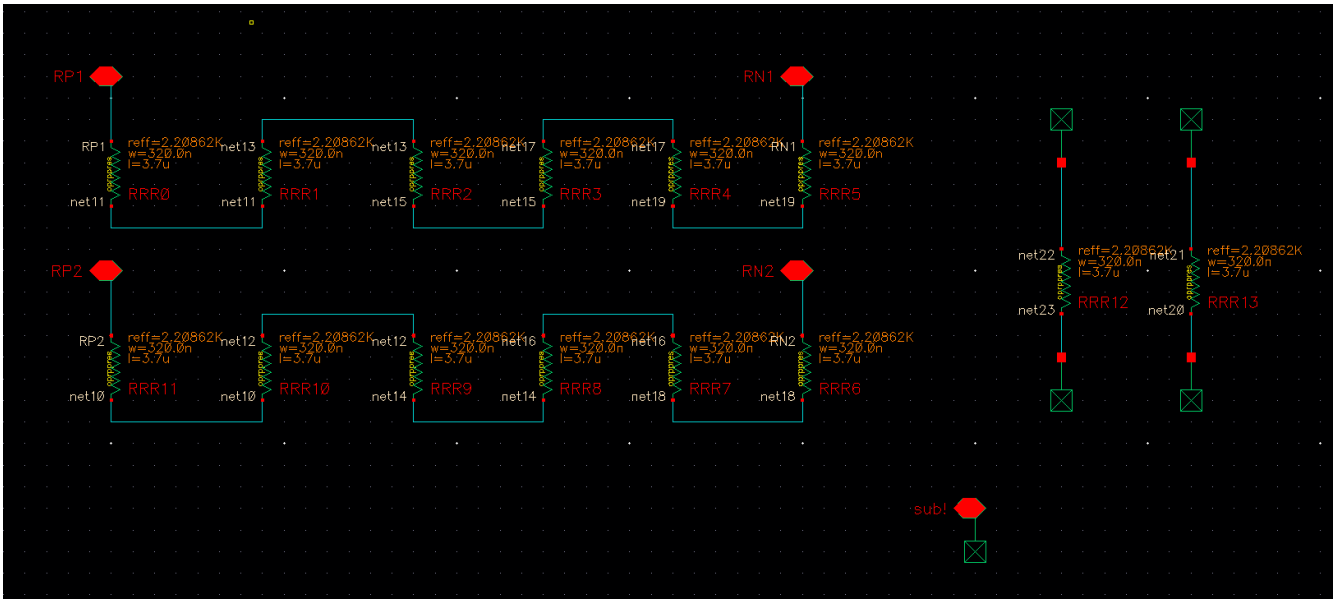


Figure 12: Matched Resistors Schematic

Next, the layout was performed. All wiring was done using metal 1.

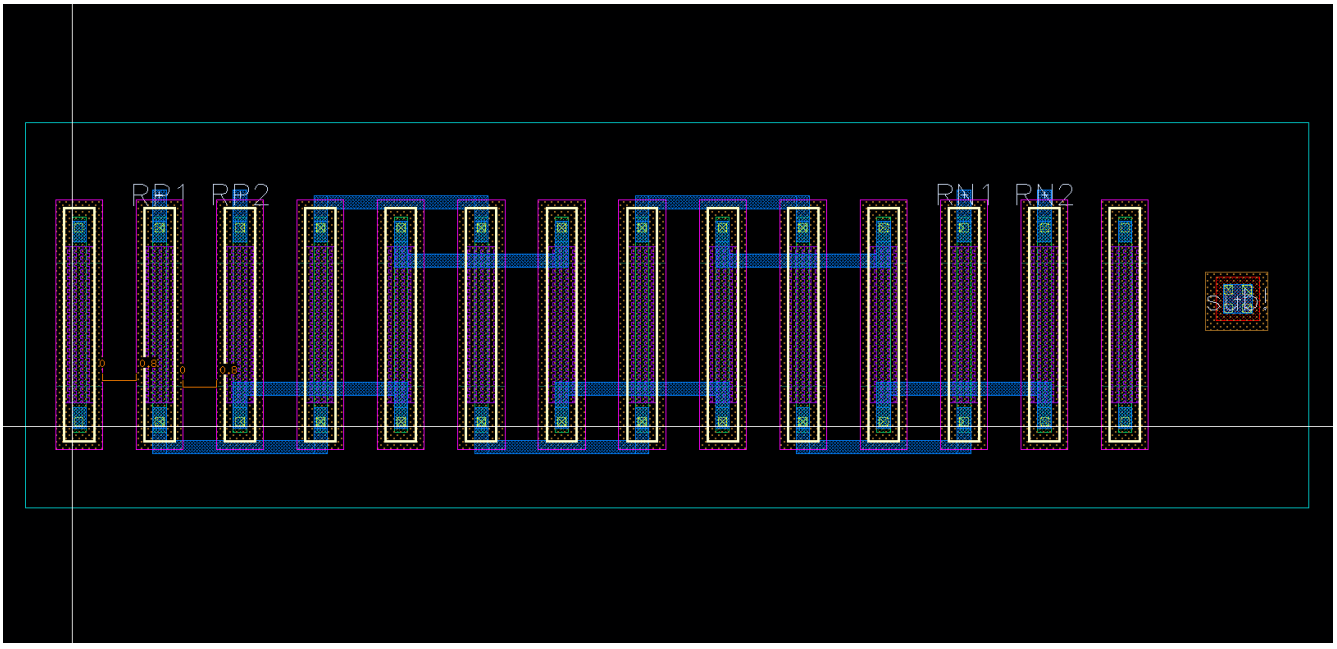


Figure 13: Matched Resistors Layout

Finally, verification of the layout was completed using DRC and LVS. Both were successful with the exception of DRC density errors, again as expected.

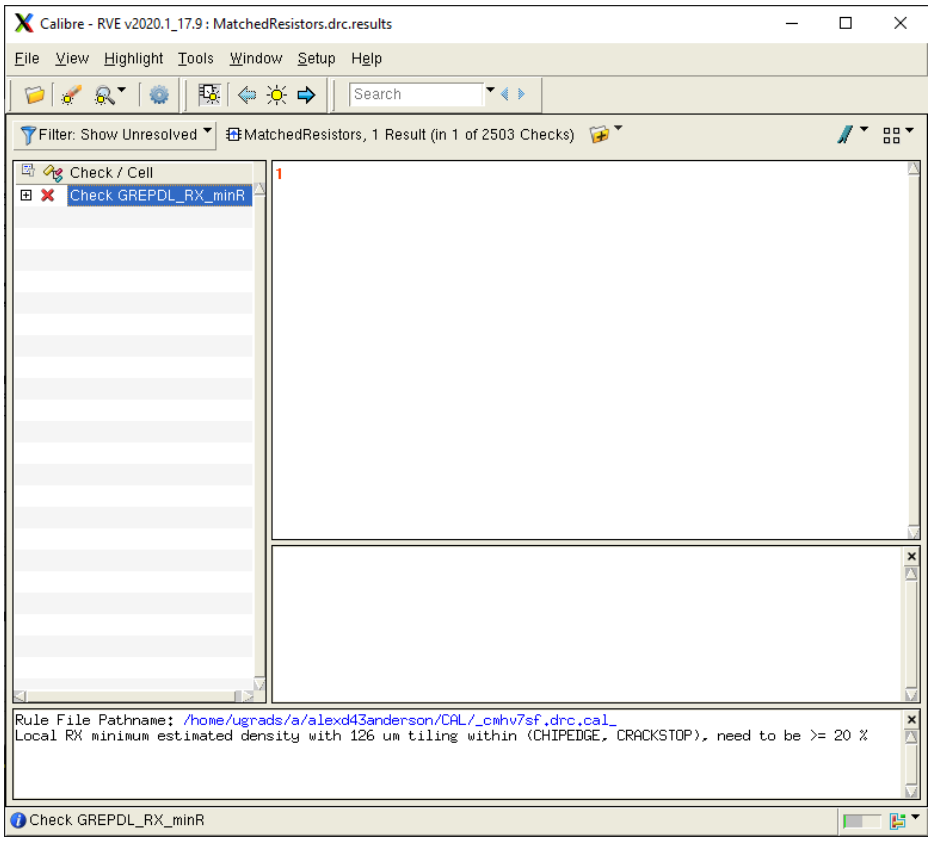


Figure 14: Matched Resistors DRC

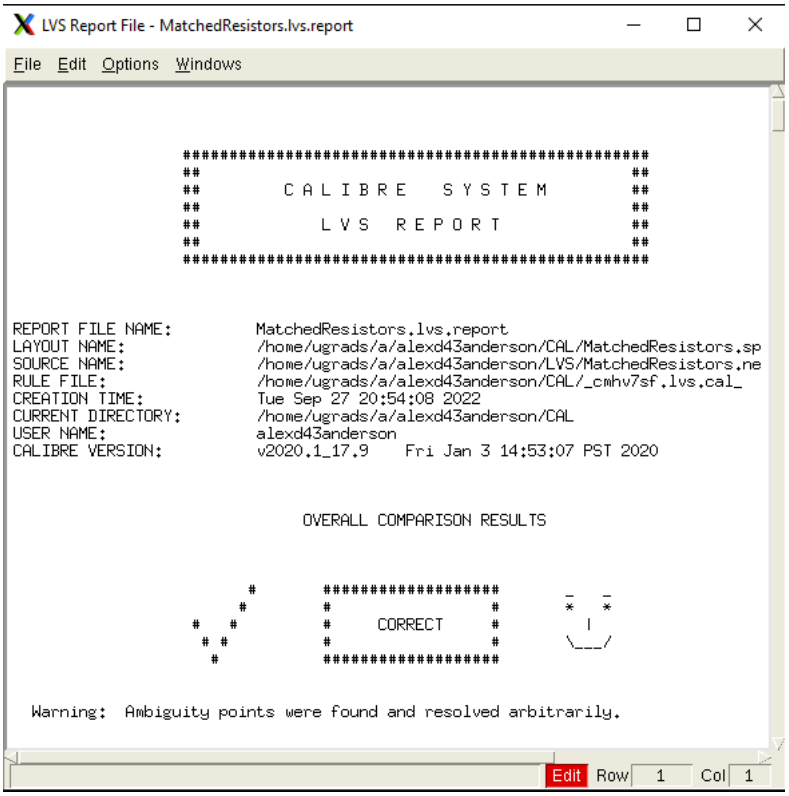


Figure 15: Matched Resistors LVS

Discussion

Layout techniques such as inter-digitization and common centroid are extremely useful in producing matched elements. Due to process and wafer variations, common centroid places the “center of mass” of each element in the same spot, ensuring the process variations will average out for both devices. This strategy is useful for devices such as current mirrors or differential amplifiers, where symmetry must be maintained to ensure linear and consistent operation.

Dummy elements are used to ensure that critical devices are fabricated correctly and accurately by acting as a “buffer”. By combining these techniques and using symmetrical design practices, chip robustness to process variation can be increased greatly.

Conclusion

In this lab, layout techniques such as inter-digitization, common centroid, and dummy elements were used to ensure effective device matching for a simple current mirror, capacitor array, and pair of resistors. Additionally, greater familiarity with the process and design rules was obtained during the layout process.