Lab 2: Introduction to Cadence Schematic Capture & Simulation

Alex Anderson

UIN: 728001757

ECEN 714-603

Inverter:

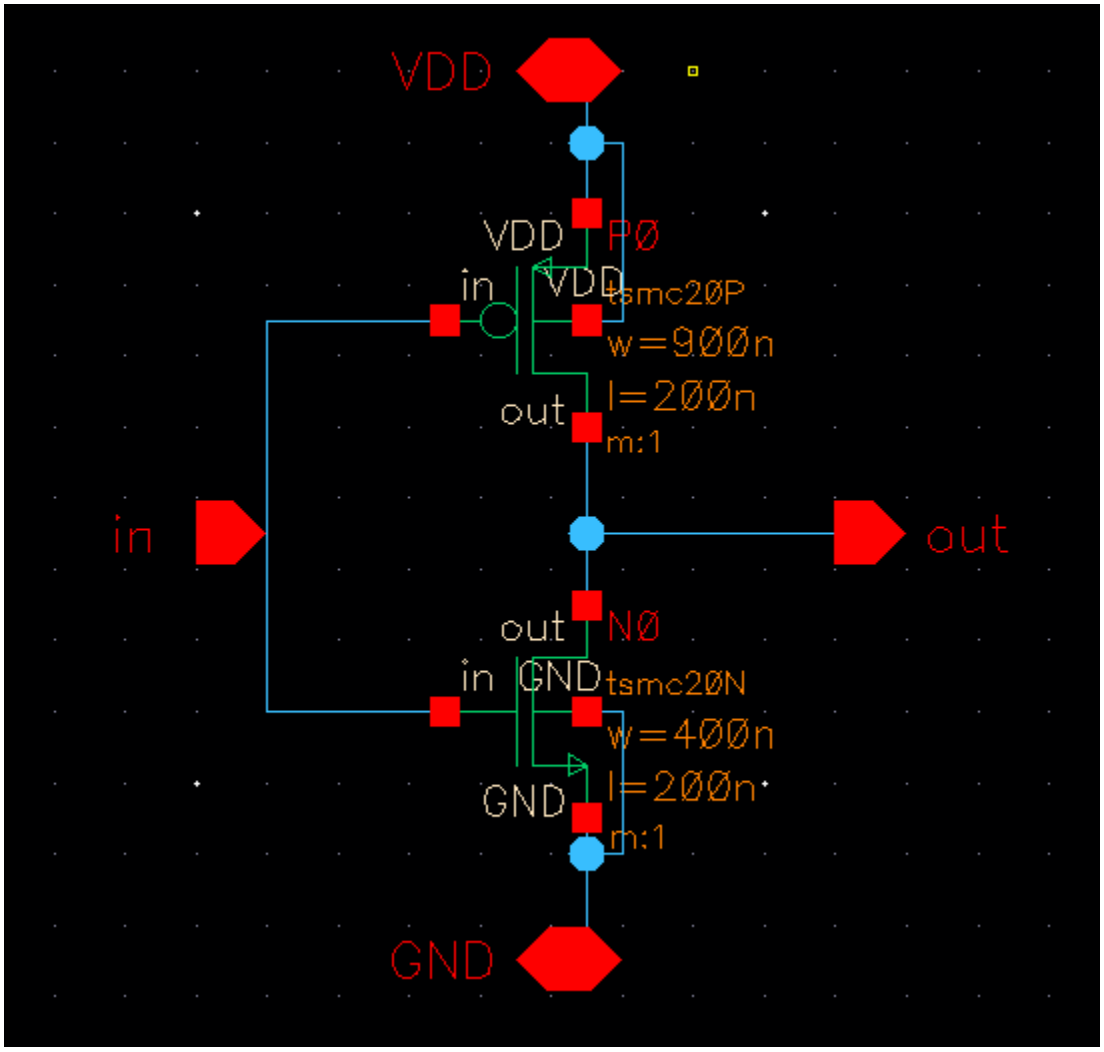

Figure 1: Inverter Schematic

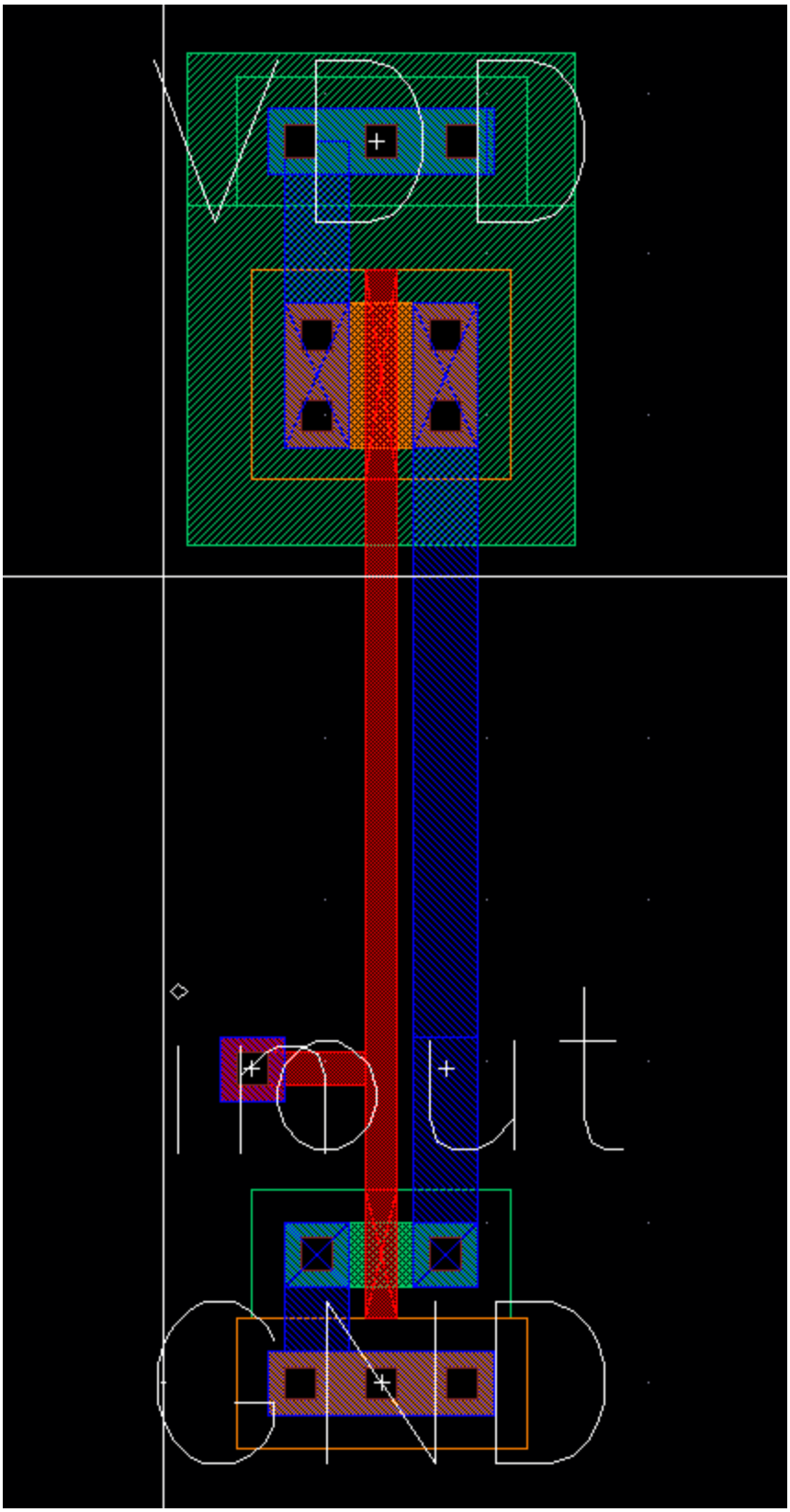

Figure 2: Inverter Layout

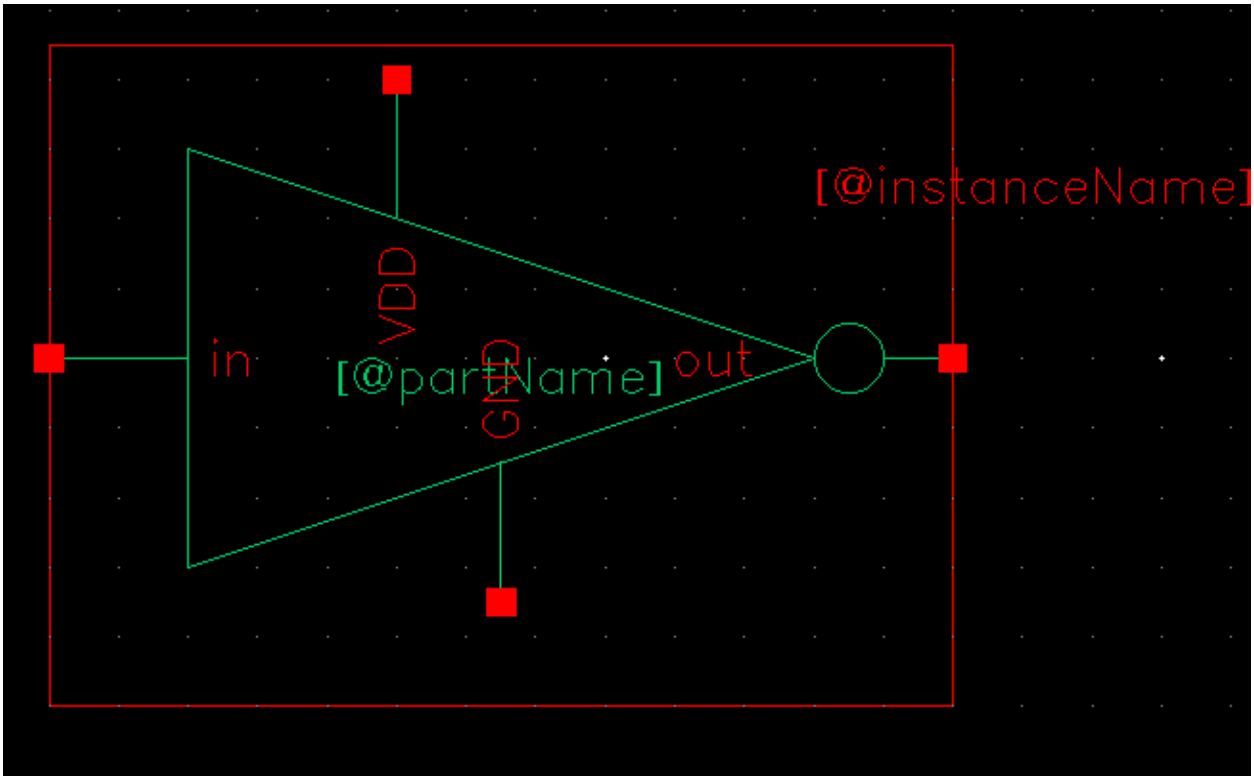

Figure 3: Inverter Symbol

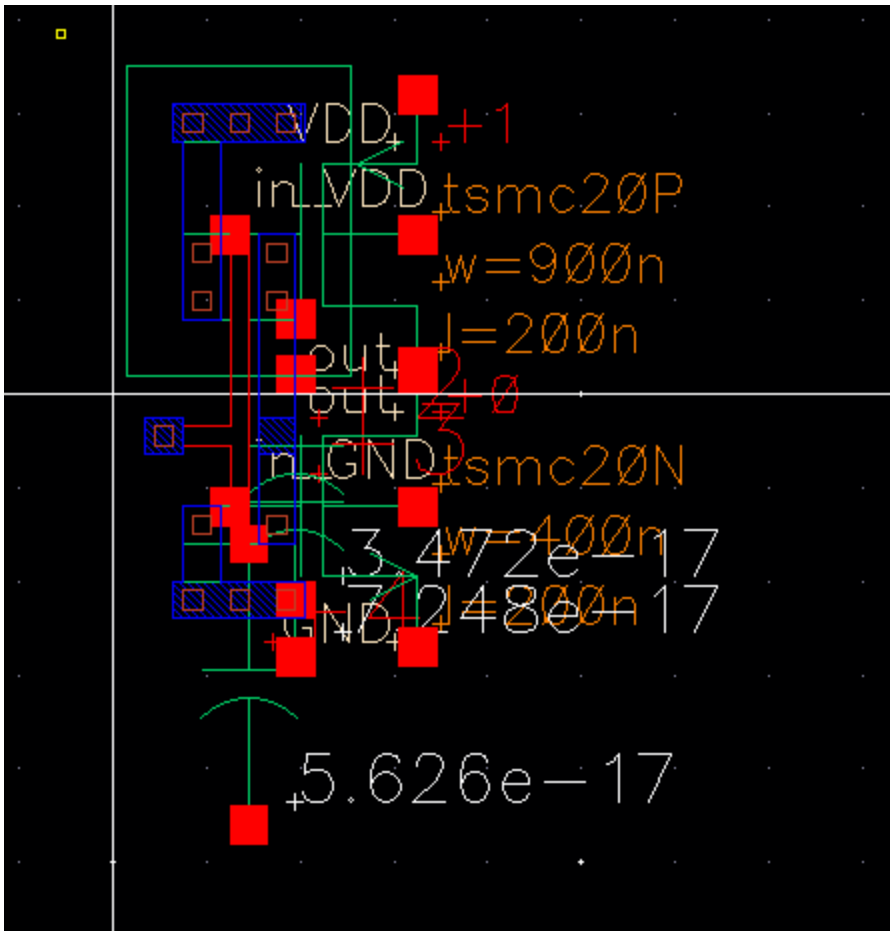

Figure 4: Inverter Extracted View

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@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexd43anderson/ecen714/LVS -l -s -t /home/ug
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0          N3          GND
    N3          N1          VDD
    N2          N0          in
    N1          N2          out

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched                  0       0
        rewired                     0       0
        size errors                 0       0
        pruned                      0       0
        active                      2       2
        total                       2       2
```

Figure 5: Inverter LVS Check

NAND2:

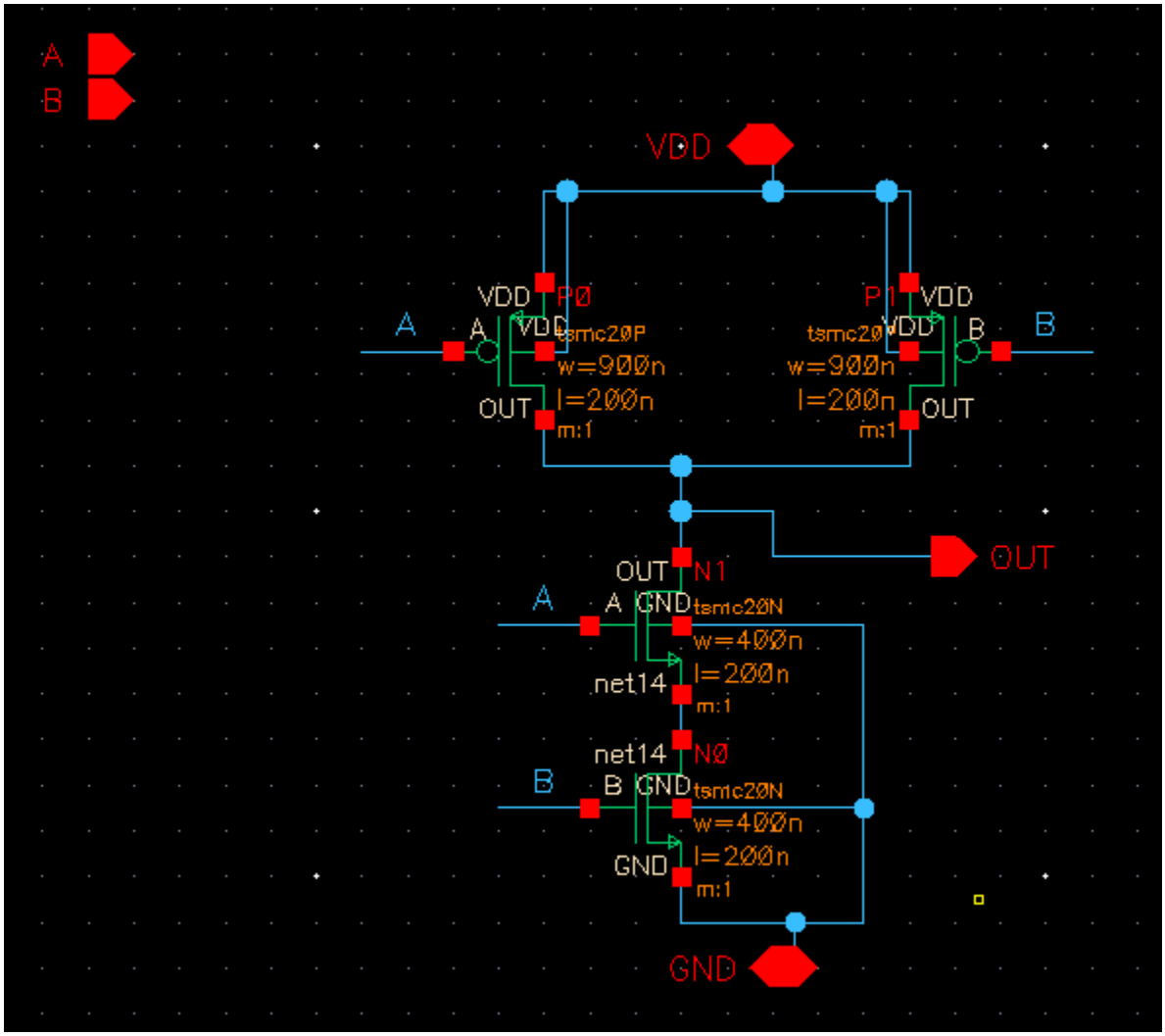

Figure 6: NAND2 Schematic

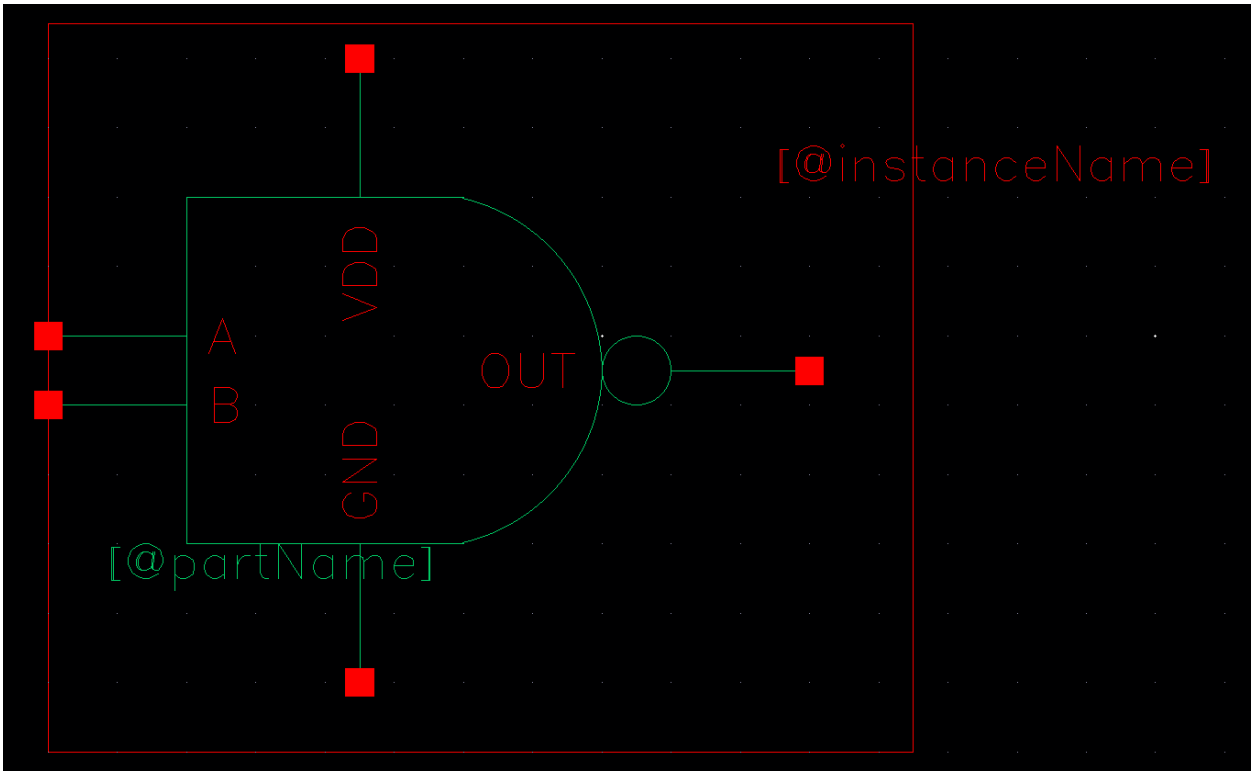

Figure 7: NAND2 Symbol

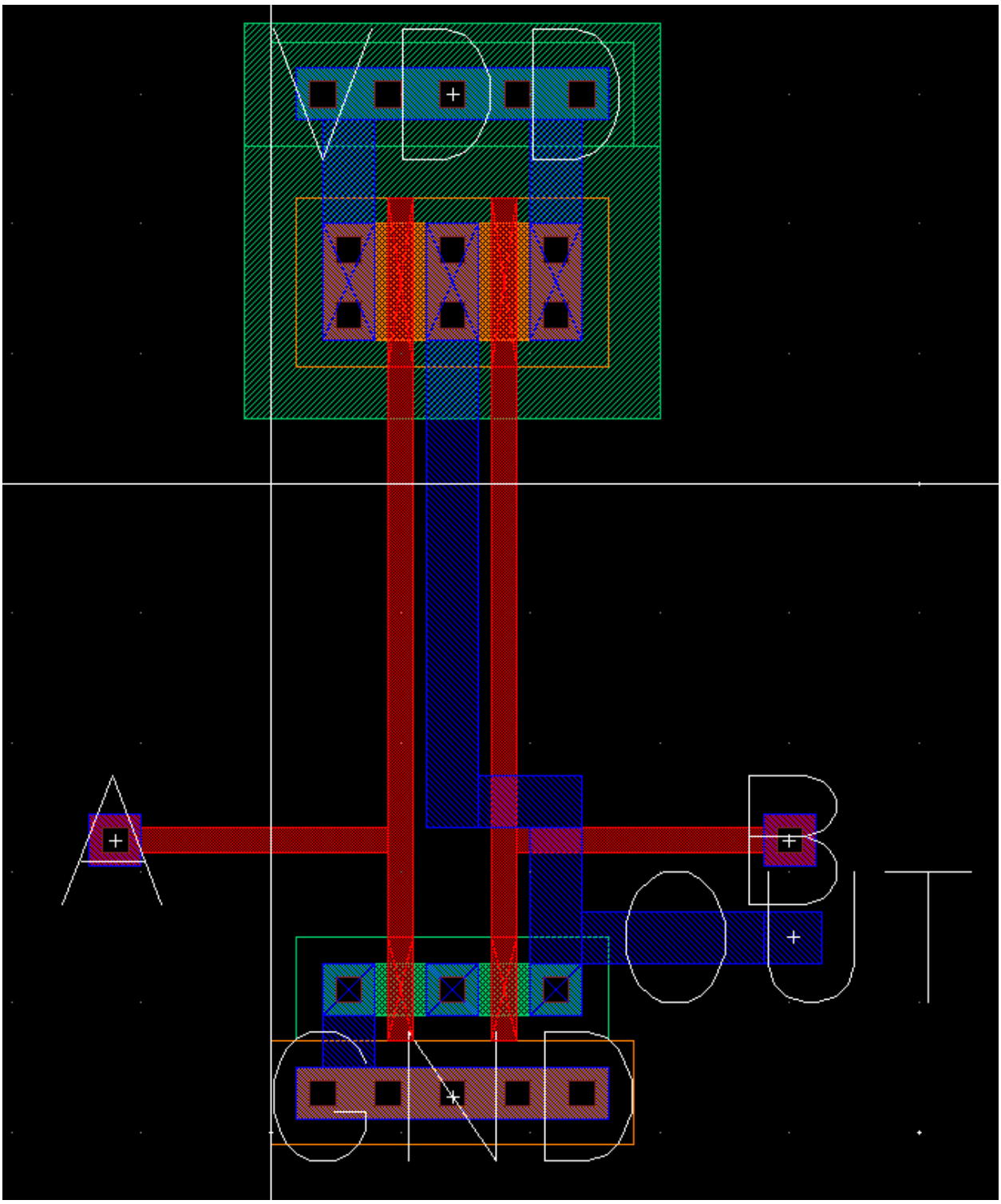

Figure 8: NAND2 Layout

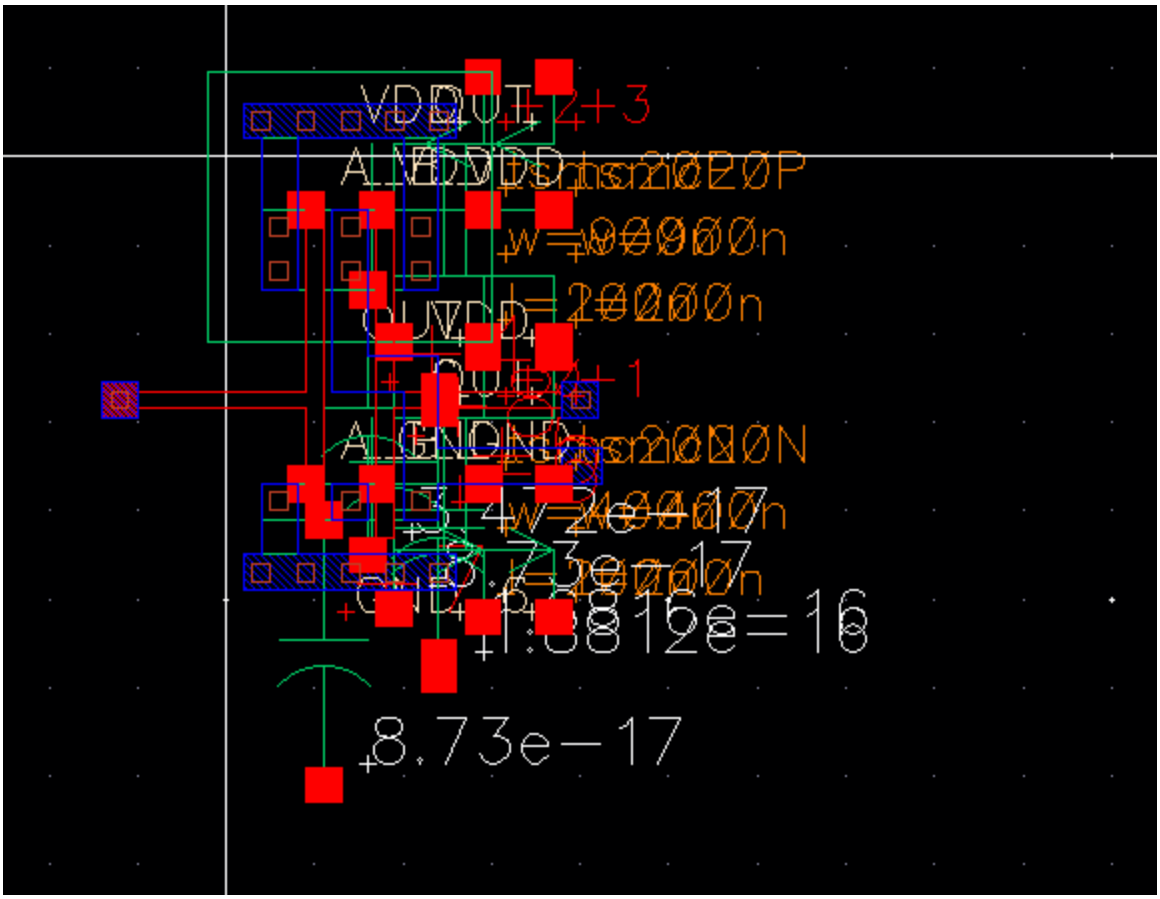

Figure 9: NAND2 Extracted View

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@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexd43anderson/ecen714/LVS -l -s -t /home/u
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N4        N3        A
    N3        N5        B
    N1        N0        GND
    N2        N1        OUT
    N5        N2        VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4
```

Figure 10: NAND2 LVS Check

XOR2:

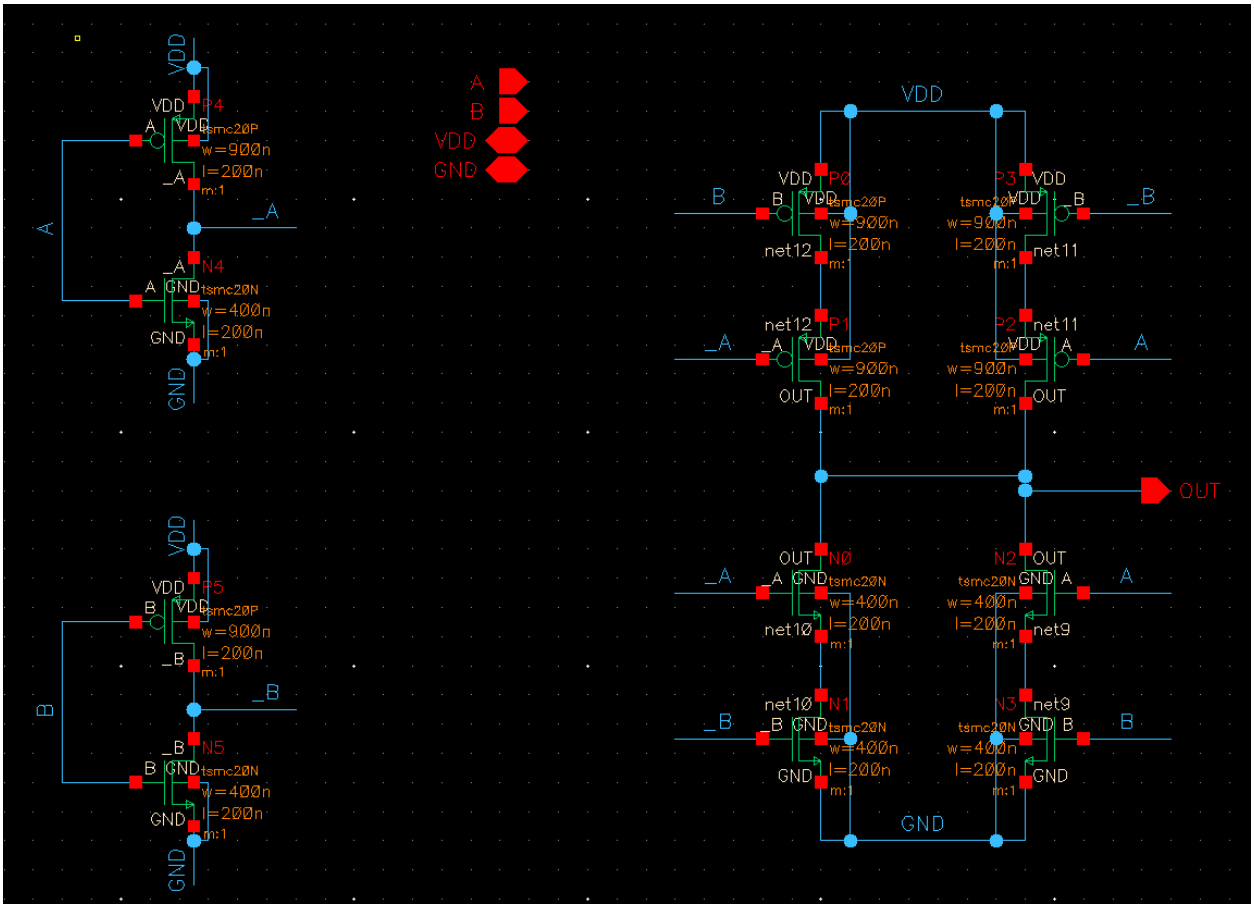

Figure 11: XOR2 Schematic

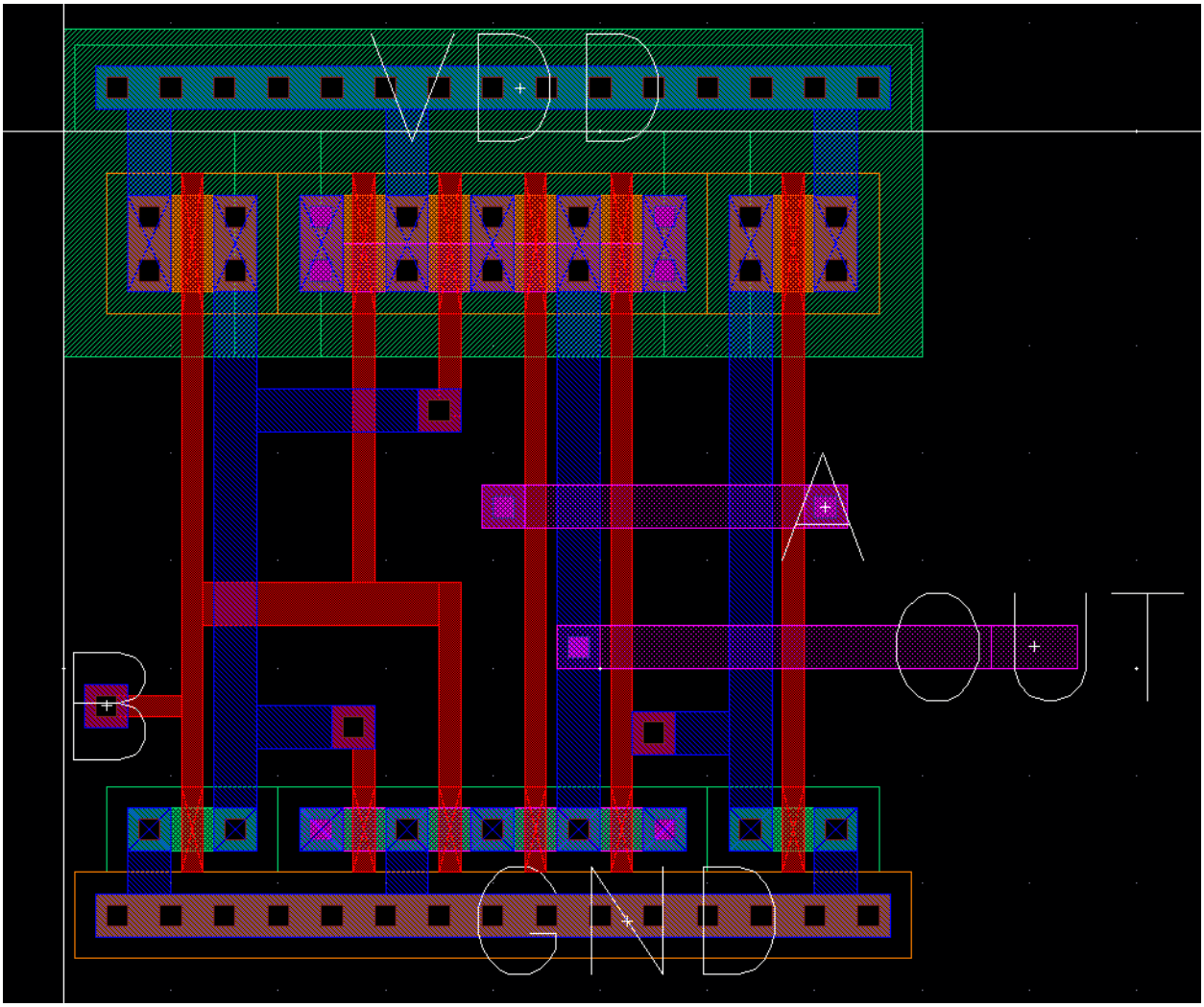

Figure 12: XOR2 Layout

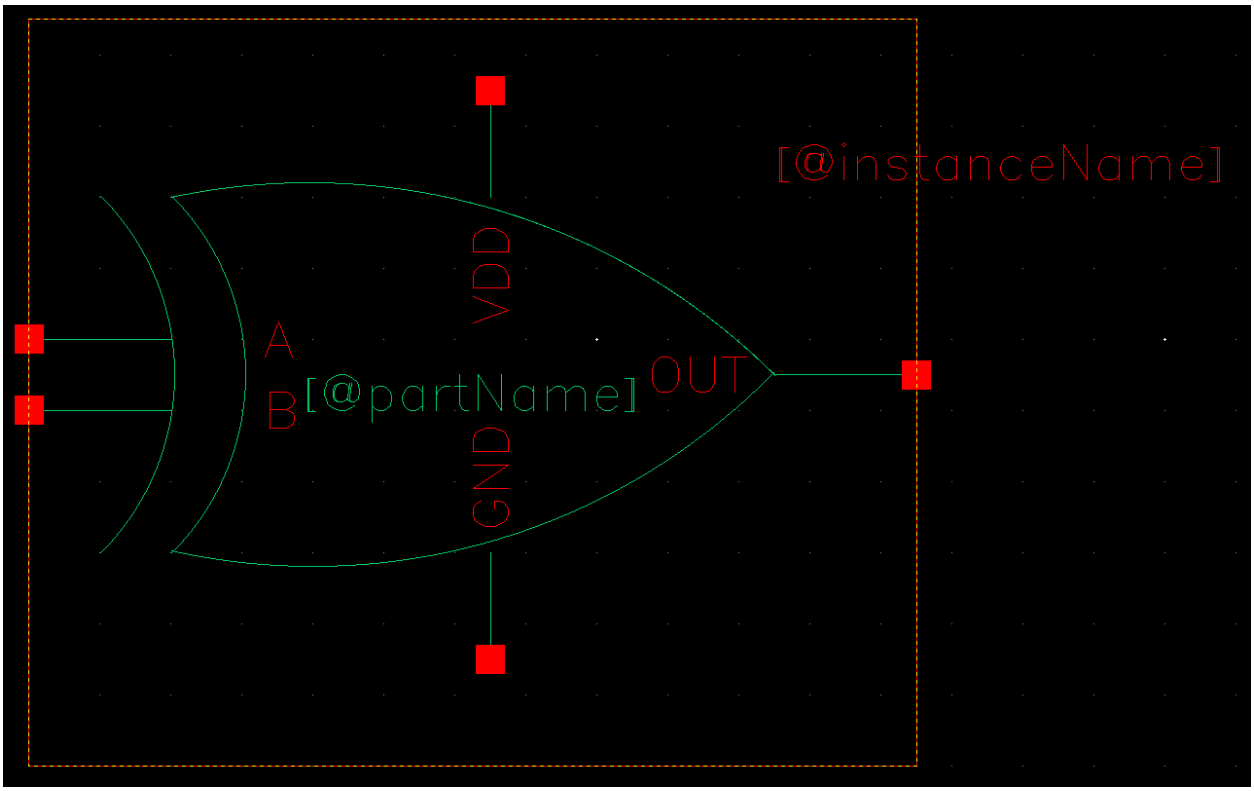

Figure 13: XOR2 Symbol

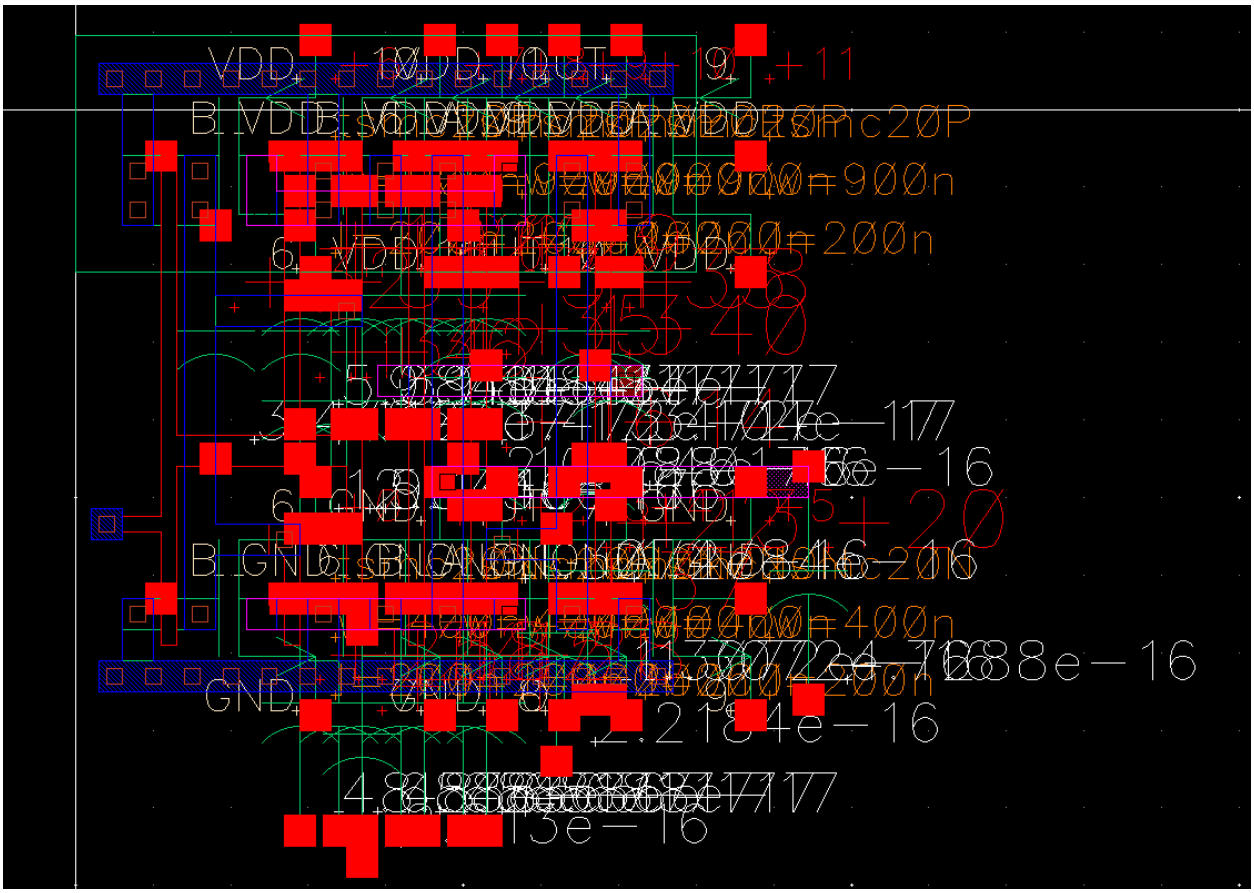

Figure 14: XOR2 Extracted View

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@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/a/alexd43anderson/ecen714/LVS -l -s -t /home/ug
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/layout/netlist
       count
        11              nets
        5               terminals
        6               pmos
        6               nmos

    Net-list summary for /home/ugrads/a/alexd43anderson/ecen714/LVS/schematic/netlist
       count
        11              nets
        5               terminals
        6               pmos
        6               nmos


    Terminal correspondence points
    N9        N3        A
    N8        N7        B
    N6        N1        GND
    N7        N0        OUT
    N10       N5        VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  12      12
        total                   12      12
```

Figure 15: XOR2 LVS Check