Lab 7: Frequency Response of Inverting Amplifiers

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Description

In this lab, the design of four different types of inverting amplifiers was explored: an inverter with a current mirror load, a digital CMOS inverter, a PMOS only self-biased inverter, and a CMOS self-biased inverter. In all designs, a capacitor was introduced between the input and output to take advantage of the Miller effect. The frequency response and phase margin was measured for each design considering this Miller capacitance. As always, good practice layout techniques were used such as common centroid, dummy elements, and guard rings.

Design

First, the inverter with current mirror load was designed. Using the expression for gain, a minimum value for gm1 was derived. From here, some margin was added to account for the body effect and constant assumptions. Next, by setting a value for Ibias, the Veff of the transistor can be found and used to get the aspect ratio.

Since the transconductance of the active load should be matched closely to that of the M1, the aspect ratios of the current mirror devices can be easily found using the known bias current and transconductance.

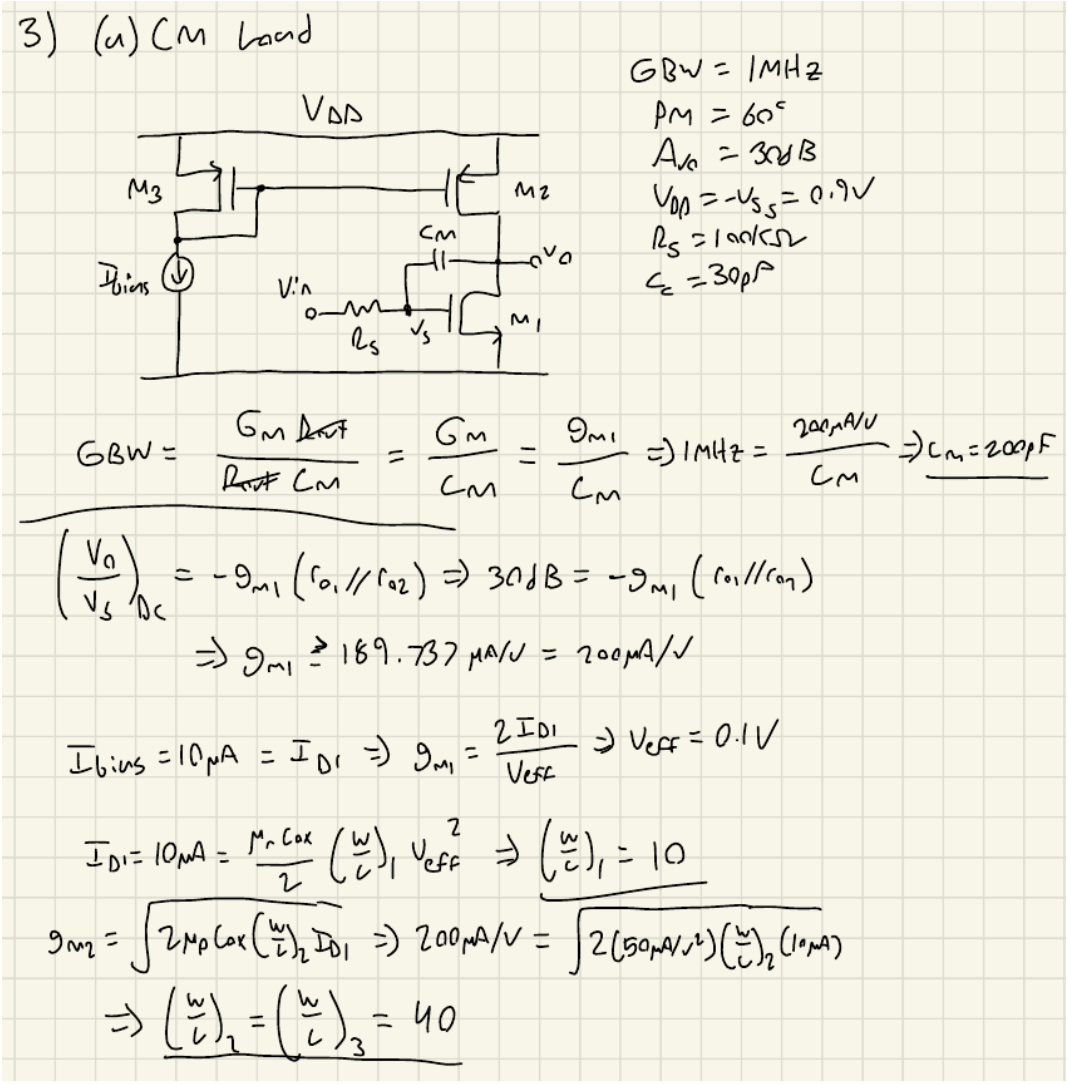

Figure 1: Inverter with Current Mirror Load Calculations

Next, the digital CMOS inverter was designed. A similar procedure was used to determine the aspect ratio of the NMOS and PMOS devices since the transconductances should be matched. Finally, the Miller capacitor was determined from the gain bandwidth product.

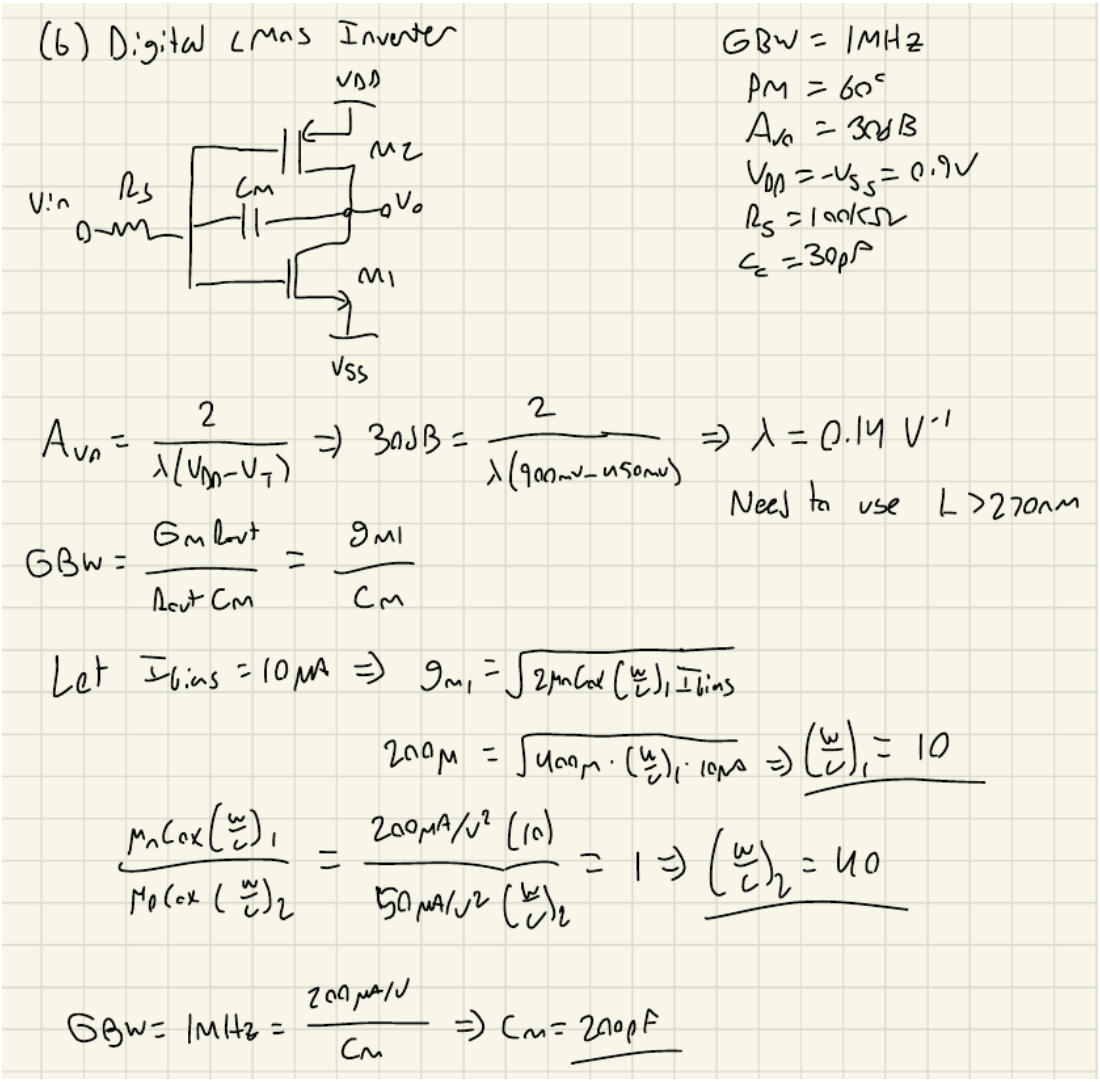

Figure 2: Digital Inverter Calculations

Next, the PMOS only self-biased inverter was designed. Since the desired gain is 0dB, the transconductances will be identical between the two devices. From here, the aspect ratio of each device was determined. The Miller capacitor was found from the gain bandwidth product once again.

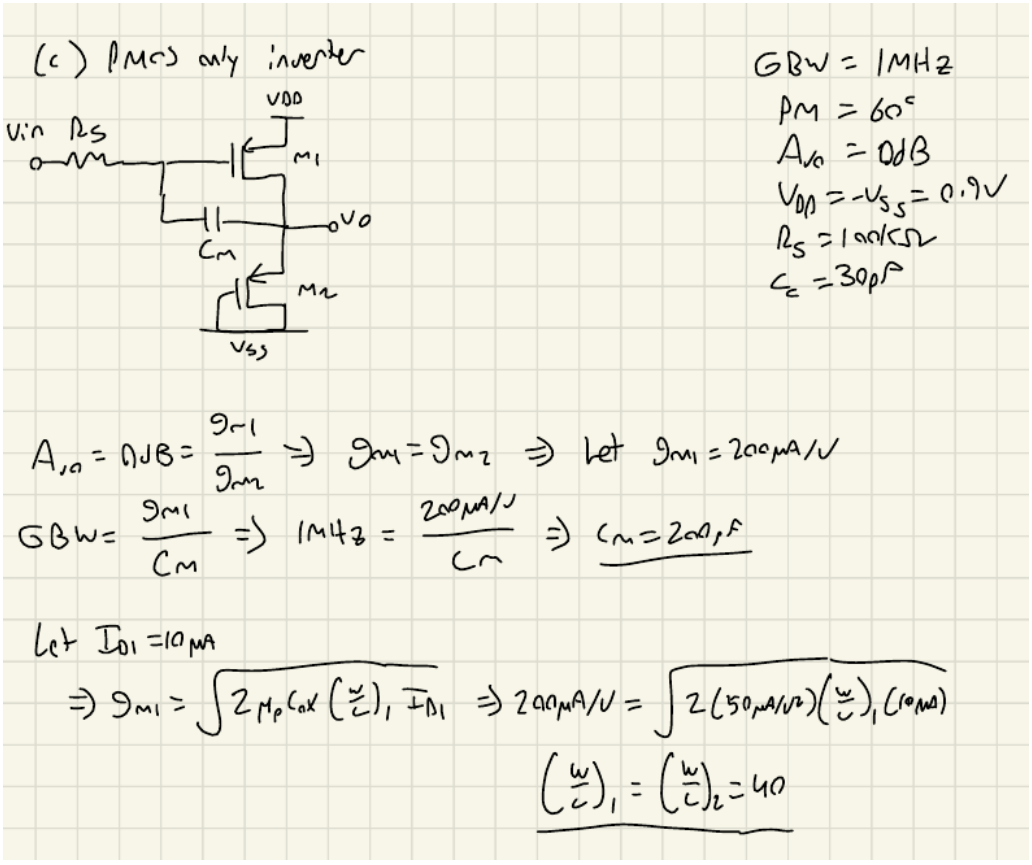

Figure 3: PMOS Only Self-Biased Inverter Calculations

Finally, the CMOS self-biased inverter was designed. Similar to the last topology, by setting the devices' transconductance equal, the aspect ratios were calculated. The Miller capacitance was found from the gain bandwidth product.

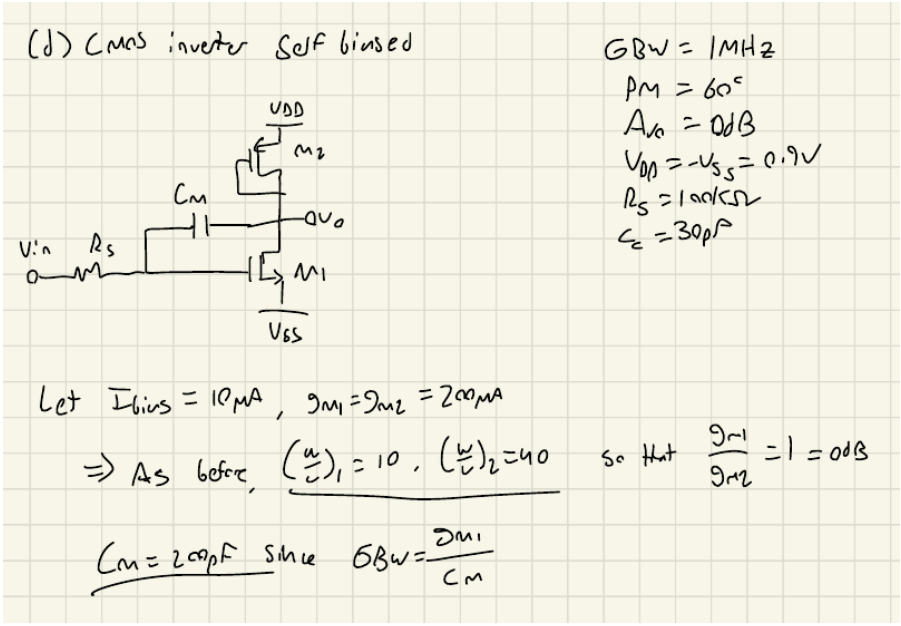

Figure 4: CMOS Only Self-Biased Inverter Calculations

From here, each design was simulated and adjusted accordingly to achieve the desired specifications. Lengths of devices in each design were increased or decreased accordingly to achieve the bandwidth needed.

Results

The schematic for the inverter with current mirror load is shown below in Figure 5, including dummy elements.

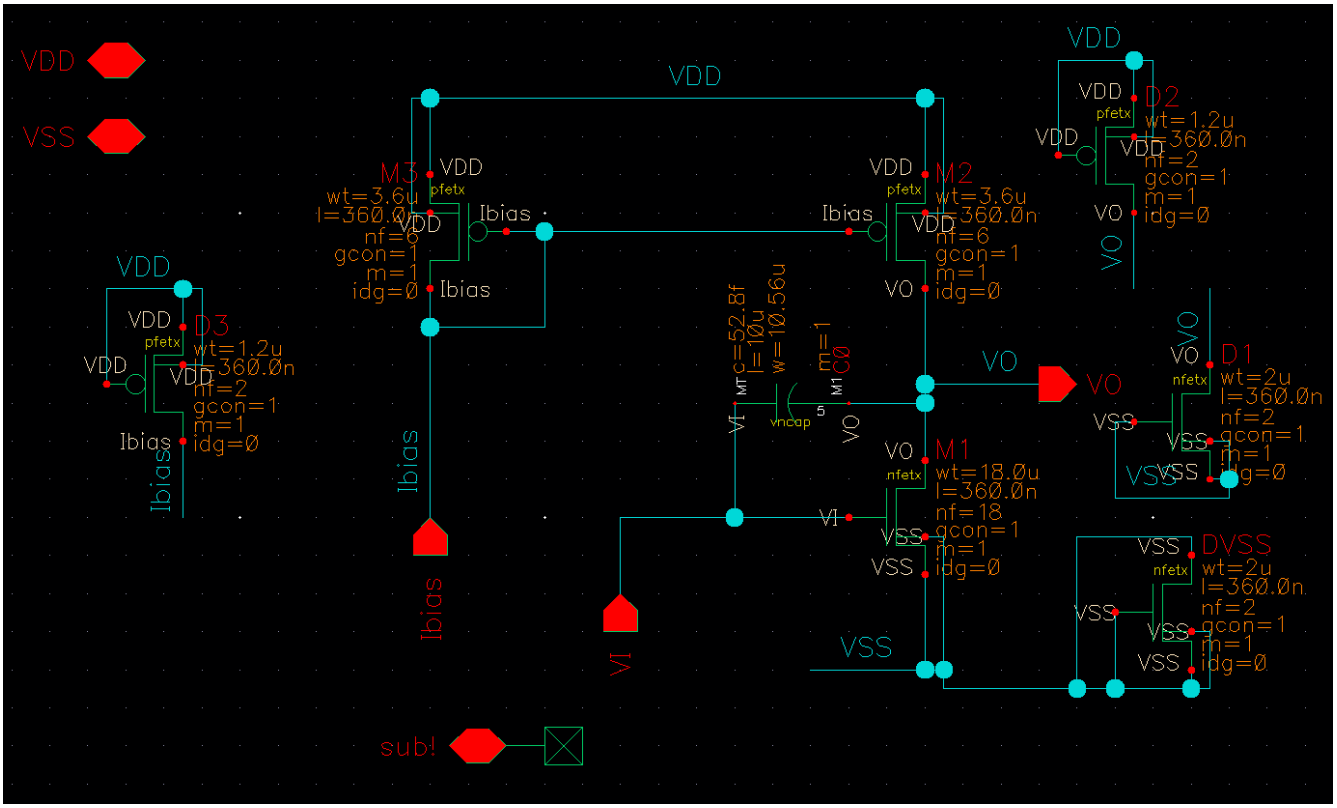

Figure 5: CM Load Schematic

From here, a test bench for the system was created and simulations for the AC and DC behavior were performed.

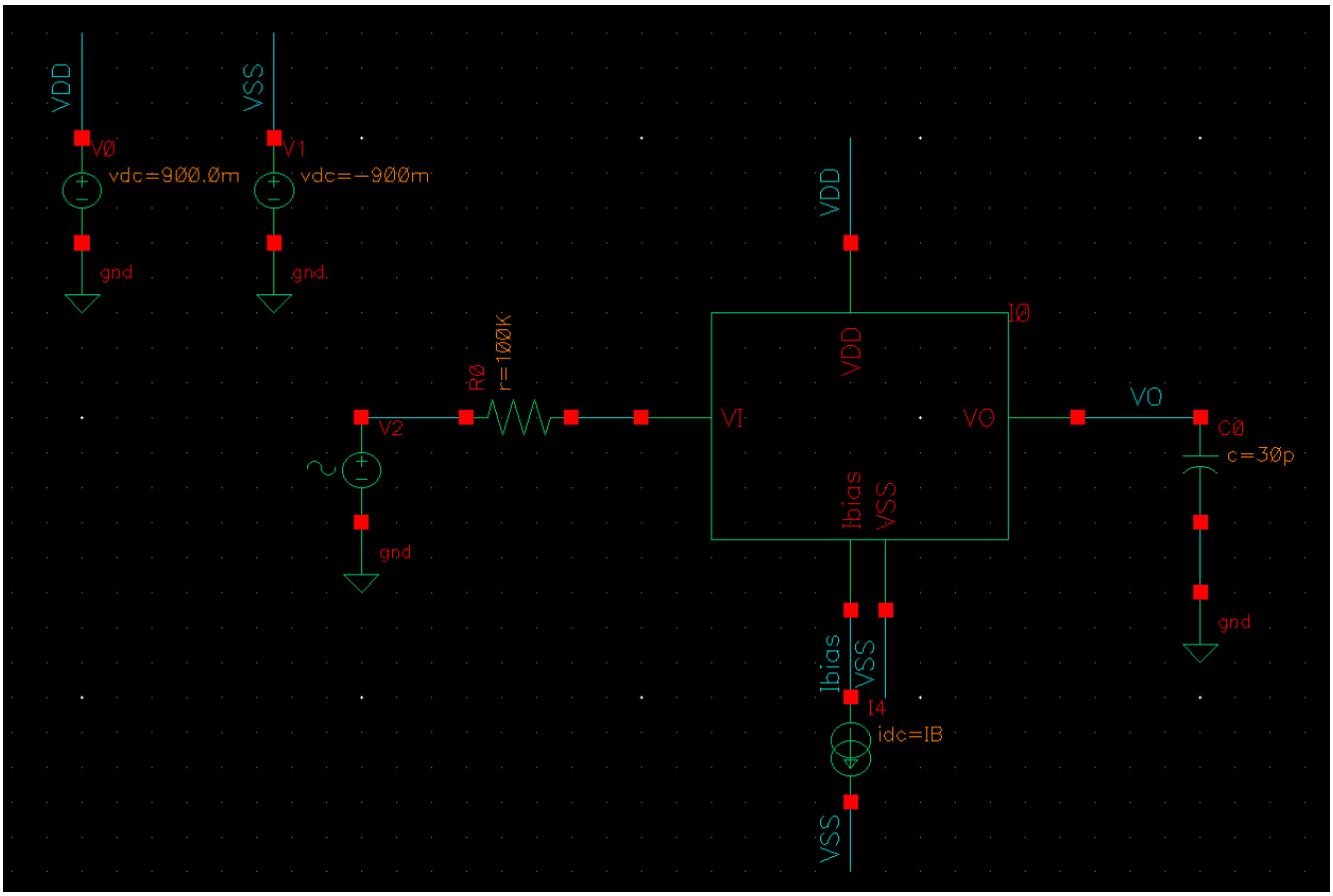

Figure 6: CM Load Test Bench

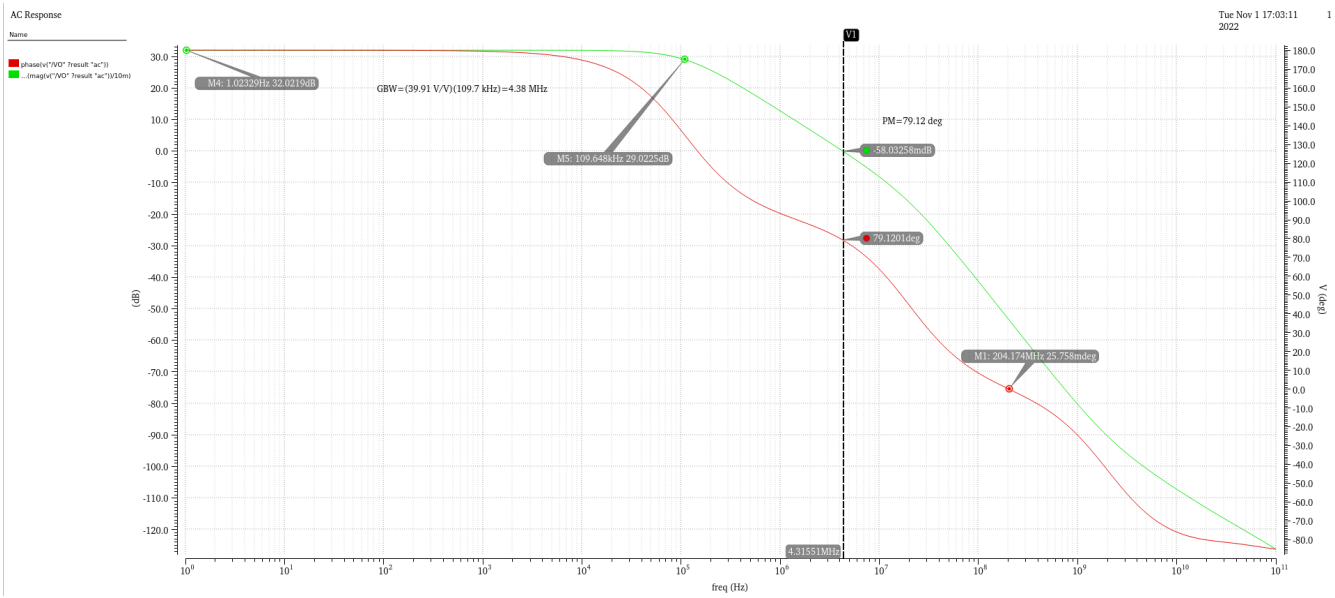

Figure 7: CM Load AC Simulations

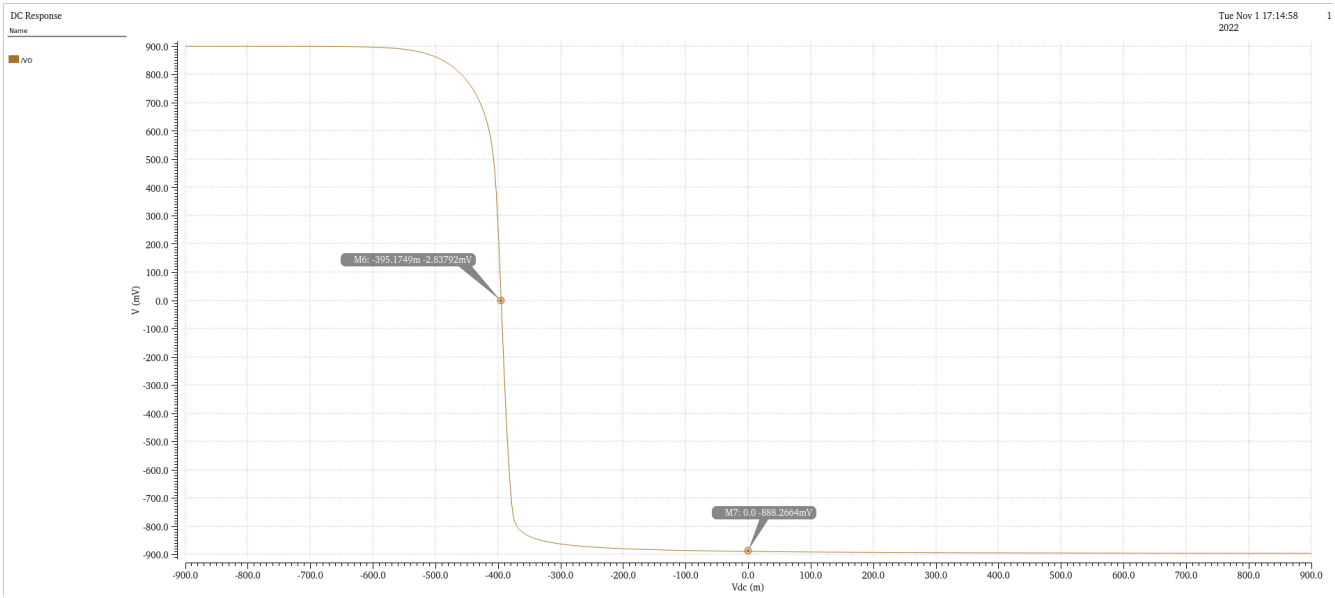

Figure 8: CM Load DC Simulations

Next, the layout was completed. The design was verified successfully using DRC and LVS.

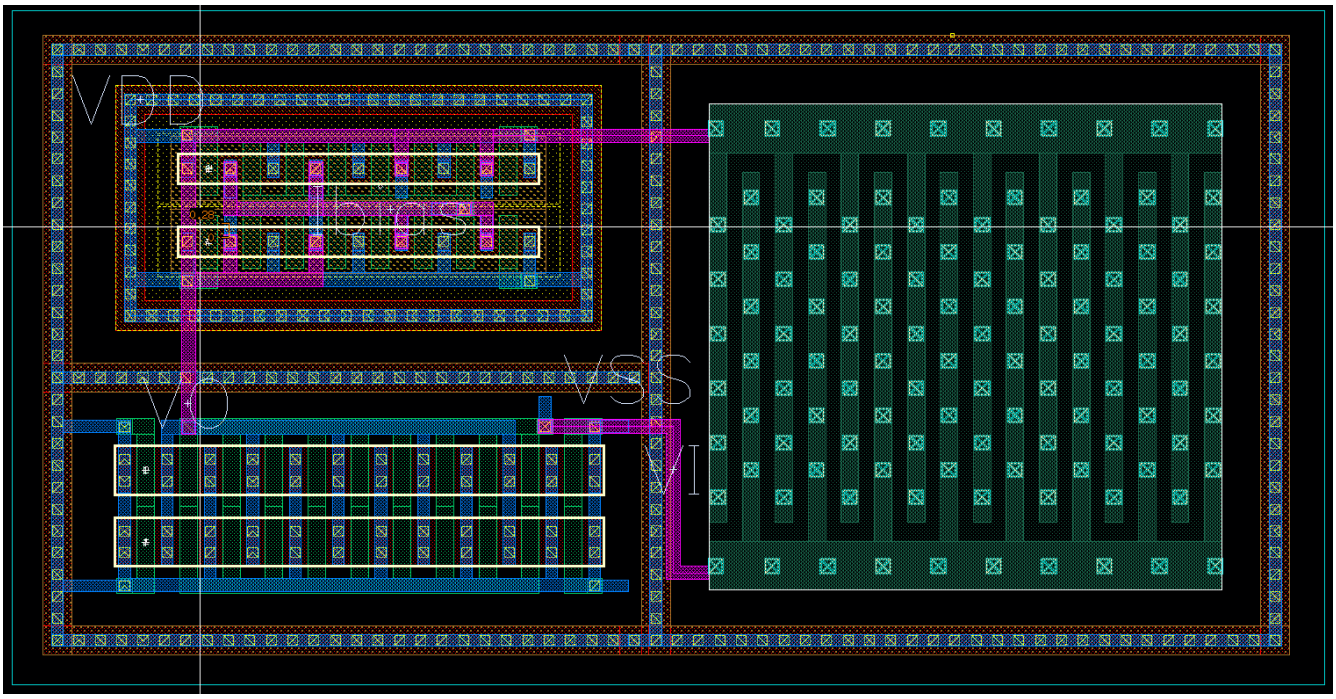

Figure 9: CM Load Layout

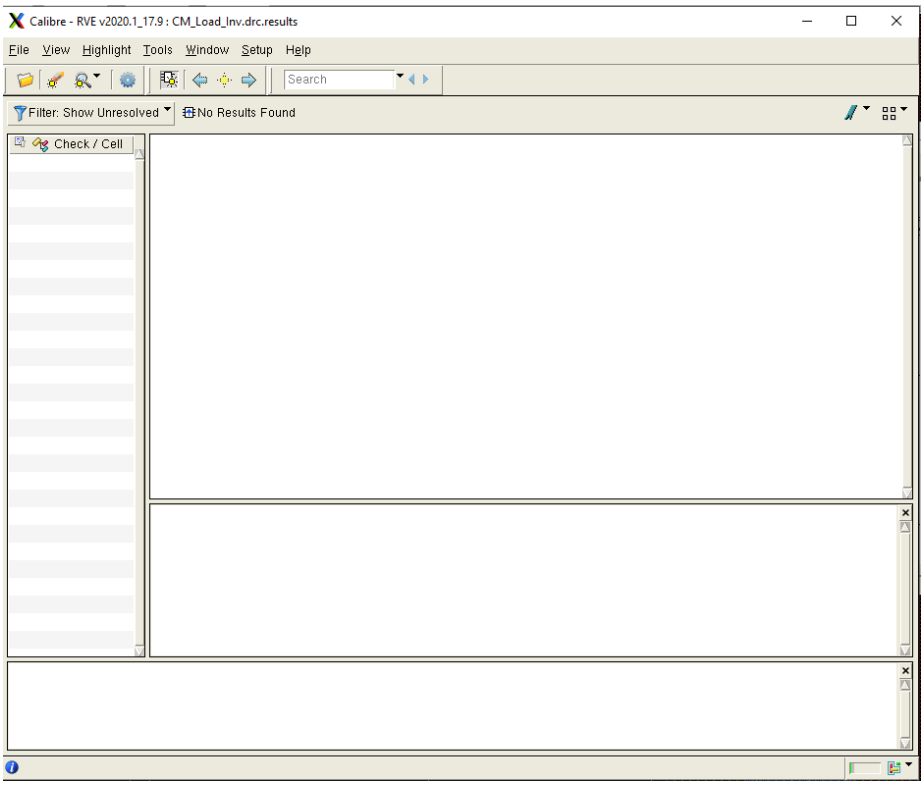

Figure 10: CM Load DRC

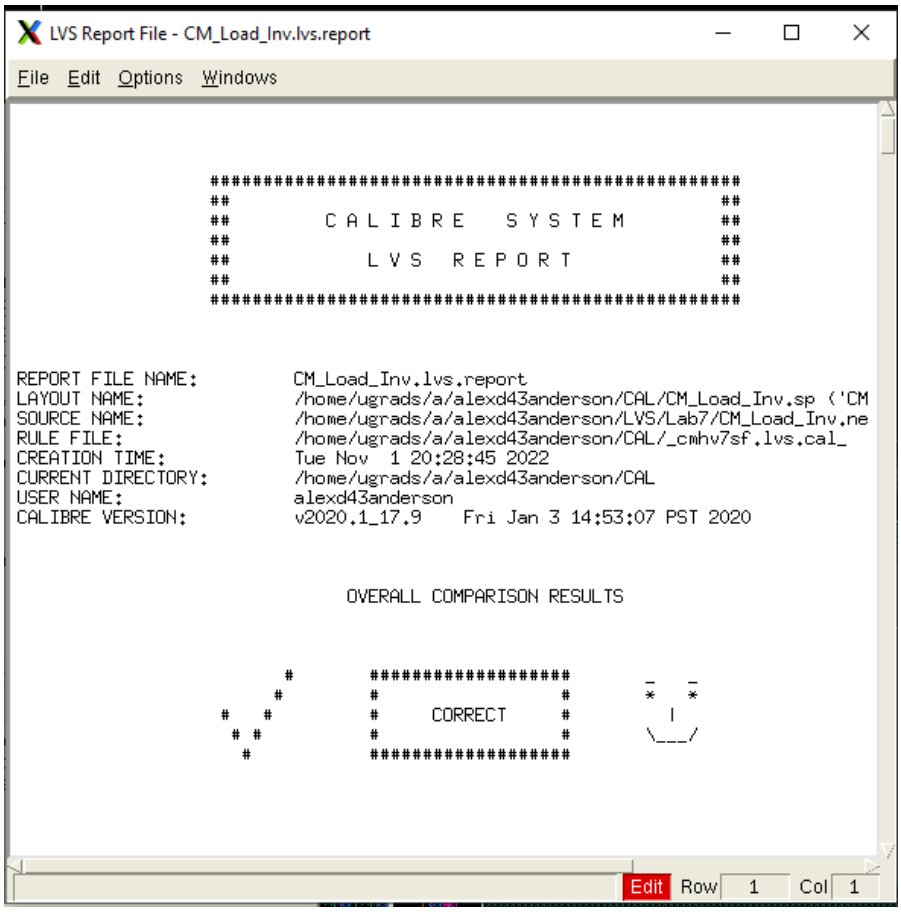

Figure 11: CM Load LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the AC and DC behavior.

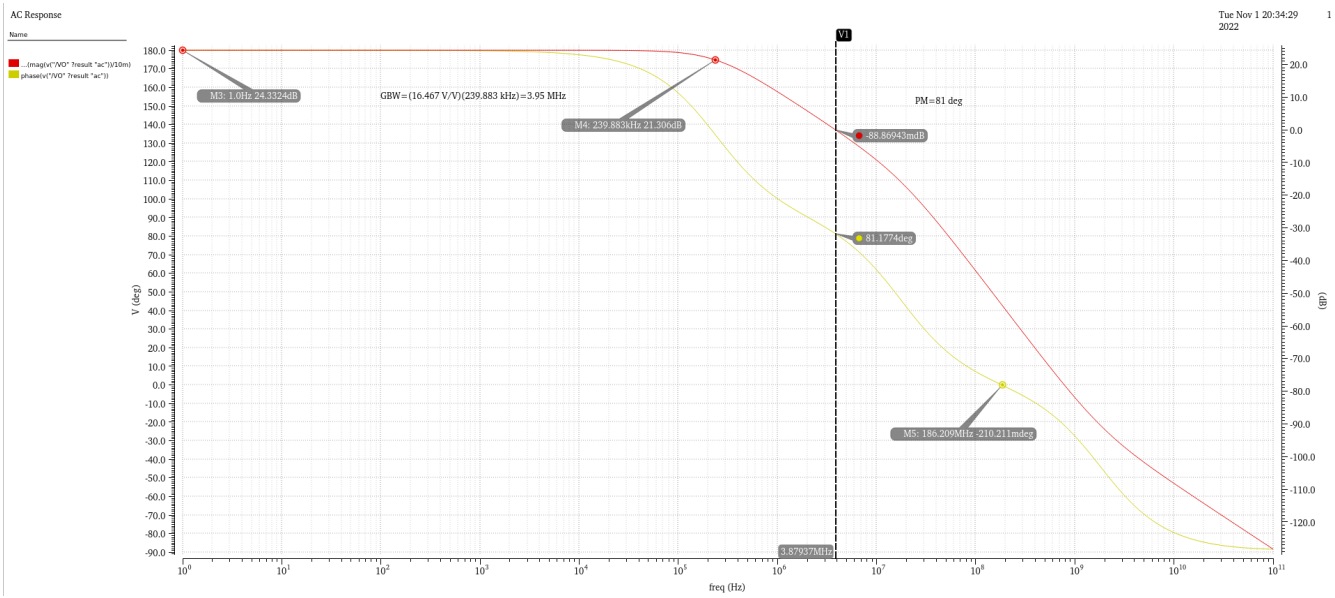

Figure 12: CM Load AC Post Simulation

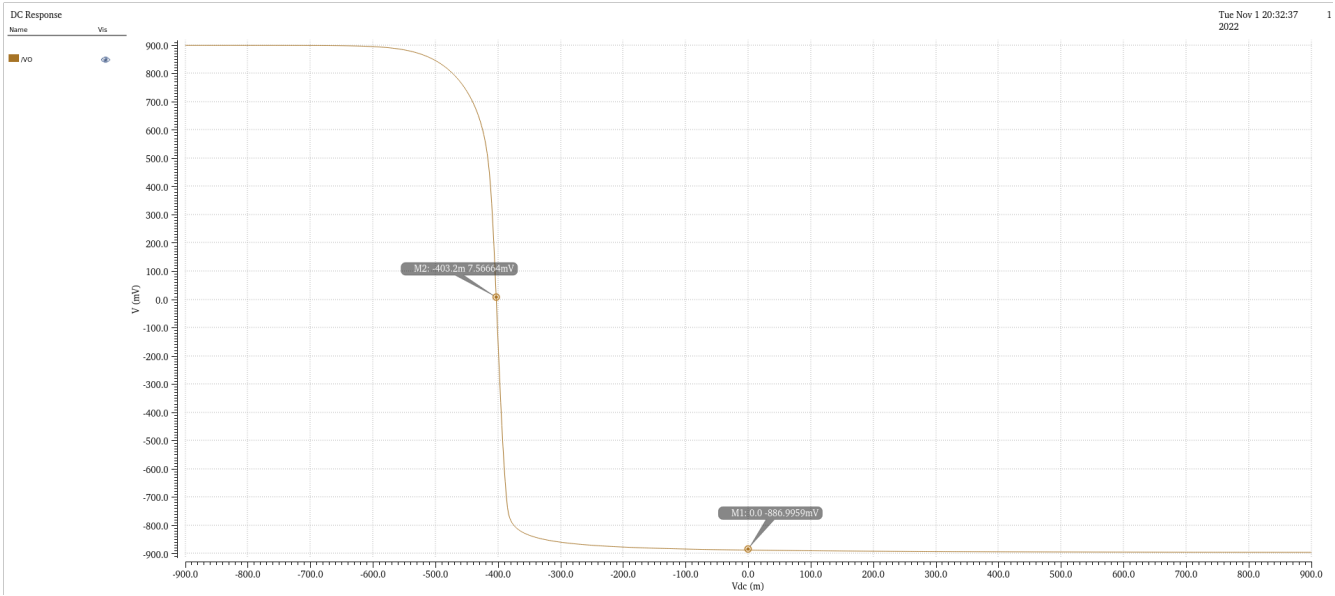

Figure 13: CM Load DC Post Simulations

The schematic for the digital CMOS inverter is shown below in Figure 14, including dummy elements that were added post-layout.

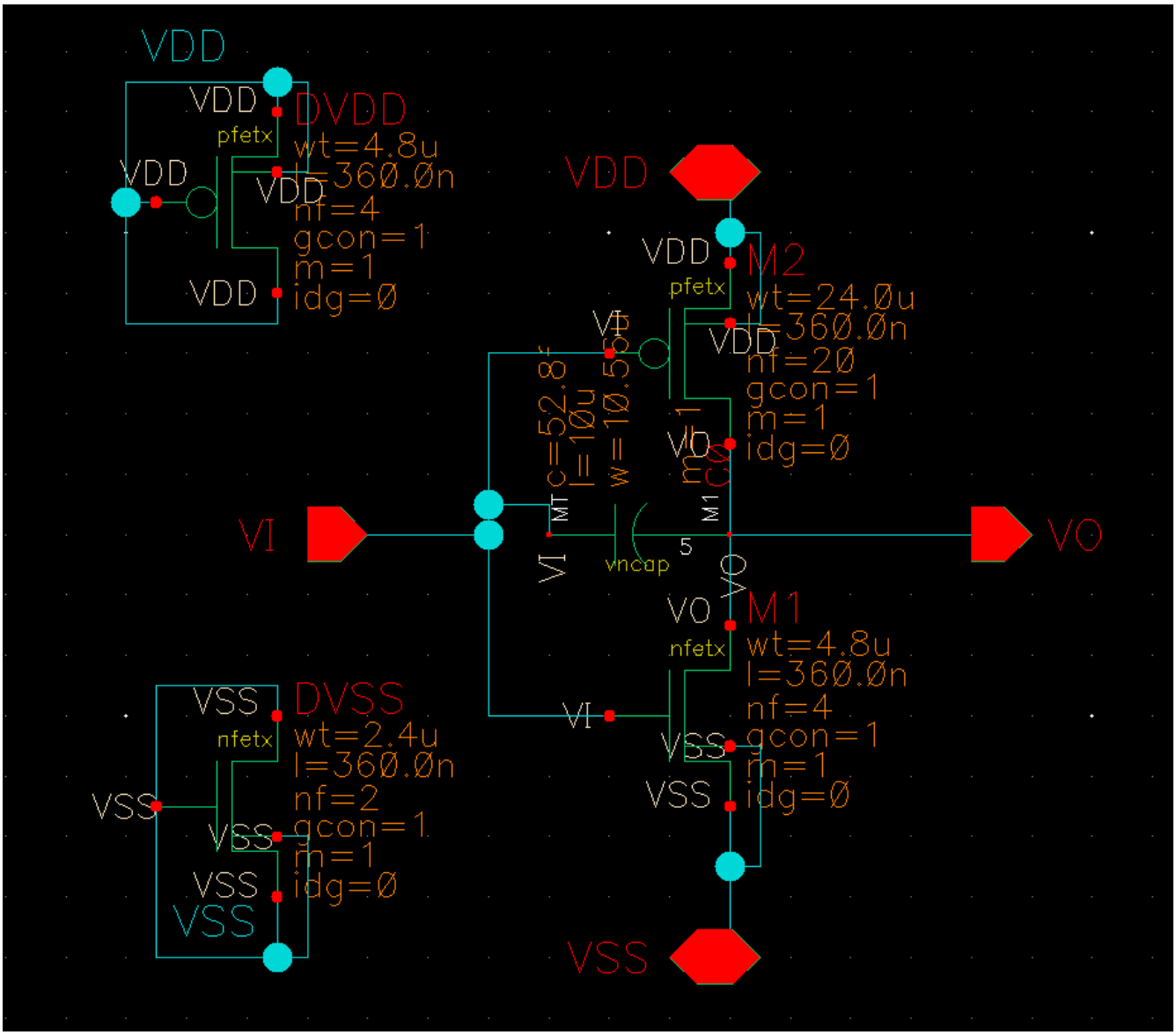

Figure 14: Digital Inverter Schematic

From here, a test bench for the system was created and simulations for the AC and DC behavior were performed.

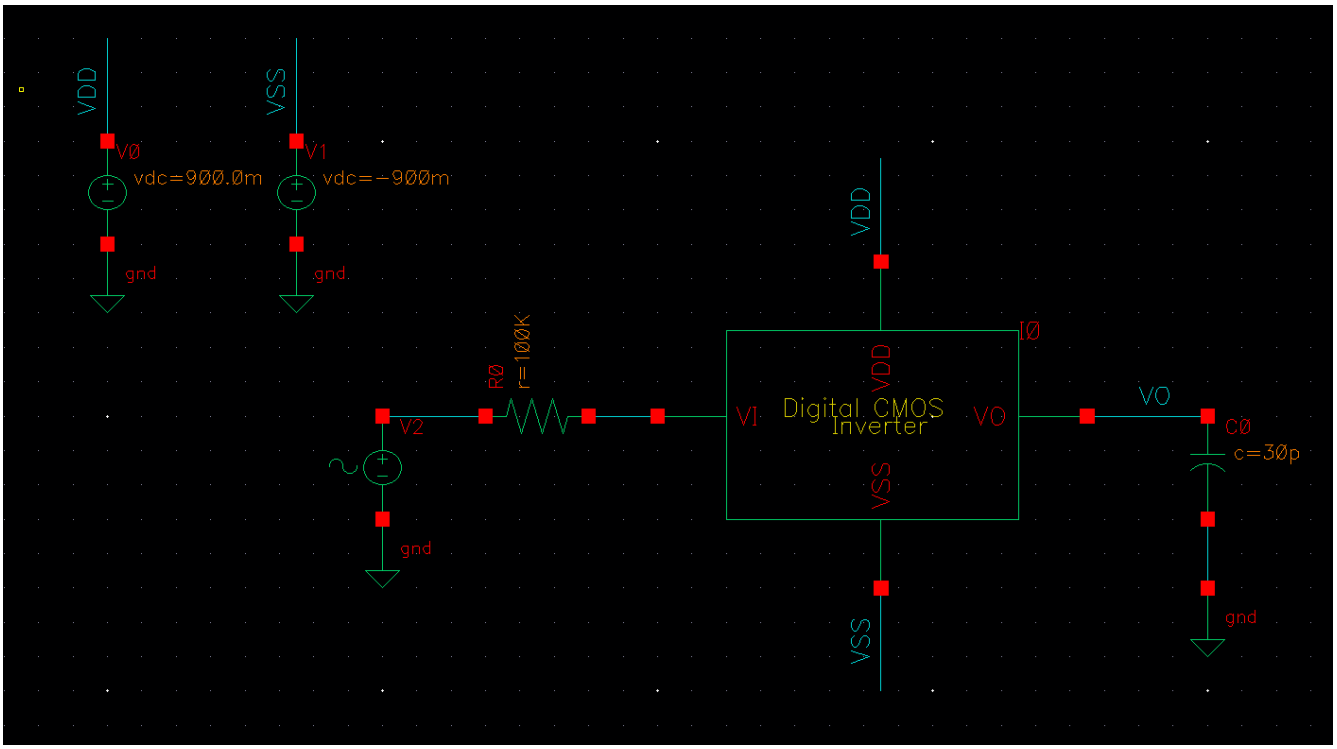

Figure 15: Digital Inverter Test Bench

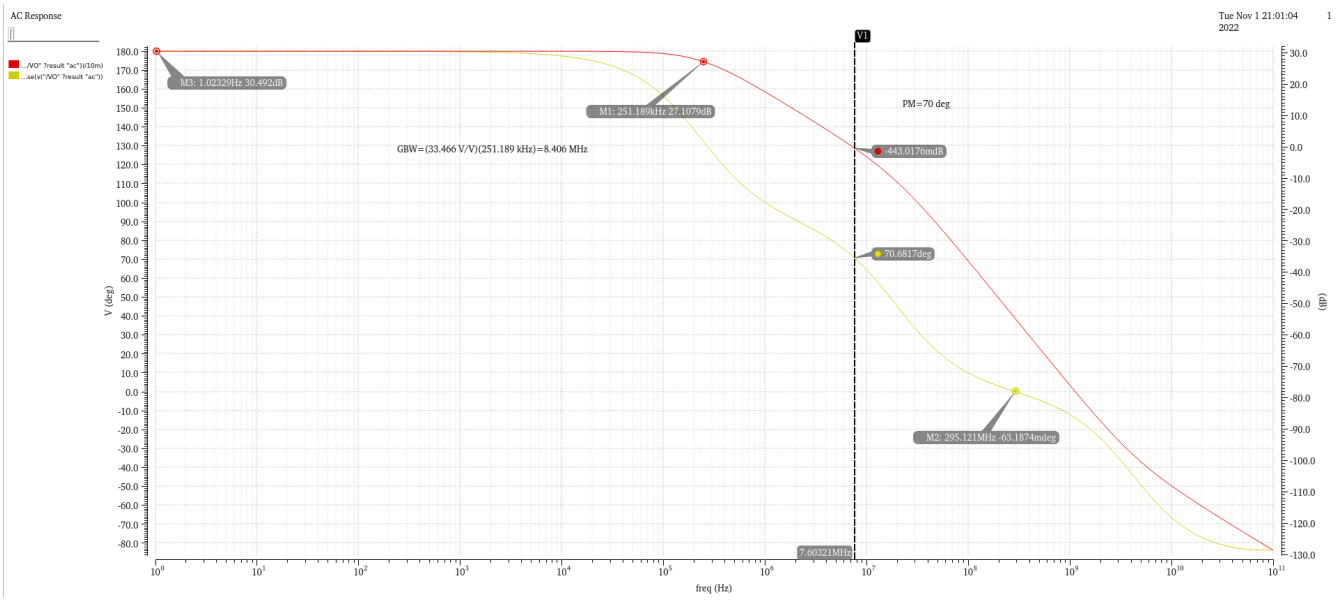

Figure 16: Digital Inverter AC Simulation

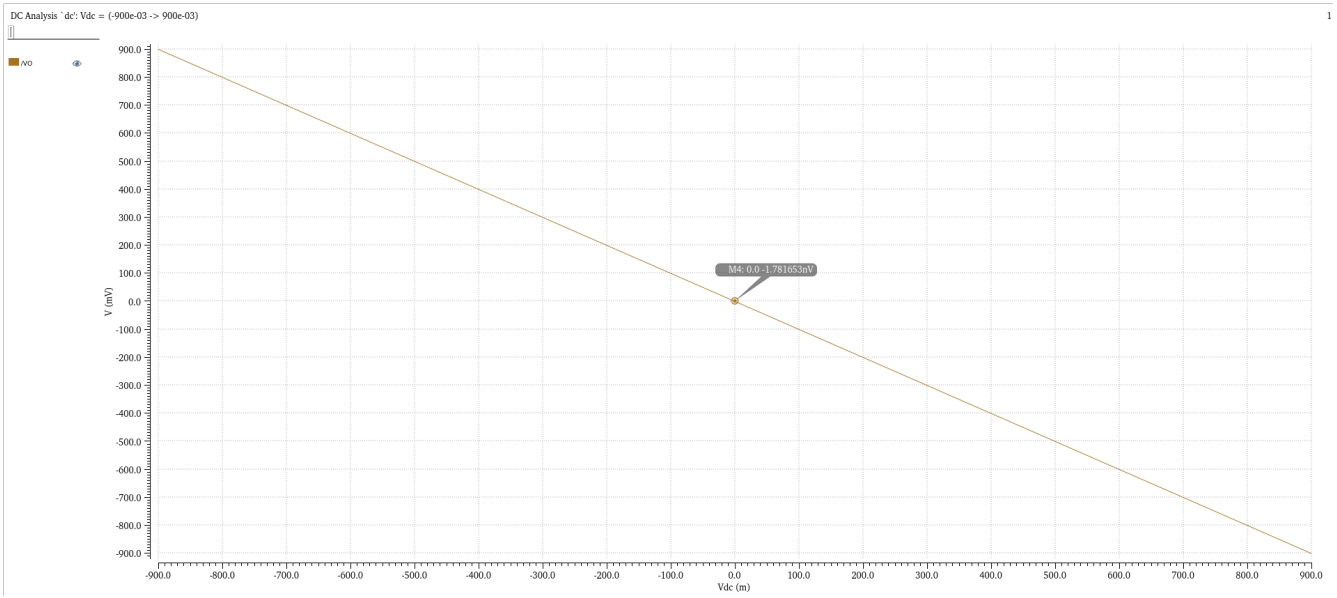

Figure 17: Digital Inverter DC Simulation

Next, the layout was completed. The design was verified successfully using DRC and LVS.

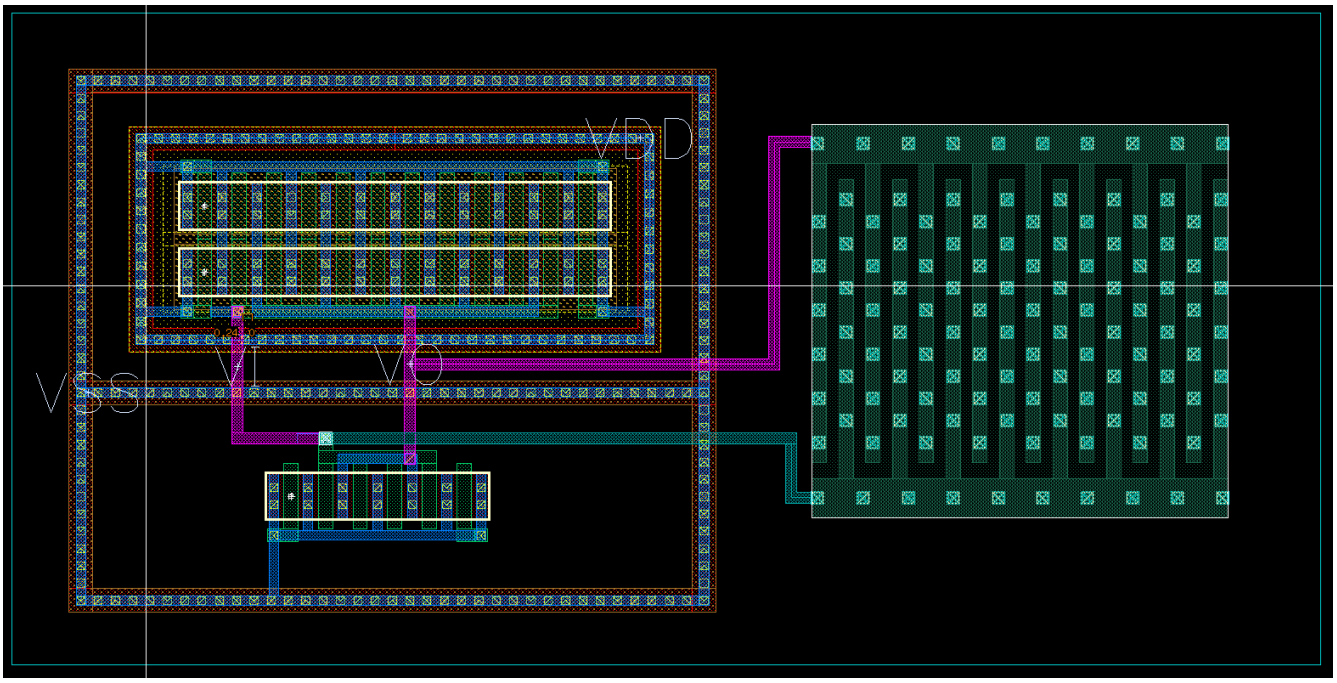

Figure 18: Digital Inverter Layout

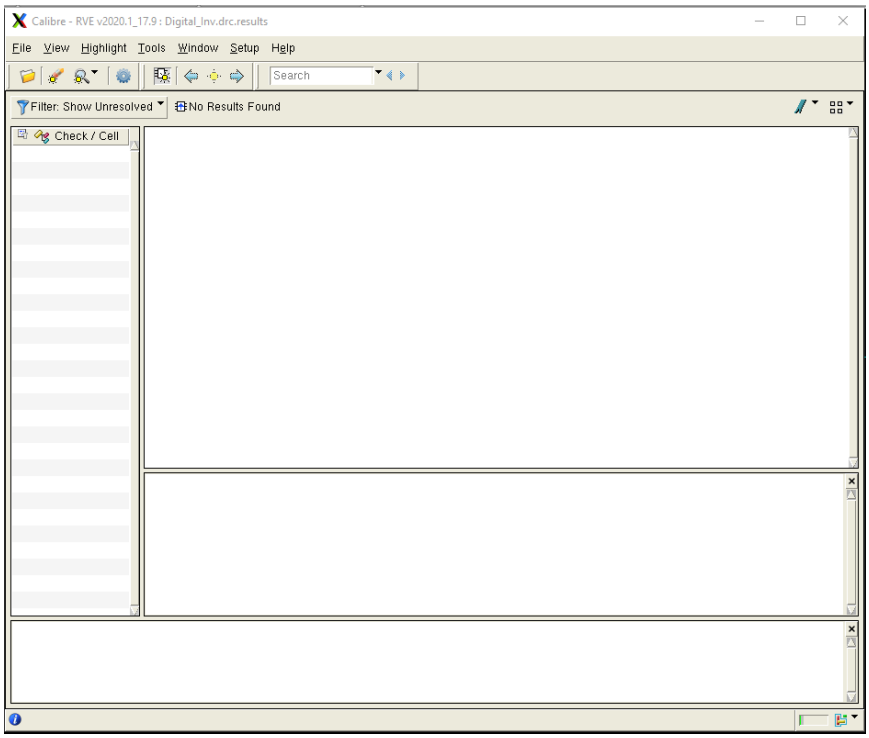

Figure 19: Digital Inverter DRC

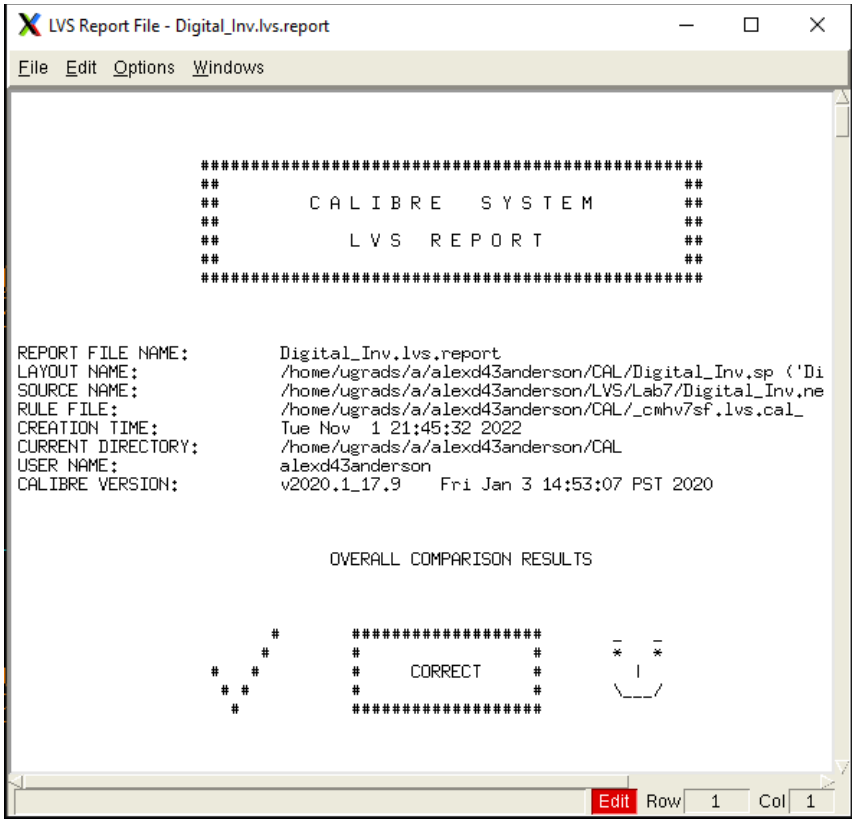

Figure 20: Digital Inverter LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the AC and DC behavior.

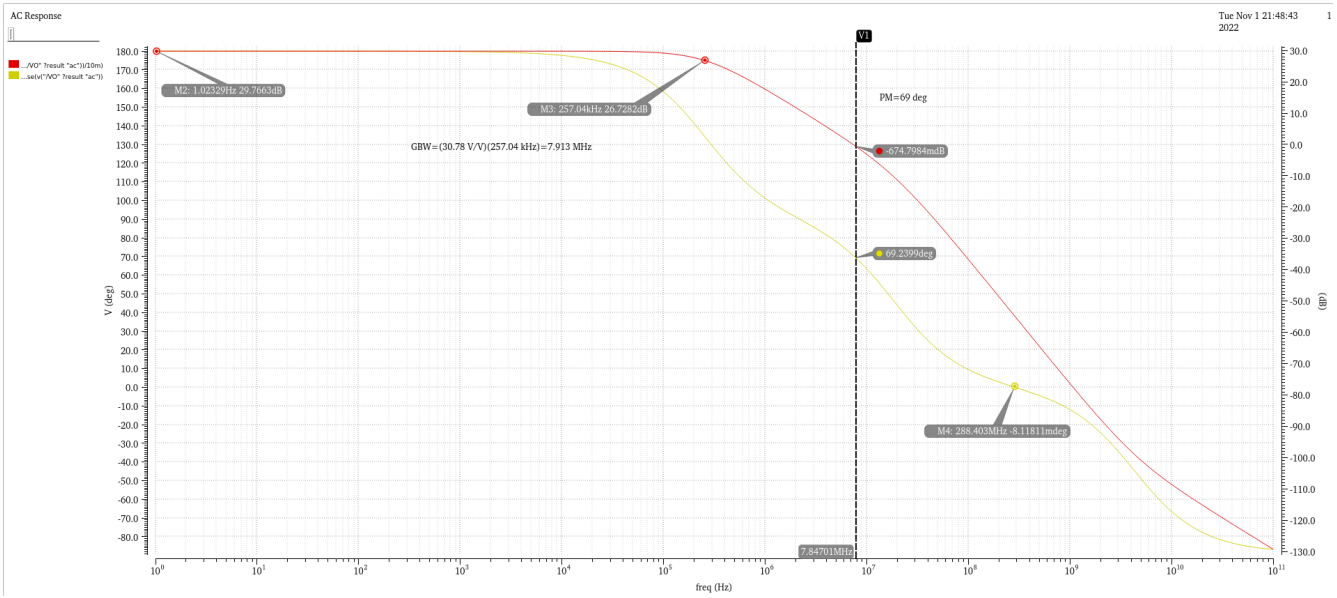

Figure 21: Digital Inverter AC Post Simulation

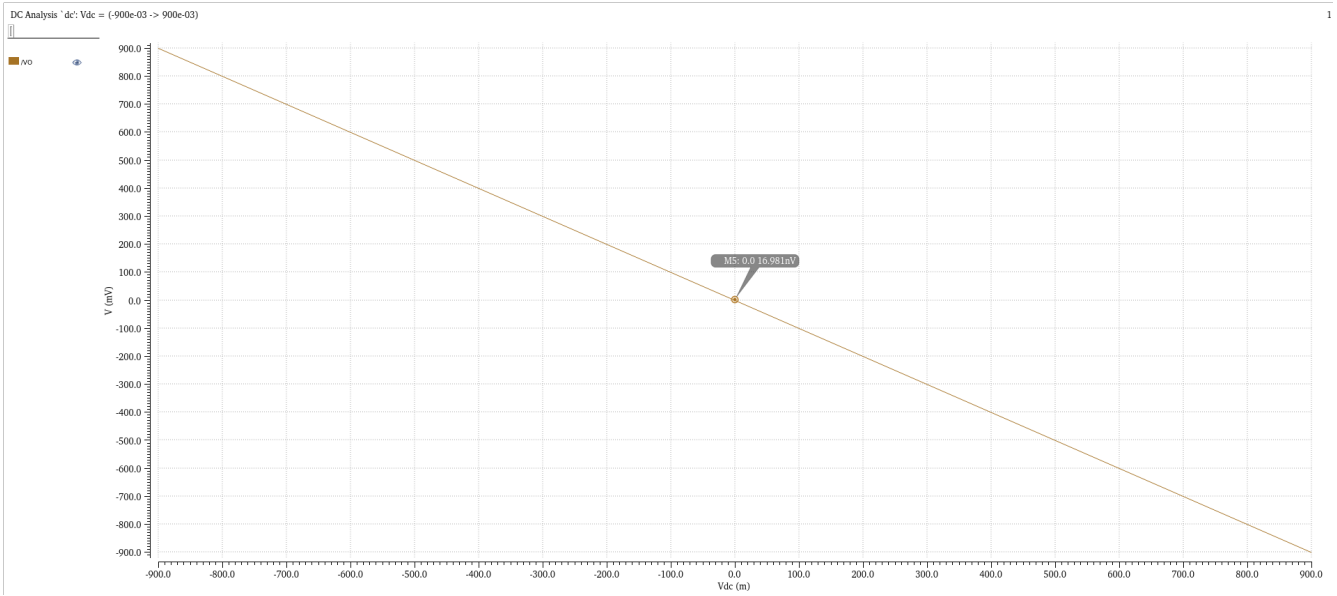

Figure 22: Digital Inverter DC Post Simulation

The schematic for the PMOS only self-biased inverter is shown below in Figure 23, including dummy elements that were added post-layout.

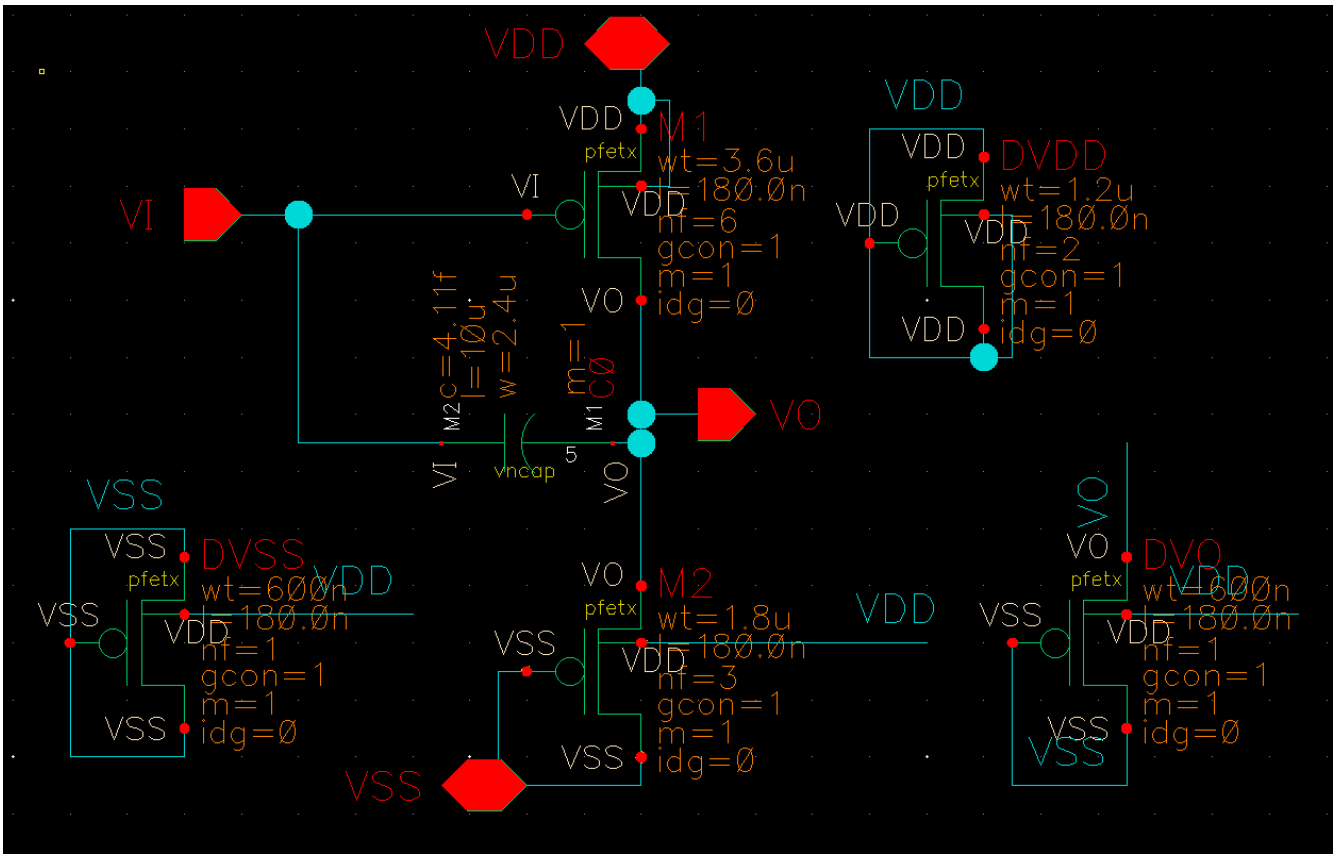

Figure 23: PMOS Inverter Schematic

From here, a test bench for the system was created and simulations for the AC and DC behavior were performed.

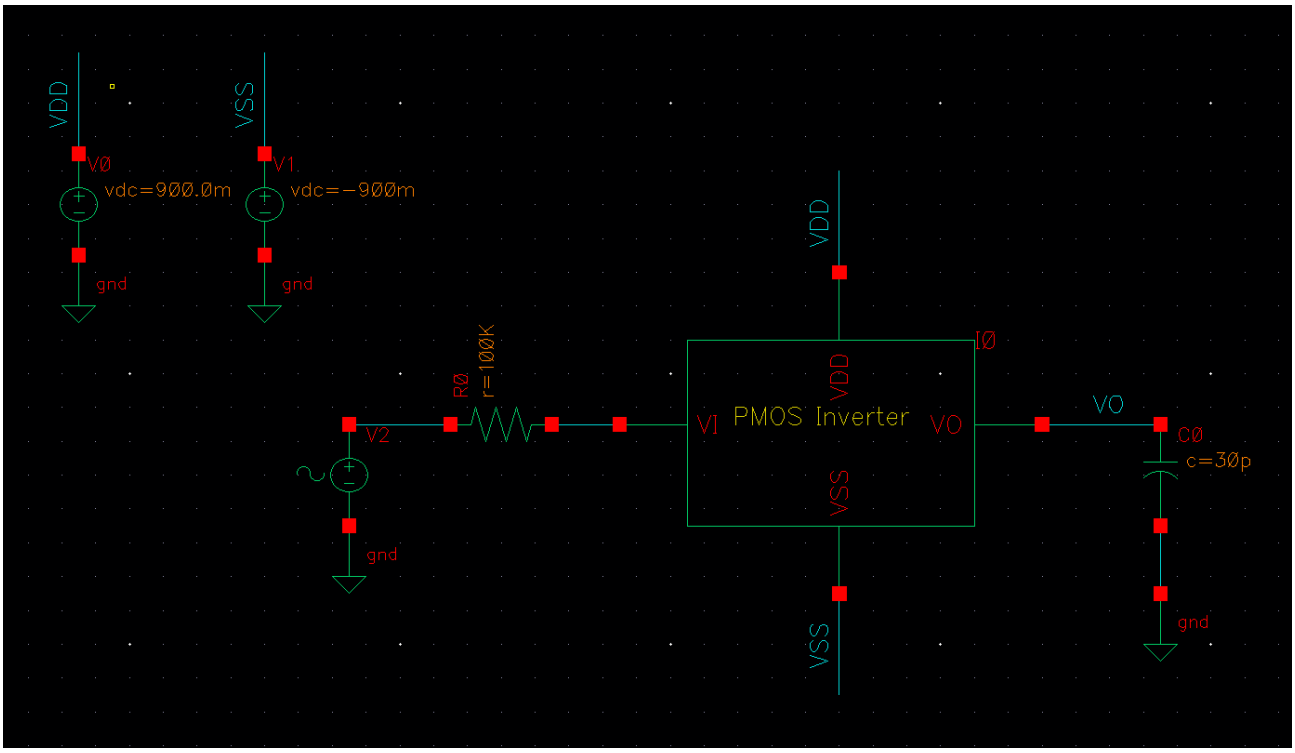

Figure 24: PMOS Inverter Test Bench

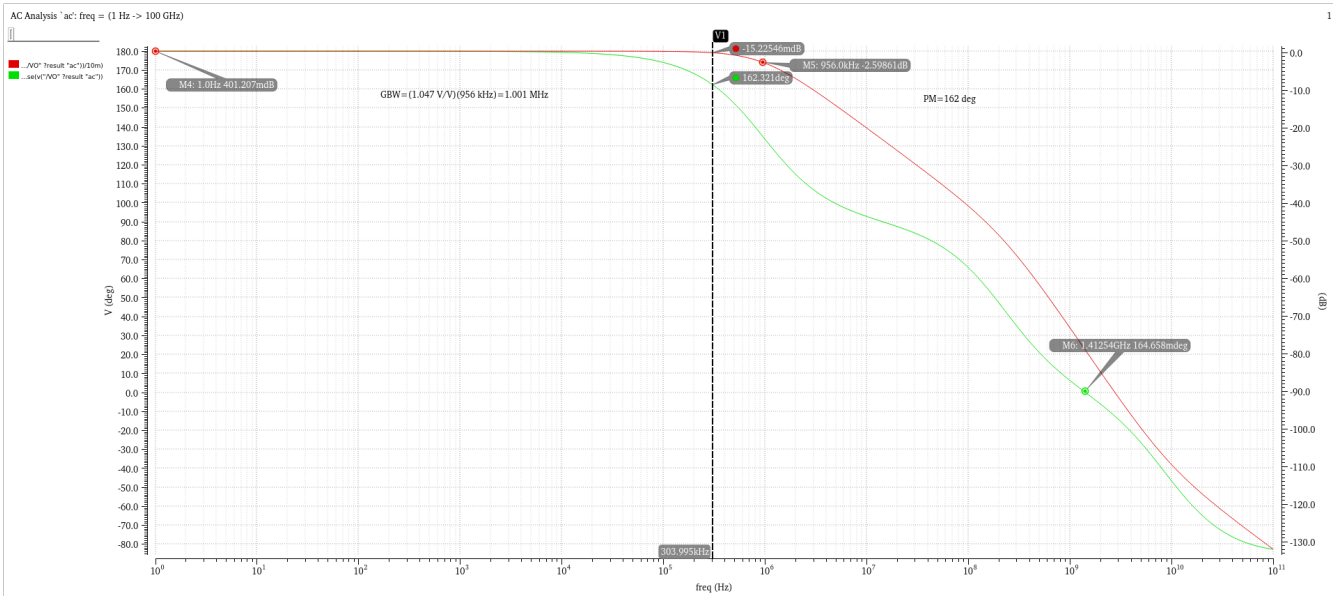

Figure 25: PMOS AC Simulation

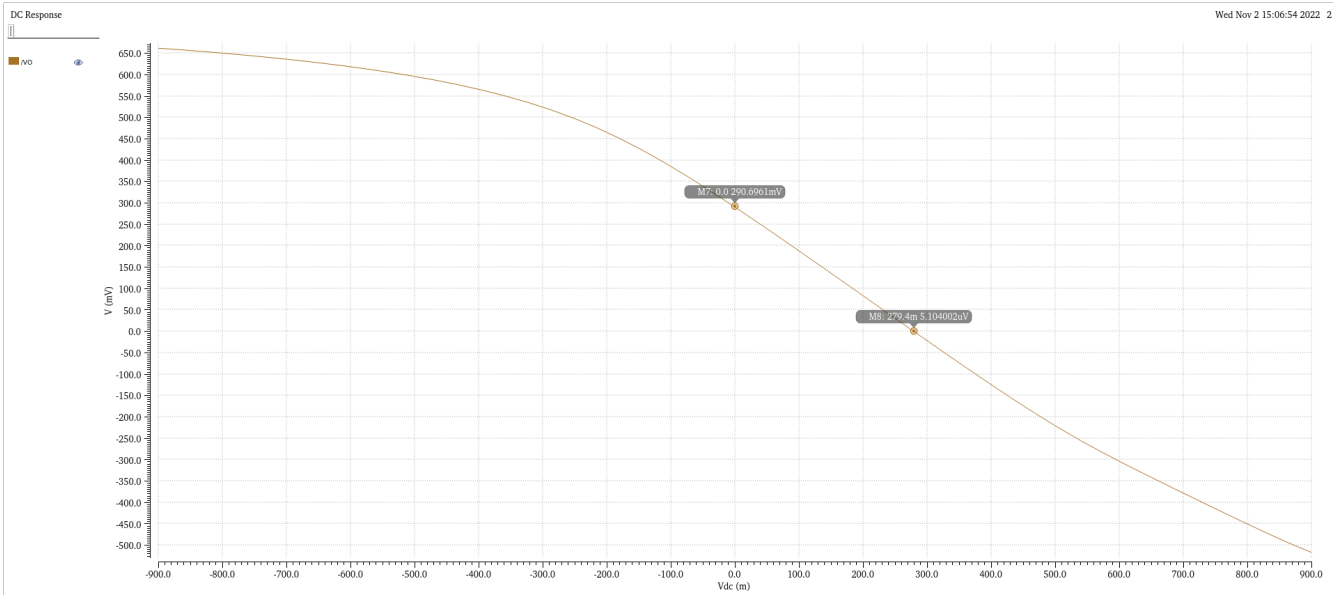

Figure 26: PMOS DC Simulation

Next, the layout was completed. The design was verified successfully using DRC and LVS.

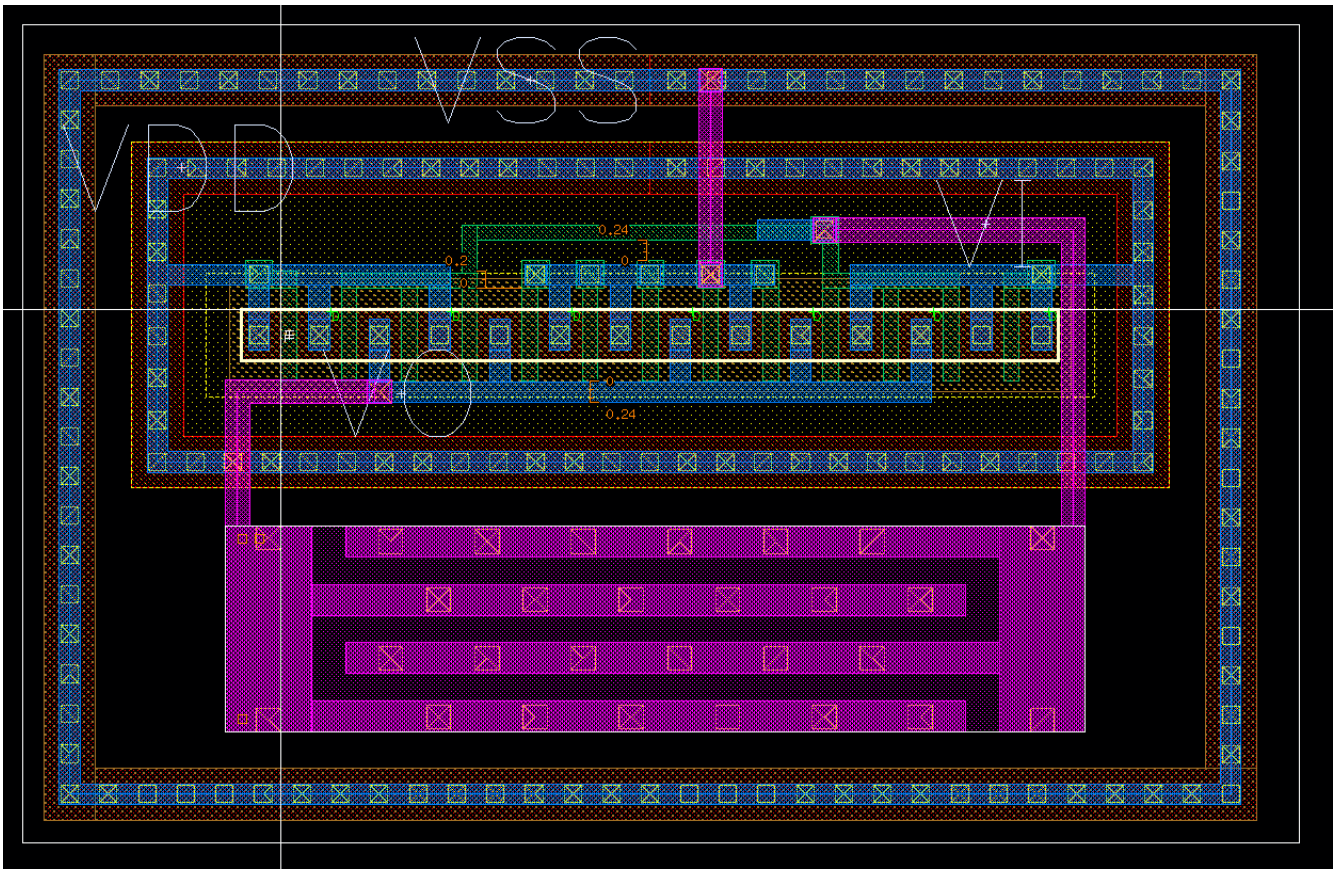

Figure 27: PMOS Inverter Layout

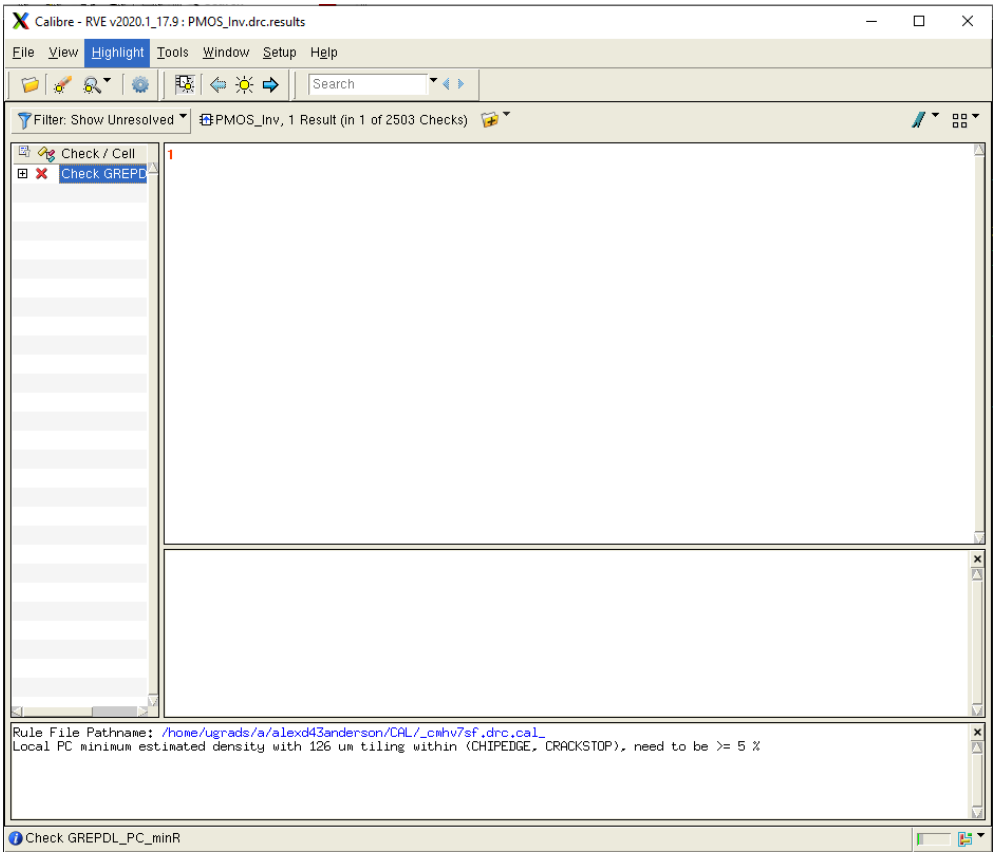

Figure 28: PMOS Inverter DRC

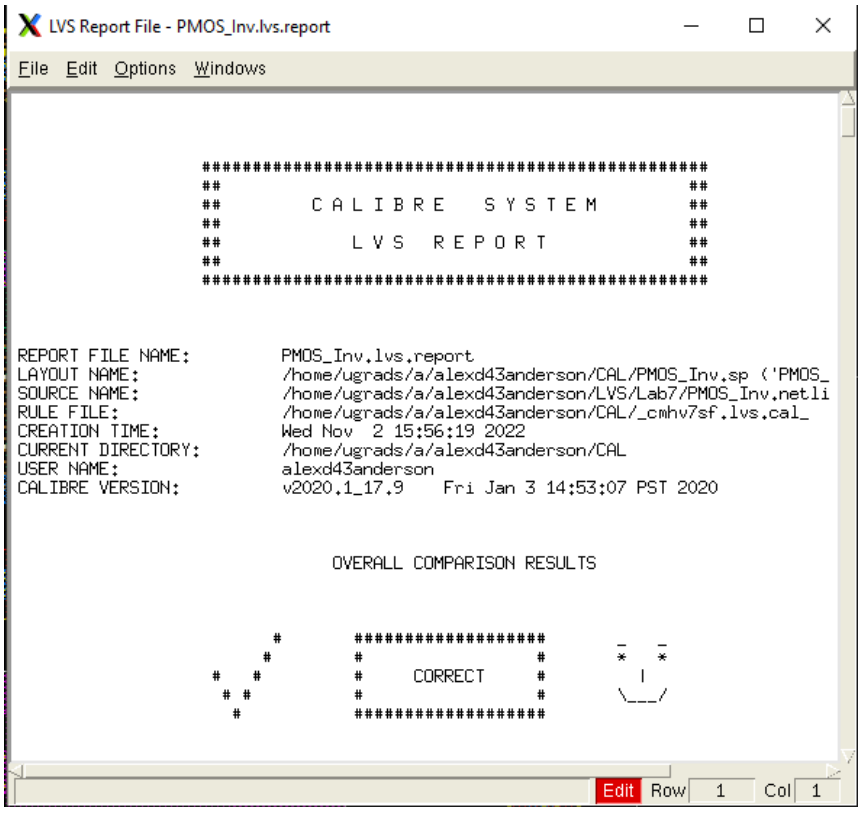

Figure 29: PMOS Inverter LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the AC and DC behavior.

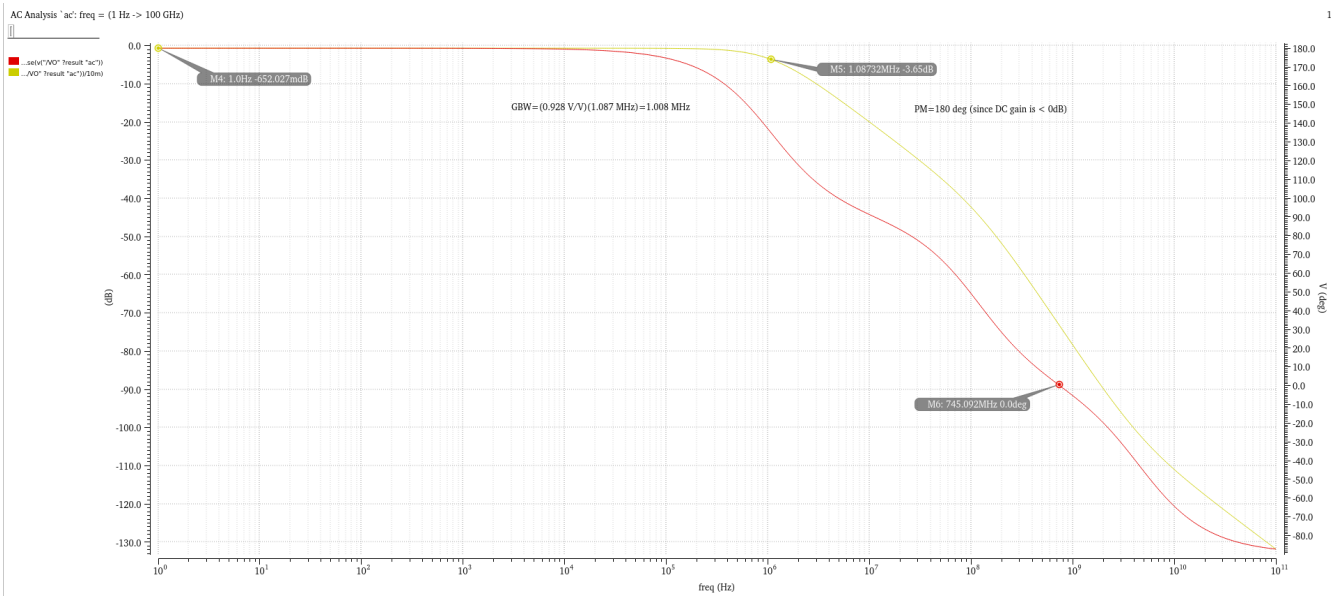

Figure 30: PMOS Inverter AC Post Simulation

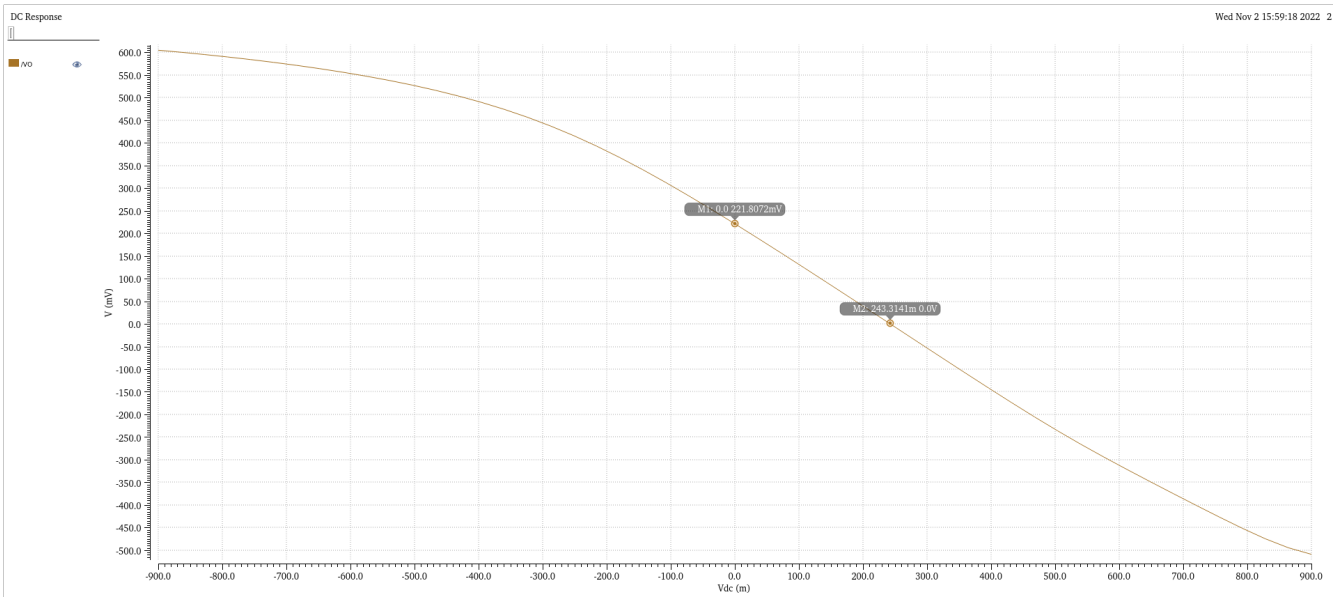

Figure 31: PMOS Inverter DC Post Simulation

The schematic for the CMOS self-biased inverter is shown below in Figure 32, including dummy elements that were added post-layout.

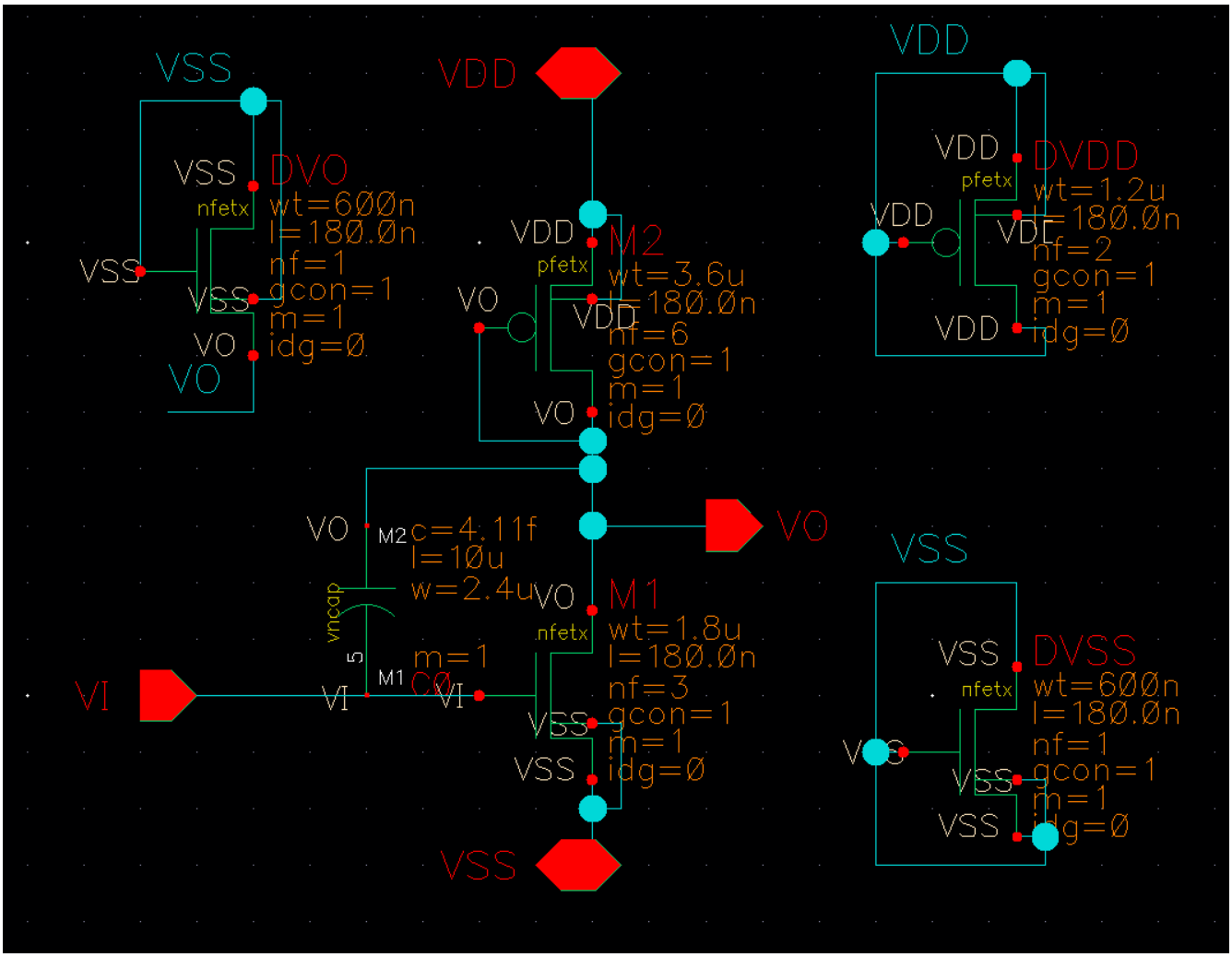

Figure 32: CMOS Inverter Schematic

From here, a test bench for the system was created and simulations for the AC and DC behavior were performed.

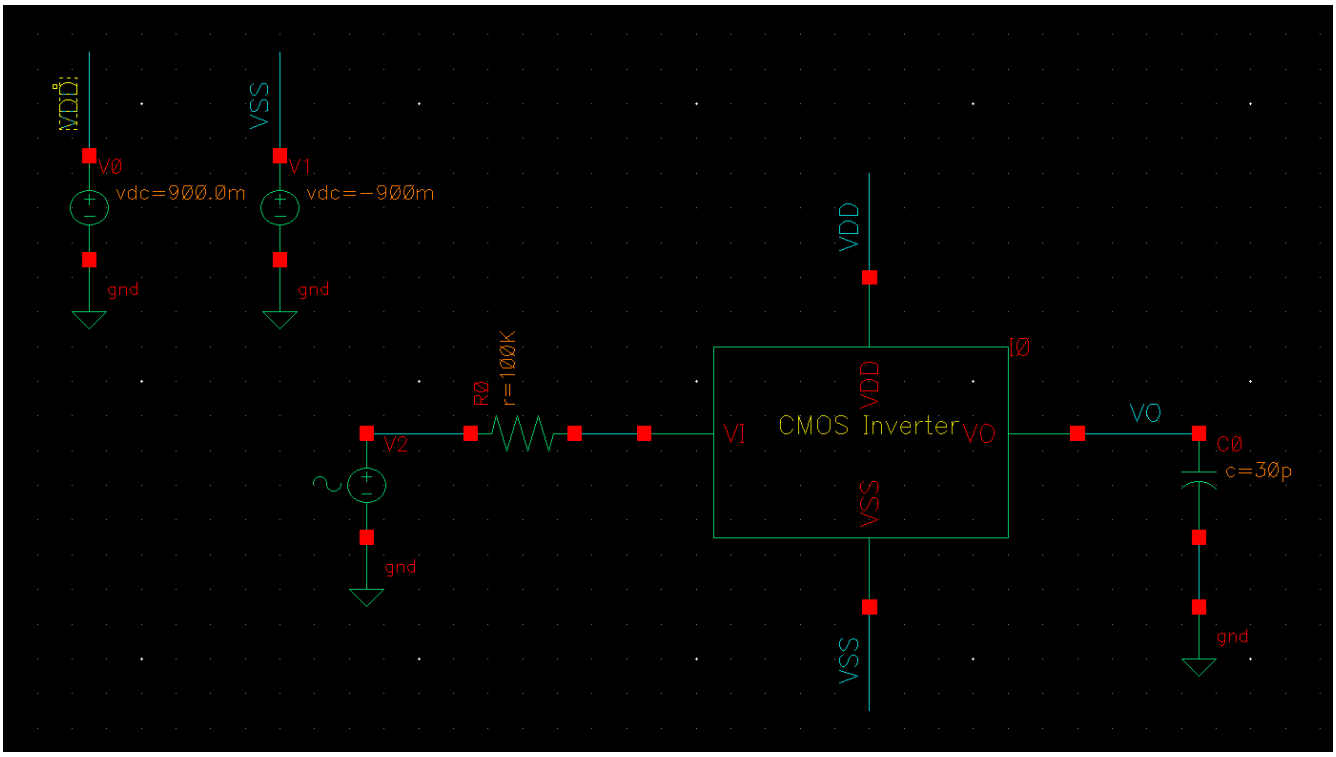

Figure 33: CMOS Inverter Test Bench

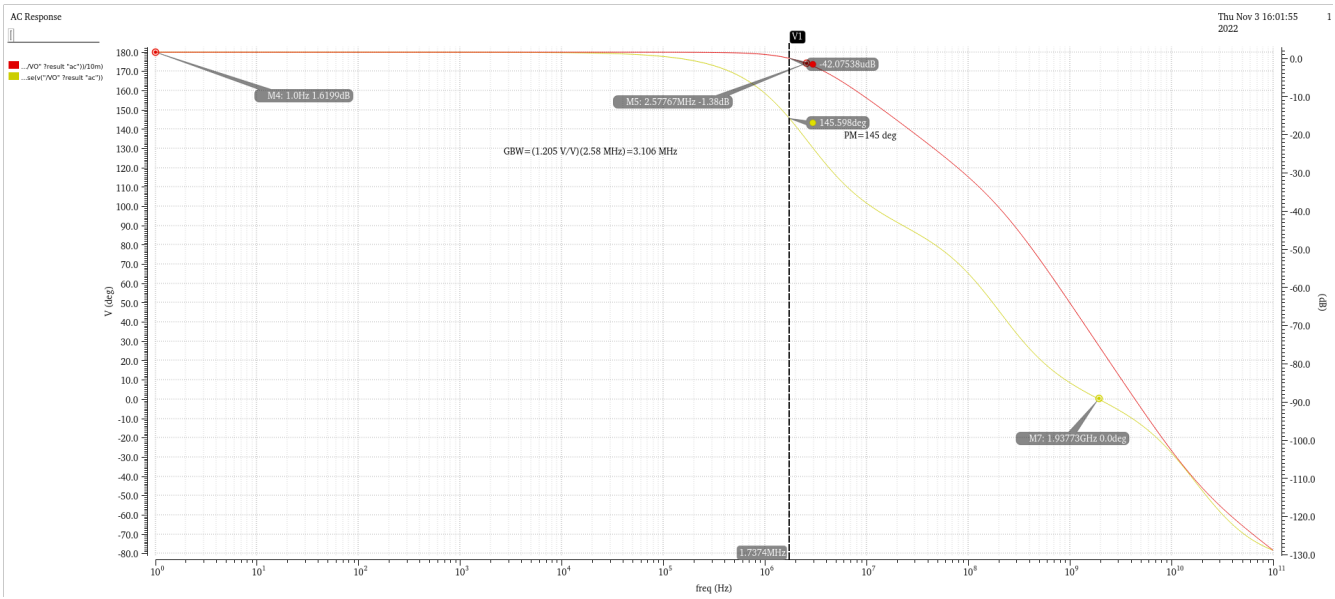

Figure 34: CMOS Inverter AC Simulation

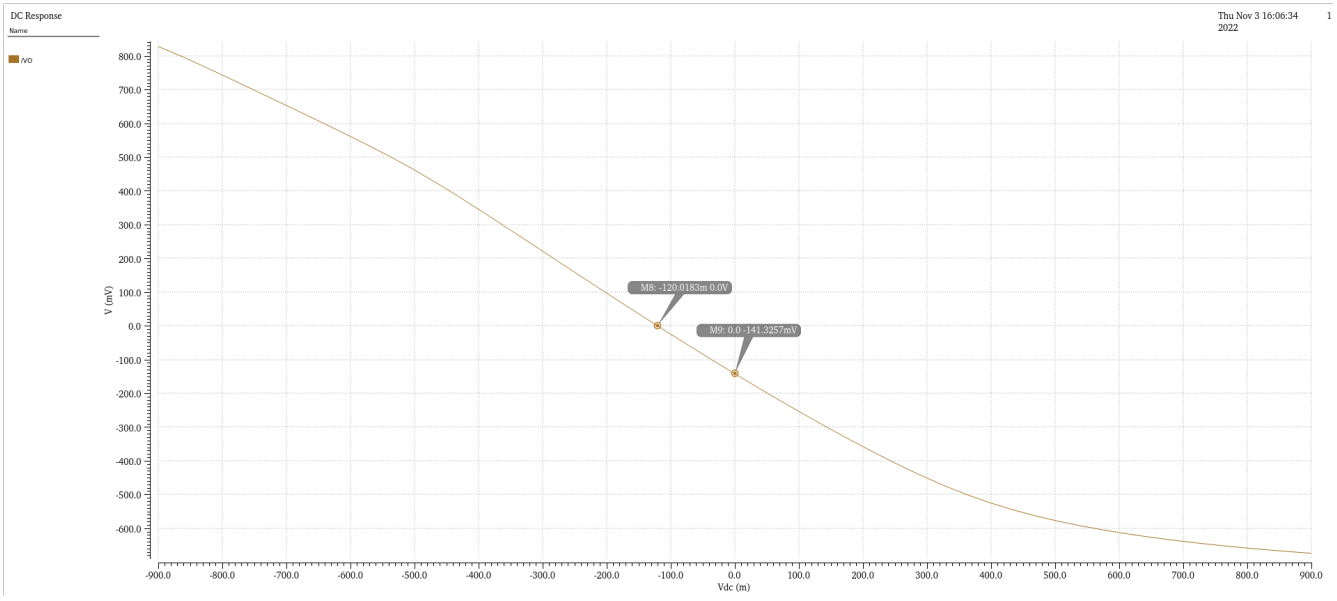

Figure 35: CMOS Inverter DC Simulation

Next, the layout was completed. The design was verified successfully using DRC and LVS.

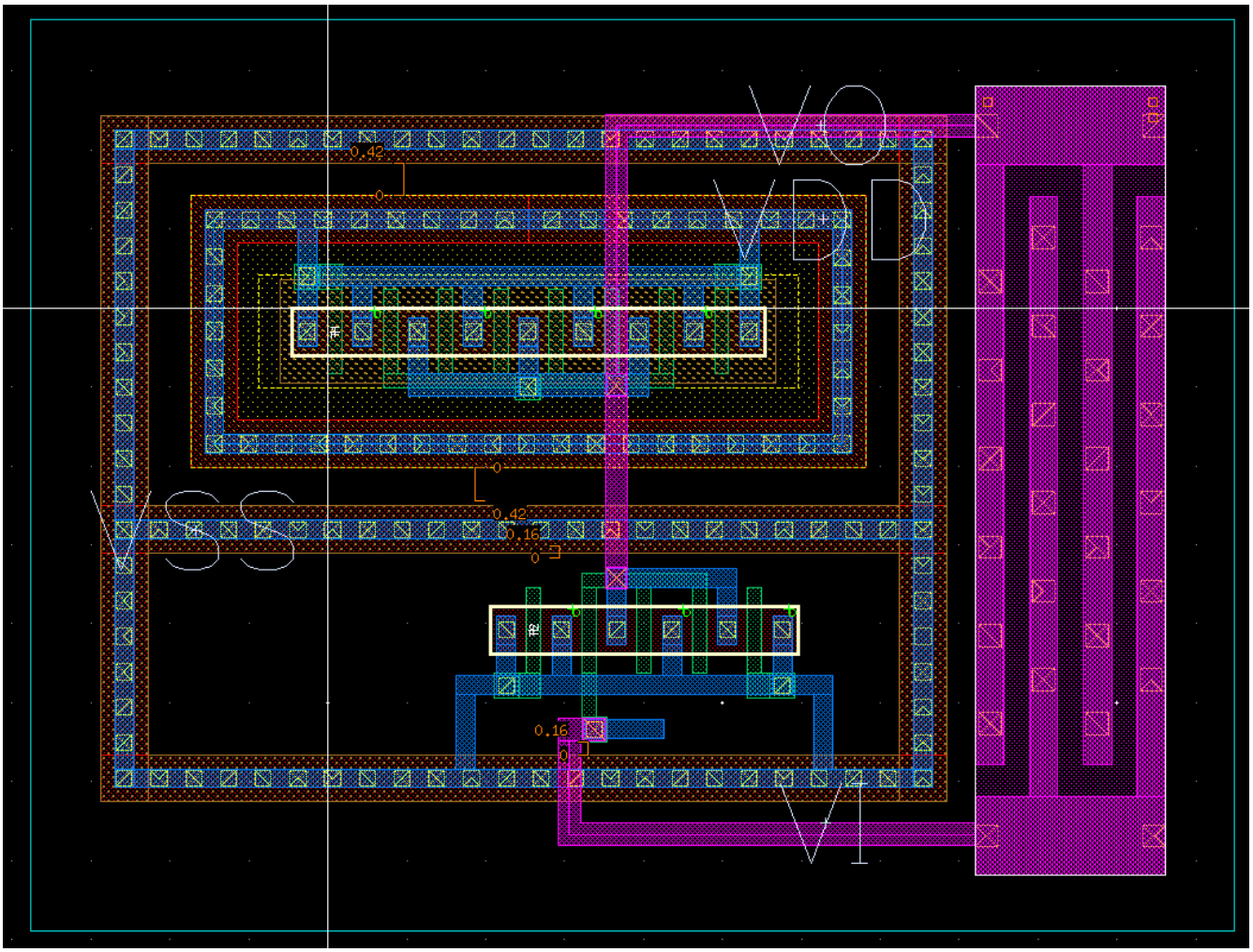

Figure 36: CMOS Inverter Layout

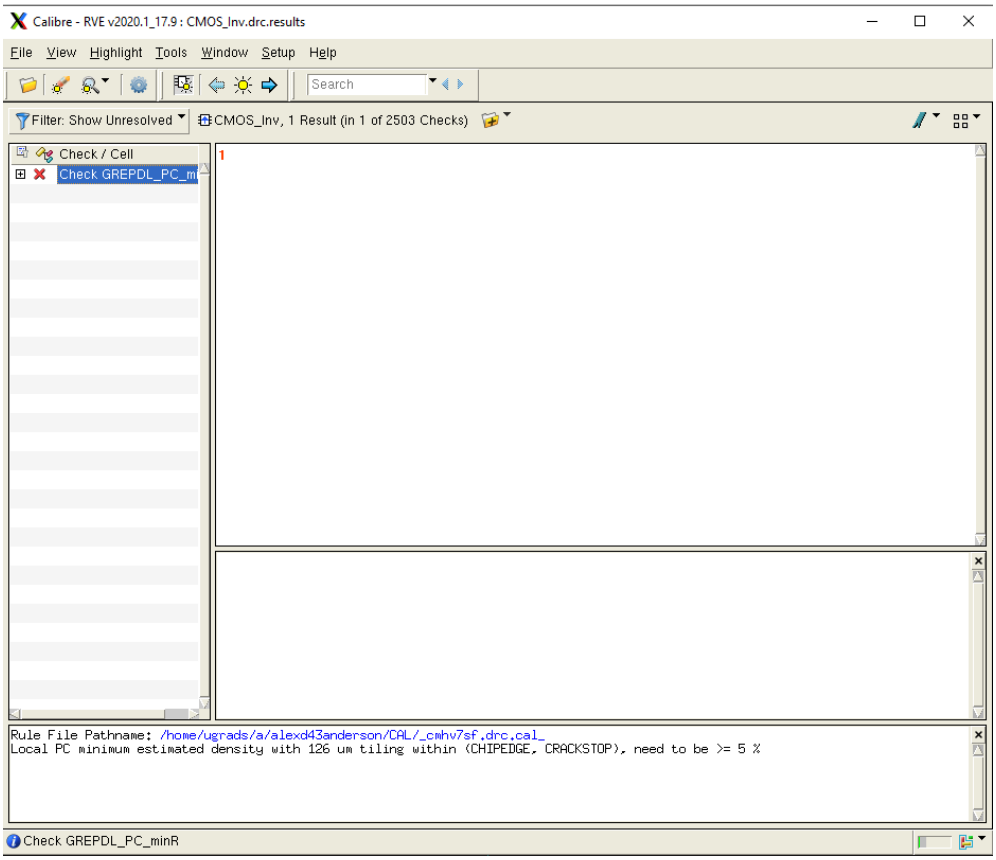

Figure 37: CMOS Inverter DRC

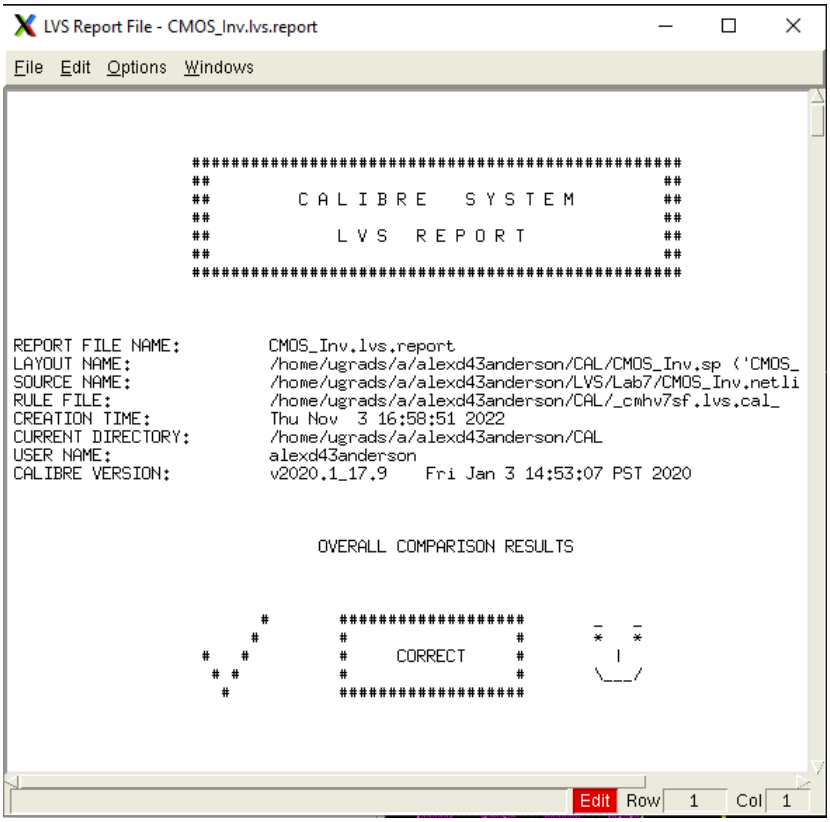

Figure 38: CMOS Inverter LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the AC and DC behavior.

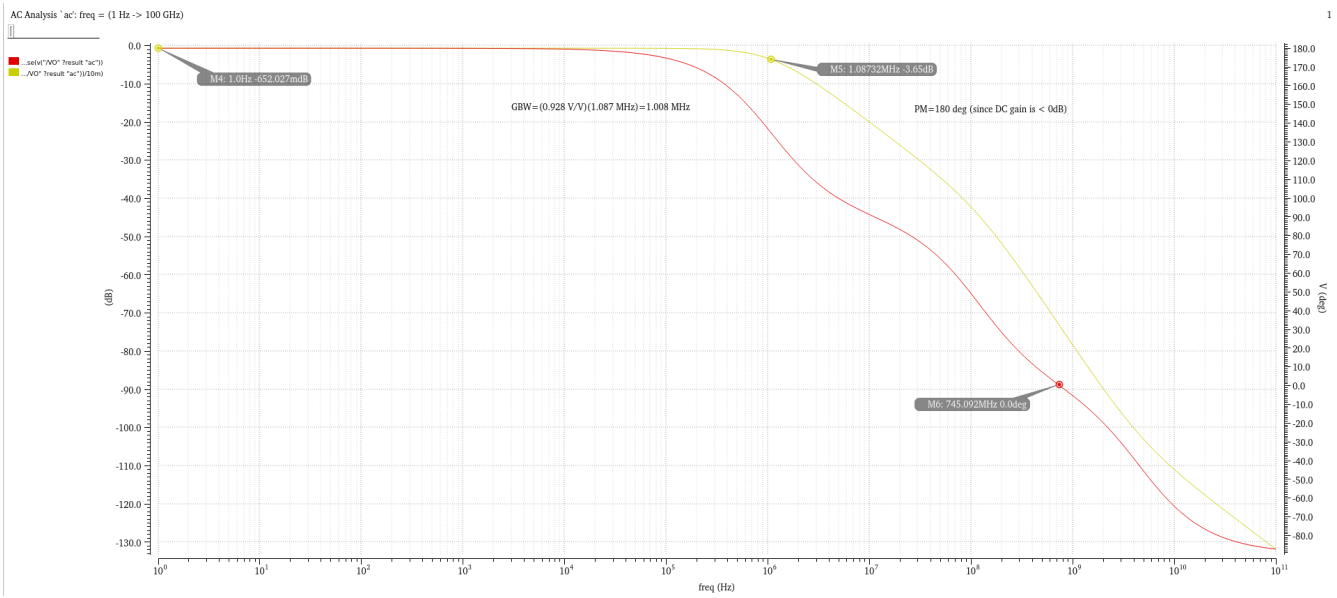

Figure 39: CMOS Inverter AC Post Simulation

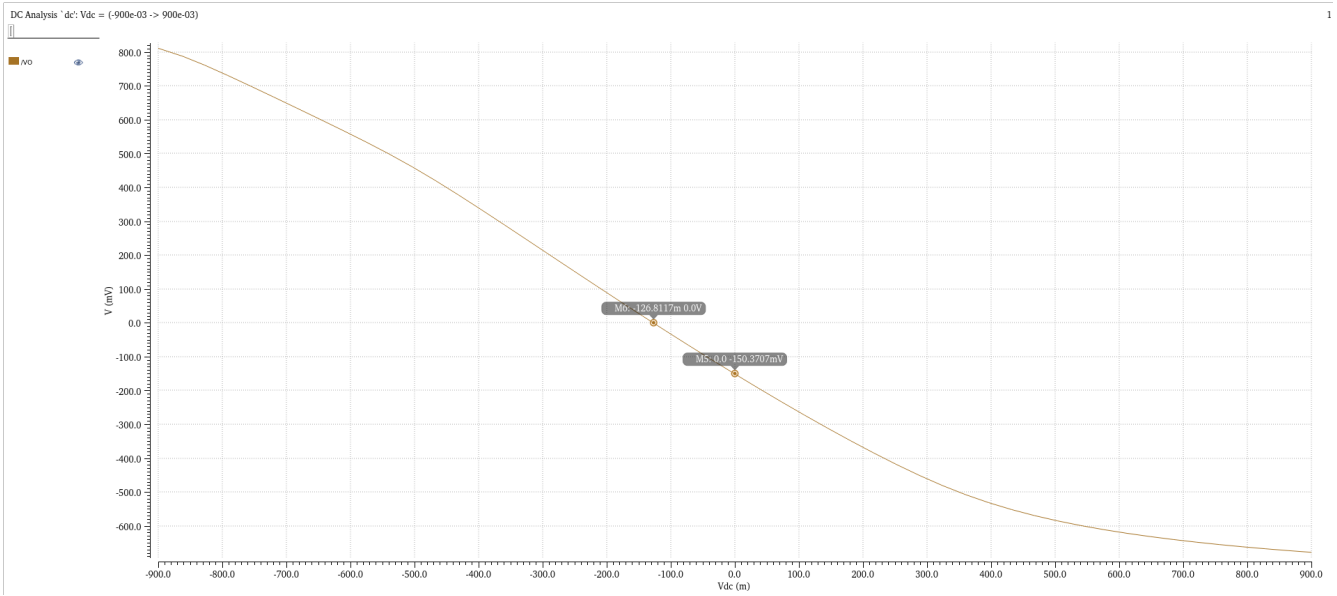

Figure 40: CMOS Inverter DC Post Simulation

Discussion

Overall, the DC behaviors were similar for all designs, particularly the last three. The zero crossing output voltage varied based on design type and device sizes. In all cases, this voltage decreased post-layout, which is understandable when considering additional resistances of traces.

The bandwidth of the self-biased inverters were considerably higher than the first two designs. This was done purposely by using a smaller transistor length (180nm vs. 360nm) in order to meet the GBW specification. In all cases, the bandwidth greatly increased post-layout. In turn, this leads to a larger phase margin. This can be explained by the Miller effect and its methods used in the design. The gain in each case decreased slightly post-layout, which is also reasonable considering resistances of traces.

Conclusion

In this lab, four inverter topographies were designed and compared. Particular attention was given to the frequency response and stability of each system. Post layout simulations were used to compare the behavior of the topologies when considering layout parasitics. As always, good design practices were used in the layout such as common centroid, dummy elements, and guard rings.