Lab 5: Current Mirrors

ECEN 704-601
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Description

In this lab, the design of current mirrors was explored. Two primary circuits were analyzed: a simple current mirror and a low voltage cascode current mirror. As always, good practice layout techniques were used such as common centroid, dummy elements, and guard rings.

Design

First, the simple current mirror was designed. This topography possesses low compliance voltage with the drawback of low output resistance and poor accuracy. The current mirror was designed for a 1:1 ratio with a 100uA input. The compliance voltage was designed to be 100-150mV.

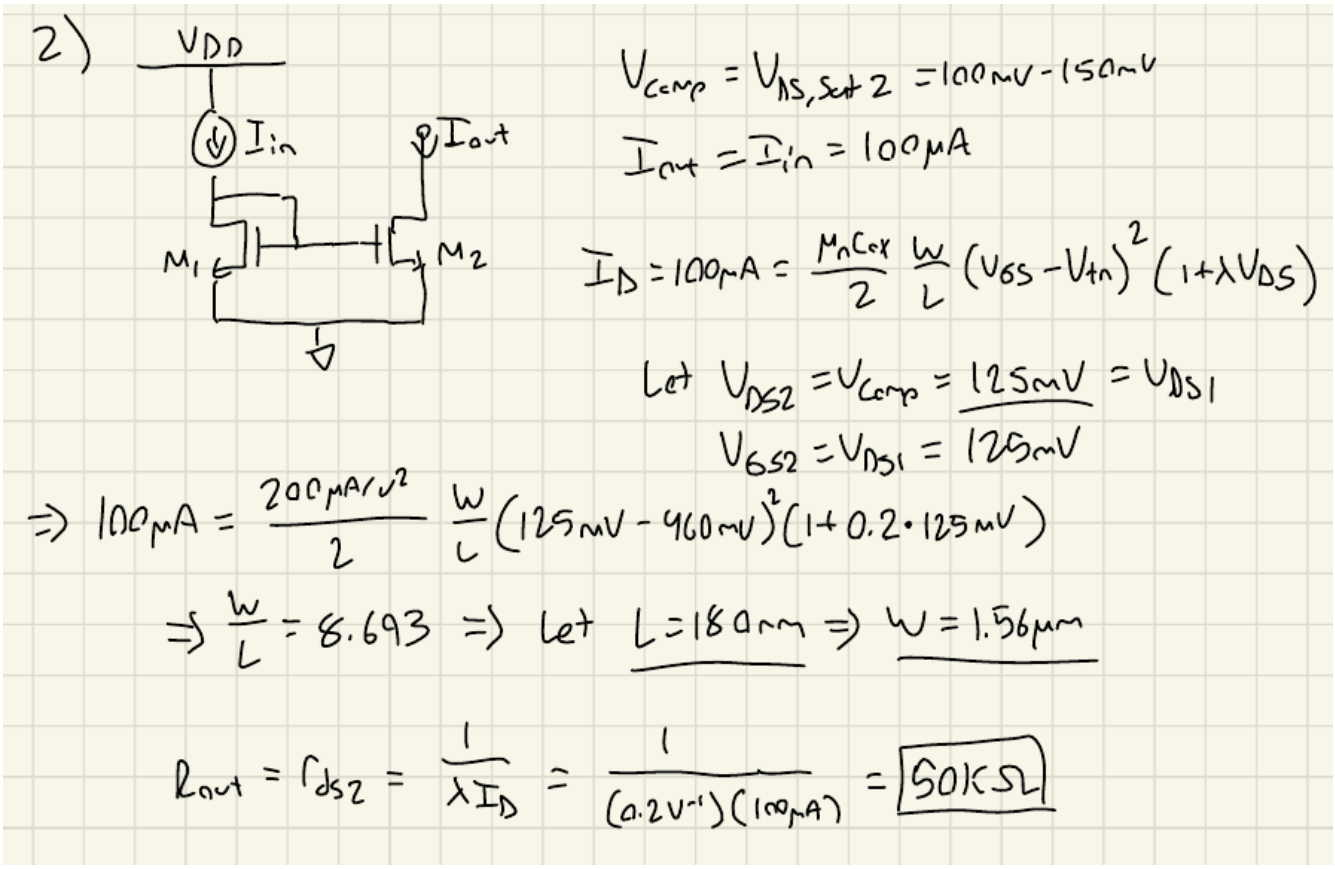

Figure 1: Simple Current Mirror Calculations

From these specifications, a W of 1.56um was calculated given a length of 180nm. The output resistance was found to be 50kΩ.

Next, the low voltage cascode current mirror was designed. This topography offers high output resistance and good accuracy at the cost of complexity and relatively high compliance voltage. The current mirror was designed for a 1:2 ratio with an input current of 50uA. The low frequency output resistance was designed to be more than 1MΩ.

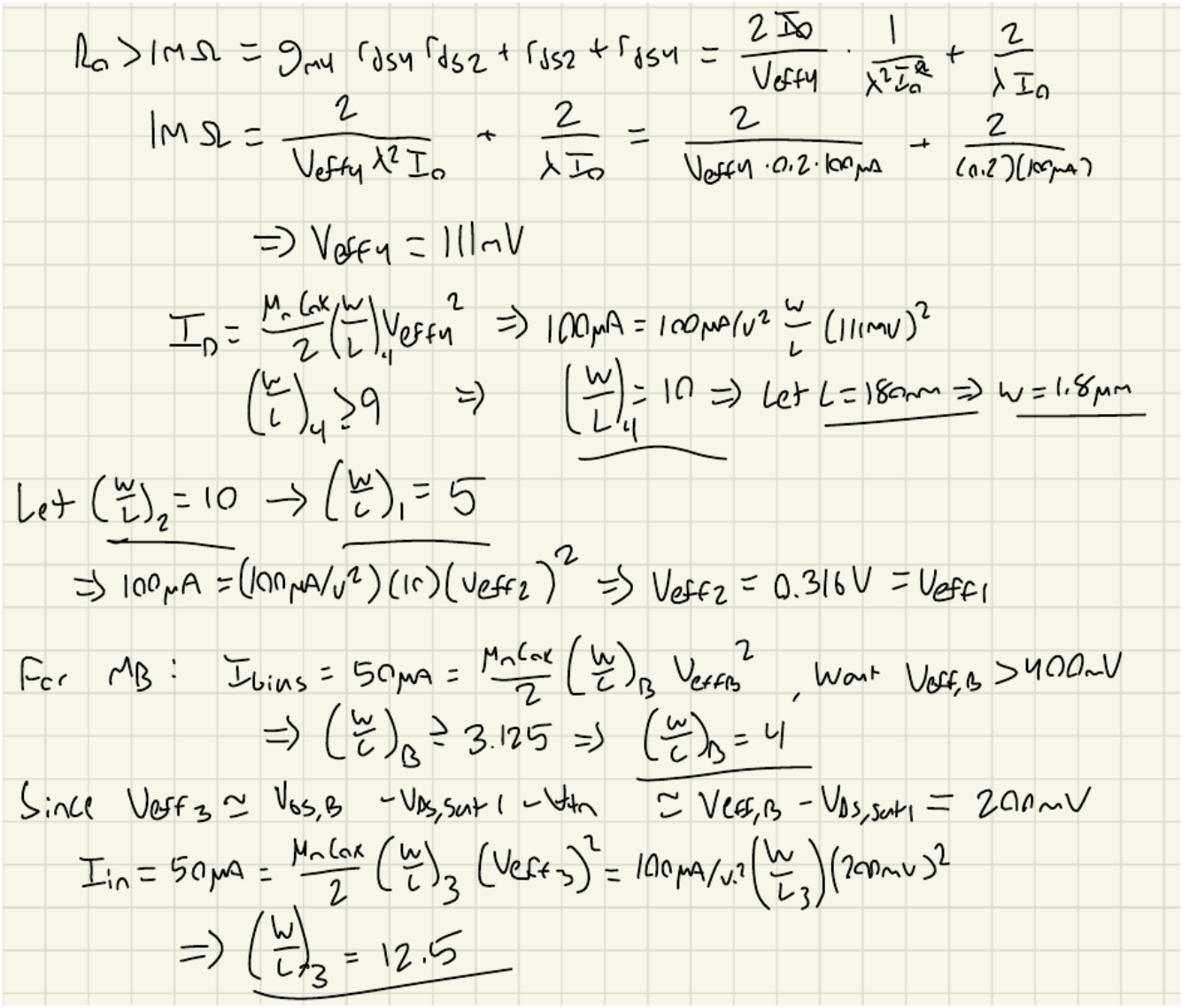

Figure 2: Low Voltage Cascode Current Mirror Calculations

From here, both devices were simulated and adjusted accordingly to achieve the desired specifications. For the low voltage cascode current mirror, the lengths of all devices was increased to 360nm. Doing this increased lambda, thus increasing the overall output resistance. Changes to device sizes were also made in order to correctly adjust the DC outputs and compliance voltages.

Results

The schematic for the simple current mirror is shown below in Figure 3, including dummy elements.

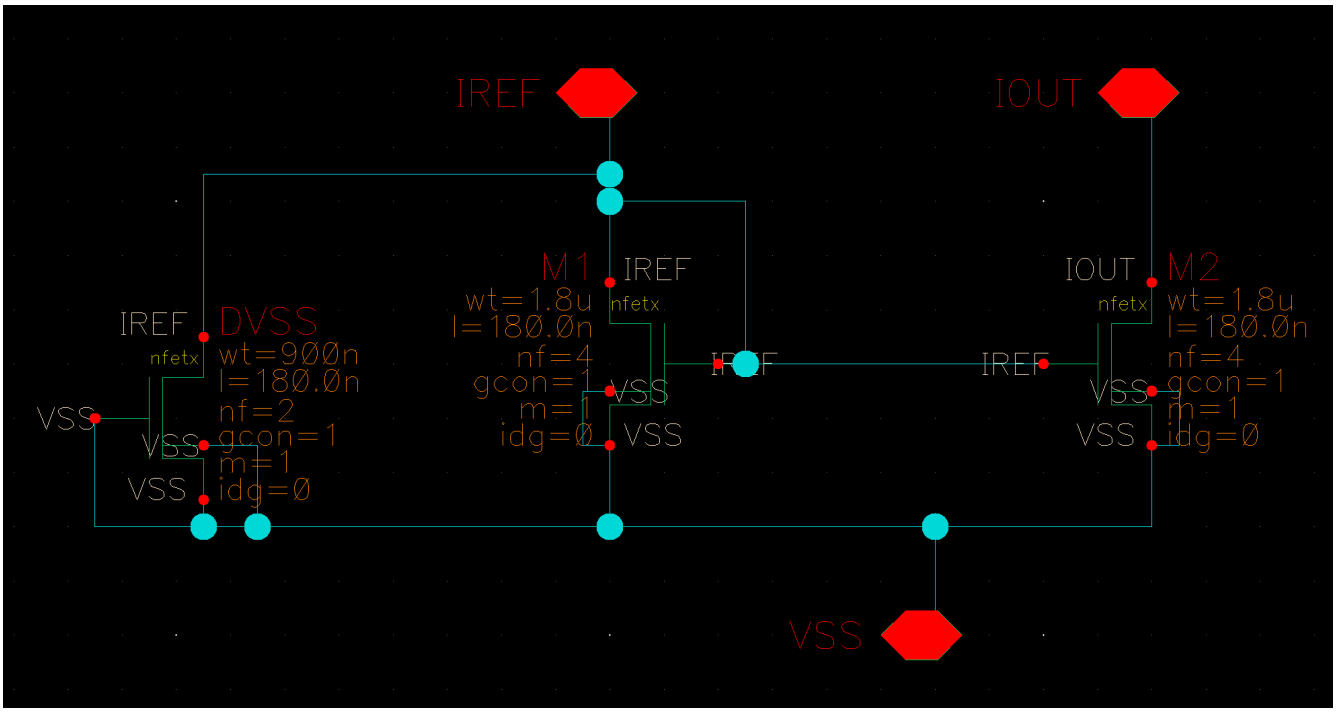

Figure 3: Simple Current Mirror Schematic

From here, a test bench for the system was created and simulations for the compliance voltage and output resistance were performed.

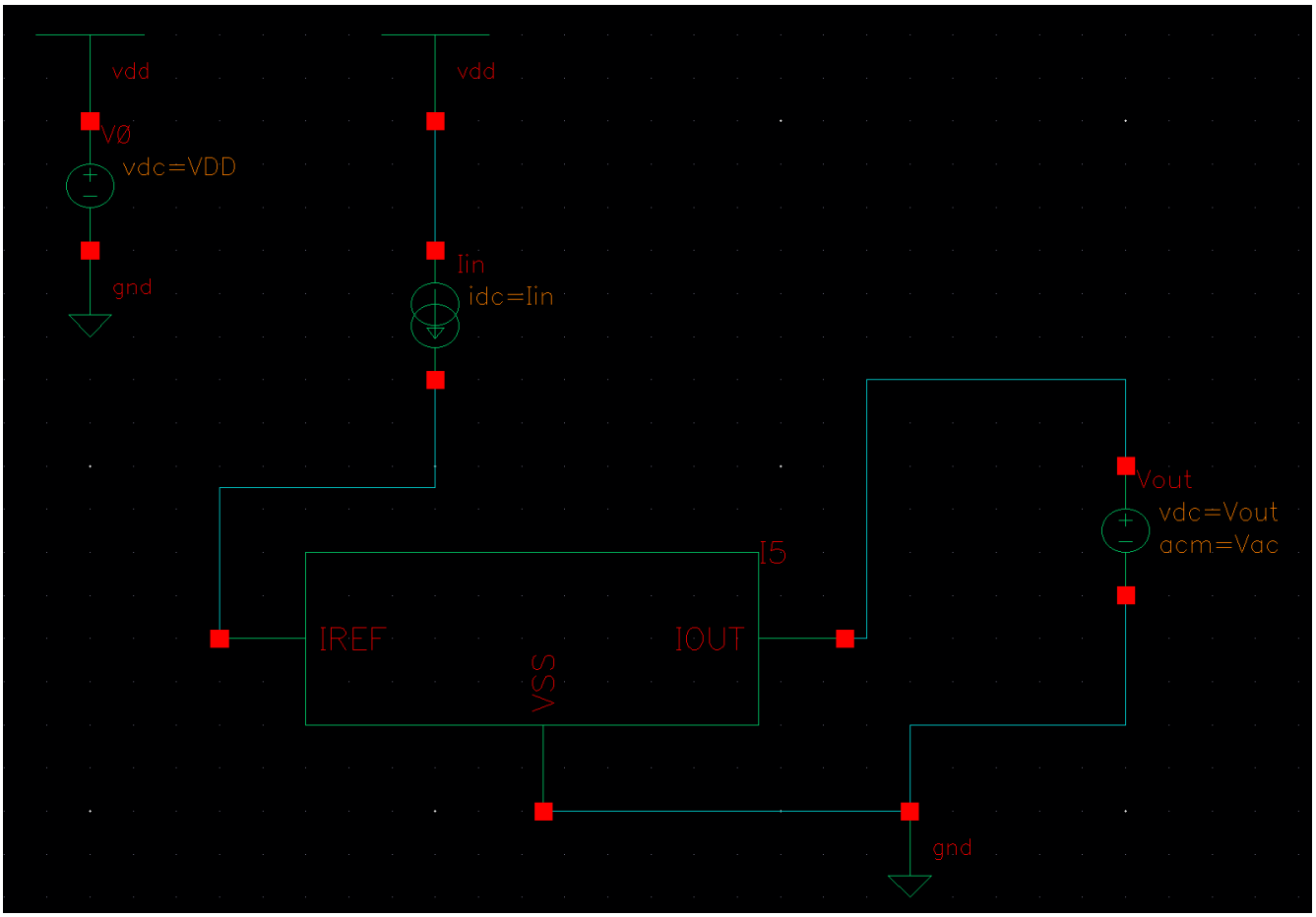

Figure 4: Simple Current Mirror Test Bench

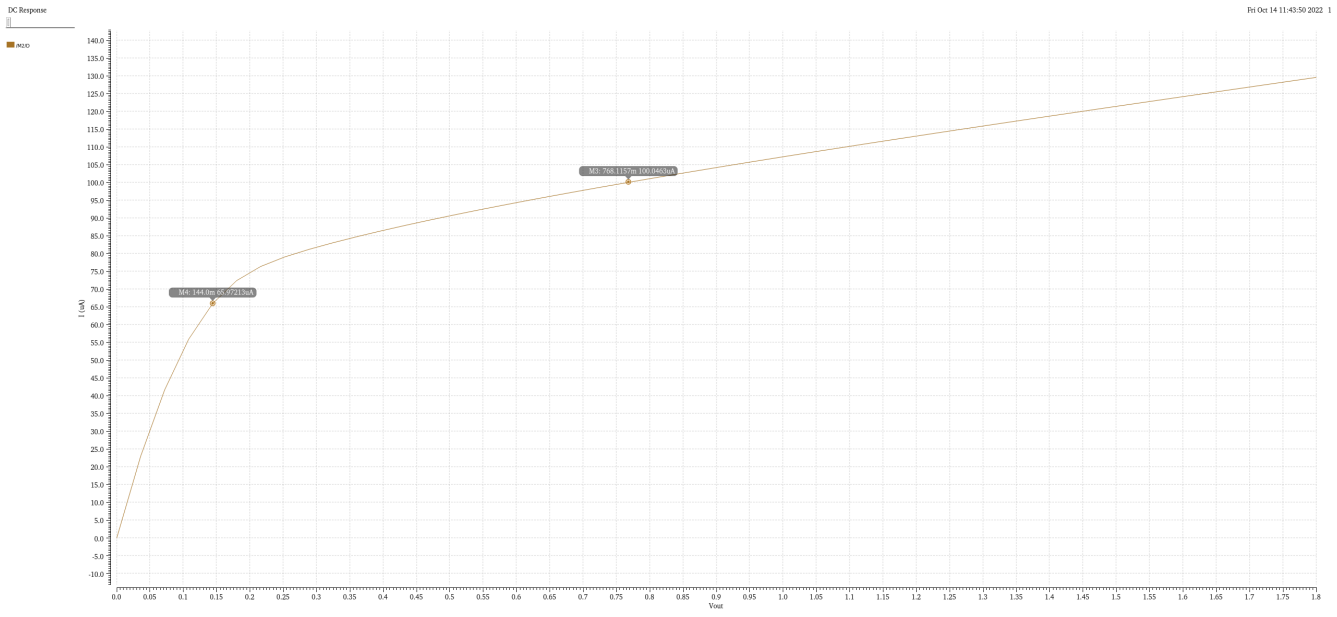

Figure 5: Simple Current Mirror Compliance Voltage

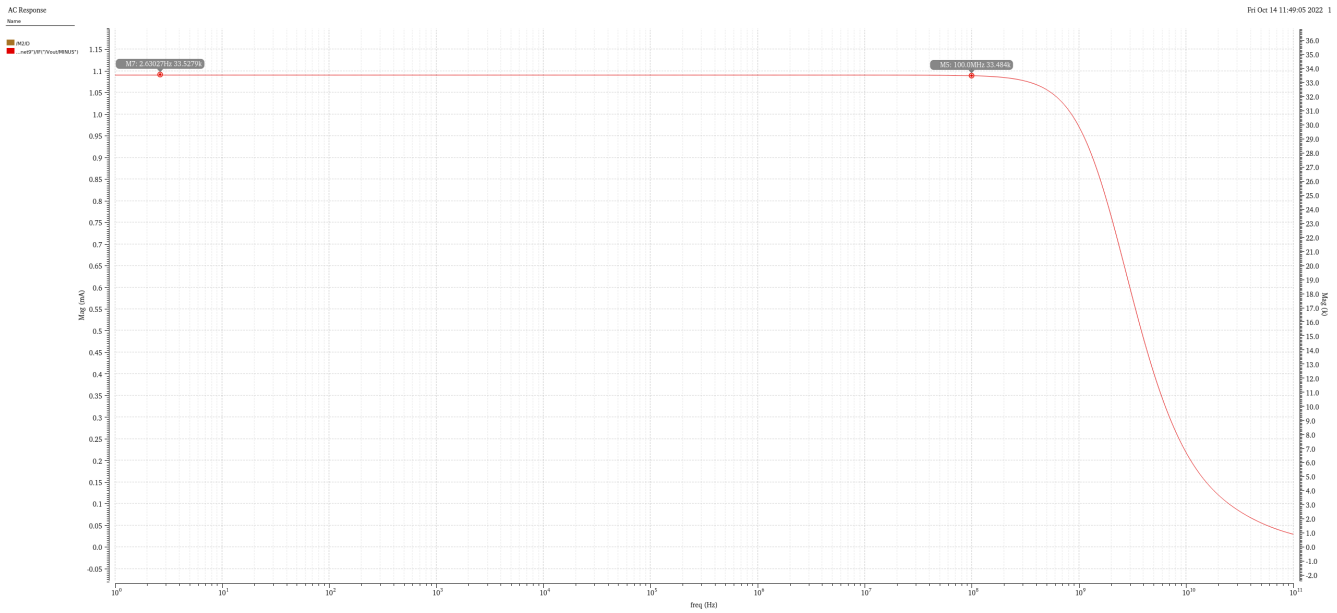

Figure 6: Simple Current Mirror Output Resistance

Next, the layout was completed. The design was verified successfully using DRC and LVS.

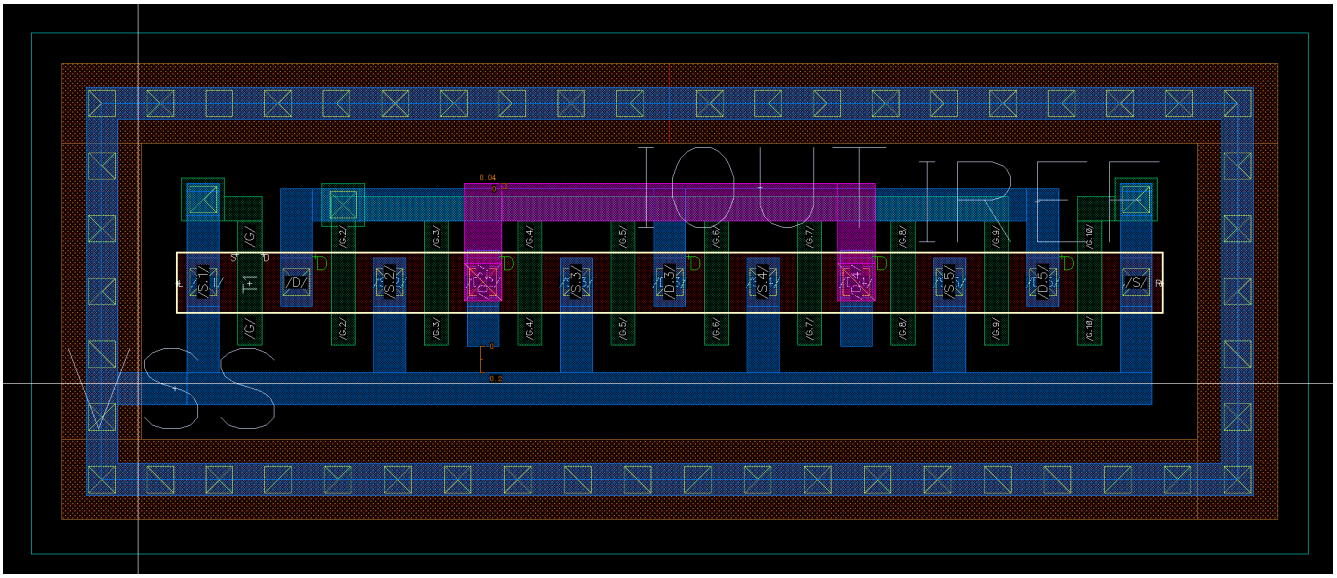

Figure 7: Simple Current Mirror Layout

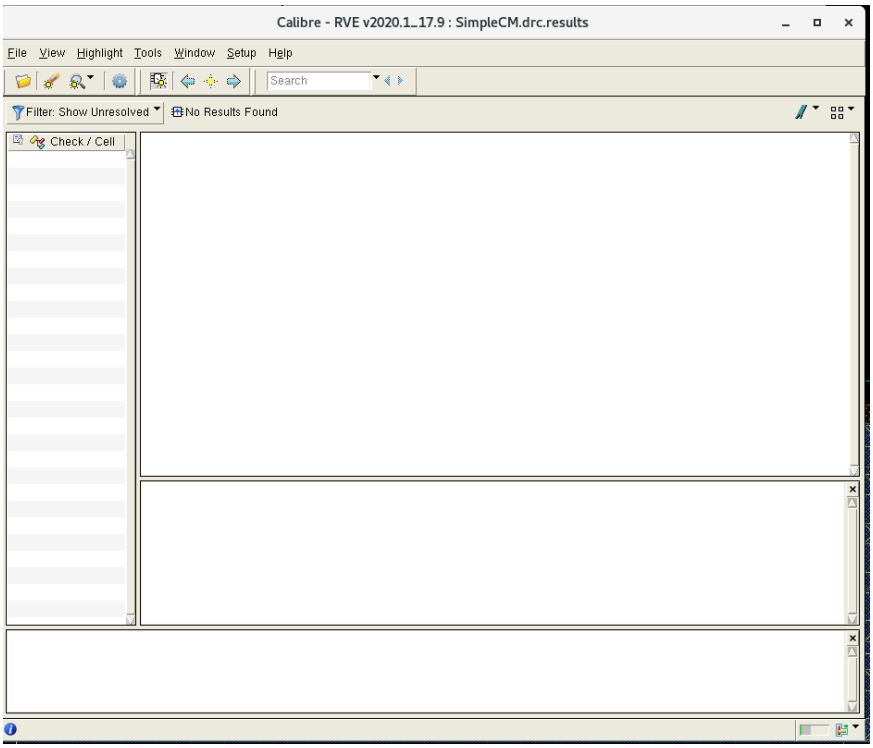

Figure 8: Simple Current Mirror DRC

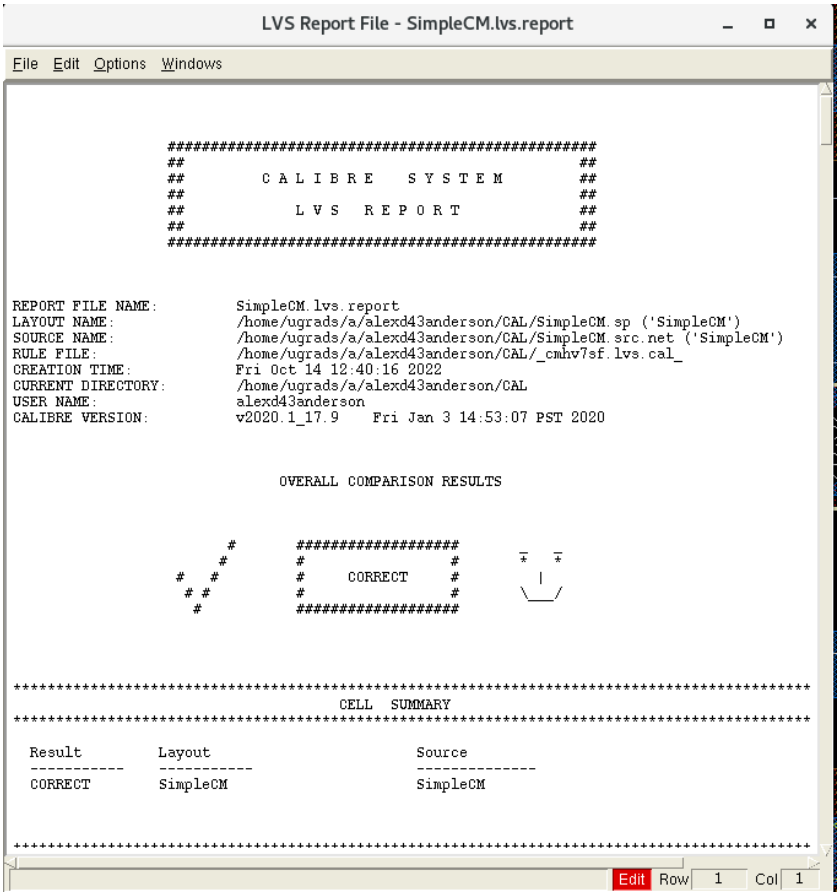

Figure 9: Simple Current Mirror LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the output resistance and compliance voltage.

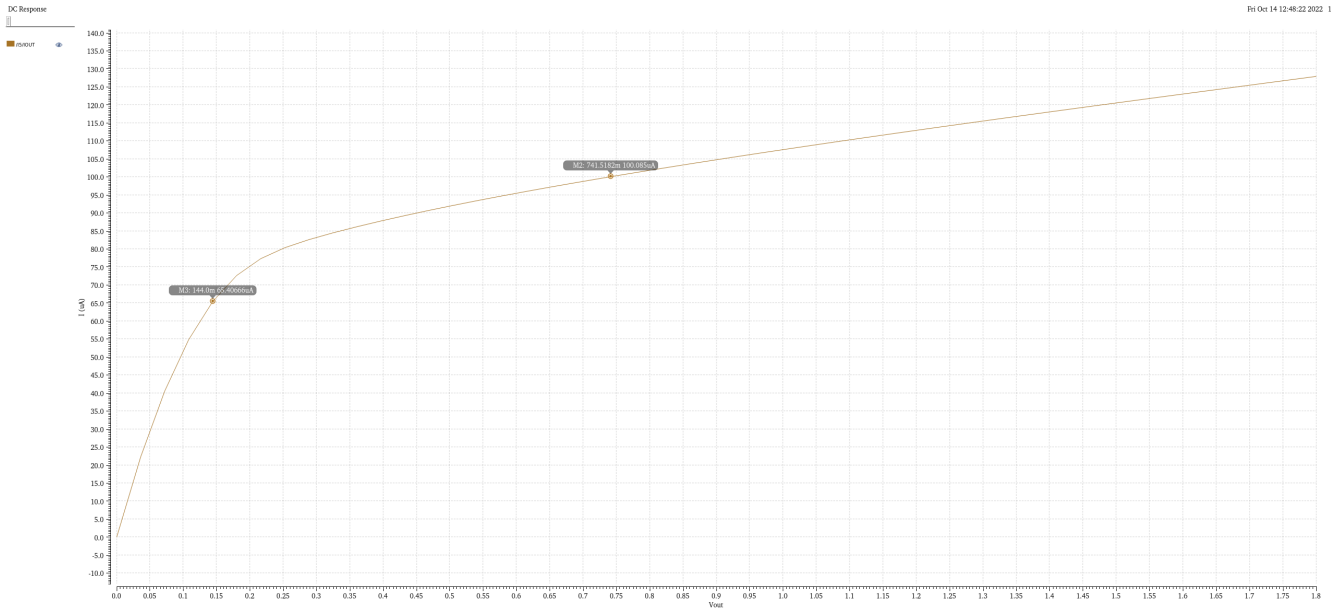

Figure 10: Simple Current Mirror Post Layout Compliance

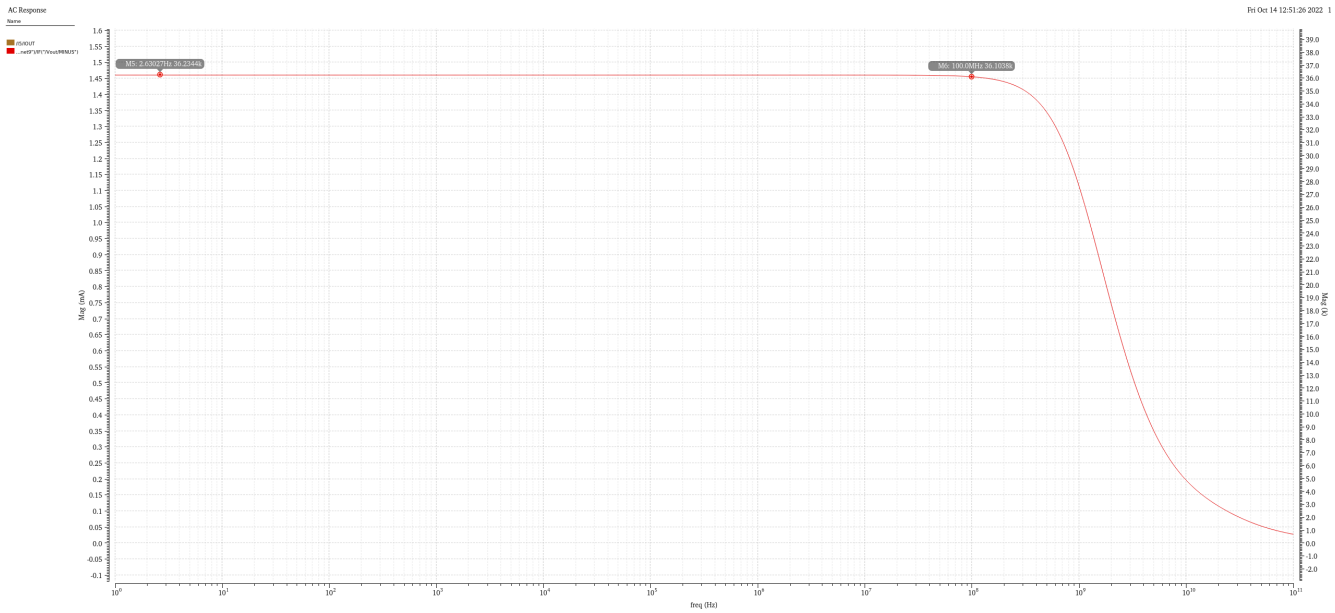

Figure 11: Simple Current Mirror Post Layout Output Resistance

The schematic for the low voltage cascode current mirror is shown below in Figure 12, including dummy elements that were added post-layout.

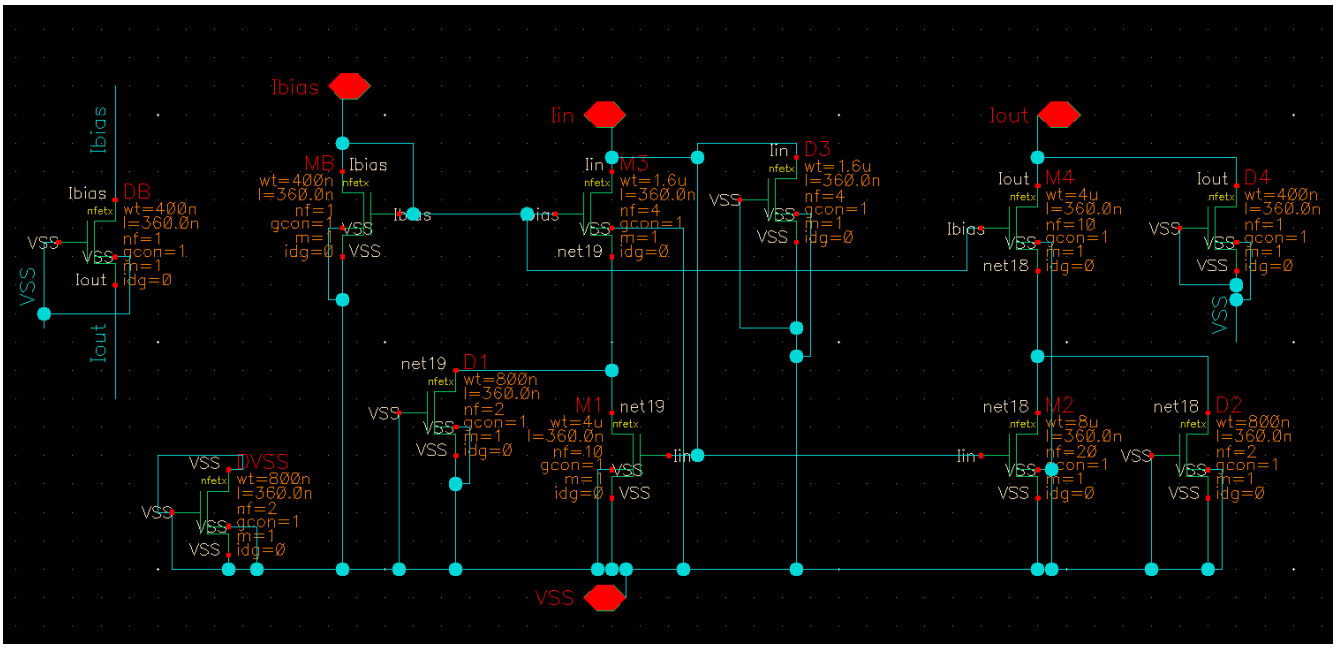

Figure 12: LV Cascode CM Schematic

From here, a test bench for the system was created and simulations for the compliance voltage and output resistance were performed.

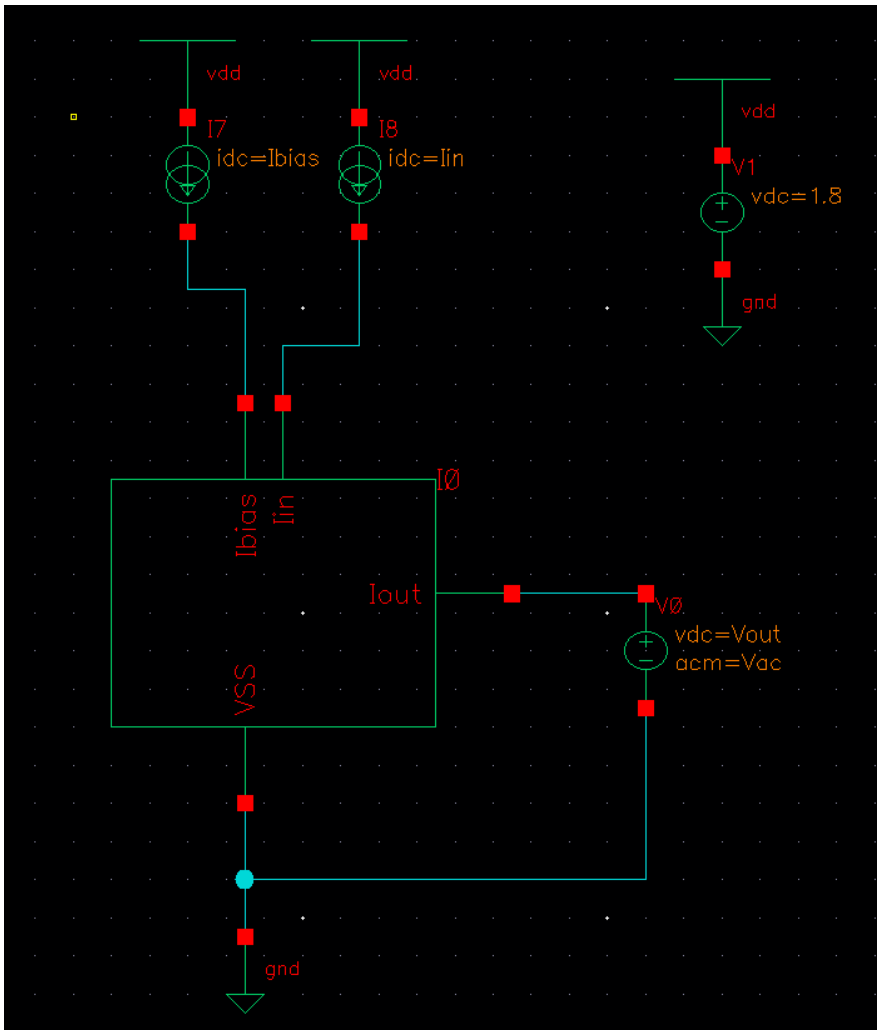

Figure 13: LV Cascode CM Test Bench

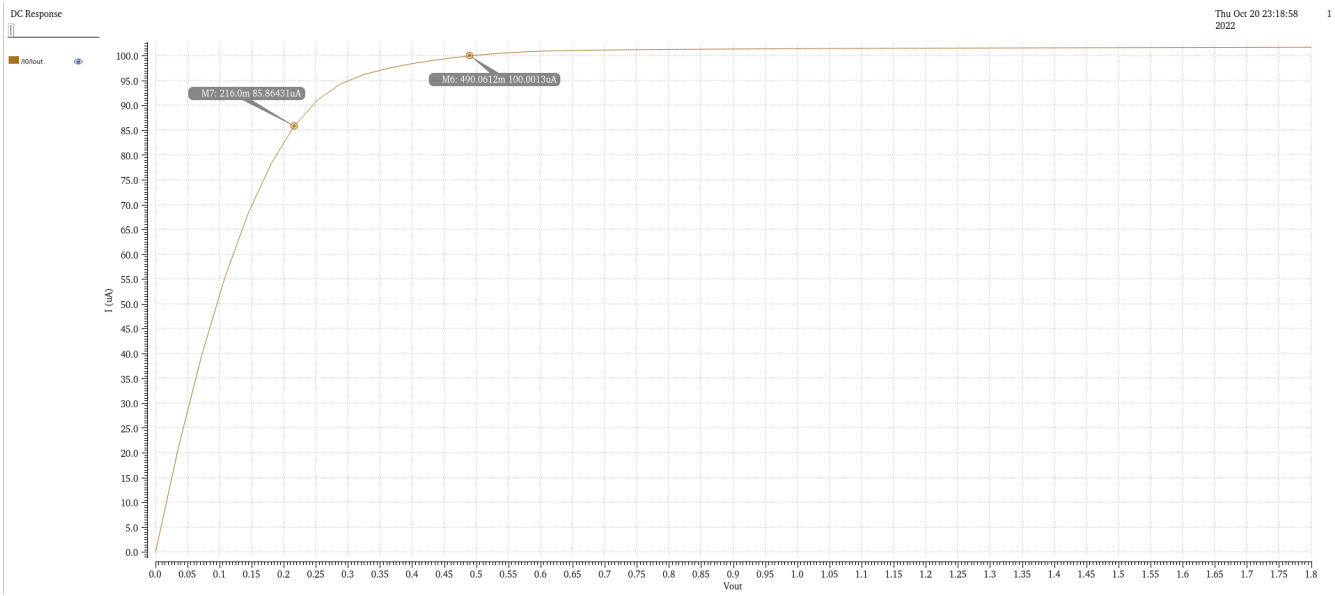

Figure 14: LV Cascode CM Compliance Voltage

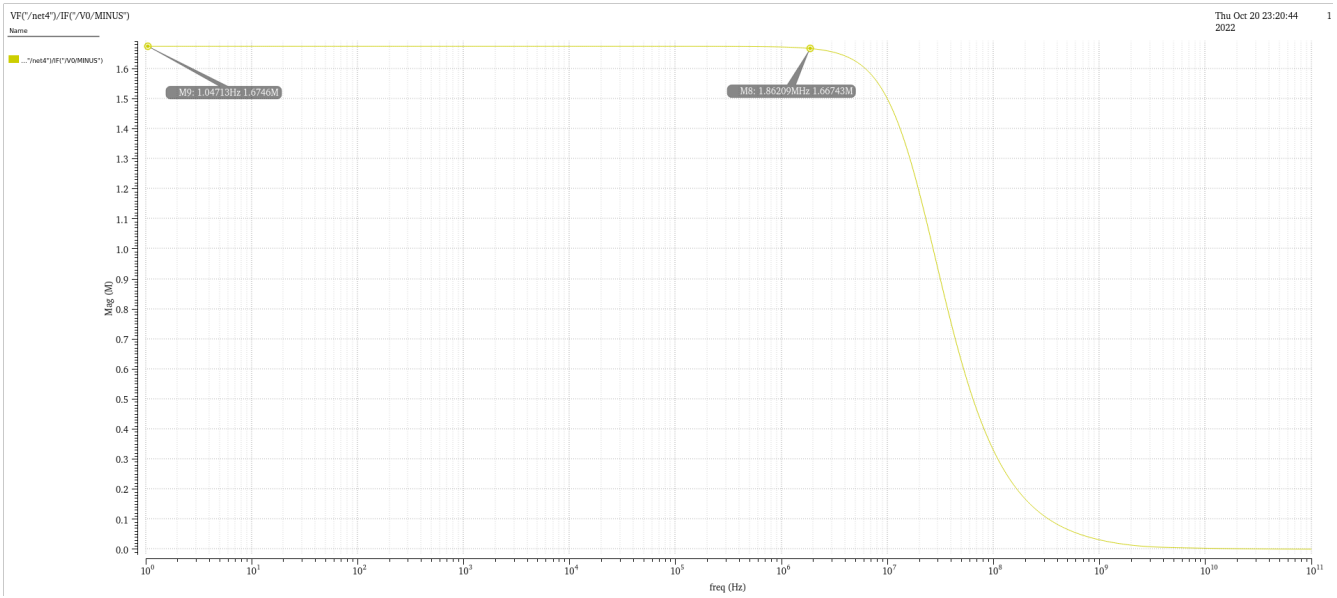

Figure 15: LV Cascode CM Output Resistance

Next, the layout was completed. The design was verified successfully using DRC and LVS.

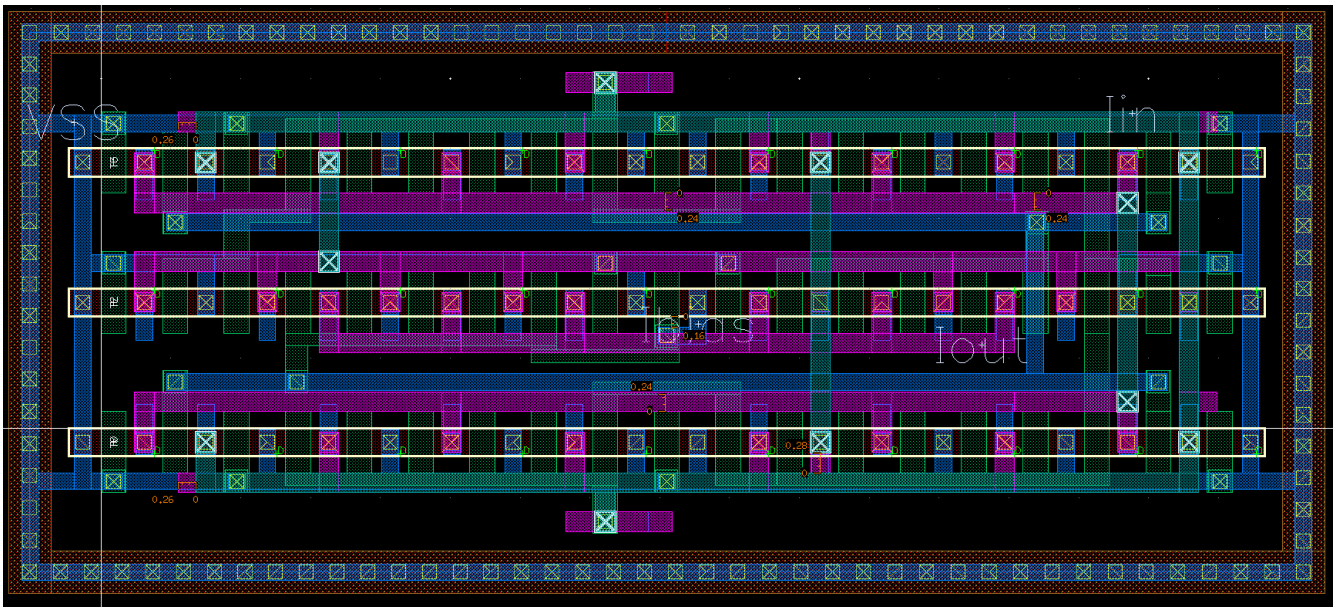

Figure 16: LV Cascode CM Layout

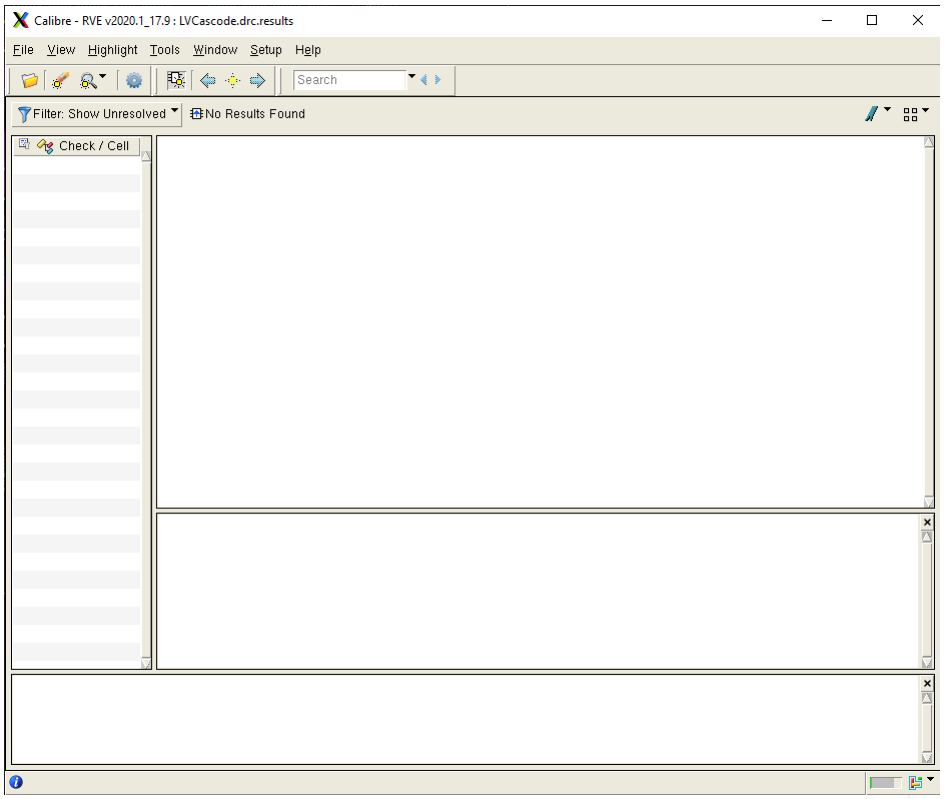

Figure 17: LV Cascode CM DRC

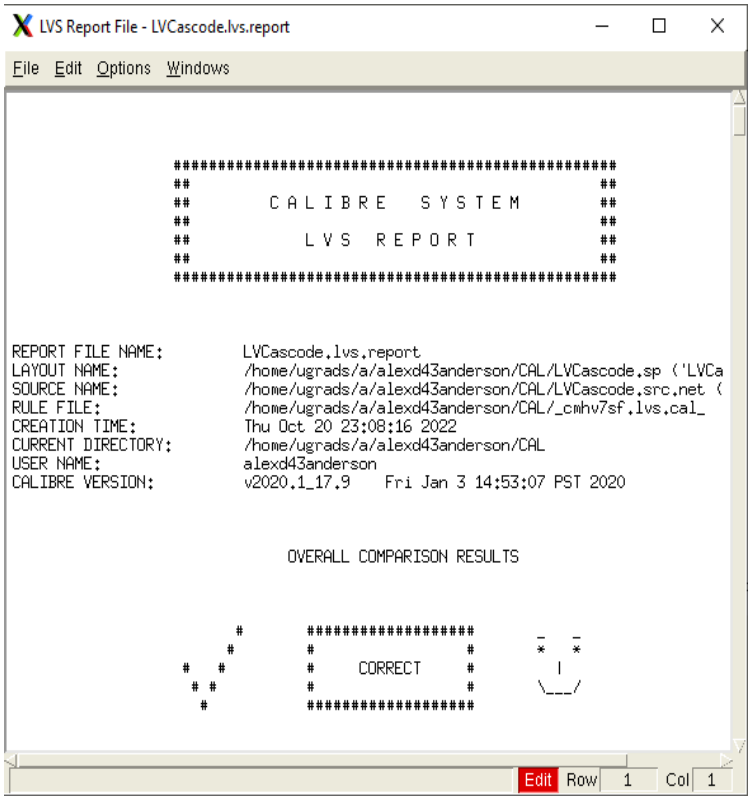

Figure 18: LV Cascode CM LVS

Finally, with the layout complete and checked, the parasitics were extracted and used to perform post layout simulations of the output resistance and compliance voltage.

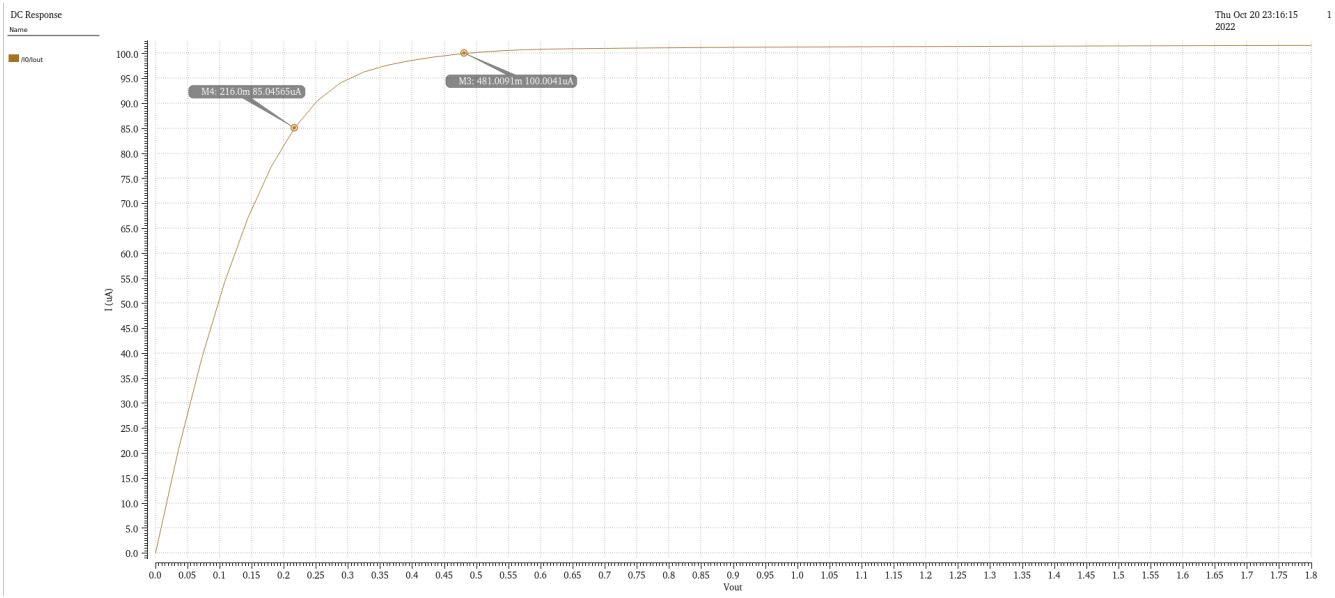

Figure 19: LV Cascode CM Post Layout Compliance Voltage

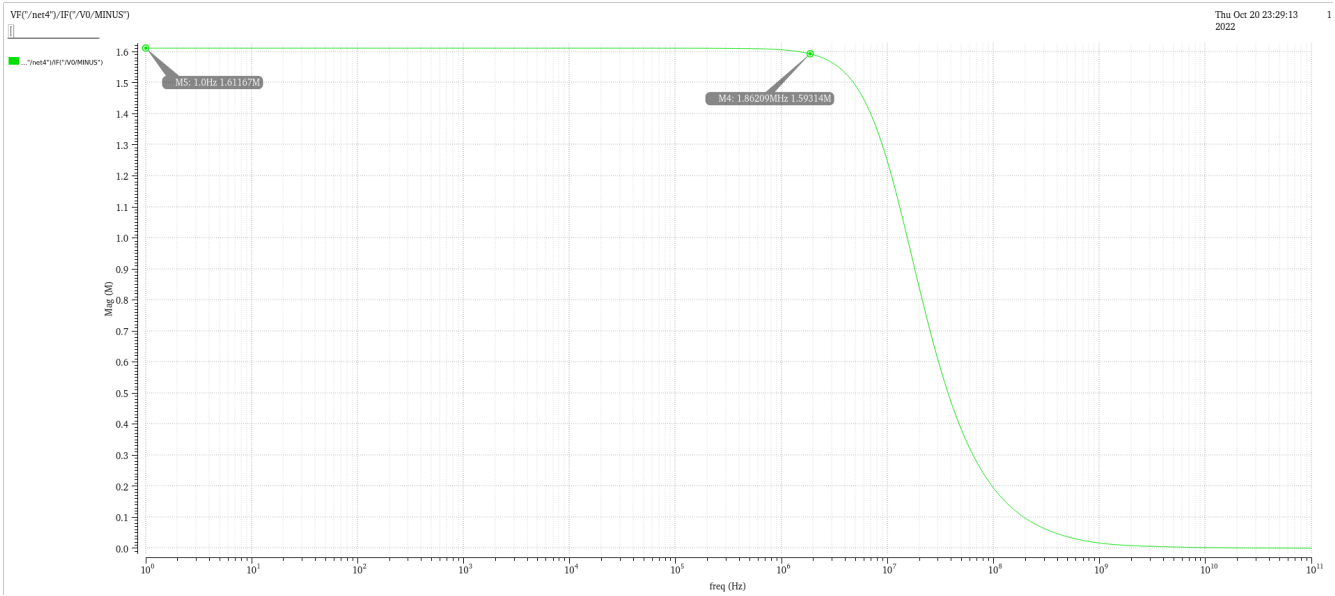

Figure 20: LV Cascode CM Post Layout Output Resistance

Discussion

In both cases, the compliance voltage decreased slightly when considering layout parasitics. This is likely due to slight variations in DC currents due to resistive parasitics of the metal interconnects. Similarly, the output resistance increases and the bandwidth decreases in both cases. Variation in the output resistance can also be attributed to DC factors such as trace resistance, while the bandwidth decrease can be attributed to the capacitances and inductances of the traces, vias, and transistors. While this variation was extremely small, for larger designs care must be taken in layout to ensure that large differences in device behavior do not occur.

Comparing the simple current mirror to the low voltage cascode current mirror, the simple current mirror displays slightly superior compliance voltage (144mV vs. 216mV) while possessing vastly inferior output resistance (36.23kΩ vs. 1.61MΩ). The simple current mirror does also have the upside of low complexity, as is evident in comparing the layouts of the two topographies.

Conclusion

In this lab, two current mirror topographies were designed and compared. Post layout simulations were used to compare the behavior of the systems when considering layout parasitics. As always, good design practices were used in the layout such as common centroid, dummy elements, and guard rings.