Lab 9: Optimization using Logical Effort

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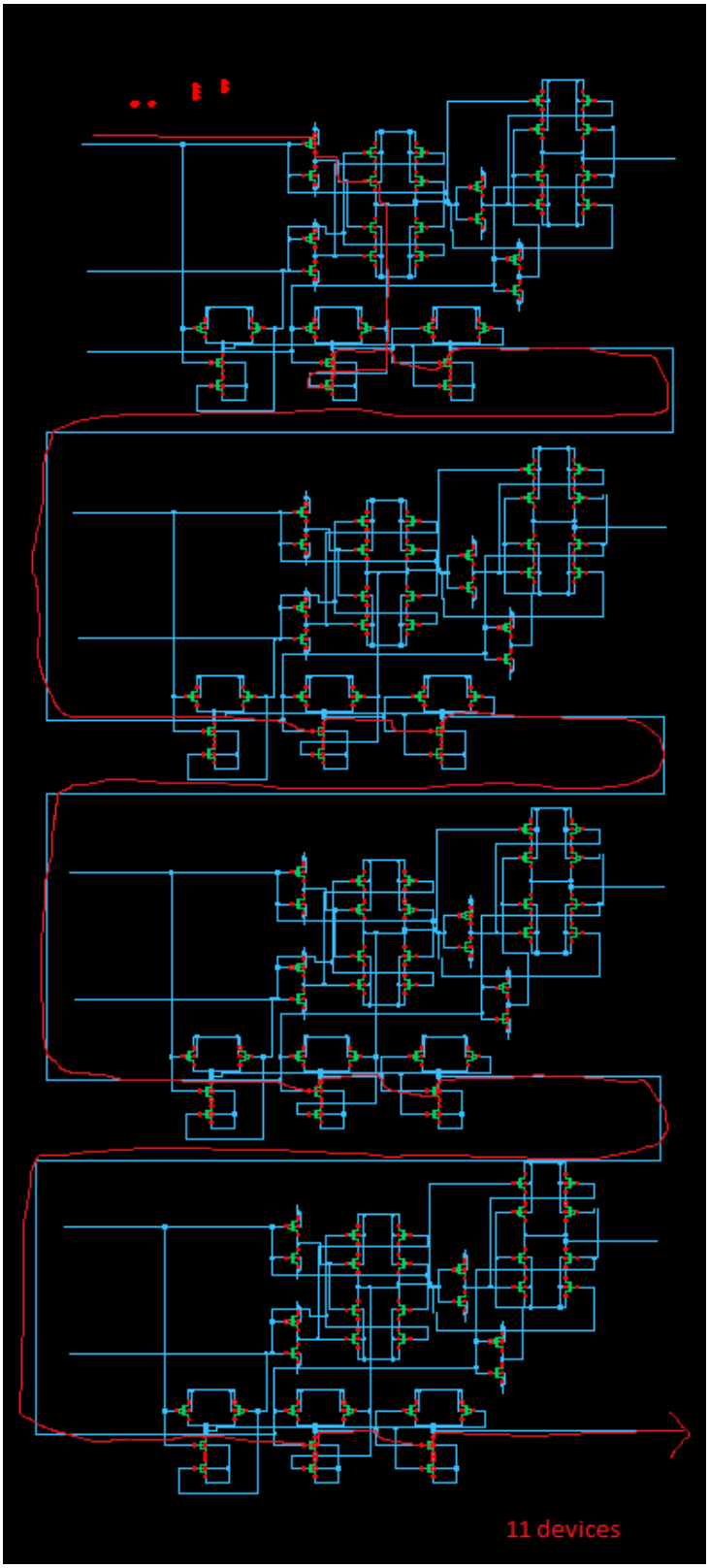
ECEN 714-603

First, the critical path was determined from the 4-bit adder circuit:



From this, there are 9 stages (8 NAND and 1 XOR). The calculations of the logical effort are below:

(2) $G = \prod g_i$:

$$g_{xor} = \frac{C_{in}}{C_{inv}} = \frac{8}{3}$$

$$g_{nand} = \frac{C_{in}}{C_{in,inv}} = \frac{4}{3}$$

$$G = g_{xor} \cdot g_{nand}^{\,8} = \frac{8}{3} + \left(\frac{4}{3}\right)^8 = \frac{40}{3} = 26.637$$

$$H = \frac{C_{out,path}}{C_{in,path}} = \frac{30fF}{6.548fF} = 4.582$$

$$B = \prod b_i = \left(\frac{C_{xor} + C_{nand}}{C_{nand}}\right) \cdot \left(\frac{C_{nand} + C_{xor}}{C_{xor}}\right)^8$$

$$= \left(\frac{6.548fF + 3.275fF}{3.275fF}\right) \cdot \left(\frac{3.275fF + 6.548fF}{6.548fF}\right)^8$$

$$= 76.934$$

$$\hat{f} = F^{1/N} = (G \cdot B \cdot H)^{1/9} = (26.637 \cdot 4.582 \cdot 76.934)^{1/9} = 2.763$$

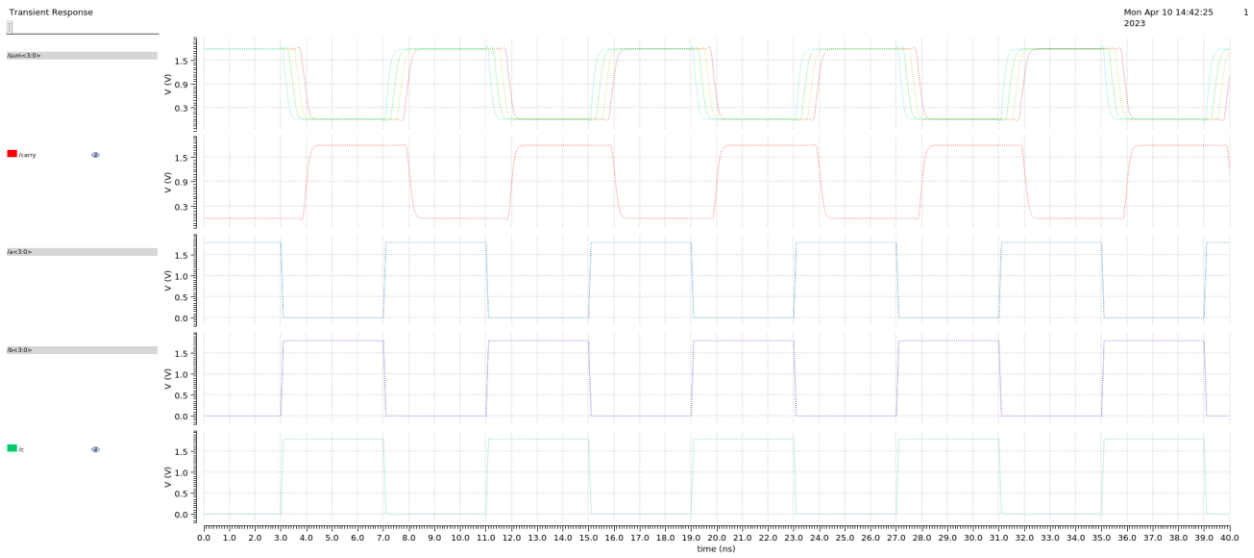
(3) $$C_{in,nand} = \frac{g_{nand} C_{out}}{\hat{f}} = \frac{\frac{4}{3} \cdot 30fF}{2.763} = 14.477fF$$

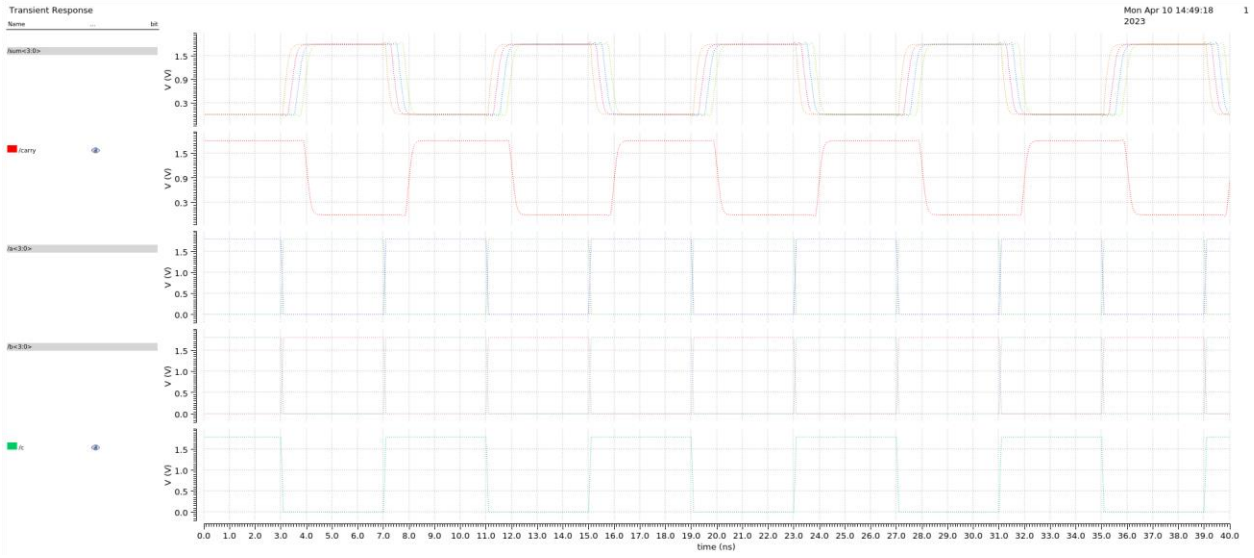
$$\frac{14.477fF}{2.519\ fF/\mu m} = 5.747\ \mu m \Rightarrow \boxed{\begin{array}{l} W_p = 1.92\ \mu m \\ W_n = 0.96\ \mu m \end{array}}$$ NAND

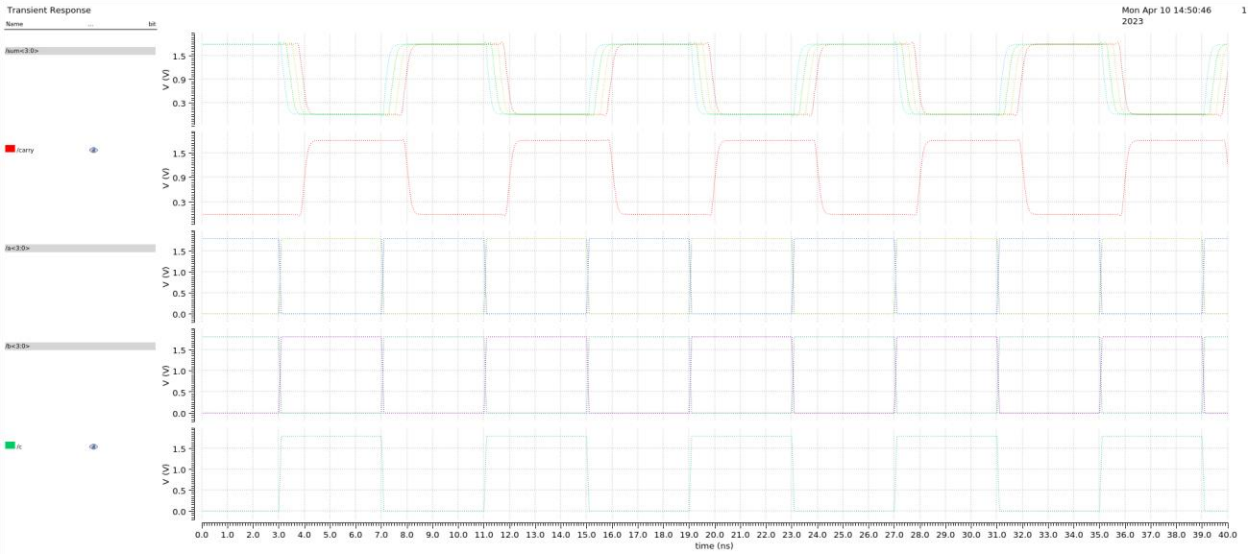
$$C_{in,xor} = \frac{g_{xor} C_{out}}{\hat{f}} = \frac{\frac{8}{3} \cdot 30fF}{2.763} = 28.954fF$$

$$\frac{28.954fF}{5.037\ fF/\mu m} = 5.748\mu m \Rightarrow \boxed{\begin{array}{l} W_p = 4.311\ \mu m \\ W_n = 1.437\ \mu m \end{array}}$$ XOR

The design with the updated sizing was tested using the same cases as Lab 5:






Transient Response
Mon Apr 10 14:50:46 2023
1
Name
bit
Sum<3:0>
fcarry
fa<3:0>
fb<3:0>
fc
V (V)
time (ns)

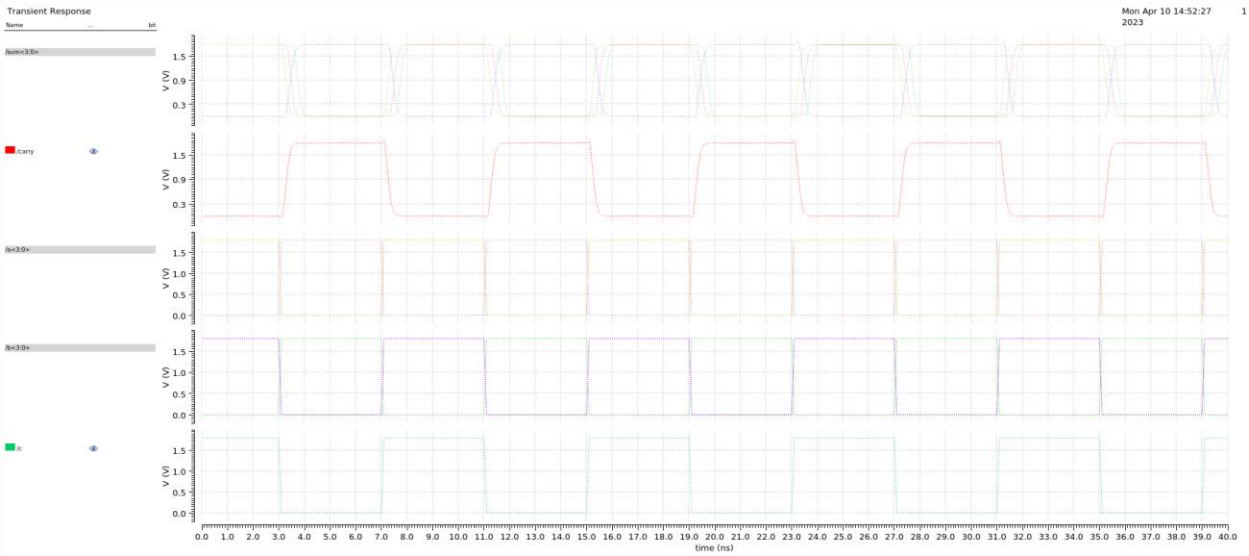

Transient Response
Mon Apr 10 14:52:27 2023
1
Name
bit
Sum<3:0>
fcarry
fa<3:0>
fb<3:0>
fc
V (V)
time (ns)

Table 1: Non-Optimized Results

Input Case	Power	Sum Delay	Carry Delay
A=0000 B=1111 C=1	204.6uW	S3=1.102nS S2=850ps S1=598.5ps S0=361ps	1.202ns
A=1010 B=0101 C=0	207.1uW	S3=1.157ns S2=907.5ps S1=658.2ps S0=416.7ps	1.176ns
A=1010 B=0101 C=1	204.6uW	S3=1.102ns S2=850.7ps S1=599.1ps S0=358.3ps	1.202ns
A=1100 B=1000 C=0	209.9uW	S3=850.1ps S2=636.5ps S1=602.6ps S0=392.8ps	463.3ps

Table 2: Optimized Results

Input Case	Power	Sum Delay	Carry Delay
A=0000 B=1111 C=1	394.7uW	S3=899.4ps S2=659.1ps S1=418.6ps S0=162.3ps	956.5ps
A=1010 B=0101 C=0	392.8uW	S3=918.2ps S2=666.2ps S1=414.5ps S0=150.9ps	1ns
A=1010 B=0101 C=1	394.5uW	S3=899.4ps S2=659.1ps S1=418.6ps S0=162.3ps	956.5ps
A=1100 B=1000 C=0	430.6uW	S3=692.8ps S2=400.3ps S1=436.0ps S0=277.3ps	254.5ps

Overall, the delays improved on average by **18%** while the power consumption increased by **95%**.

Table 3: Area Comparison

Design	**Approx. Area (um^2)**
Optimized	59.424
Non-Optimized	17.12