Lab 4: Design & Simulation of 1-bit Adder

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Post layout verification was first done for the inverter, NAND2, and XOR cells. Changes were made to all gates to optimize the delay.

Inverter:

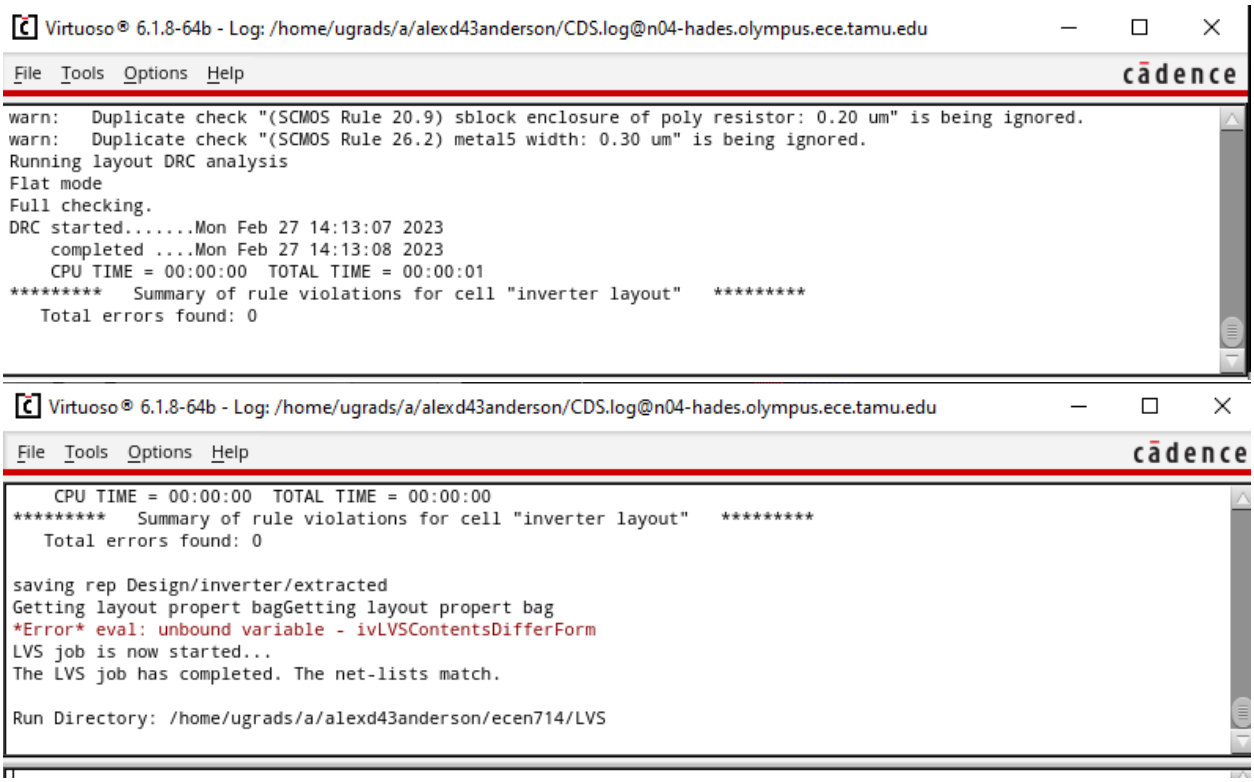
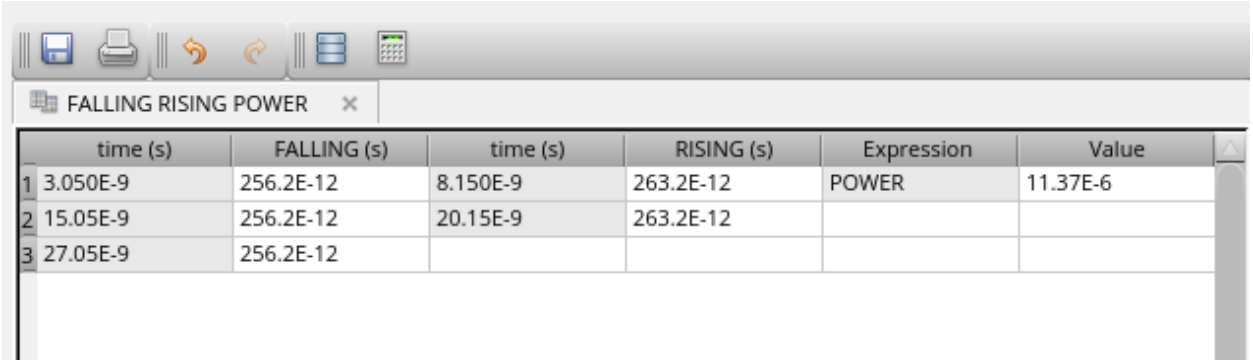


Figure 1: Inverter DRC and LVS



	time (s)	FALLING (s)	time (s)	RISING (s)	Expression	Value
1	3.050E-9	256.2E-12	8.150E-9	263.2E-12	POWER	11.37E-6
2	15.05E-9	256.2E-12	20.15E-9	263.2E-12		
3	27.05E-9	256.2E-12				

Figure 2: Inverter Transient Data

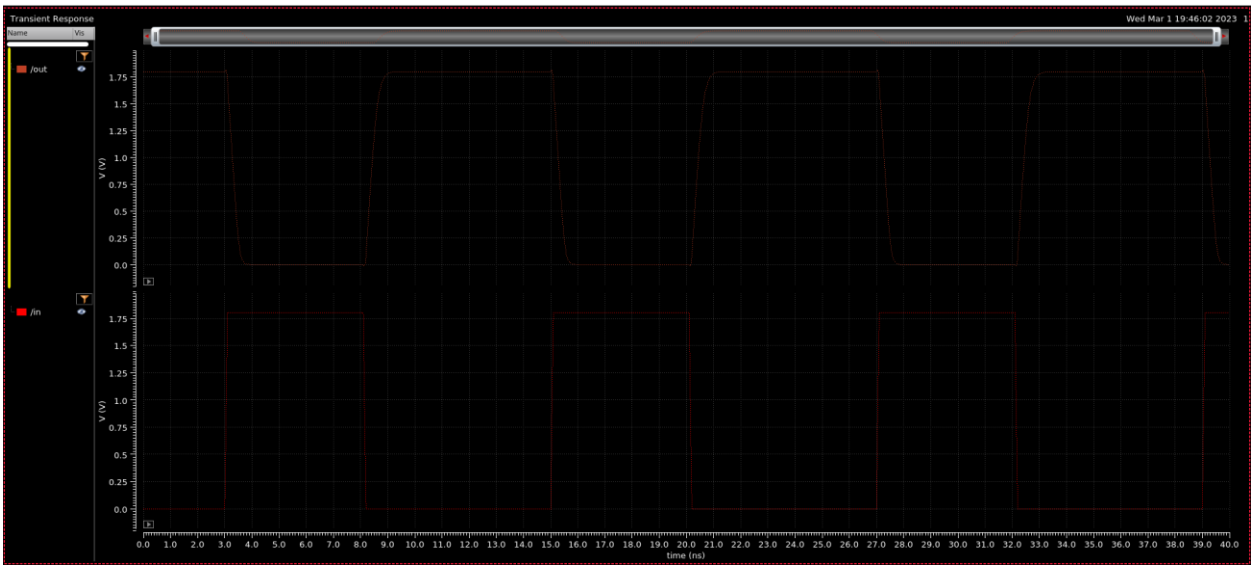


Figure 3: Inverter Waveform

NAND2:

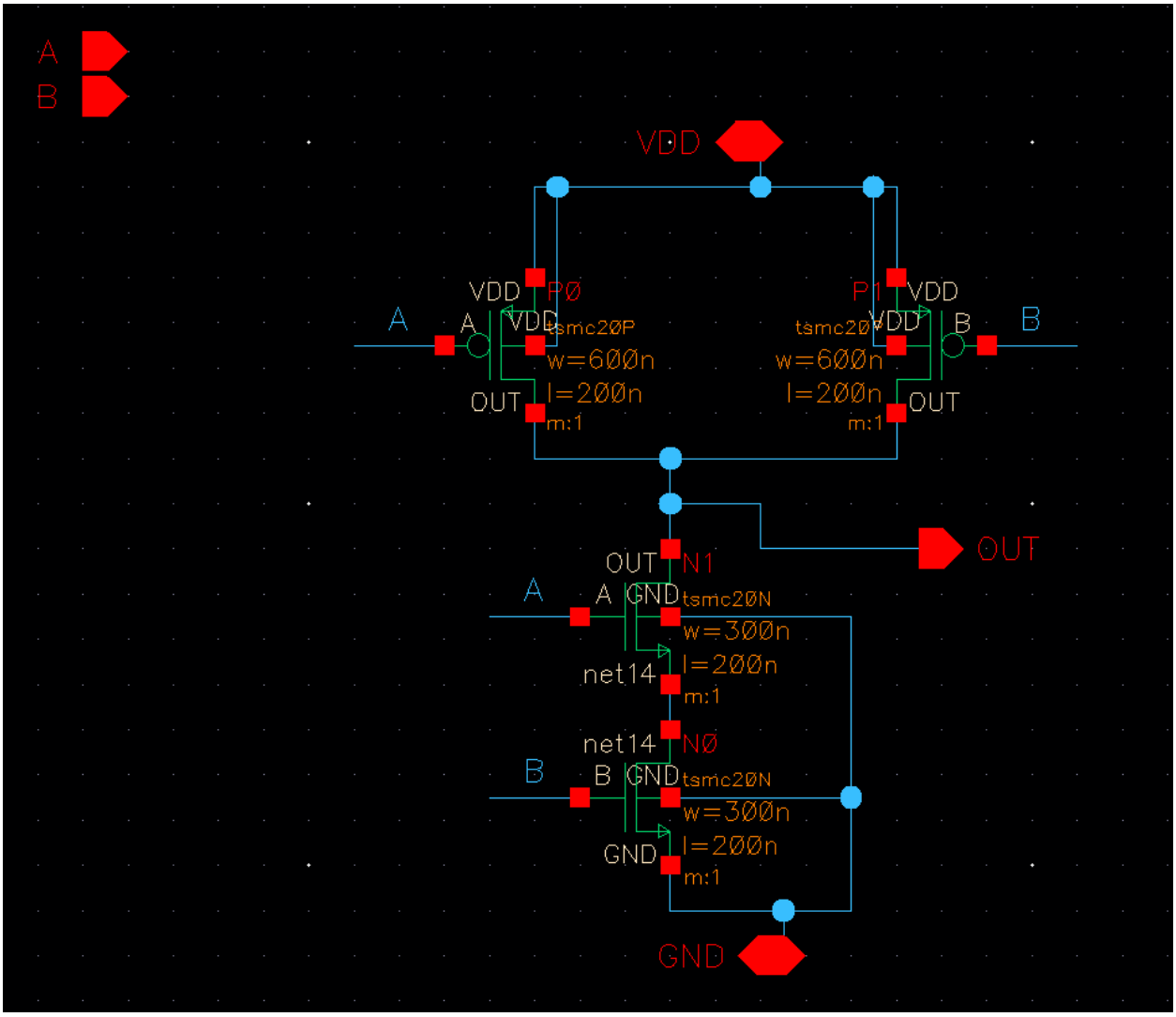


Figure 4: NAND2 Schematic

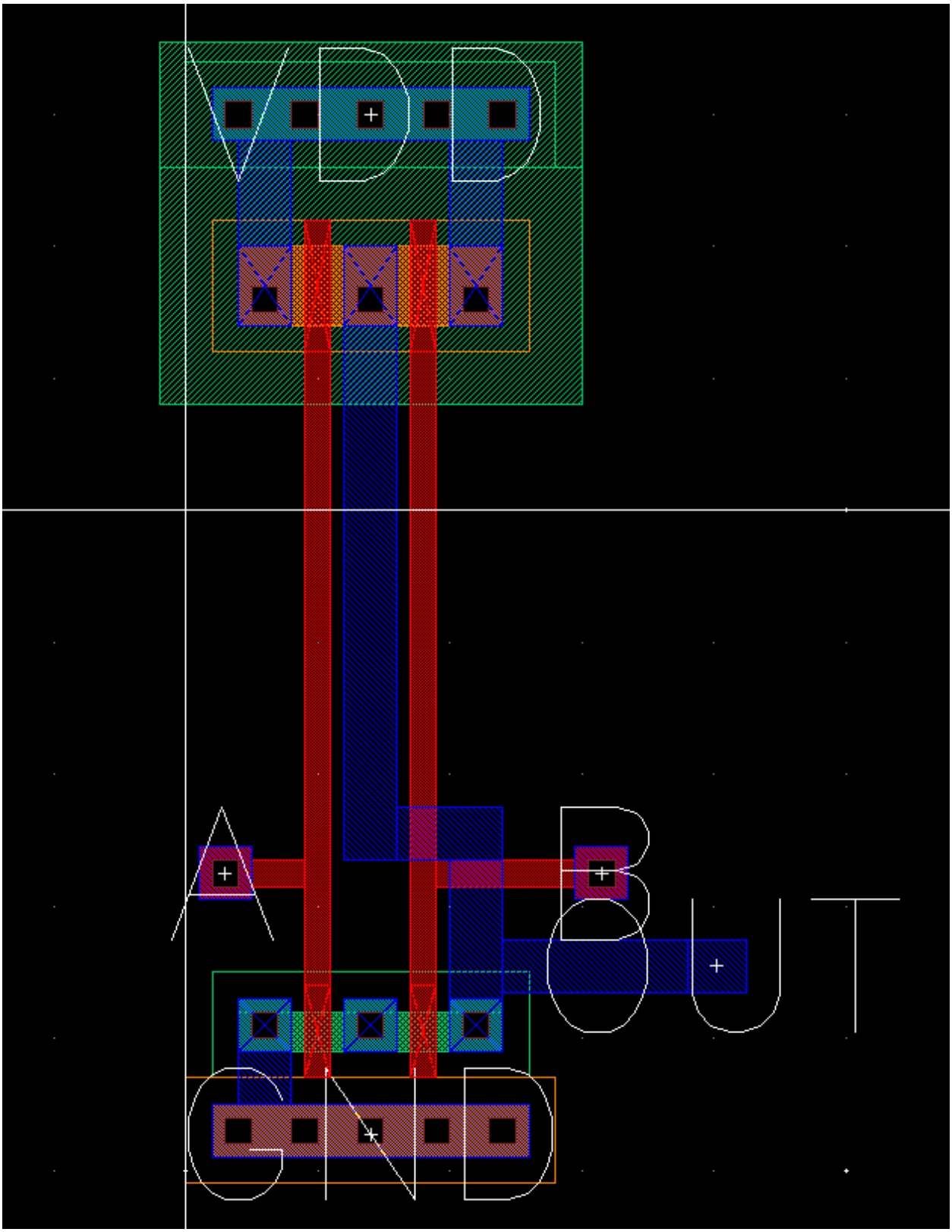


Figure 5: NAND2 Layout

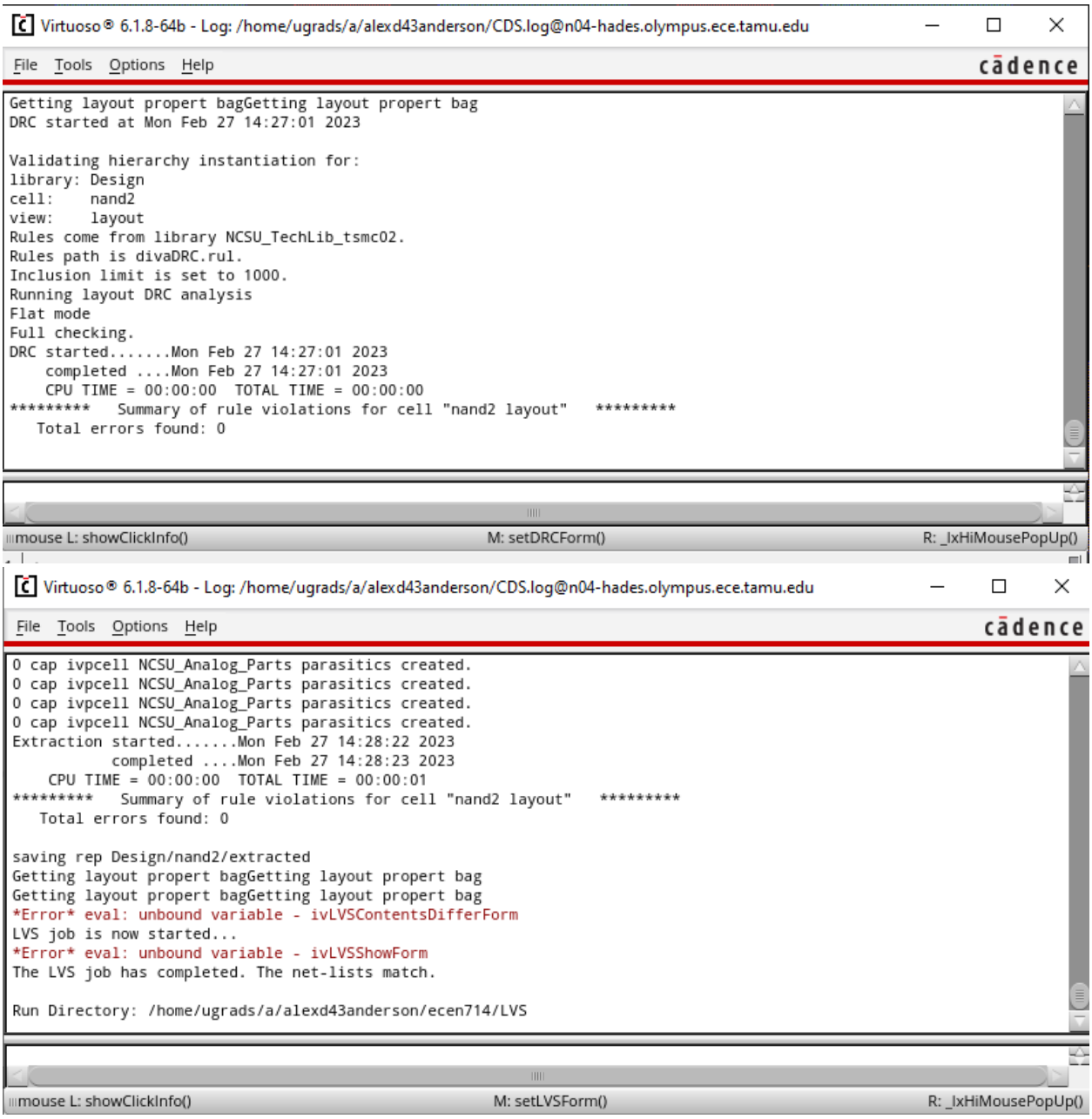


Figure 6: NAND2 DRC and LVS

RISING FALLING POWER

	time (s)	RISING (s)	time (s)	FALLING (s)	Expression	Value
1	8.150E-9	374.8E-12	3.050E-9	350.6E-12	POWER	11.59E-6
2	20.15E-9	375.0E-12	15.05E-9	347.4E-12		
3			27.05E-9	347.4E-12		

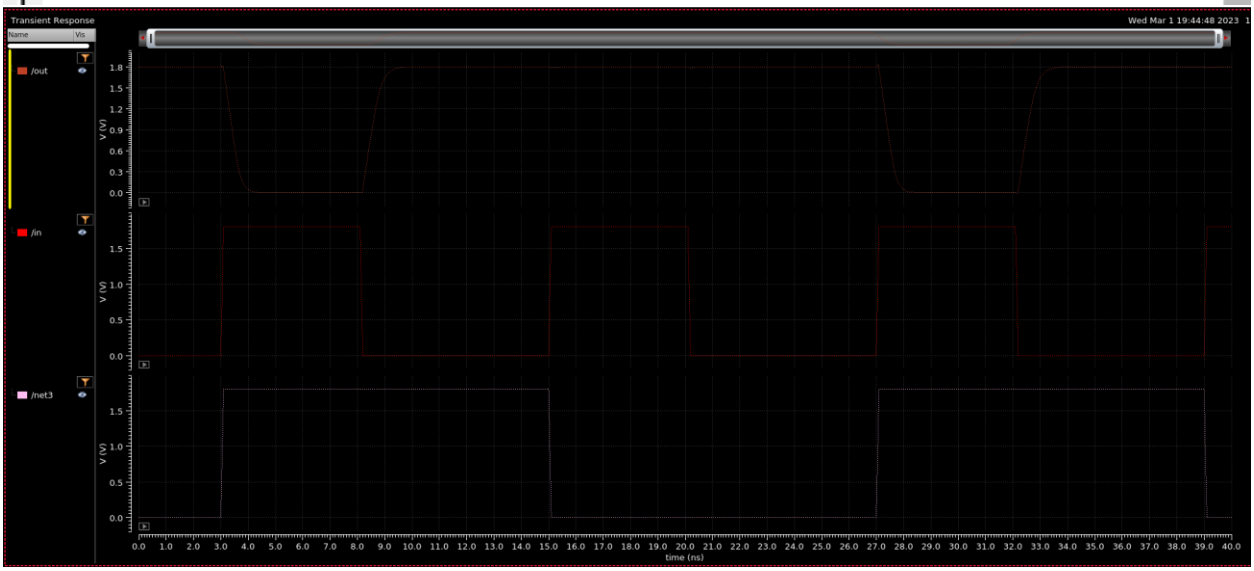


Figure 7: NAND2 Transient Data and Waveform

XOR2:

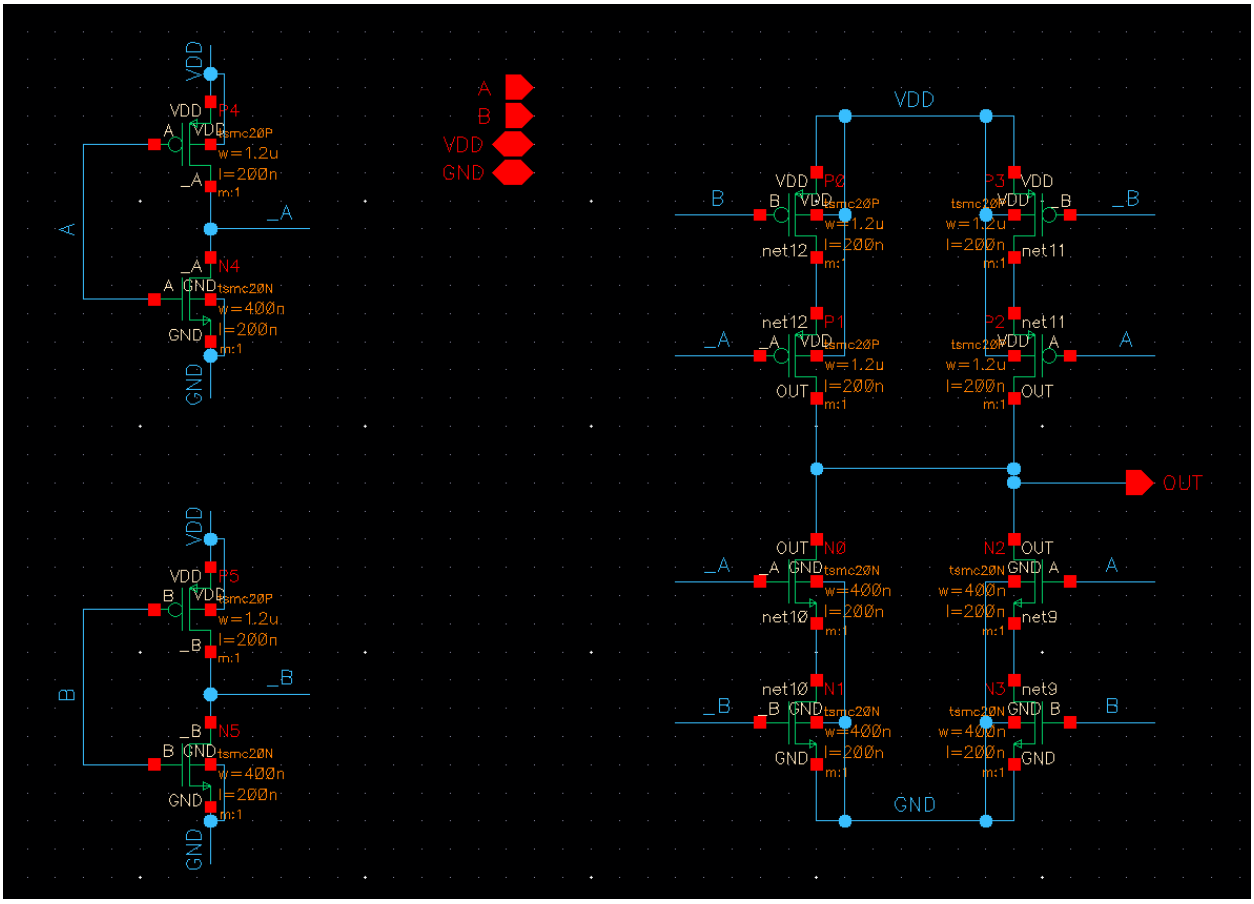


Figure 8: XOR2 Schematic

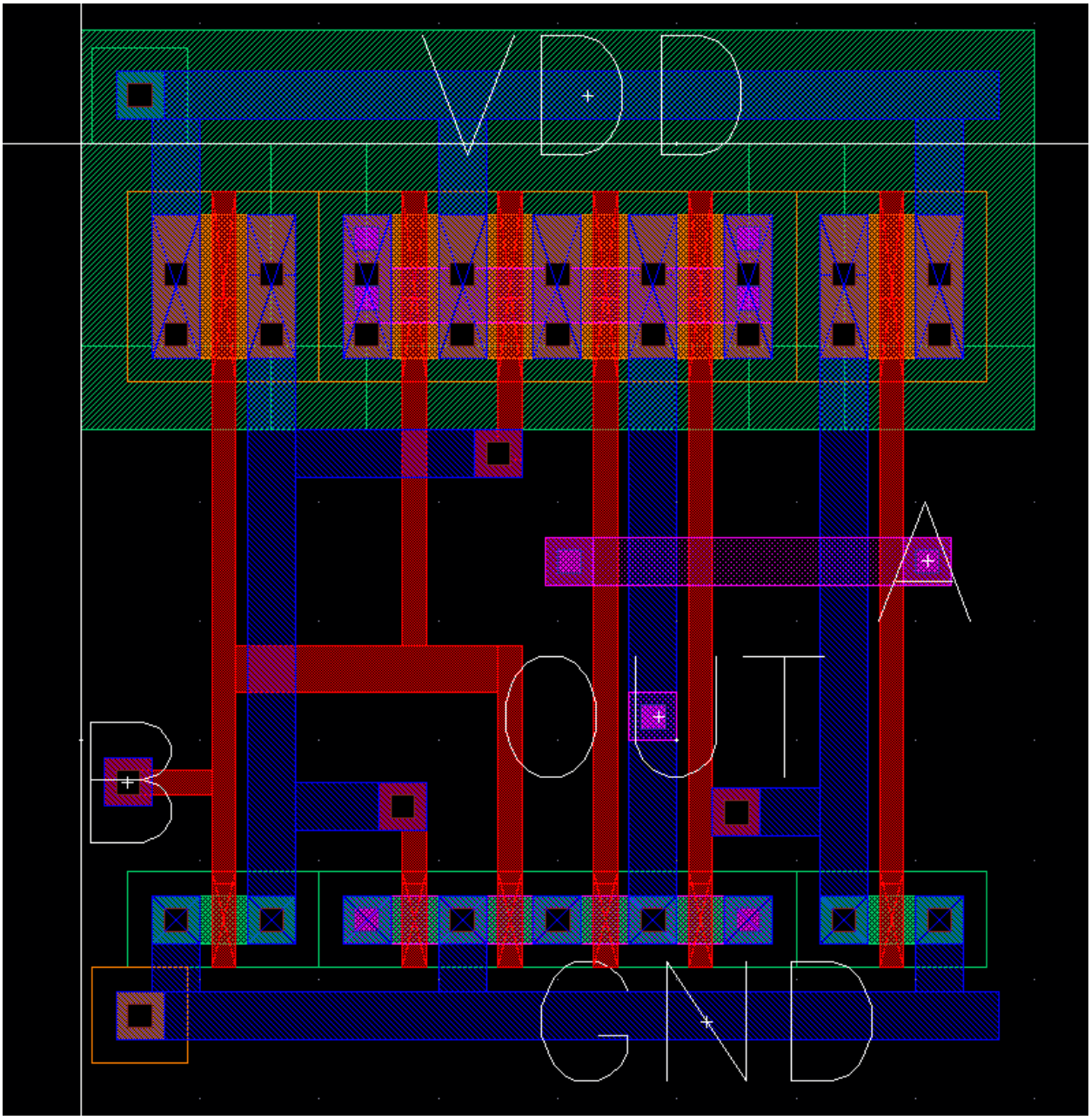


Figure 9: XOR2 Layout

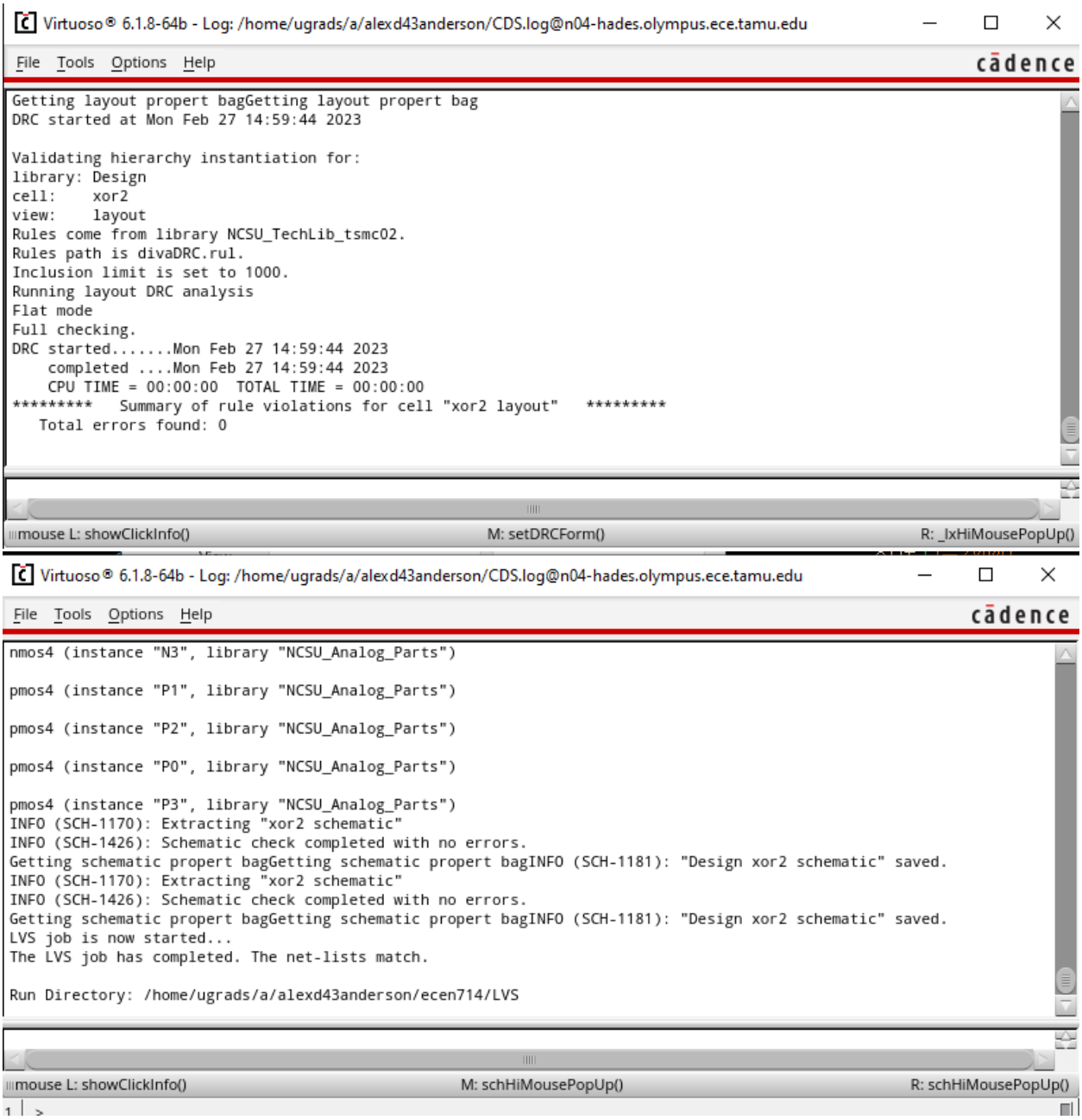


Figure 10: XOR2 DRC and LVS

FALLING RISING POWER

	time (s)	FALLING (s)	time (s)	RISING (s)	Expression	Value
1	3.050E-9	307.6E-12	8.150E-9	361.5E-12	POWER	12.61E-6
2	15.05E-9	289.6E-12	20.15E-9	363.3E-12		
3	27.05E-9	289.6E-12				

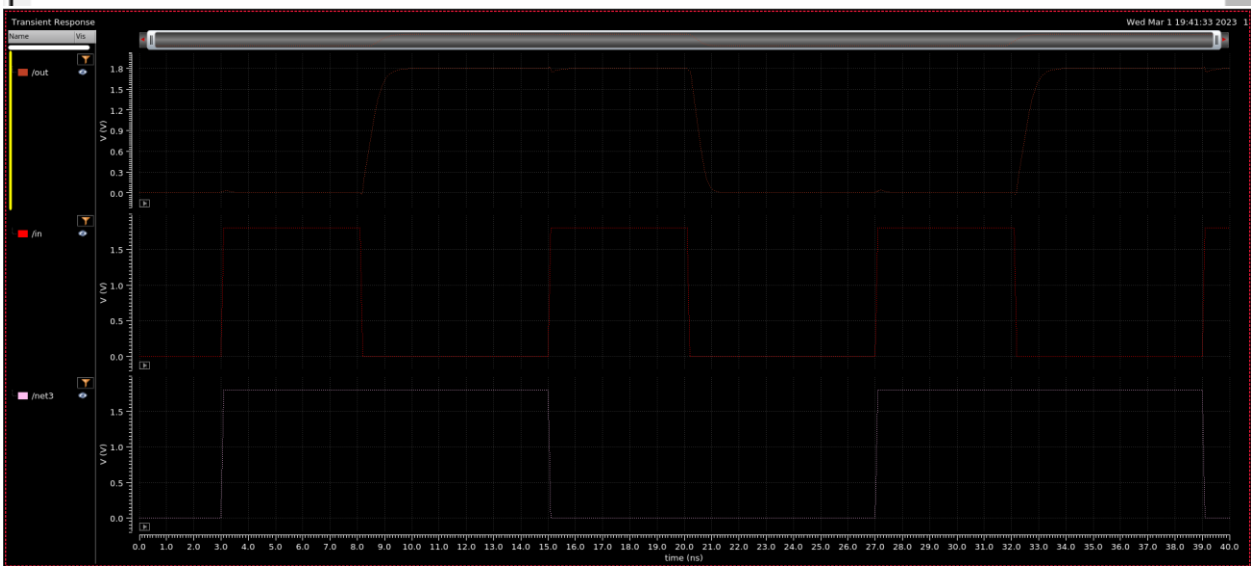


Figure 11: XOR2 Data and Waveform

Now, the 1-bit adder was assembled and tested using all the above blocks. **Due to a problem with Cadence, hierarchical design could not be used, so the individual transistors had to be copied into the top cell view (see my post on Piazza for more info).**

1-bit adder:

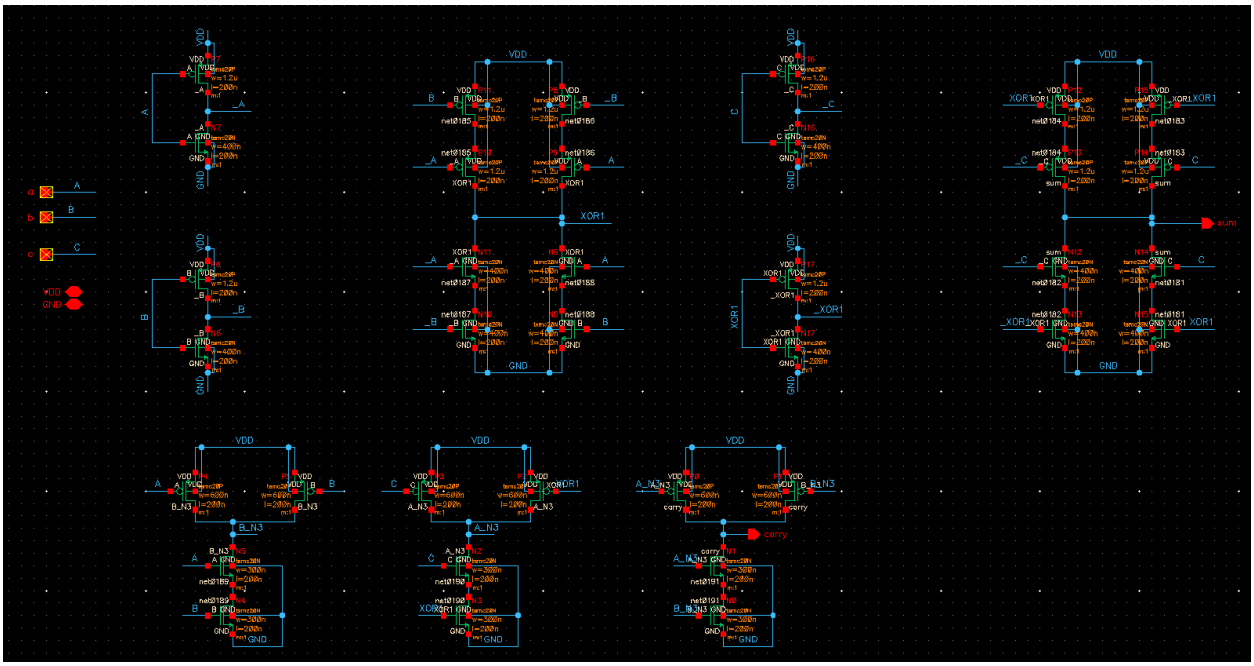


Figure 12: 1-bit Adder Schematic

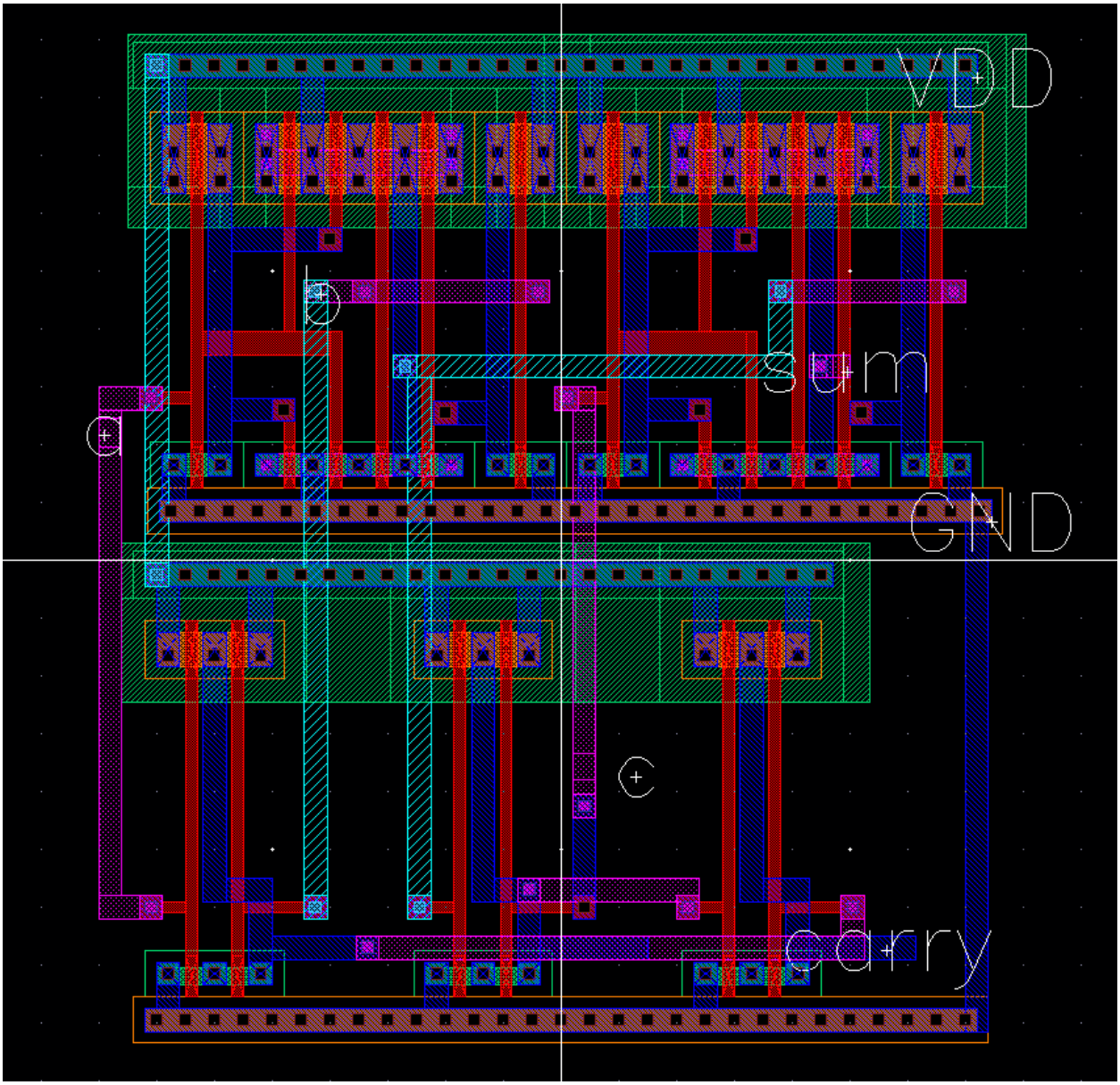


Figure 13: 1-bit Adder Layout

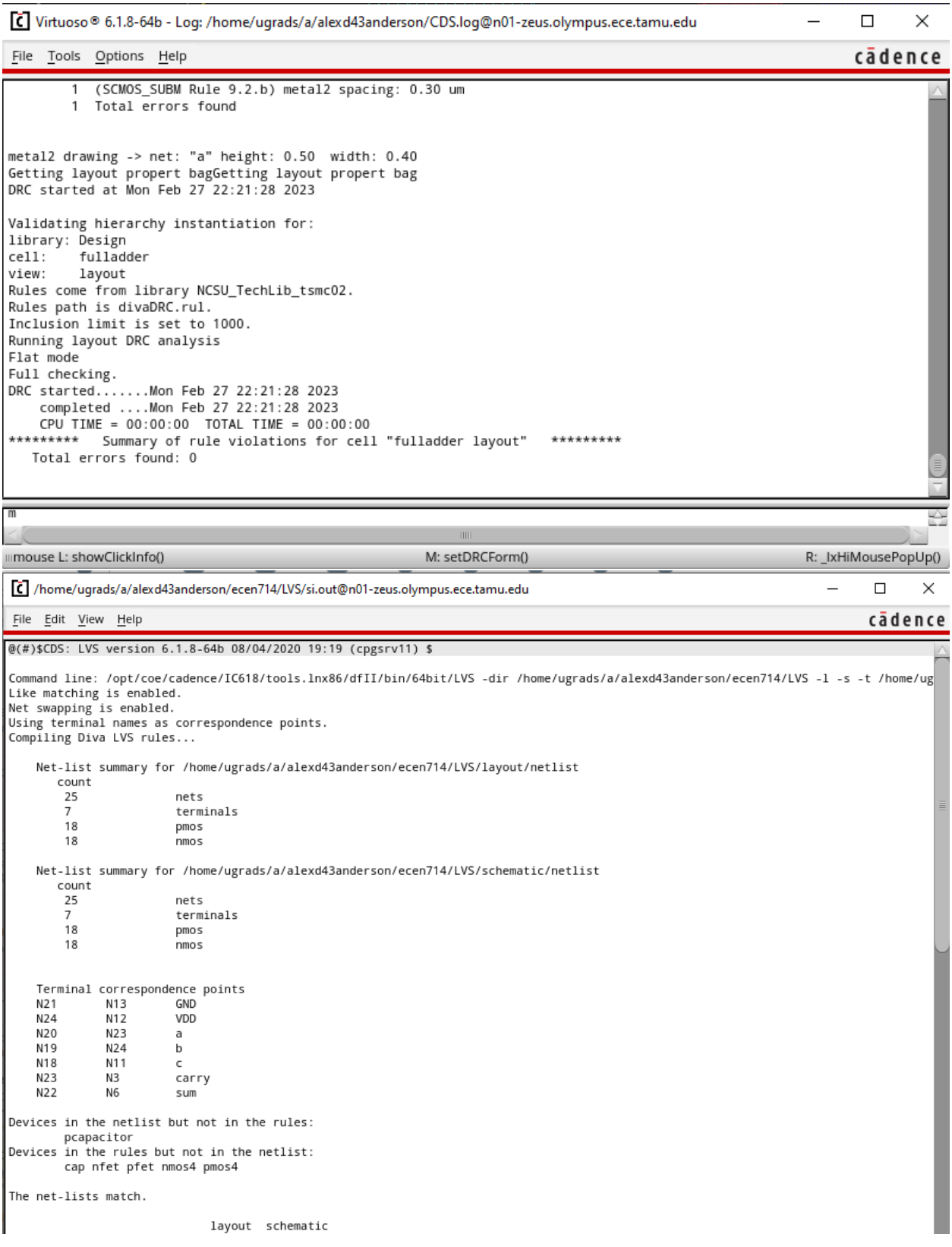


Figure 14: 1-bit Adder DRC and LVS

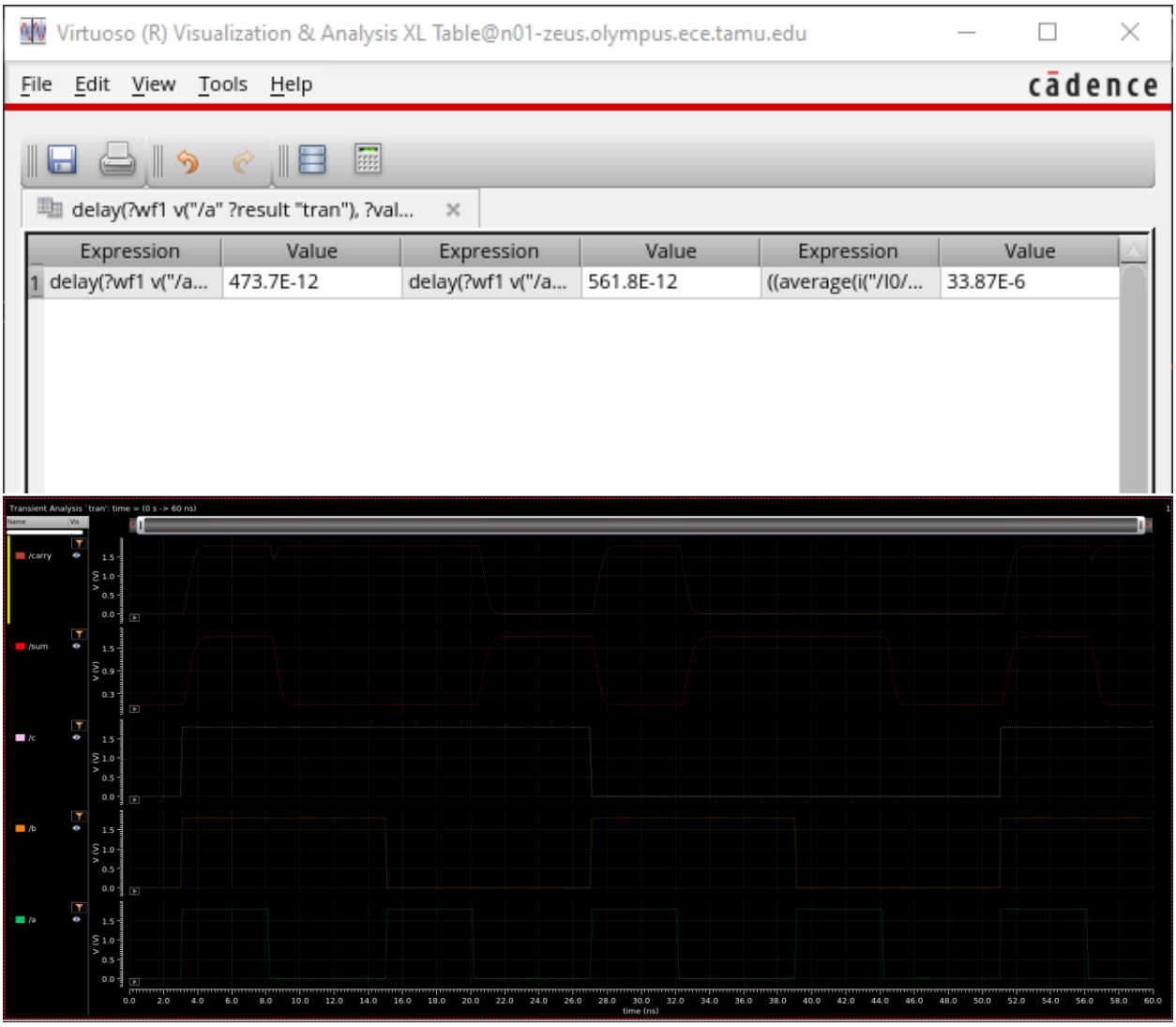


Figure 15: 1-bit Adder Data and Waveform

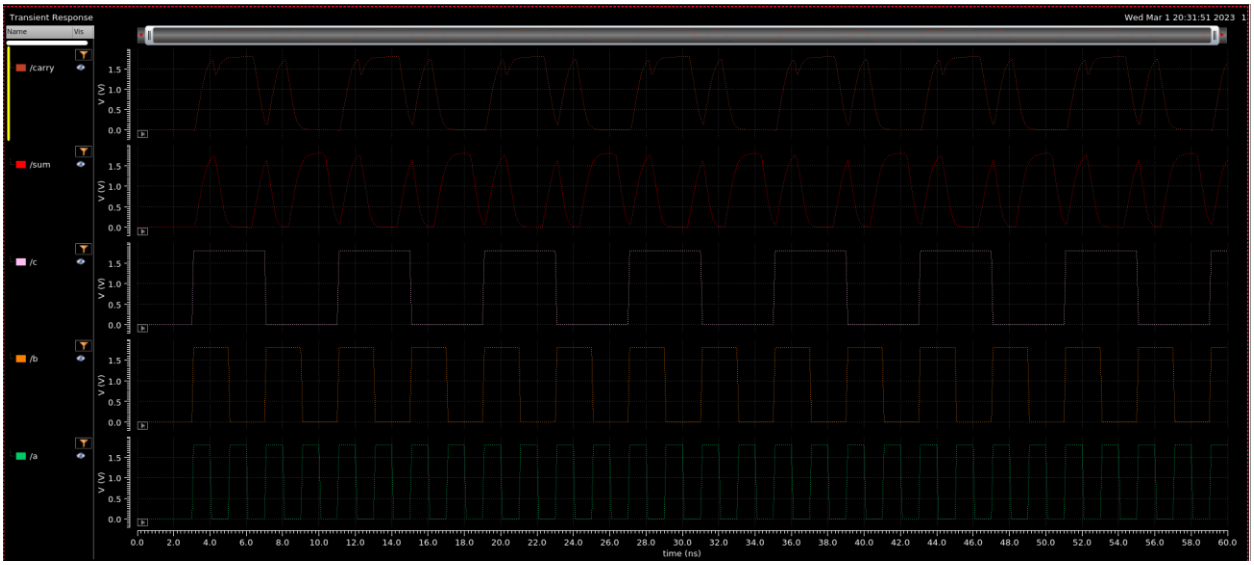


Figure 16: 1-bit Adder Max Frequency

The minimum period for the 1-bit adder was found to be 1ns, thus the max frequency is **0.5 GHz.**