Lab 9: Two-Stage Miller Operational Amplifier

ECEN 704-601
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Description

In this lab, a fundamental analog building block, the opamp, was realized using a two-stage Miller amplifier. The full layout was completed including good matching and design practices such as dummy elements, common centroid, and guard rings. The design was tested post-layout and Monte Carlo simulations were performed to analyze the effect of process variation and mismatch on key circuit parameters.

Design

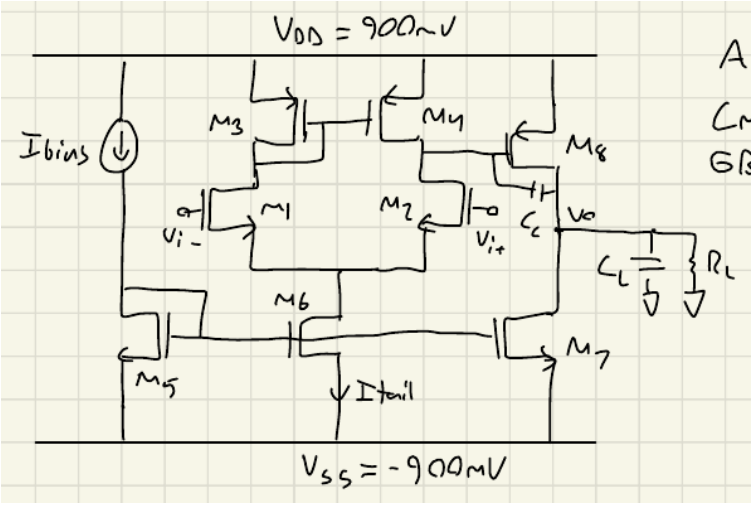

Figure 1: Two-Stage Miller Opamp Schematic

To begin, supply voltages of +/- 900mV were used to allow for sufficient headroom in biasing the transistors. The tail current was taken to be 50uA in order to meet the desired power consumption specification. The bias current was set to be slightly larger, 55uA, in order to allow for identical aspect ratios in the tail current mirror while accounting for lambda effects.

Next, the transconductance of M1 and M2 can be solved to meet the necessary gain specifications. The aspect ratio was taken to be 10, allowing the transconductance to be found as

$$g_{m1,2}=\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2}\frac{I_{tail}}{2}}=316\,\mu A/V$$

Assuming a 1:1 mirroring ratio in the output branch, a value for g_{m8} can be found from the gain specification, assuming a large load resistance of 100kΩ:

$$A_{v0}=g_{m1,2}g_{m8}(r_{o2}\|r_{o4})(r_{o7}\|r_{o8}\|R_L)=50\,dB$$

$$g_{m8}\geq 507\,\mu A/V\Rightarrow\left(\frac{W}{L}\right)_8\geq 12.87=20$$

The aspect ratios for load devices M3 and M4 were determined using the specification for CMRR and the expression for common mode gain:

$$|A_{CM}|\simeq\frac{1}{2r_{o6}g_{m3}}$$

$$CMRR\geq 60\,dB=20\log_{10}\left(\left|\frac{A_{CM}}{A_{DM}}\right|\right)\Rightarrow A_{CM}\leq 3.165\Rightarrow g_{m3}\geq 2\,\mu A/V\Rightarrow\left(\frac{W}{L}\right)_{3,4}=10$$

To match branch currents, the aspect ratios of M5, M6, and M7 were taken to be equal:

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_7 = 10$$

Finally, the Miller compensation capacitor was found according to the gain bandwidth specification:

$$GBW = 2\,MHz = \frac{g_{m1,2}}{C_C} \Rightarrow C_C = 158\,pF$$

The phase margin was verified at this capacitor value to be above the desired 45 degrees

$$PM \simeq 90 - \tan^{-1}\left(\frac{GBW\,C_L}{g_{m8}}\right) - \tan^{-1}\left(\frac{GBW\,C_C}{g_{m8}}\right) = 65$$

From here, the circuit was simulated and adjusted accordingly to achieve the desired specifications.

Results

The schematic for the opamp including dummy elements in shown below in Figure 2.

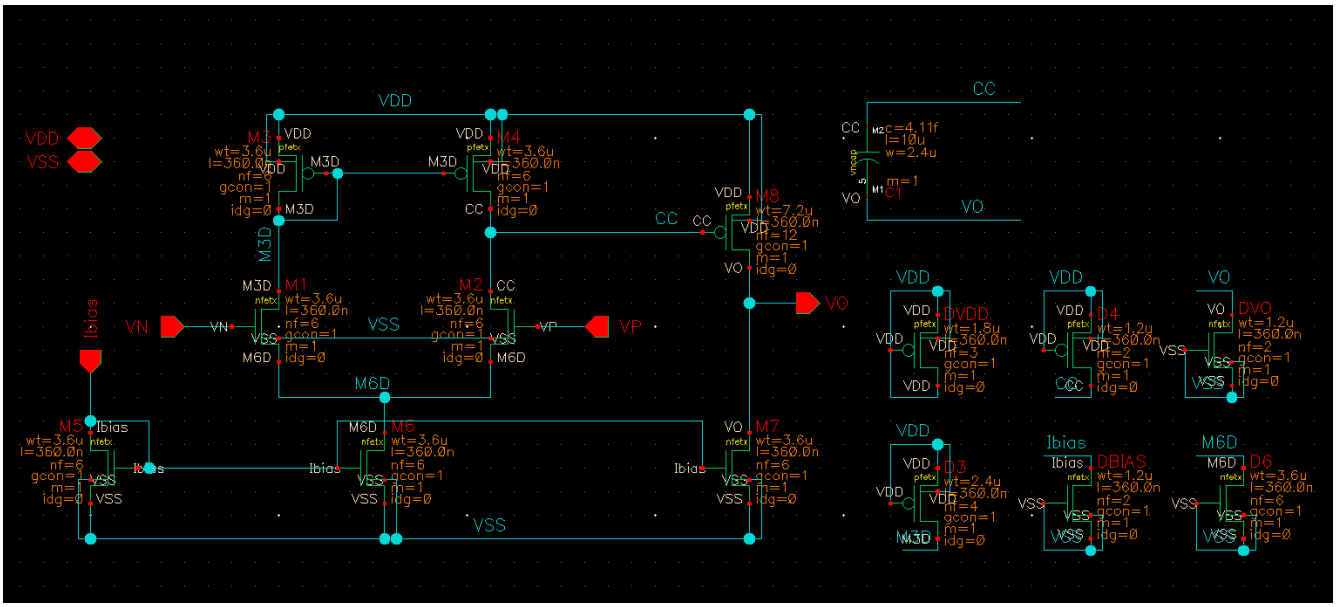

Figure 2: Opamp Schematic

Next, a test bench was created to verify the performance of the circuit.

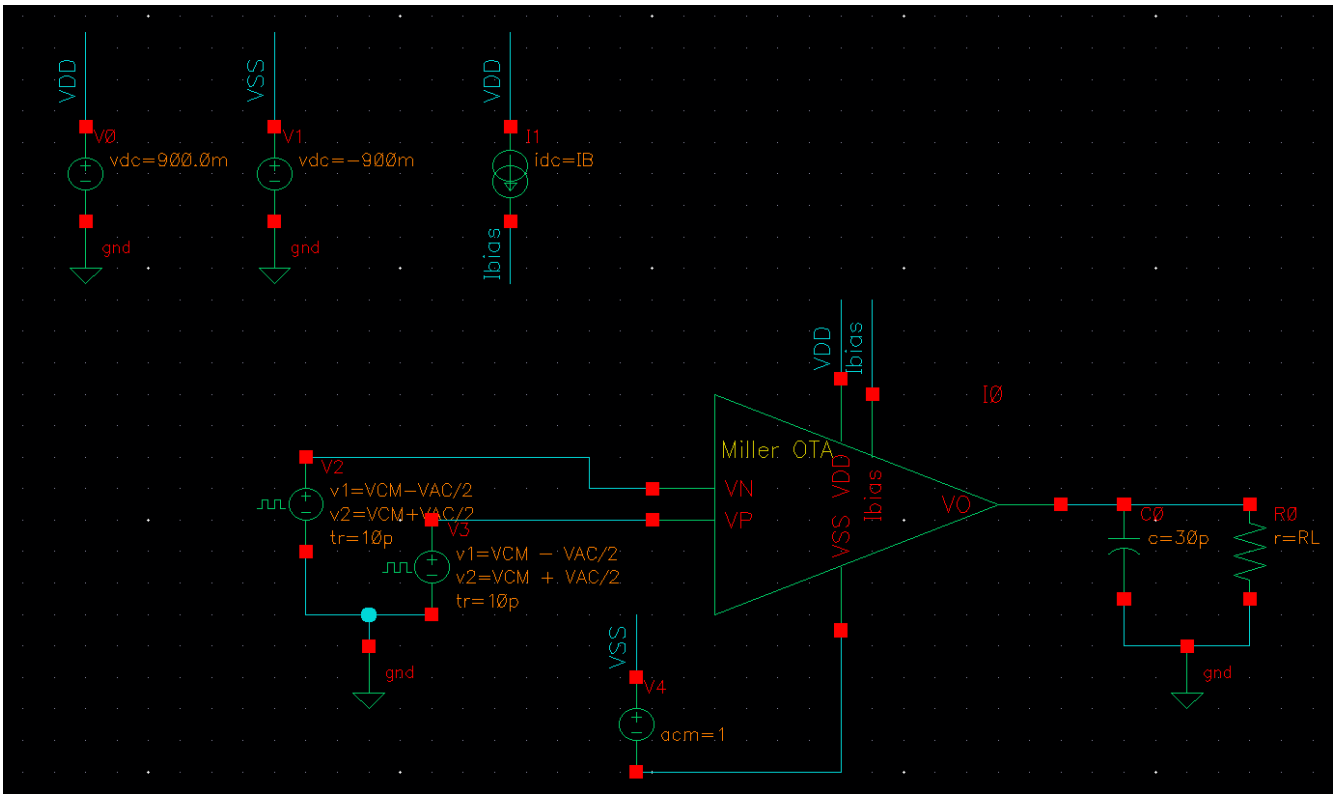

Figure 3: Opamp Test Bench

From here, simulations were performed for the ac response, transient response, CMRR, power consumption, and power supply rejection (PSRR).

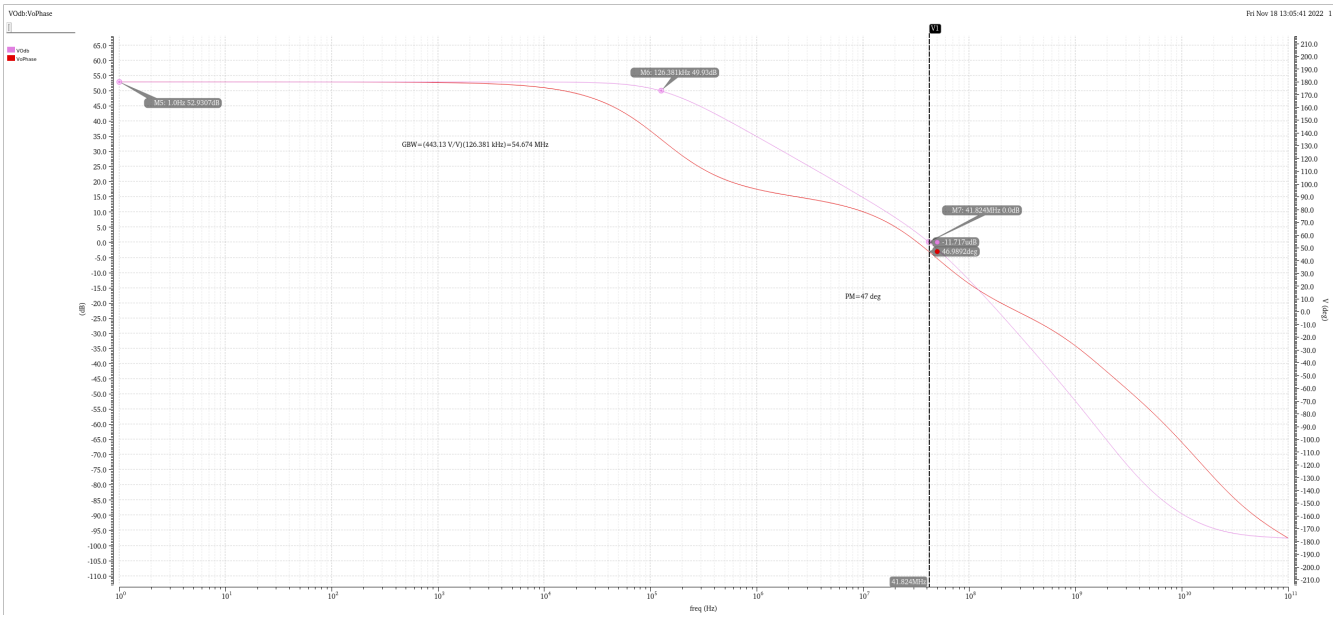

Figure 4: AC Simulation

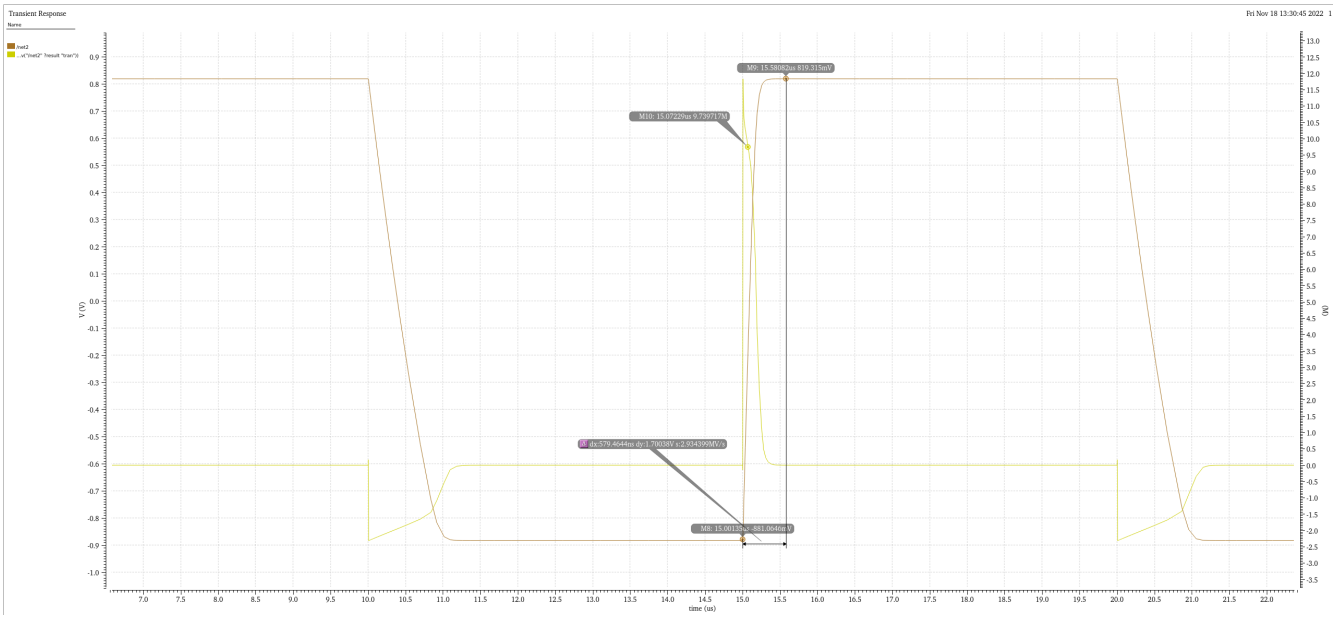

Figure 5: Transient Simulation

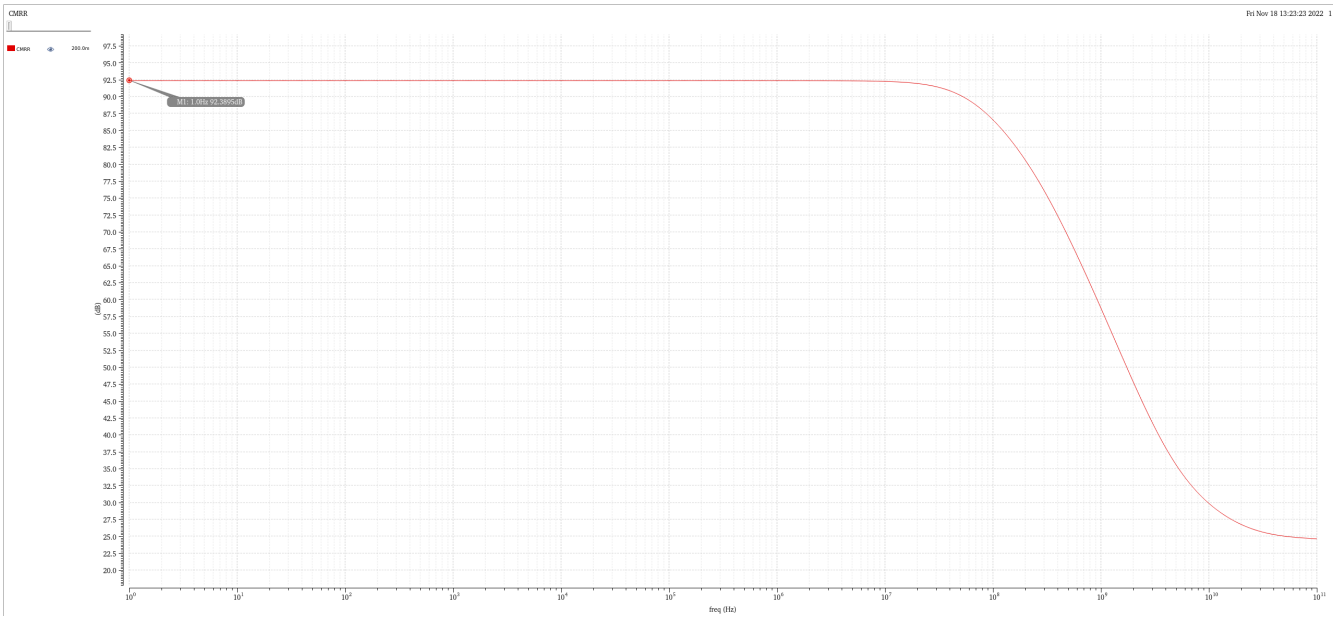

Figure 6: CMRR Simulation

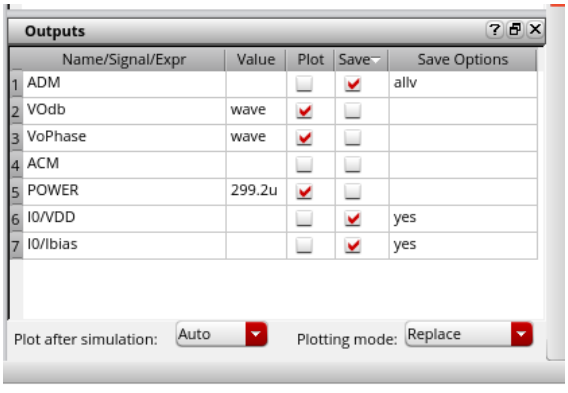

Figure 7: Power Consumption

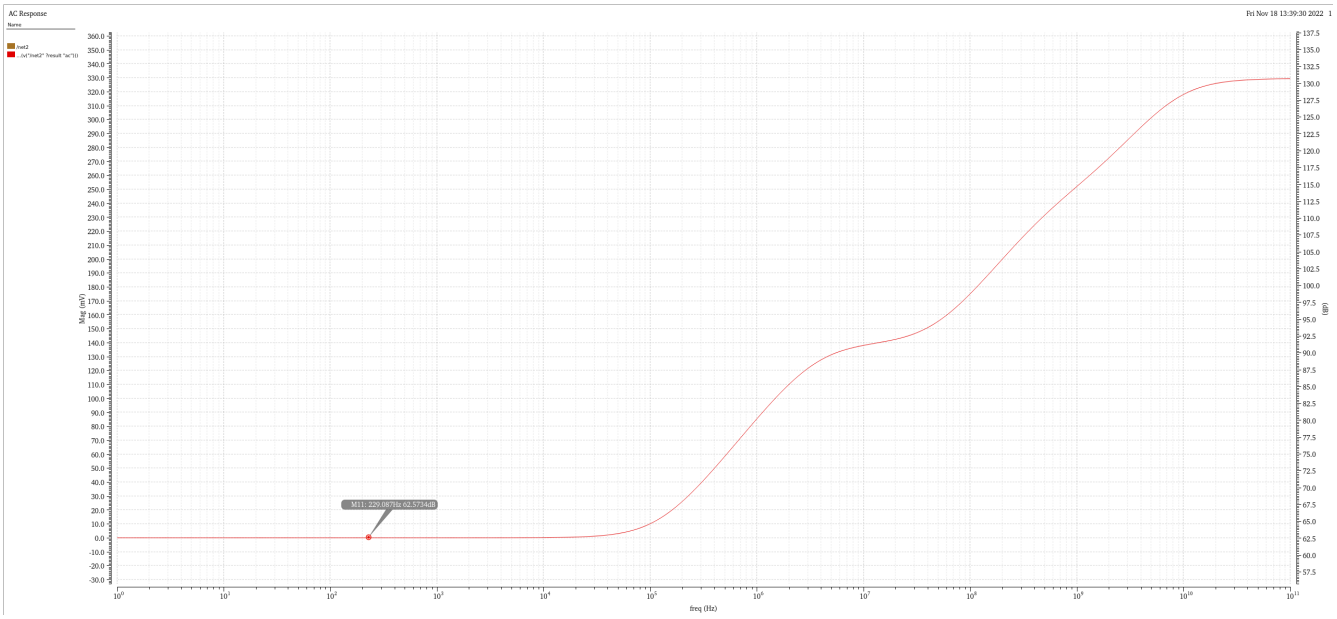

Figure 8: VDD Power Supply Rejection (PSRR+)

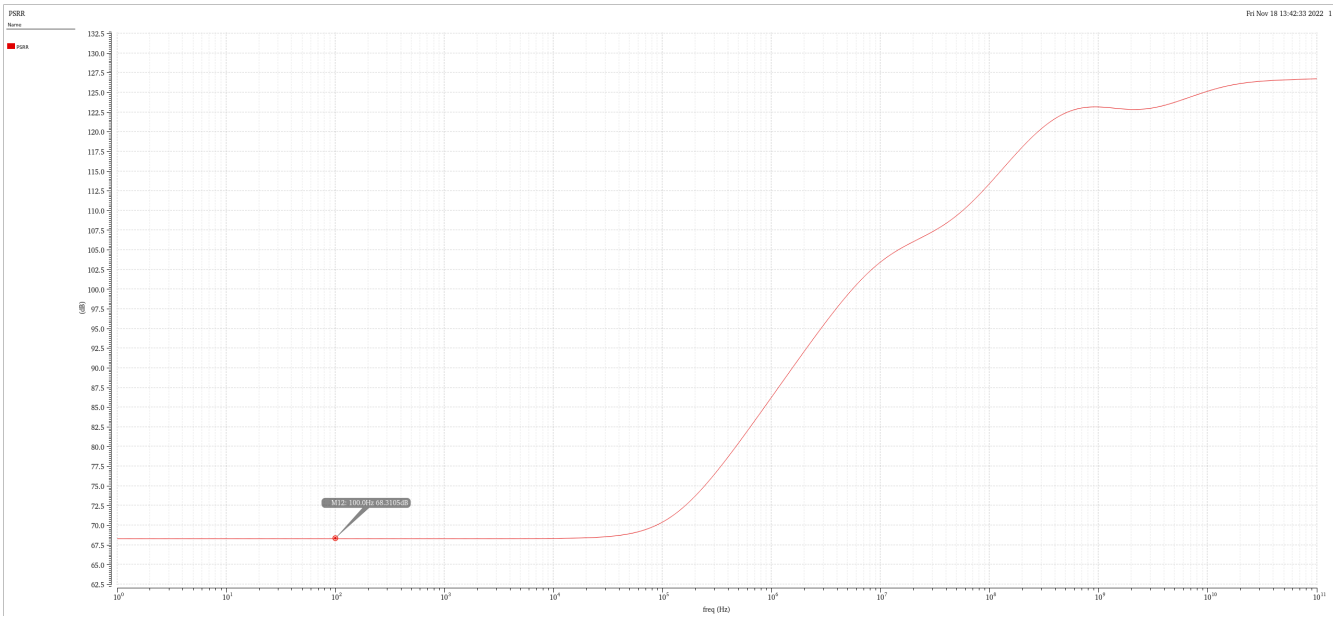

Figure 9: VSS Power Supply Rejection (PSRR-)

Next, the layout of the circuit was completed, including the compensation capacitor. The use of common centroid matching was incorporated into the design, as well as guard rings to isolate the PMOS devices and reduce the likelihood of latch-up. Once complete, the layout was successfully verified using LVS and DRC.

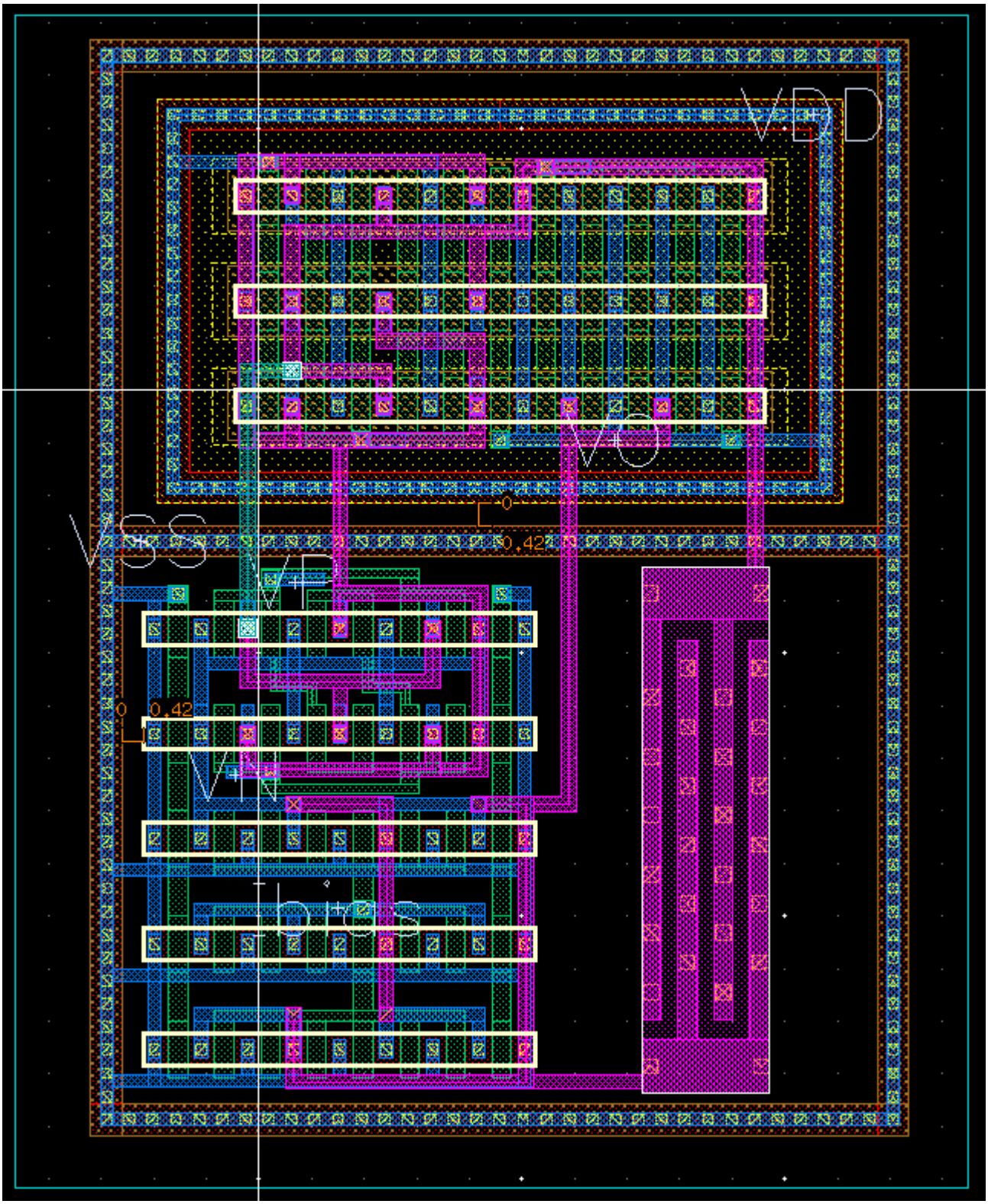

Figure 10: Opamp Layout

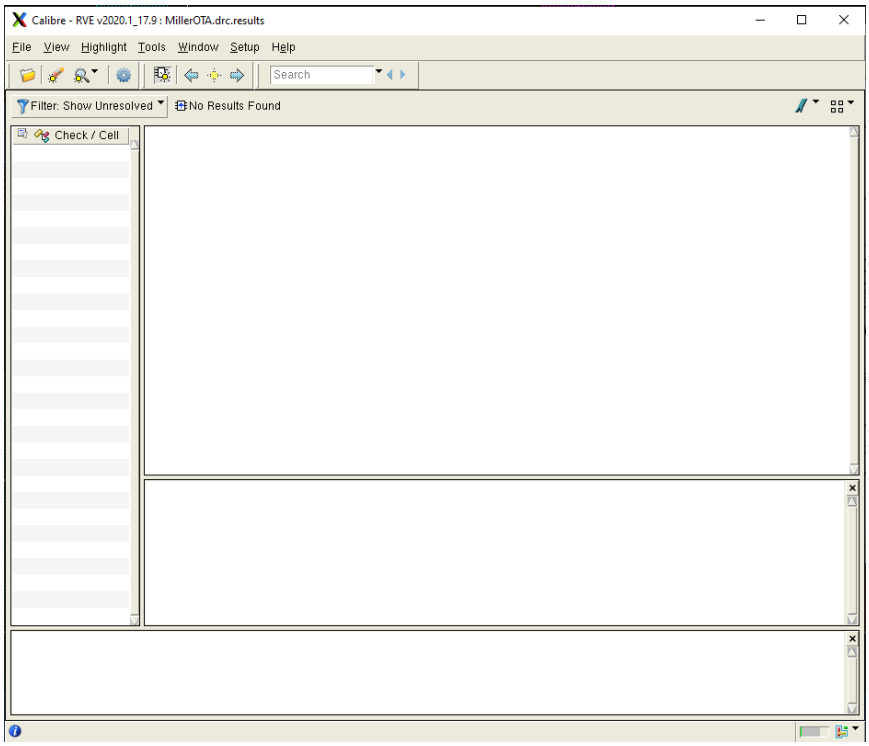

Figure 11: DRC

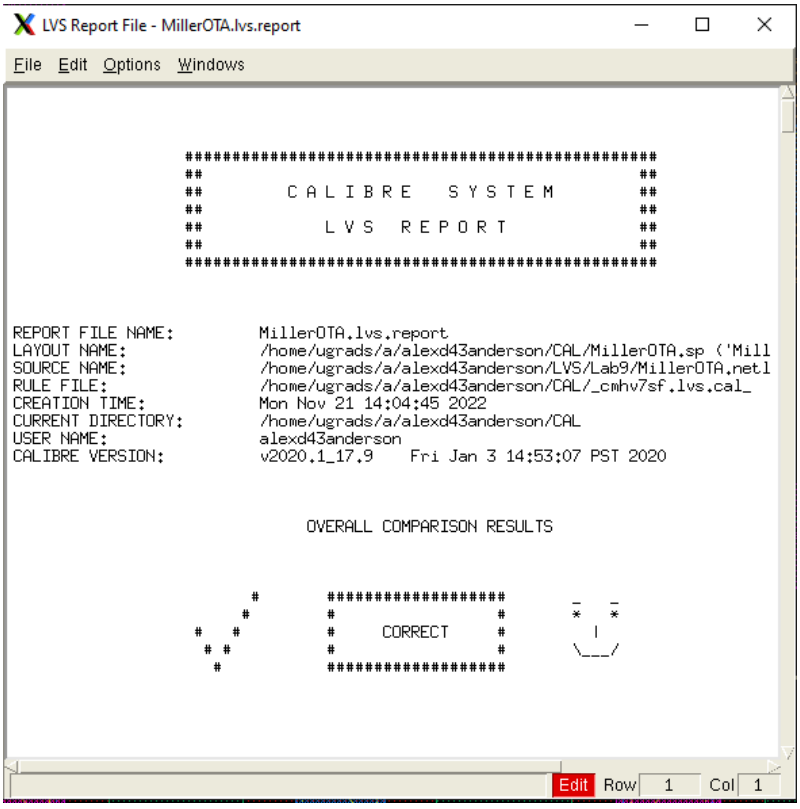

Figure 12: LVS

Next, the layout parasitics were extracted and used to complete post-layout simulations of all the previously acquired parameters.

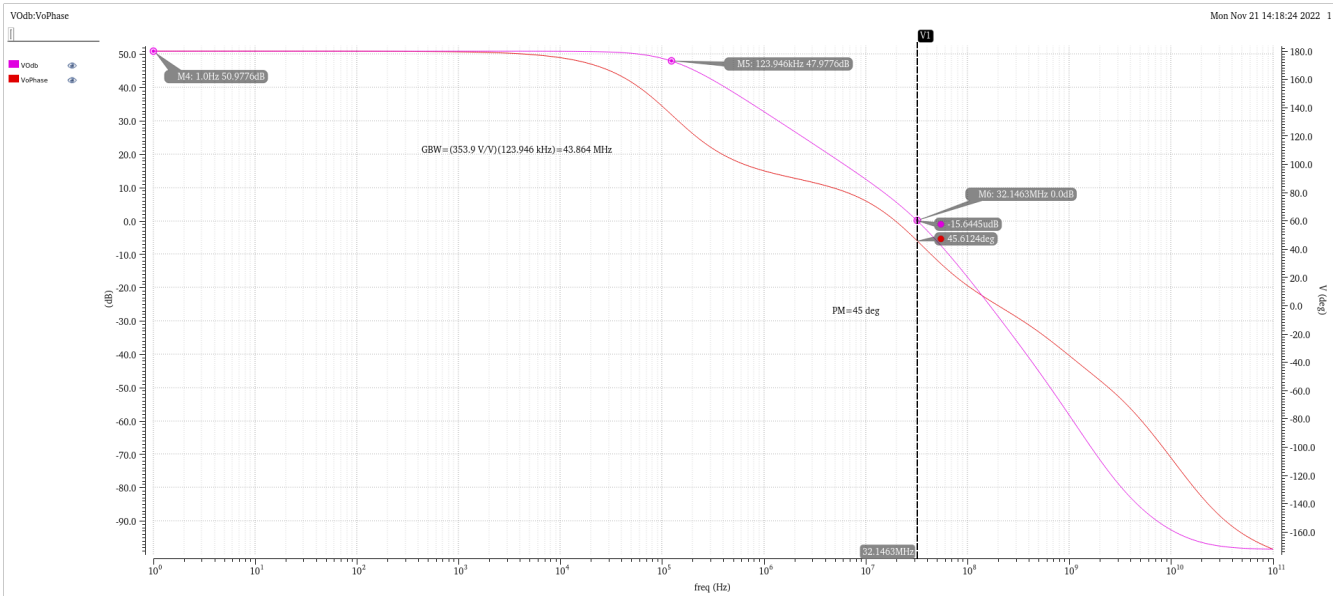

Figure 13: AC Post Simulation

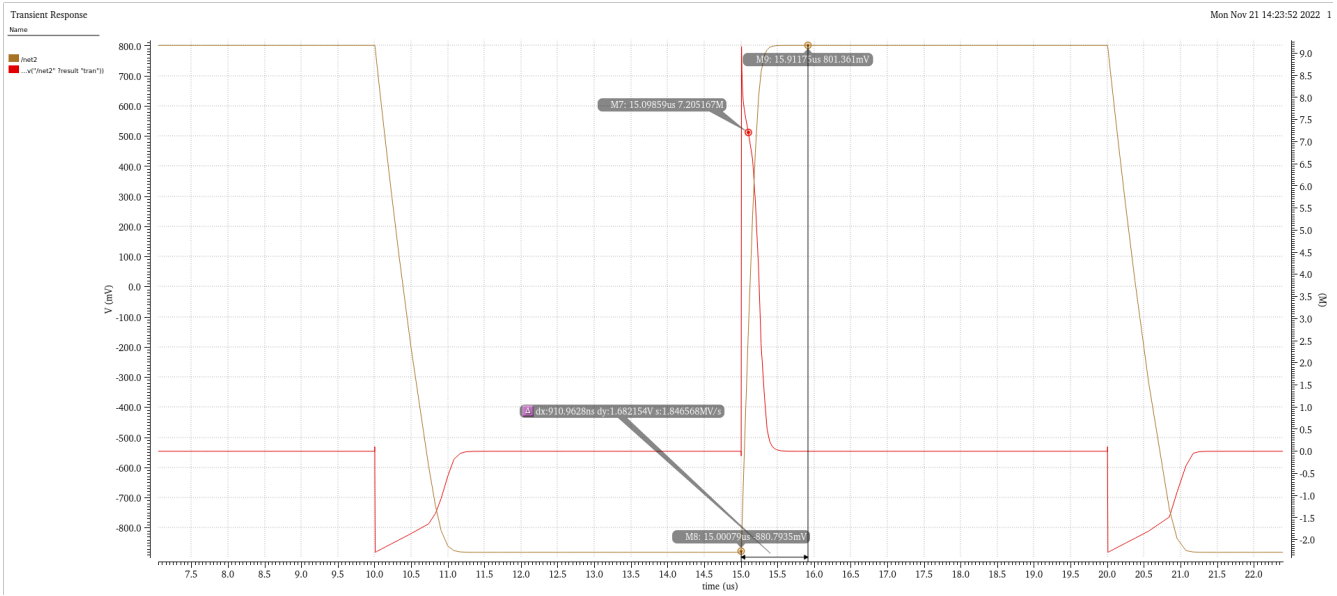

Figure 14: Transient Post Simulation

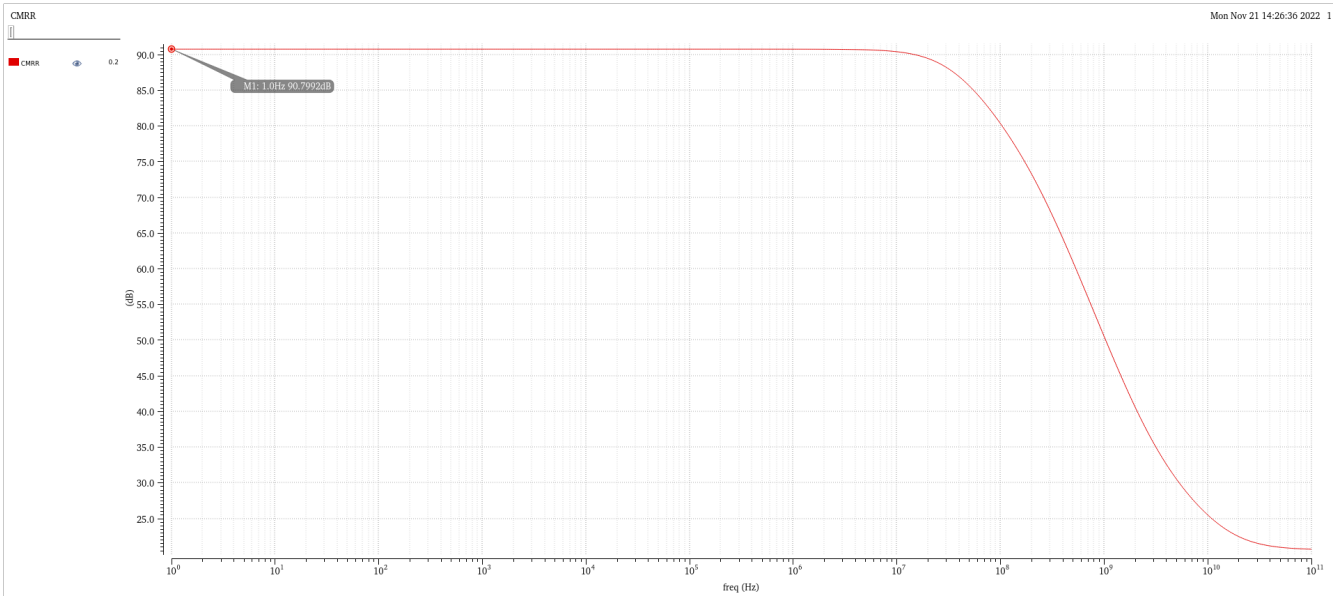

Figure 15: CMRR Post Simulation

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	VO		☐	☑	allv
2	VOdb	wave	☑	☐	
3	VoPhase	wave	☑	☐	
4	ACM		☐	☐	
5	POWER	292.7u	☑	☐	
6	I0/VDD		☐	☑	yes
7	I0/Ibias		☐	☑	yes
8	PSRR		☐	☐	

Figure 16: Power Consumption Post Simulation

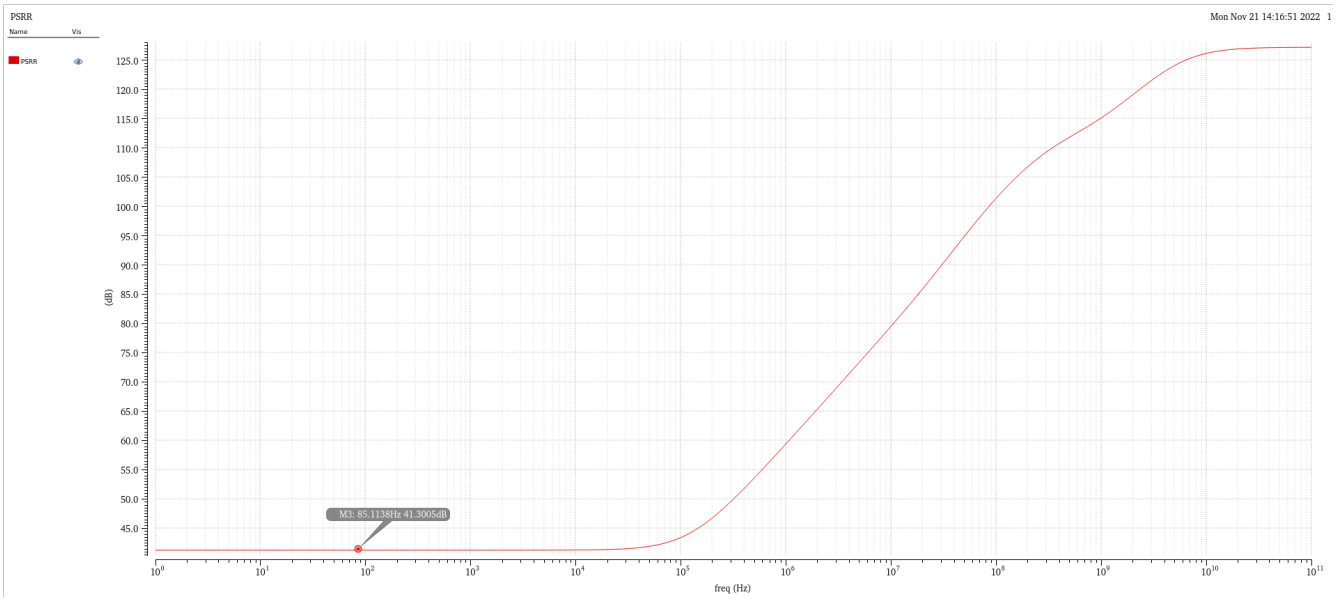

Figure 17: VDD Power Supply Rejection Post Simulation (PSRR+)

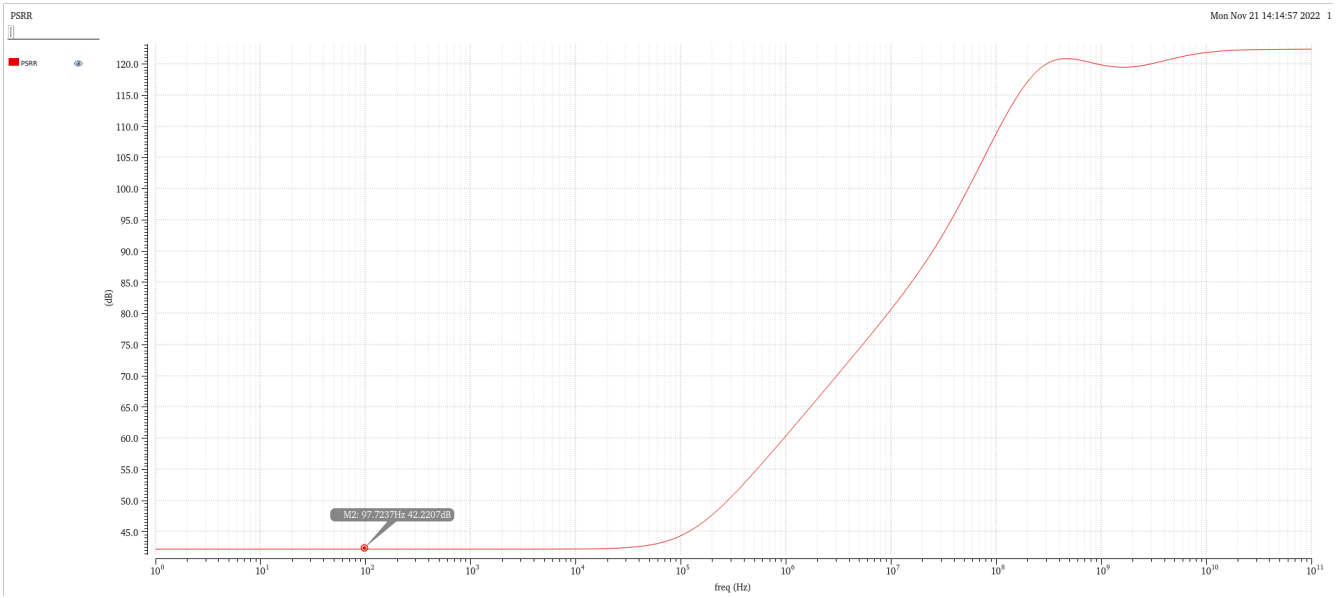

Figure 18: VSS Power Supply Rejection Post Simulation (PSRR-)

Next, Monte Carlo simulations over process variation and mismatch were run to observe the behavior of the low-frequency gain, dominant pole, gain-bandwidth product, and phase margin. Histograms were generated for 200 random points.

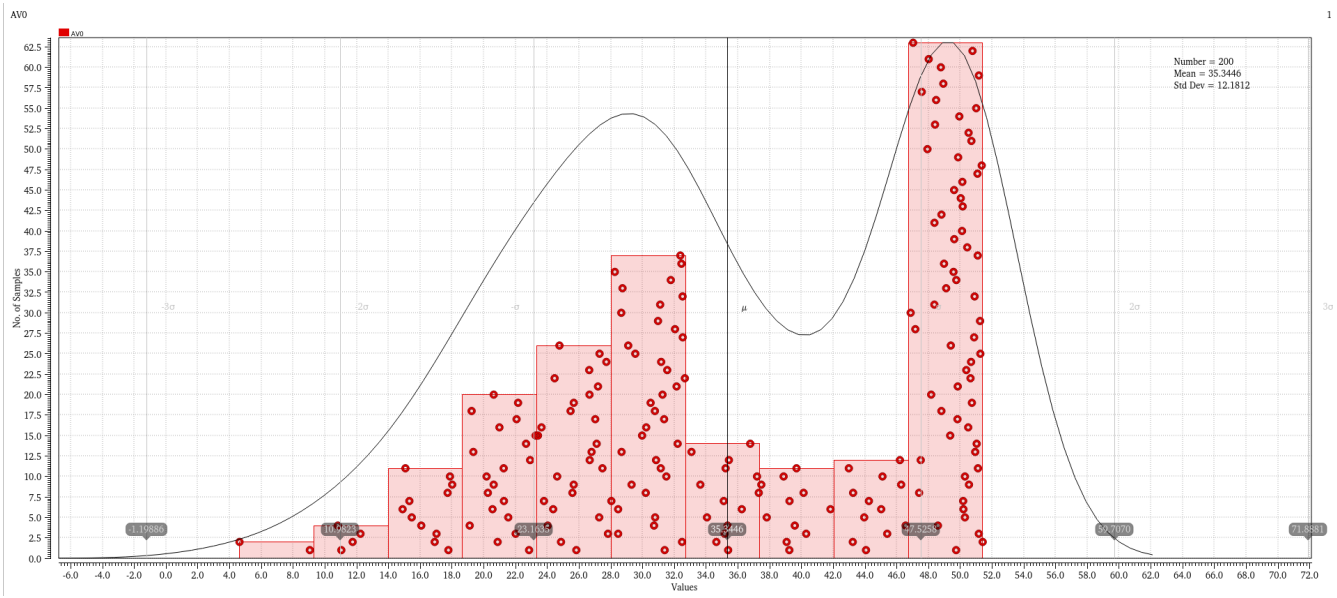

Figure 19: Low-Frequency Gain Monte Carlo

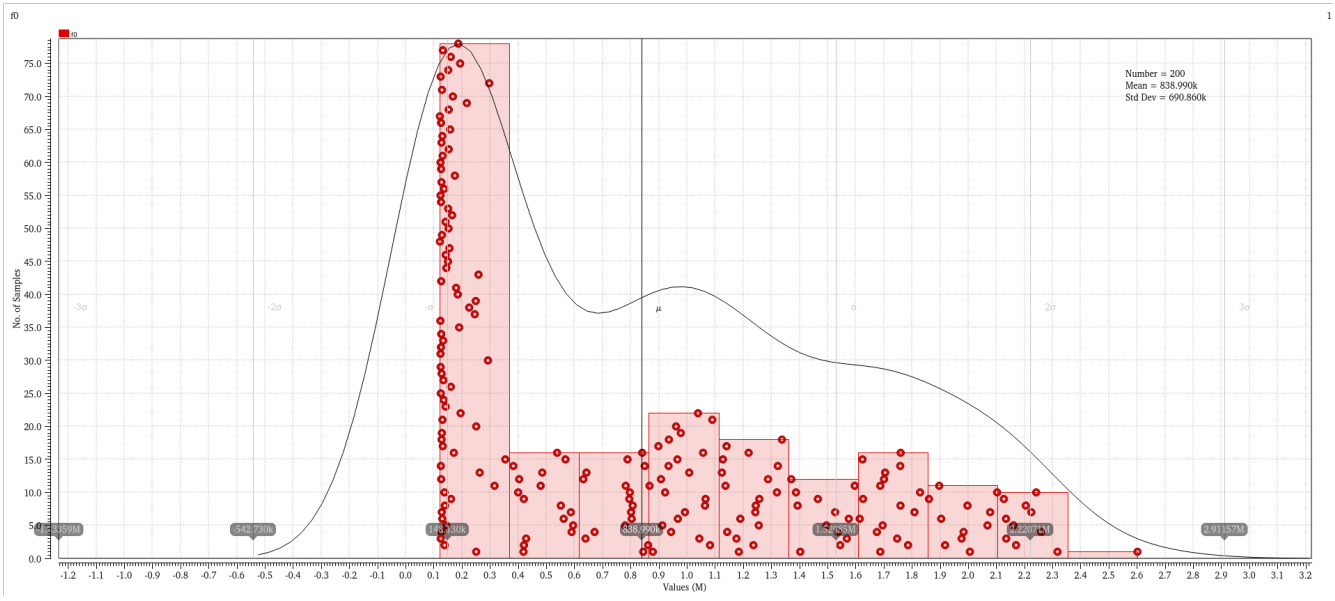

Figure 20: Dominant Pole Monte Carlo

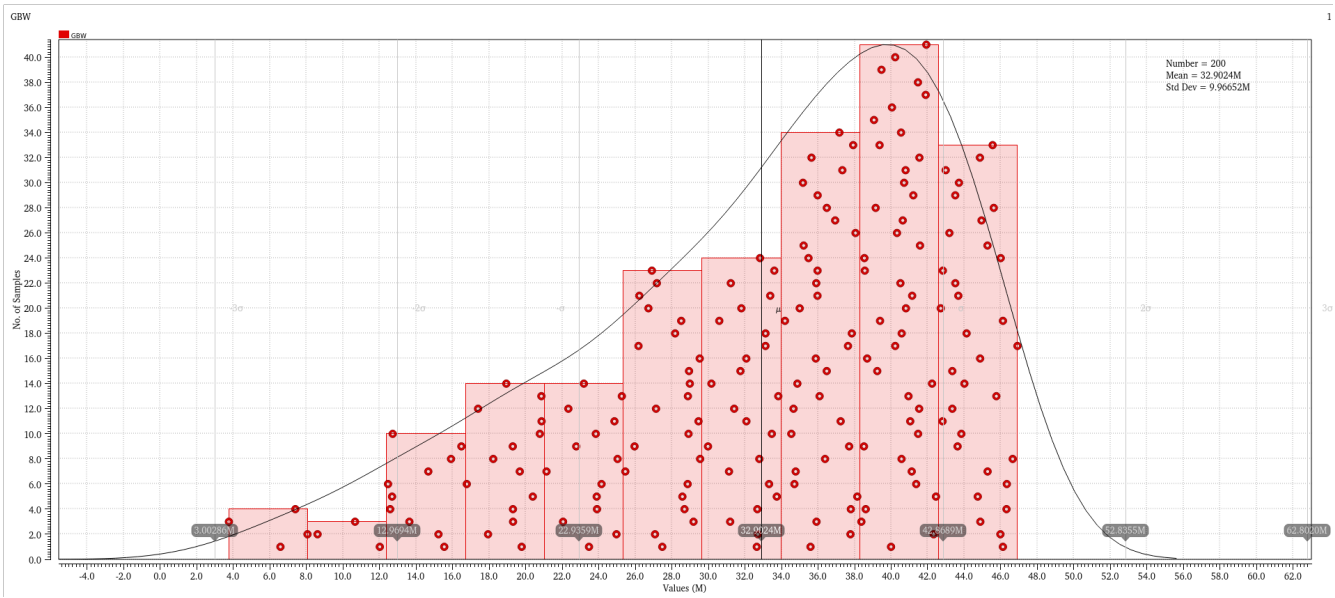

Figure 21: GBW Monte Carlo

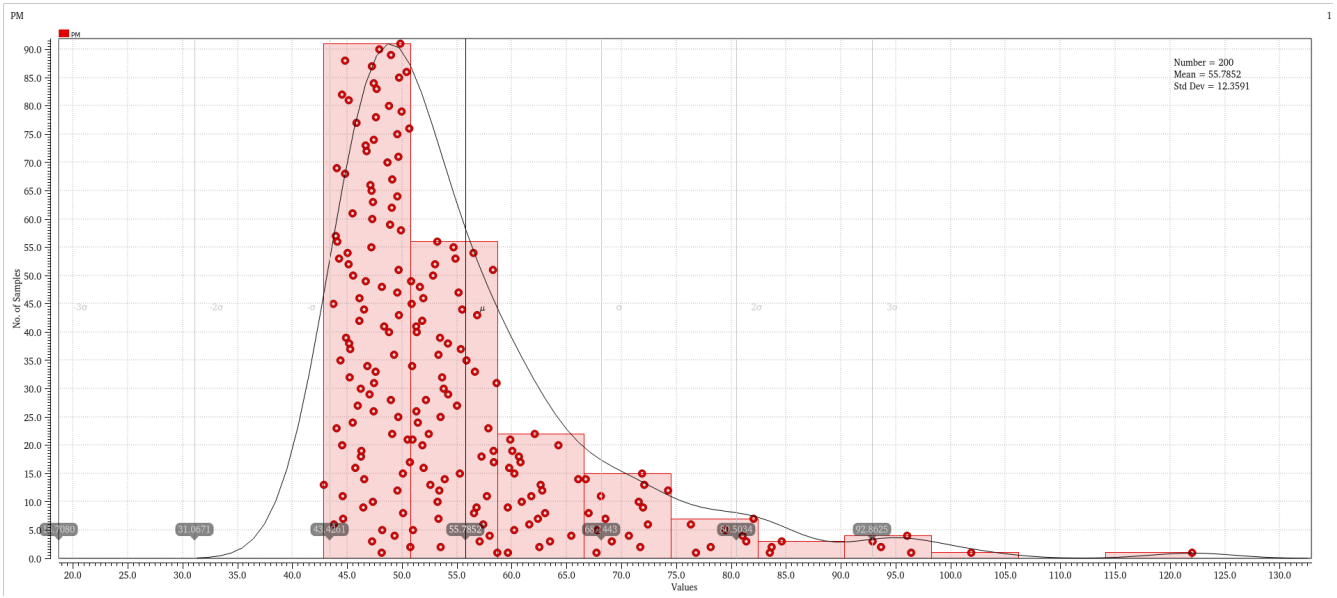

Figure 22: Phase Margin Monte Carlo

Discussion

Considering the impact of layout parasitics on the circuit's AC behavior, the gain was slightly reduced to 51dB and the bandwidth remained approximately the same. Consequently, the GBW was reduced slightly. This reduction in gain can be attributed to the impedance of traces and interconnects. Another consequence of this reduction in gain was a slight decrease in the CMRR, from 92dB to 90dB post-layout. Similarly, the capacitances of traces and vias impacted the transient behavior, lowering the slew rate slightly. From a DC perspective, the power consumption was slightly reduced due to the reduction in gain. The power supply rejection ratio decreased for both supplies, possibly again due to the reduction in gain.

The Monte Carlo simulations revealed some interesting behaviors of the circuit over process variations and mismatch. First, the low-frequency gain displayed a somewhat bimodal behavior, with the majority of points centered around the nominal value of 50dB, and a secondary peak around 30dB. This behavior occurs due to a variation in the device transconductance vs. a consistent drain current. The pole frequency displayed a clear mean around the nominal value of 150kHz, with points sparsely distributed up to 2.6MHz. This large variation can likely be attributed to the dominant gate capacitance of the devices, which is sensitive to process variation. The GBW had a larger spread, centered at the nominal value of 40 MHz and ramping down somewhat linearly to a minimum of 4 MHz. This greater deviation is due to the opposing behavior of the pole frequency vs. low frequency gain. Lastly, the phase margin shows a strong mean around the nominal value of 47 degrees, with values up to 120 degrees, but no less than 43 degrees. Variation in the Miller compensation capacitor is likely the root cause of this distribution.

Conclusion

In this lab, a two-stage operational amplifier including Miller compensation was designed. Post-layout simulations were used to compare the behavior of the circuit including layout parasitics to the ideal model. Monte Carlo simulations were used to visualize how key parameters vary over process variation and mismatch. As usual, good layout practices were used to ensure robustness and hardness to these variations.