Lab 8: Operational Transconductance Amplifiers

ECEN 704-601

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Description

In this lab, the design of operational transconductance amplifiers (OTAs) was explored. One topology was designed and analyzed: the three current mirror OTA, also known as the symmetric OTA. In addition to schematic design, the amplifier was laid out using good matching and layout practices. Simulation was performed both before and after layout to compare how the design parasitics impact the circuit parameters.

Design

To begin, using specifications for the slew rate and power, a value for the tail current was derived from the following system of inequalities

$$SR = K\frac{I_{tail}}{C_L} > 10\frac{V}{\mu s}$$

$$P_{DD} = I_{DD}V_{DD} = (K+1)I_{tail}V_{DD} < 1\ mW$$

Allowing K to equal 1 and providing some margin in the inequalities, I_{tail} can be found to be 300uA, still meeting the power specification.

Next given a desired value for G_m and adding a 20% margin for any lambda effects, the aspect ratios of M1 and M2 can be found as

$$G_m = 600\frac{\mu A}{V} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} I_{tail}}$$

Evaluating this expression, the sizing for M1 and M2 is found to be 6.25.

To set the size of the PMOS active load devices, given that K=1 and allowing them to be twice the size of M1 and M2, we have

$$\left(\frac{W}{L}\right)_{3,4,5,6} = 2\left(\frac{W}{L}\right)_{1,2} = 12.5$$

Additionally, in order to match currents on the outer branches

$$\left(\frac{W}{L}\right)_{7,8} = \left(\frac{W}{L}\right)_{5,6} = 12.5$$

Finally, to set the value of the bias resistor we use the following system of equations

$$R_{bias} = \frac{V_{DD} - (V_{GS} + V_{SS})}{I_{tail}}$$

$$V_{GS} = \sqrt{\frac{2I_{tail}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_9}} + V_{tn}$$

Allowing $\left(\frac{W}{L}\right)_9$ to equal 3, R_{bias} is found to be 2.667kΩ, while still keeping V_{GS9} relatively low at 1V.

From here, the design was tested in simulations and adjusted accordingly to achieve the necessary DC bias points and other specifications.

Results

The schematic for the OTA is shown below in Figure 1, including dummy elements. A finger width of 600nm was used, with a length of 360nm for each transistor.

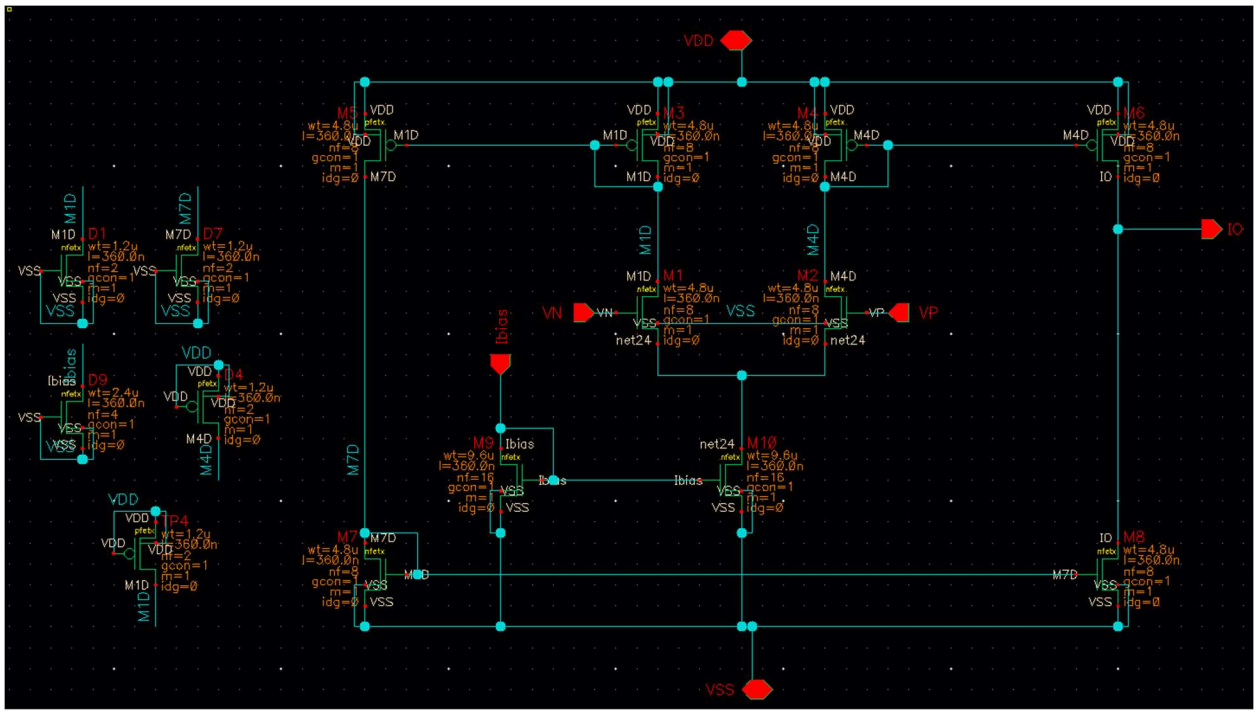

Figure 1: OTA Schematic

From here, a symbol and test bench were created to simulate the circuit.

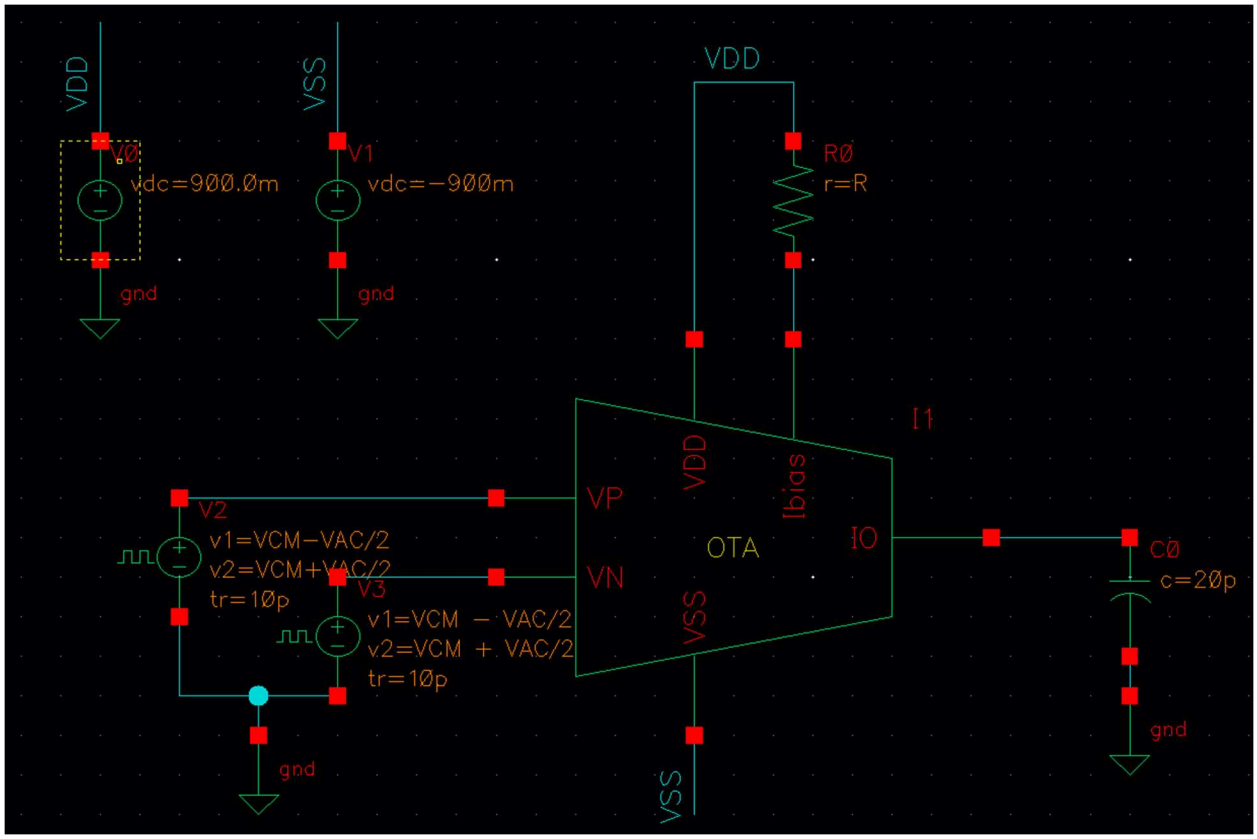

Figure 2: OTA Test Bench

Next, the necessary simulations were performed for the transconductance, slew rate, power consumption, AC gain, dominant pole, phase margin, and gain bandwidth product.

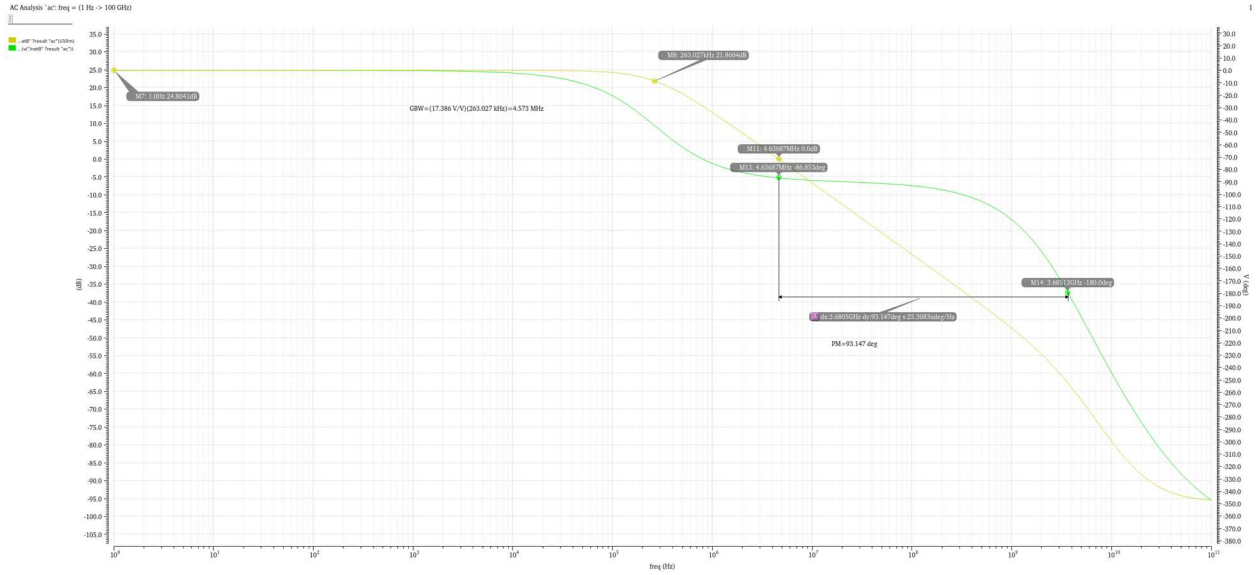

Figure 3: AC Simulations

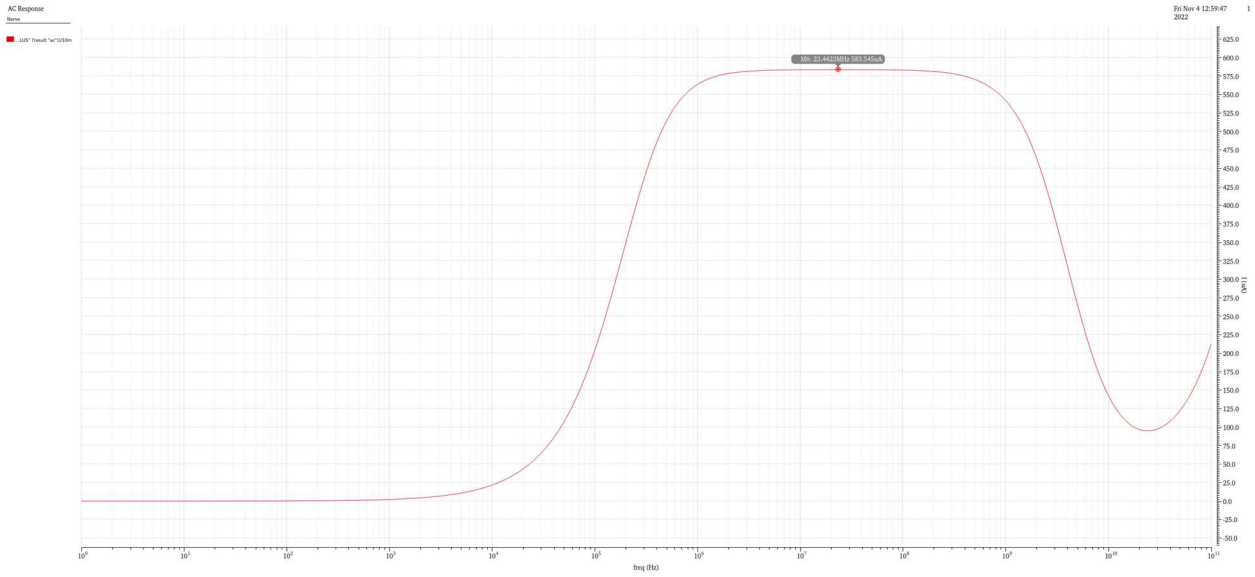

Figure 4: Transconductance Simulation

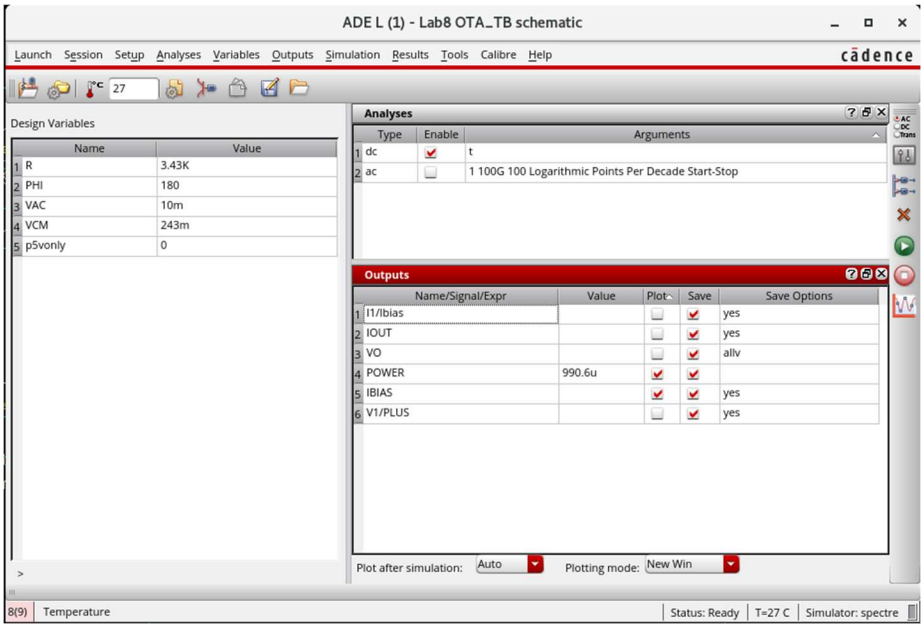

Figure 5: Power Consumption Simulation

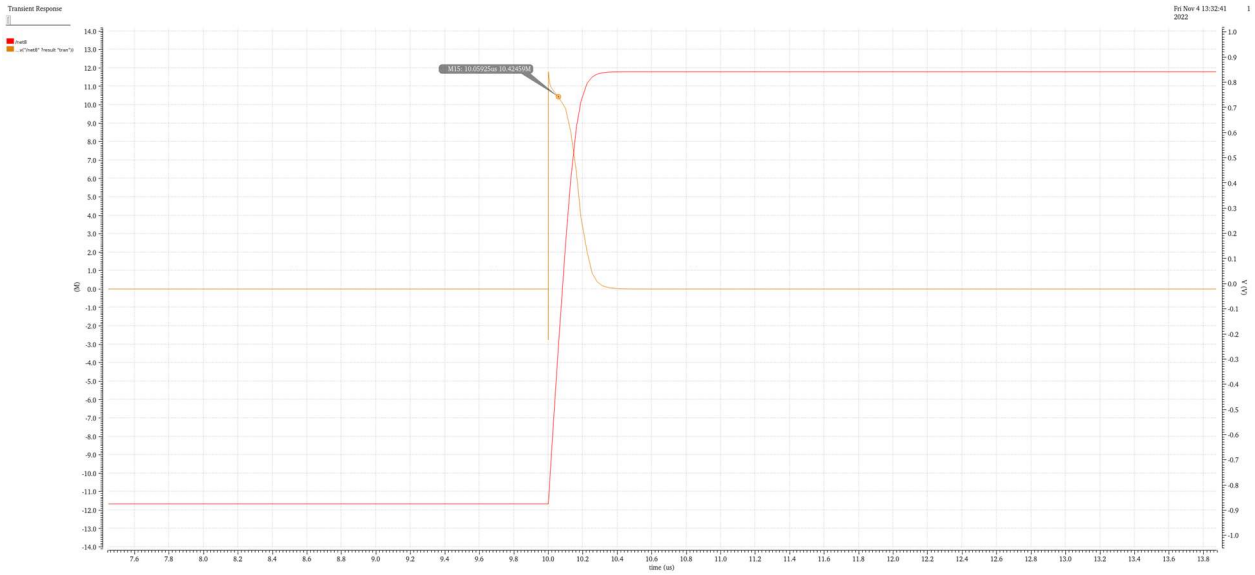

Figure 6: Slew Rate Simulation

Next, the layout was completed. The design was successfully verified using DRC and LVS.

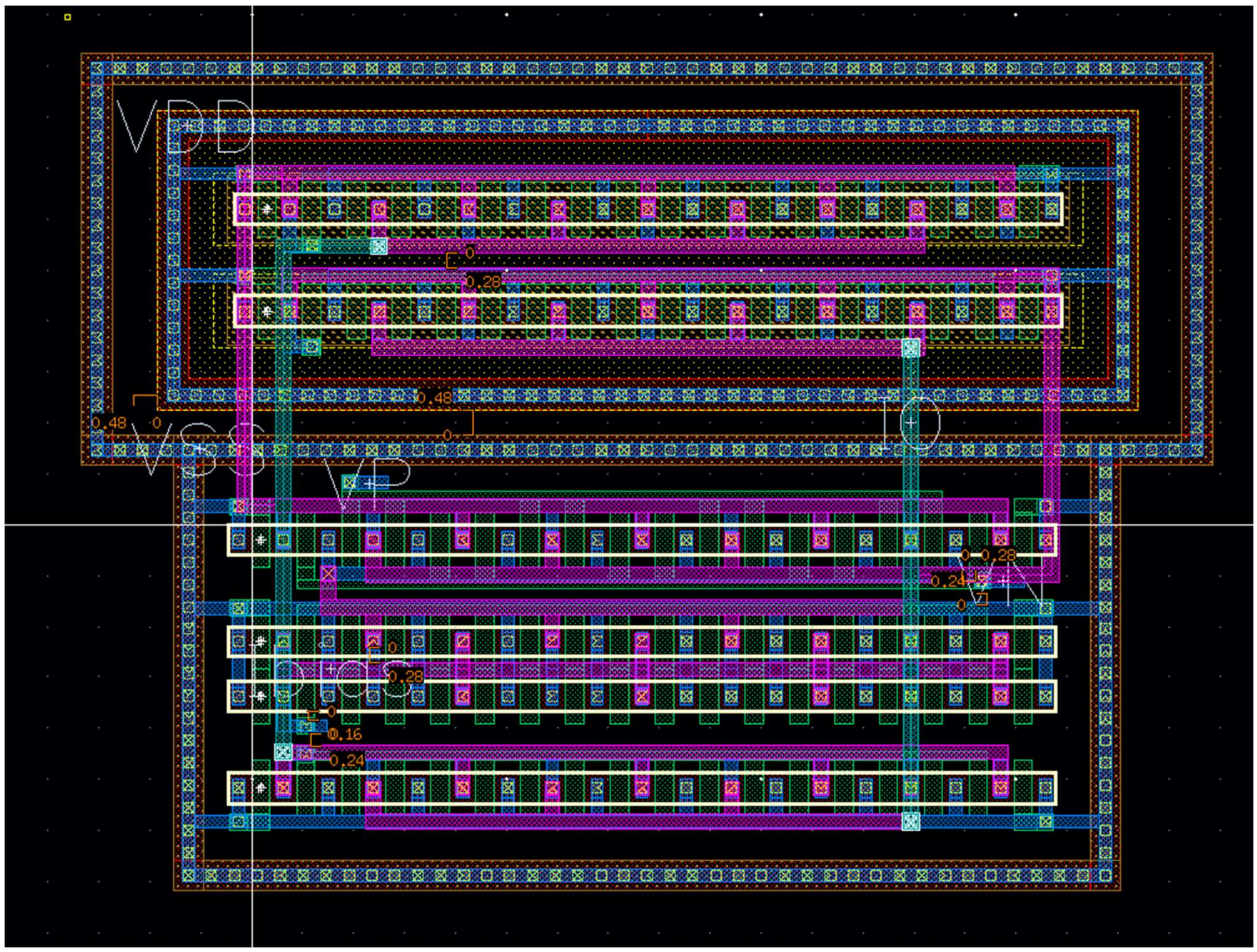

Figure 7: OTA Layout

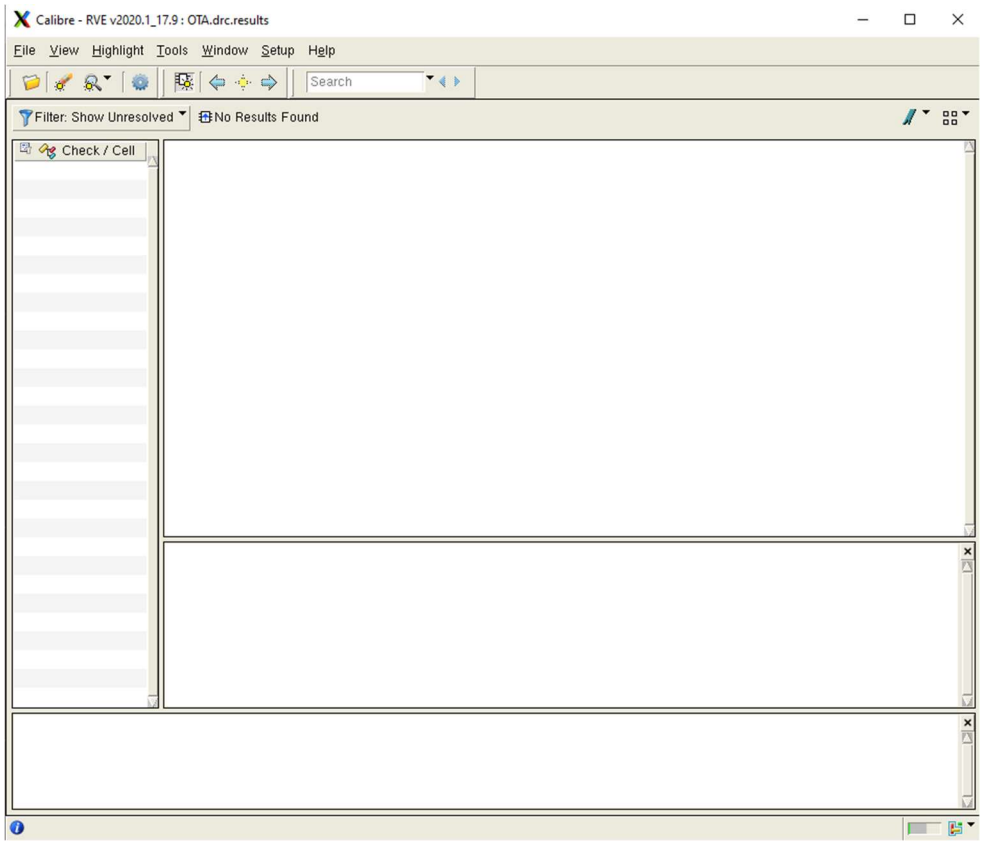

Figure 8: DRC

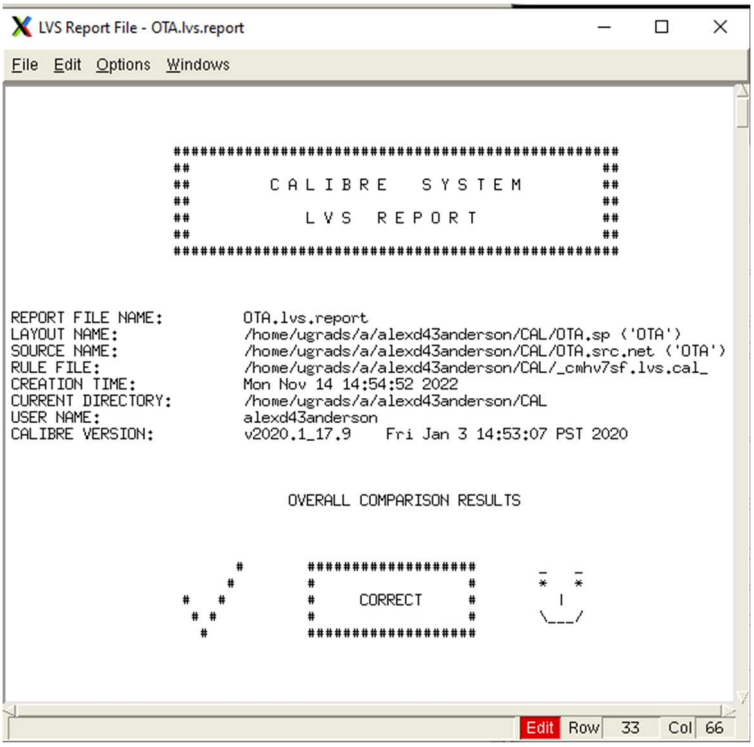

Figure 9: LVS

Finally, with the layout complete, the parasitics were extracted and used to perform post-layout simulations for all the above specifications.

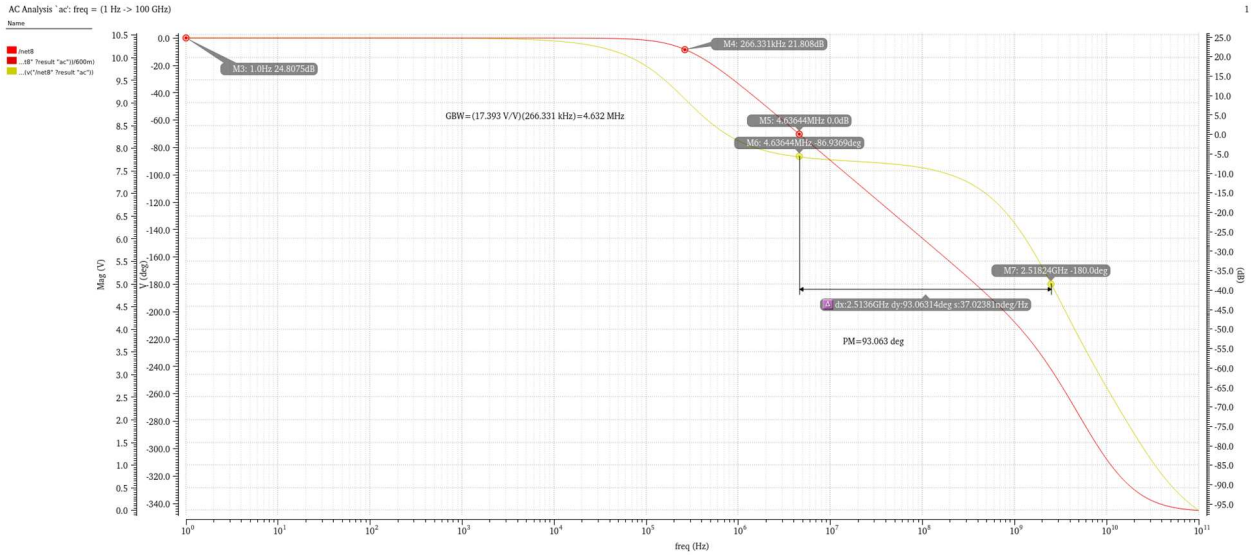

Figure 10: AC Post Simulation

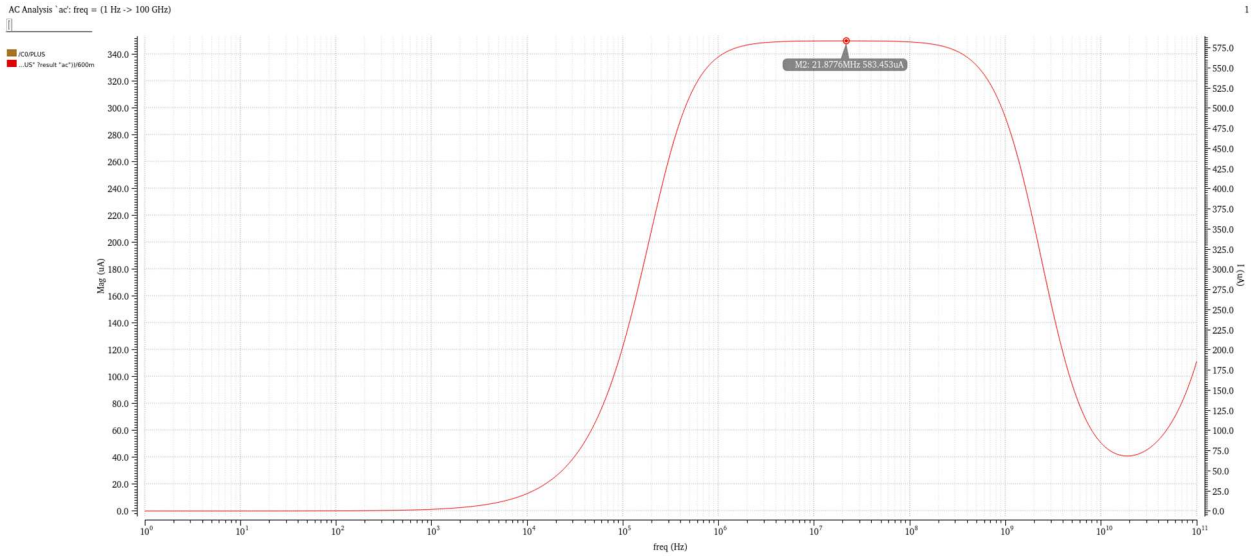

Figure 11: Transconductance Post Simulation

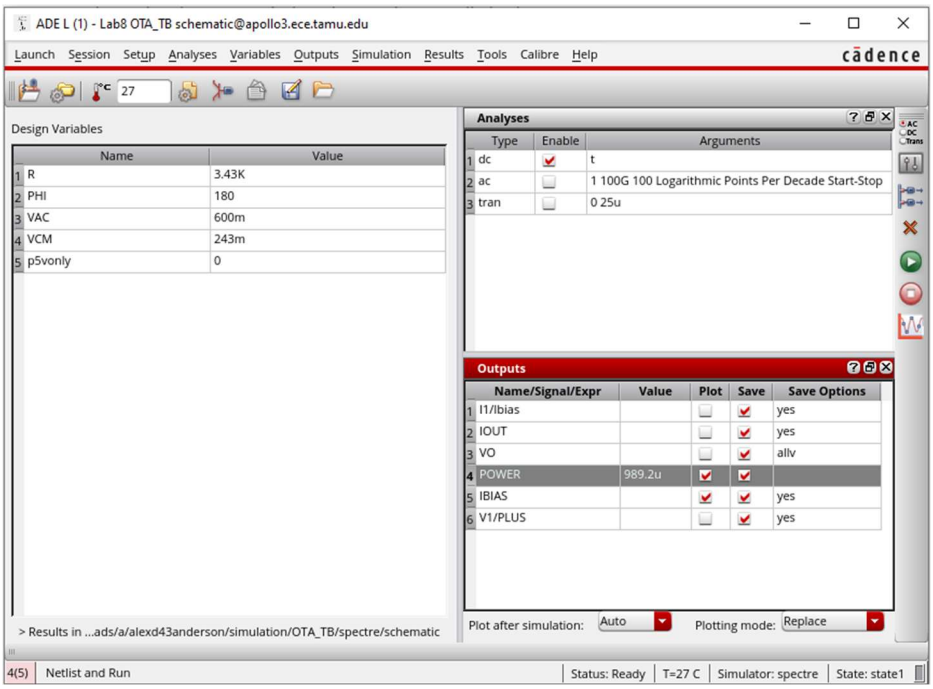

Figure 12: Power Post Simulation

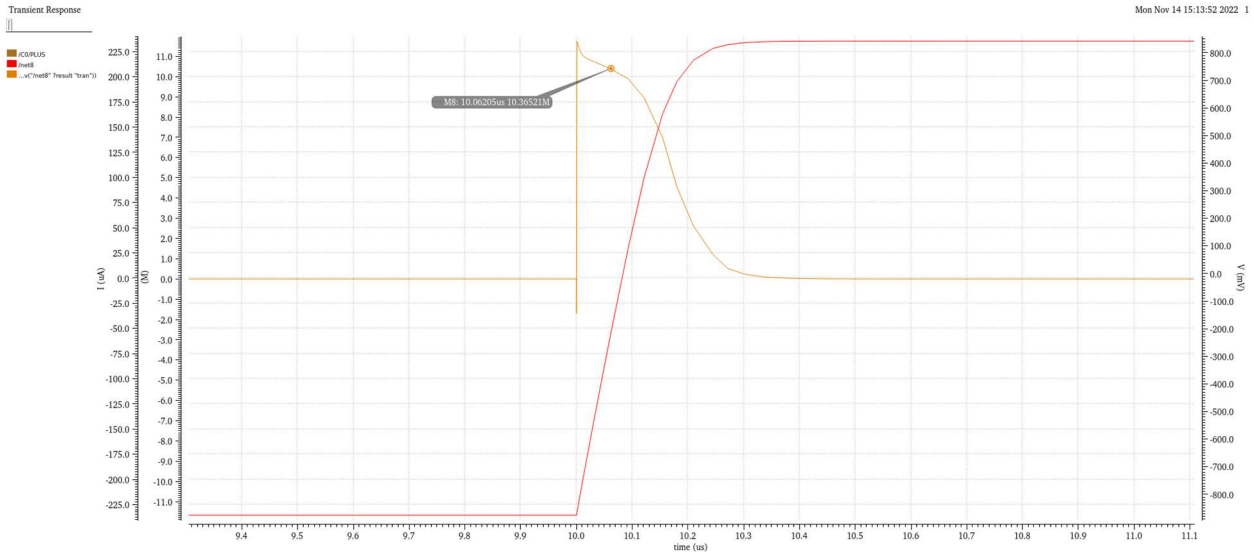

Figure 13: Slew Rate Post Simulation

Discussion

The three-current mirror OTA is an improvement over the basic differential OTA by providing self-biased loads and the addition of an output stage. This design has a larger overall transconductance and gain bandwidth product than the simple differential OTA. Since all of the matched pairs should be equal in size, this design allows for a much easier and systematic common-centroid layout as well.

After layout, the transconductance and gain bandwidth product stayed almost the same when considering parasitics. The power consumption decreased very slightly, about 1uW. Overall, the post layout values were very similar to the original simulations. This could be due to a very similar layout pattern used across all the pairs. The slight increase in bandwidth can perhaps be explained by the introduction of a zero due to trace and via capacitance. The slew rate decreased slightly, which is expected when considering the additional output capacitance from the layout. Overall, the circuit worked as intended both pre and post layout.

Conclusion

In this lab, a three-current mirror OTA was designed, floorplanned, and laid out. Post layout simulations were used to compare the specifications when considering layout parasitics. As always, good design practices were used in the layout such as common centroid, dummy elements, and guard rings.