Lab 5: Design & Simulation of 4-bit Adder

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ECEN 714-603

First, the 4-bit adder layout was completed using the previous 1-bit adder design. The cell was verified using DRC and LVS:
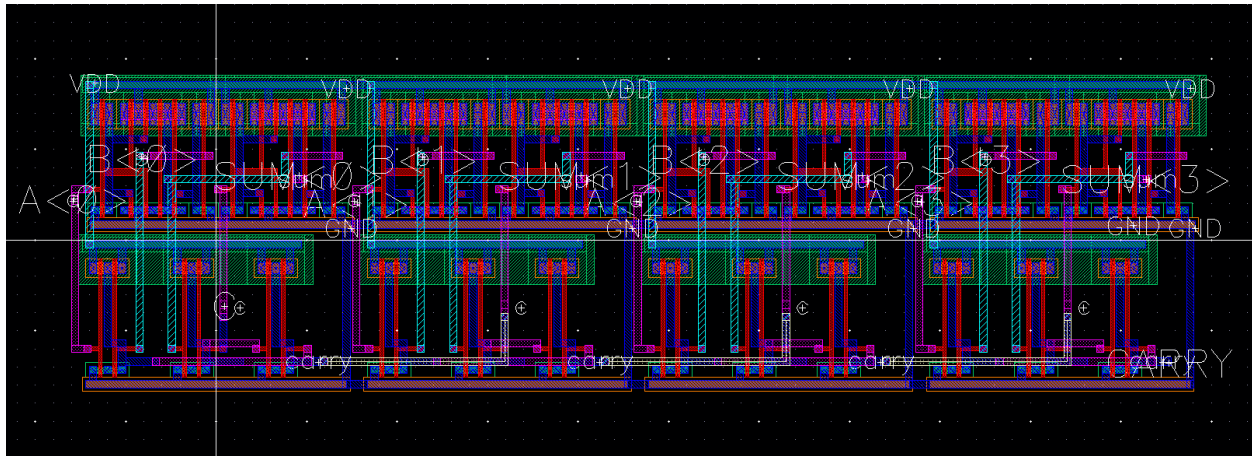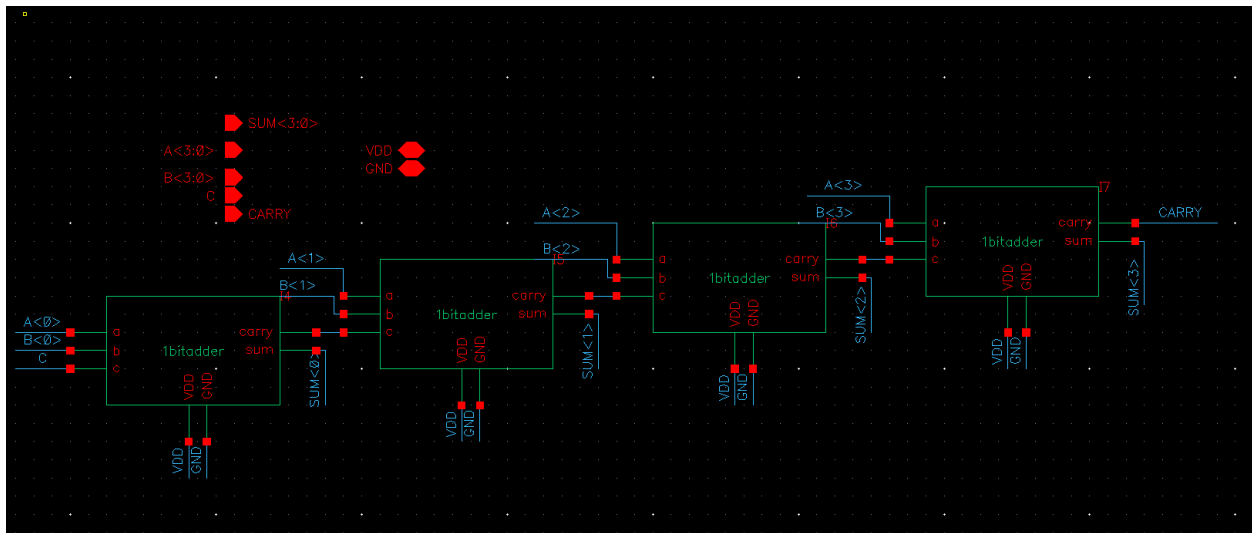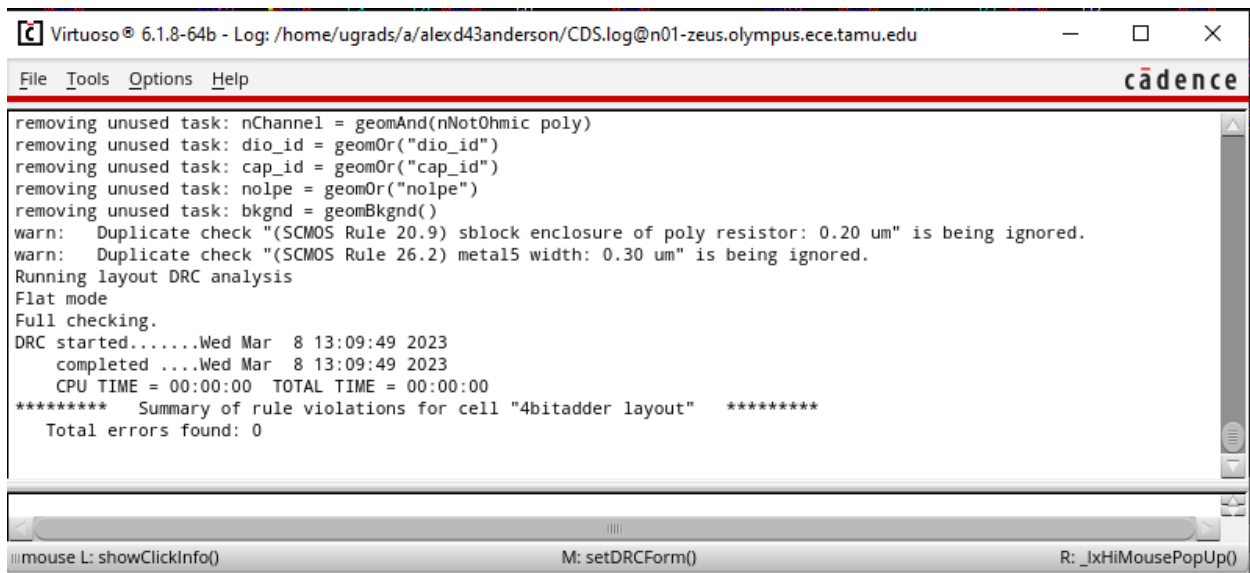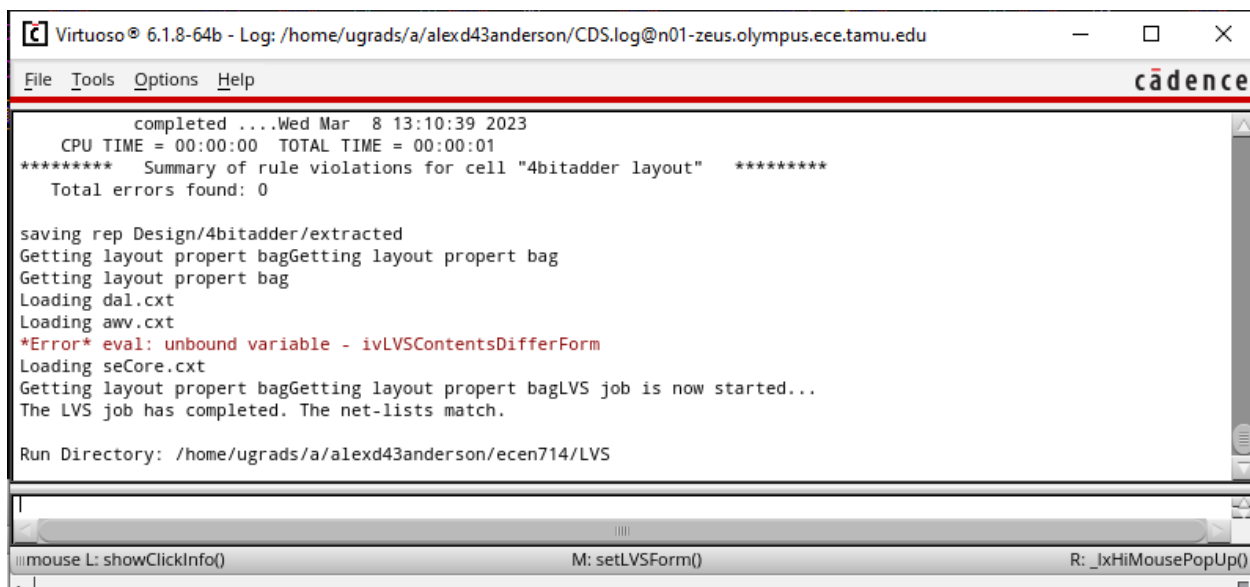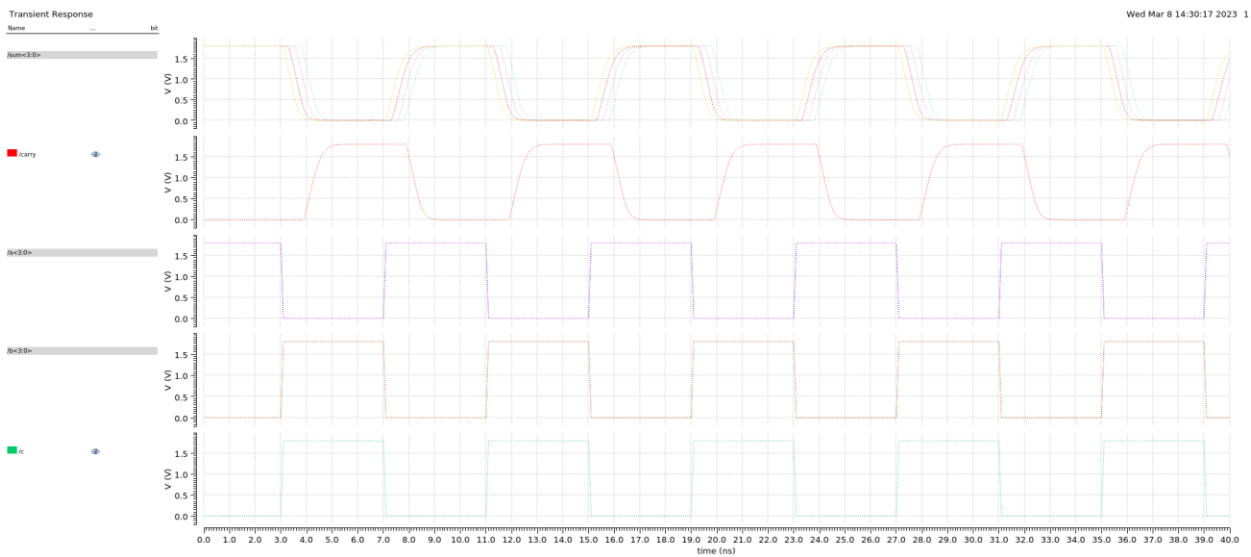

Figure 1: Layout

Figure 2: Schematic

Figure 3: DRC

Figure 4: LVS

Next, the design was tested using extracted parasitics. The test bench is included below:

Figure 5: Test Bench

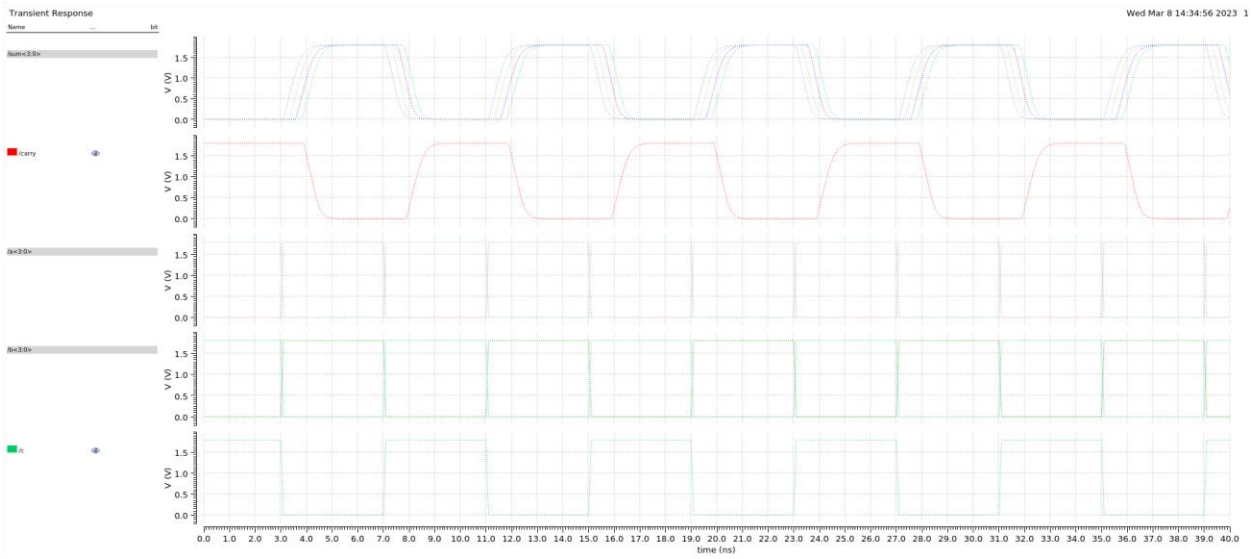The circuit was tested for 4 cases of inputs, and the delay of each output and power consumption was recorded. The results are included below and summarized in Table 1.

Table 1: 4-bit adder results

Input Case	Power	Sum Delay	Carry Delay
A=0000 B=1111 C=1	204.6uW	S3=1.102nS S2=850ps S1=598.5ps S0=361ps	1.202ns
A=1010 B=0101 C=0	207.1uW	S3=1.157ns S2=907.5ps S1=658.2ps S0=416.7ps	1.176ns
A=1010 B=0101 C=1	204.6uW	S3=1.102ns S2=850.7ps S1=599.1ps S0=358.3ps	1.202ns
A=1100 B=1000 C=0	209.9uW	S3=850.1ps S2=636.5ps S1=602.6ps S0=392.8ps	463.3ps

The waveforms for each case are also included below:

A=0000

B=1111

C=1

Expression	POWER
Value	-204.6E-6
Expression	SUM3
Value	-1.102E-9
Expression	SUM2
Value	-850.0E-12
Expression	SUM1
Value	-598.5E-12
Expression	SUM0
Value	-361.0E-12
Expression	CARRY
Value	-1.202E-9

A=1010

B=0101

C=0

A=1010

B=0101

C=1

Expression	POWER
Value	-204.6E-6
Expression	SUM3
Value	-1.102E-9
Expression	SUM2
Value	-850.7E-12
Expression	SUM1
Value	-599.1E-12
Expression	SUM0
Value	-358.3E-12
Expression	CARRY
Value	-1.202E-9

A=1100

B=1000

C=0
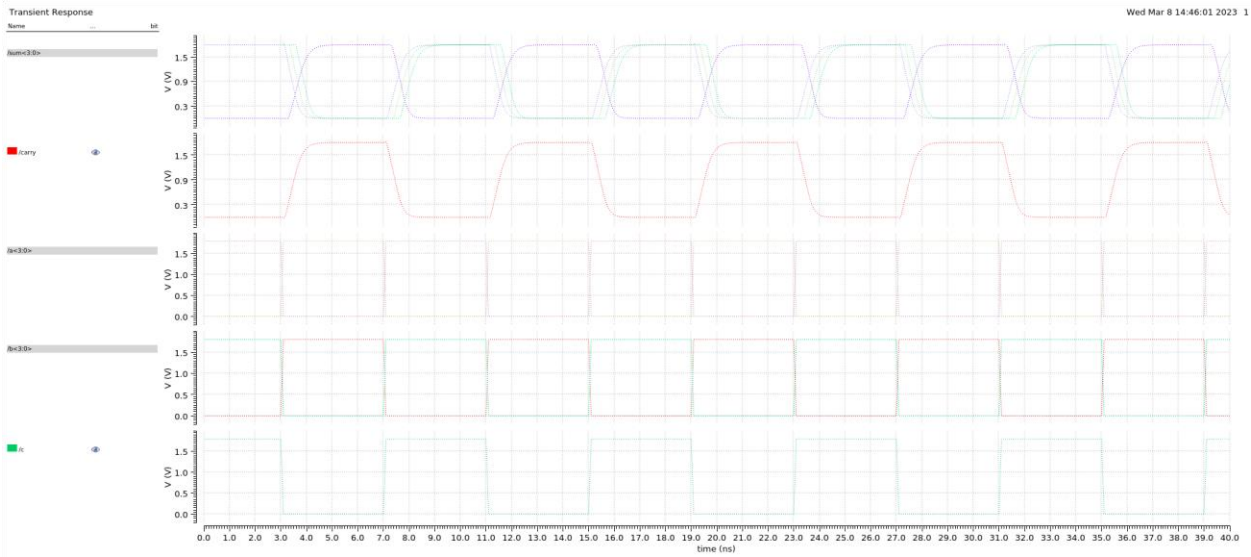
	1
Expression	POWER
Value	-209.9E-6
Expression	SUM3
Value	-850.1E-12
Expression	SUM2
Value	-636.5E-12
Expression	SUM1
Value	-602.6E-12
Expression	SUM0
Value	-392.8E-12
Expression	CARRY
Value	-463.3E-12