a

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1 Truth Table

cs2	cs1	cs0	X_i	Y_i	Z_i	C_{in}	Function
0	0	0	A_i	B_i	C_i	0	Add
0	0	1	$\bar{A}_i$	0	C_i	1	NEG A
0	1	0	A_i	B_i	C_i	0	Add
0	1	1	A_i	B_i	C_i	1	Add with carry
1	0	0	A_i	0	C_i	1	Increment A
1	0	1	A_iB_i	0	C_i	0	AND
1	1	0	$A_i \oplus B_i$	0	C_i	0	XOR
1	1	1	$A_i \oplus B_i$	0	C_i	0	XOR

Table 1: Truth Table of Intermediate I/O

cs2	cs1	cs0	X_i	S_{x_1}	S_{x_0}
0	0	0	A_i	0	0
0	0	1	$\bar{A}_i$	0	1
0	1	0	A_i	0	0
0	1	1	A_i	0	0
1	0	0	A_i	0	0
1	0	1	A_iB_i	1	1
1	1	0	$A_i \oplus B_i$	1	0
1	1	1	$A_i \oplus B_i$	1	0

Table 2: Truth Table of MUX input for X_i

cs2	cs1	cs0	X_i	S_{y_0}
0	0	0	B_i	0
0	0	1	0	1
0	1	0	B_i	0
0	1	1	B_i	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

Table 3: Truth Table of MUX input for Y_i