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8 The Simulator Used along with the Version Number

Logisim - 2.7.1

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10 Contribution of Each Member

10.1 Logic Design and Simplification of Expressions

Student ID	Surname	Contribution
2005001	Anik	Prepared block diagram with IC pin numbers mentioned, obtained simplified expressions for Sx_1, Sx_0, Sy_0
2005012	Jahin	Prepared truth tables for Sx_1, Sx_0, Sy_0
2005013	Muhit	Prepared truth tables for X_i, Y_i, C_{in}
2005017	Amim	Prepared block diagram with IC pin numbers mentioned, obtained simplified expressions for X_i, Y_i, C_{in}
2005023	Jaber	Obtained primary expressions for the Flags Z(Zero Flag) and V(Overflow Flag)

10.2 IC Count Optimization

Student ID	Surname	Contribution
2005001	Anik	Performed optimal manipulations in preprocessing to reduce the number of IC 7408, replaced a NOT gate with XOR gate to lessen one extra IC 7404
2005012	Jahin	Developed synchronization among distinct modules to efficiently use maximum ports of ICs and to keep the modules disjoint
2005013	Muhit	Introduced the possibility of using MUX to avoid using too many gates in preprocessing, resolved errors related to optimization
2005017	Amim	Found a way of determining Overflow without explicitly obtaining the penultimate carry, thereby reducing one extra IC 7483, finalized the solution containing 12 ICs
2005023	Jaber	Wrote a Python bot to scrape SOP forms from the website 32x8.com for automated comparisons

10.3 Logisim Simulation

Student ID	Surname	Contribution
2005001	Anik	Developed Control Preprocessor which generates Sx_1, Sx_0, Sy_0, C_{in} from cs_2, cs_1, cs_0
2005012	Jahin	Developed the circuitry of the full adder (IC 7483) which generates S_3, S_2, S_1, S_0
2005013	Muhit	Developed Input preprocessor (jointly) which generates X_i, Y_i from A_i, B_i, Sx_1, Sx_0, Sy_0
2005017	Amim	Developed Input preprocessor (jointly) which generates X_i, Y_i from A_i, B_i, Sx_1, Sx_0, Sy_0
2005023	Jaber	Developed the circuitry of flags calculation which generates S, C, Z, V

10.4 Hardware Implementation

Student ID	Surname	Contribution
2005001	Anik	Developed Control Preprocessor which generates Sx_1, Sx_0, Sy_0, C_{in} from cs_2, cs_1, cs_0, assisted in developing the circuitry of Full Adder and flags calculation
2005012	Jahin	Developed a switching circuit for controlling the 11 input bits through three 4-bit DIP switches, also assisted in developing an output viewer circuit consisting of LEDs
2005013	Muhit	Developed Input preprocessor (jointly) which generates X_i, Y_i from A_i, B_i, Sx_1, Sx_0, Sy_0 and assisted in the circuitry of Full Adder and flags calculation
2005017	Amim	Developed Input preprocessor (jointly) which generates X_i, Y_i from A_i, B_i, Sx_1, Sx_0, Sy_0 and assisted in the circuitry of Full Adder and flags calculation
2005023	Jaber	Assisted in developing an output viewer circuit consisting of LEDs, finalized the hardware with improvements in structural integrity

10.5 Verification and Testing

Student ID	Surname	Contribution
2005001	Anik	Developed a python script for verifying the generated truth table in Logisim through comparison with given functions
2005012	Jahin	Refurnihsed the switching circuit for easy inputting mechanism, Performed random testing
2005013	Muhit	Performed extensive random testing and resolved bugs through backtracking
2005017	Amim	Performed crucial debugging while performing the verification process, performed random testing
2005023	Jaber	Developed a python script for randomly generating testcases and their corresponding solutions based on given control bits

10.6 Report Preparation

Student ID	Surname	Contribution
2005001	Anik	Section A, B, J
2005012	Jahin	Section E, F
2005013	Muhit	Section D
2005017	Amim	Section C
2005023	Jaber	Section G, H