ALI AQDAS

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RESEARCH INTERESTS

Microarchitectural Security, Disaggregated Memory Systems (CXL)

EDUCATION

Purdue University *August 2024 - Present*
Doctorate in Computer Science CGPA: **4/4**
Advisor: Dr. Kazem Taram
Topic: Security in Compute Express Link

National University of Sciences and Technology, Islamabad *Sept 2019 - Jun 2023*
B.E. in Electrical Engineering CGPA: **3.93/4**
Thesis: SoC Implementation of RISC-V Vector Processor
Advisor: Dr. Muhammad Imran
Co-advisor: Dr. Rehan Ahmed

EXPERIENCE

SecArch Lab, Purdue University Mar 2025 - Present
Research Assistant *West Lafayette, USA*

Advisor: Dr. Kazem Taram

- Exploring cache-based side-channel vulnerabilities from CXL-attached devices at the microarchitectural level
  Collaborators: Zixuan Wang (Apple) and others

Next-G Architectures Lab, Purdue University Aug 2024 - Mar 2025
Research Assistant *West Lafayette, USA*

Advisor: Dr. Muhammad Shahbaz
Project Title: Accelerated Transport for Distributed Machine Learning

- Setup Experimental Testbed of Open-Source RDMA Implementation (CoyoteOS)
- Integrated SDNet Simulation Platform with CoyoteOS
- Implemented Custom-Transport alongside RDMA Implementation

System-on-Chip(SoC) Design Lab, NUST Jan 2024 - July 2024
Research Assistant *Islamabad, Pakistan*

Advisor: Dr. Muhammad Imran

- Surveyed Design for Testability Techniques such as SSN, Determinsitic Scan, and Multi-Cycle Tests

System-on-Chip(SoC)/Integrated Circuits Design Lab, NUST Jun 2022 - Jun 2023
Research Assistant *Islamabad, Pakistan*

Advisors: Dr. Muhammad Imran and Dr. Rehan Ahmed
Project Title: SoC Implementation of RISC-V Vector Processor

- Designed and Integrated a Single-Lane Chained Vector Processor with In-House Scalar Core
- Developed Microbenchmarks and Applications for Performance Benchmarking
- Synthesized Design for TSMC 65/22nm and ASAP 7nm

AI Lounge Jul 2021 - Jul 2024
Teaching Assistant *Islamabad, Pakistan*

Advisors: Dr. Syed Ali Raza Zaidi (Leeds) and Dr. Hassan Aqeel (Aston)
Project Title: TinyML and its Applications | GitHub

- Implemented a Fall Detection System to reduce fatality risk in elderly people through appropriate alerting system.
- Developed content for Workshop/MOOC

Signal Processing and Machine Learning Lab, NUST Jul 2020 - Oct 2020
Summer Intern *Islamabad, Pakistan*

Advisors: Dr. Hassan Aqeel (Aston)
Project Title: Keratin Pearl Localization in Whole Slide Images | GitHub

- Designed a tool to localize anomalies in whole slide images to reduce doctors' effort in diagnosing tumors.
- Performed tiling of ultra high resolution images using OpenSlide
- Binary Mask generation for image segmentation using GeoJSON and SciKit Image

TEACHING EXPERIENCE

Purdue University Aug 2024 - Present
Graduate Teaching Assistant *West Lafayette, IN*

Course List

- CS-250-DEV Computer Architecture (Summer 25')
- CS-250 Computer Architecture (Fall 24'/Spring 25')

NUST Chip Design Center May 2024 - July 2024
Instructor *Islamabad,Pakistan*

- Designing and Conducting Hands-on Labs with Dr. Muhammad Imran

PUBLICATIONS

Under Review

[IEEE TETC] V-Flow: A RISC-V Vector Processor for Machine Learning, IEEE Transactions on Emerging Technologies in Computing
Ali Aqdas, Muhammad Ibrahim, Farheen Gul, Rehan Ahmed, Joon-Sung Yang and Muhammad Imran

PROFESSIONAL SERVICE

- Volunteer Artifact Evaluator, International Symposium on Computer Architecture (ISCA '25)

HONORS AND AWARDS

- GPA-based Scholarship Award in NUST 2019-2023
- Full Scholarship Award in Higher Secondary School 2017-2019
- Merit-based Scholarship Award in Secondary School 2015-2017

NOTABLE PROJECTS

XOR-Memory Generator | GitHub

XOR-Memory is a high-bandwidth memory designed by LaForest, et al. It uses BRAMs to make multi-ported memories in FPGAs. XOR-Memory Generator is a software tool that can be used to generate

Verilog files for variable sized memory with different number of read and write ports. The word size is also adjustable. The design can also be verified through script generated testbench.

FPGA Implementation of Bresenham Circle Drawing Algorithm | **GitHub**

Bresenham Circle Drawing algorithm is a lightweight algorithm to draw circles on computer that only computes points for an octant of circle, and uses eight way symmetry to draw a full circle.

- Implemented Bresenham's Circle Drawing Algorithm in Verilog to draw circles with variable radii.
- Utilized University of Toronto's VGA Adapter to display the output on LCD using DE1-SoC. https://www.eecg.utoronto.ca/ jayar/ece241$_0$7F/vga/

Angle of Arrival Estimation in 4-6 GHz Range | **GitHub**

- Literature Survey for Angle of Arrival Estimation Algorithms
- MATLAB Simulations of Multiple Signal Classification (MUSIC) Algorithm in Uniform Circular Array (UCA)

Further Projects available on LinkedIn and GitHub

REFERENCES

1. **Dr. Kazem Taram**
   Department of Computer Science, Purdue University
   muhammad.imran1@seecs.edu.pk
2. **Dr. Muhammad Imran**
   Department of Electrical Engineering, National University of Sciences and Technology
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3. **Dr. Hasan Aqeel Khan**
   Department of Computer Science, Aston University
   h.khan54@aston.ac.uk
4. **Dr. Syed A. R. Zaidi**
   School of Electronic and Electrical Engineering, University of Leeds
   s.a.zaidi@leeds.ac.uk