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19

Field Effect Transistors

INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

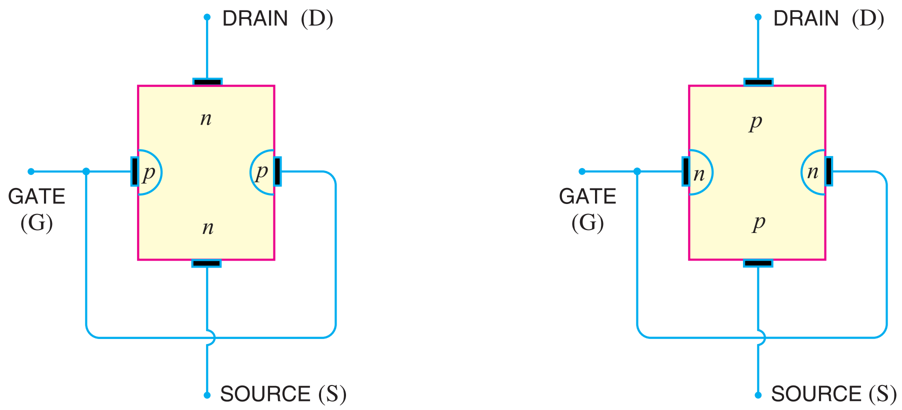
To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET.*

19.2 Junction Field Effect Transistor (JFET)

A ***junction field effect transistor*** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET
(*i*)

p-Channel JFET
(*ii*)

Fig. 19.1

* It would seem from Fig. 19.1 that there are three doped material regions. However, this is not the case. The gate material *surrounds* the channel in the same manner as a belt surrounding your waist.

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

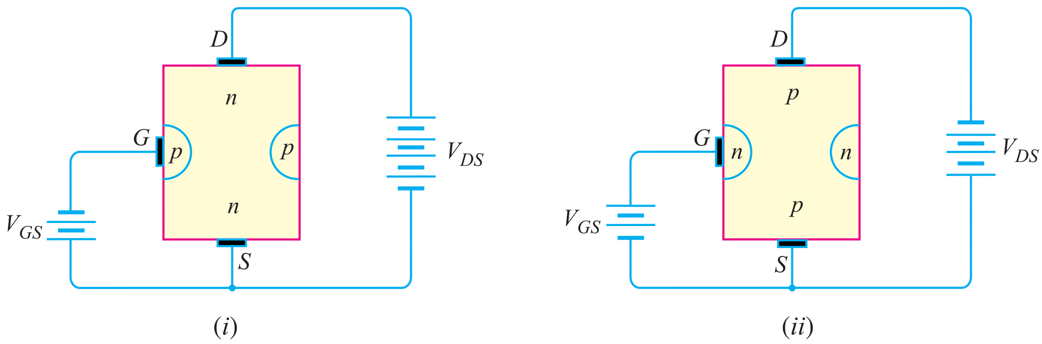


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

* The resistance of the channel depends upon its area of X-section. The greater the X-sectional area of this channel, the lower will be its resistance and the greater will be the current flow through it.

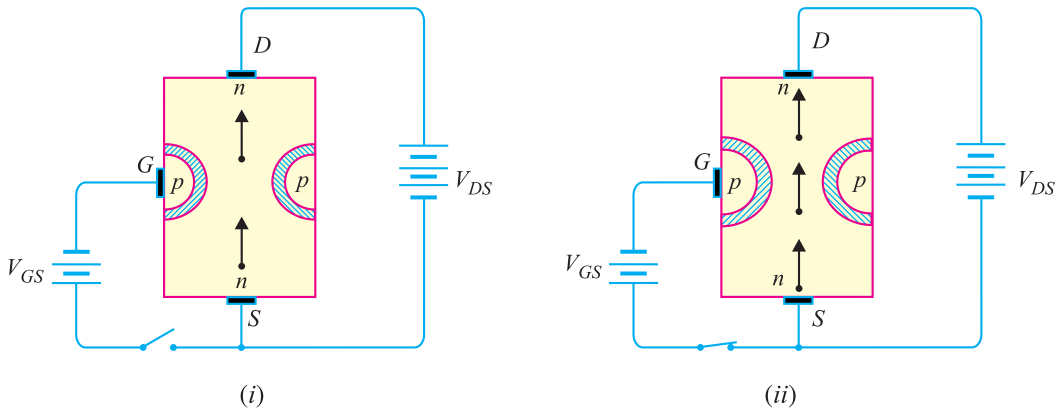
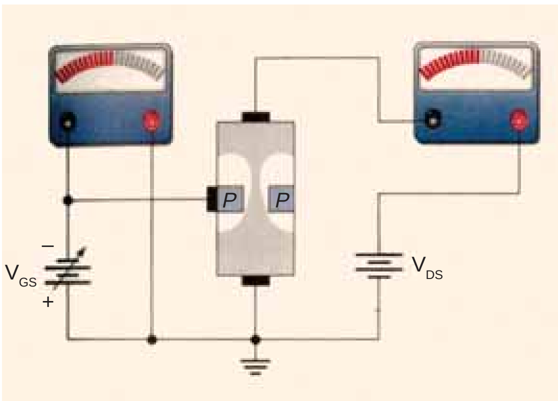


Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.



JFET biased for Conduction

Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.

19.4 Schematic Symbol of JFET

Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought

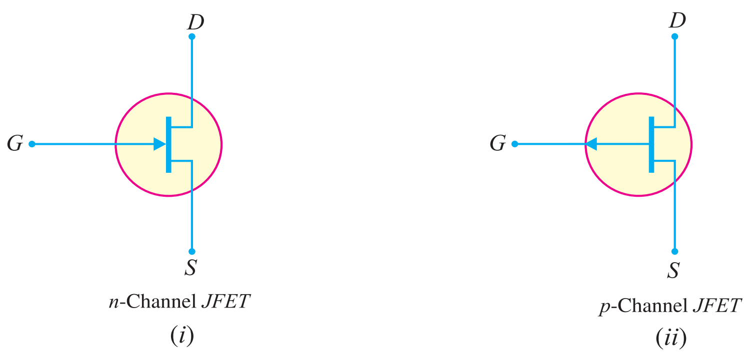
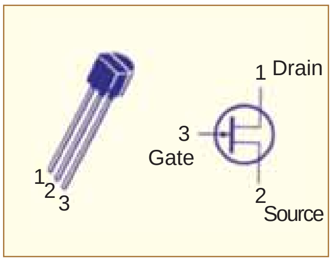


Fig. 19.4

as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].



19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few µA while *JFET* gate current a thousand times smaller [See Fig. 19.5].

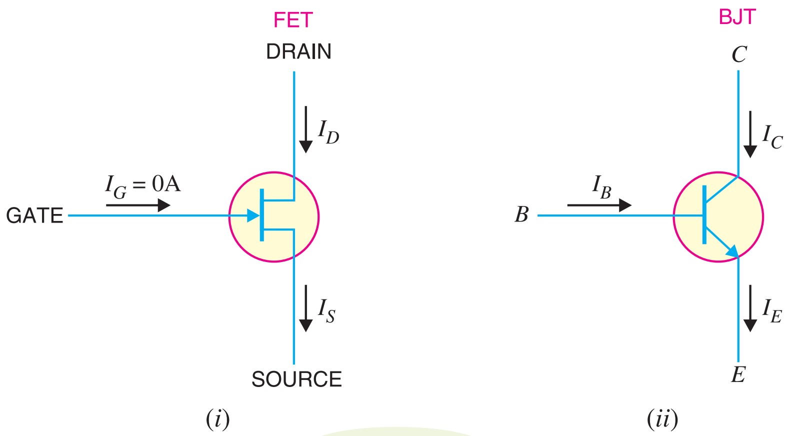


Fig. 19.5

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

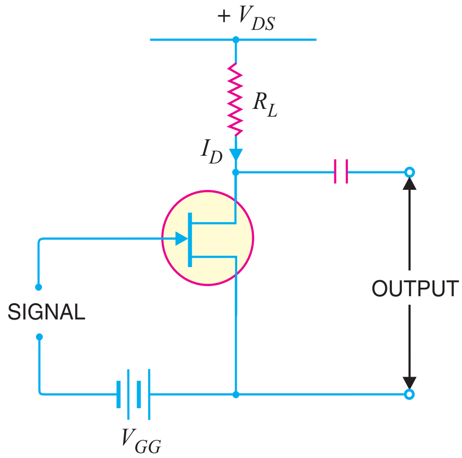


Fig. 19.6

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

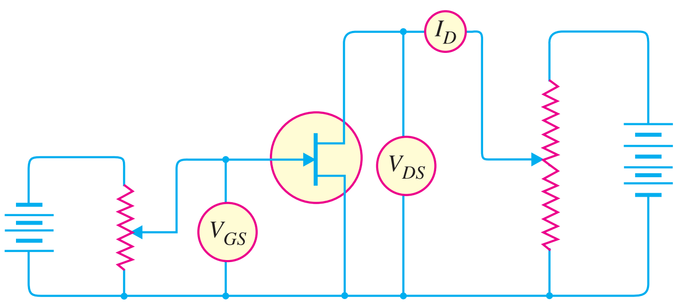


Fig. 19.7

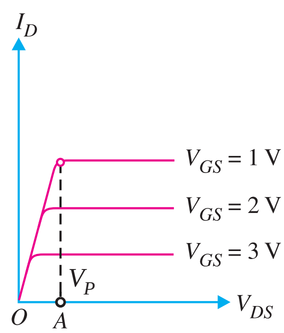


Fig. 19.8

The following points may be noted from the characteristics :

(i) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, *OA* is the *pinch off voltage* V_P.

(ii) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(iii) The characteristics resemble that of a pentode valve.

19.9 Salient Features of JFET

The following are some salient features of *JFET* :

(i) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET.*

(ii) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(iii) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(iv) Since there is no gate current, $I_D = I_S$.

(v) The *JFET* must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(vi) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(vii) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(viii) The drain current I_D is controlled by changing the channel width.

(ix) Since *JFET* has no gate current, there is no β rating of the device. We can find drain current I_D by using the eq. mentioned in Art. 19.11.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})

2. Pinch off voltage (V_P)

3. Gate-source cut off voltage [$V_{GS\,(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current*.

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

* Forward biasing gate-source *pn* junction may destroy the device.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

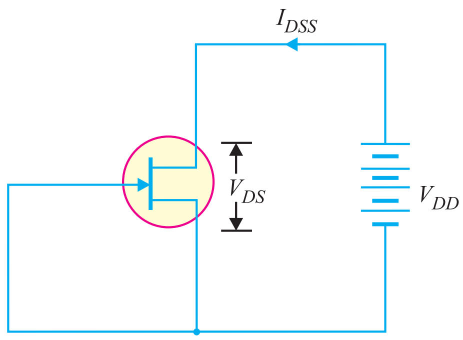


Fig. 19.9

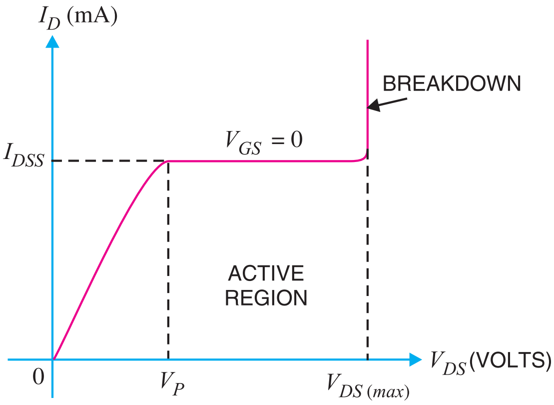


Fig. 19.10

The following points may be noted carefully :

(i) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(ii) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(iii) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for V_{GS} = 0V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

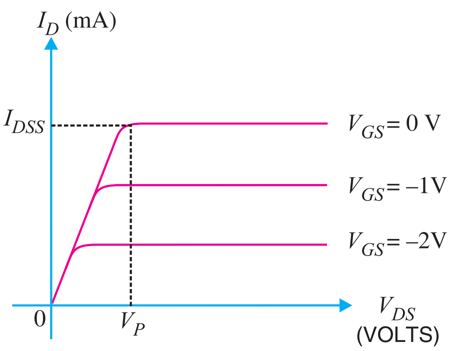


Fig . 19.11

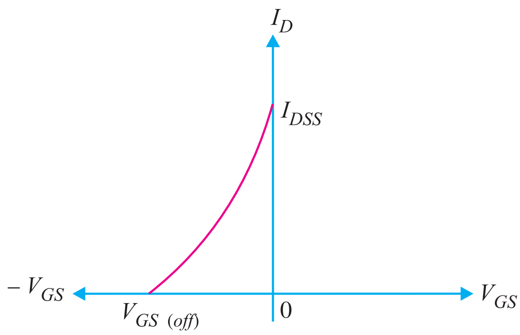


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\ (off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\ (off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\ (off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\ (off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\ (off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}. However, $V_{GS\ (off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

19.11 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 19.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\ (off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\ (off)}|$$

For example, if a *JFET* has $V_{GS\ (off)} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 19.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\ (off)}}\right]^2$$

where
I_D = drain current at given V_{GS}
I_{DSS} = shorted – gate drain current
V_{GS} = gate–source voltage
$V_{GS\ (off)}$ = gate–source cut off voltage

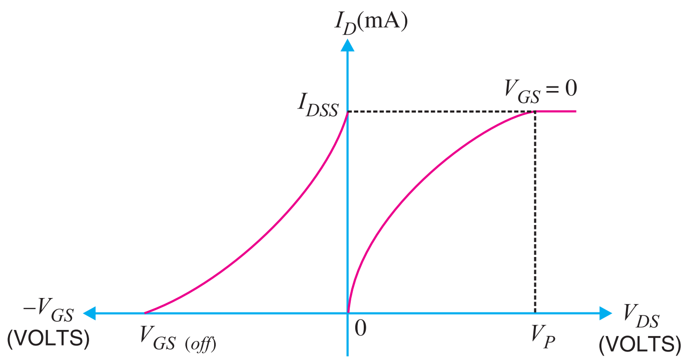


Fig. 19.13

Example 19.1. *Fig. 19.14 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

Solution. Referring to the transfer characteristic curve in Fig. 19.14, we have,

$$I_{DSS} = 12 \text{ mA}$$
$$V_{GS\,(off)} = -5 \text{ V}$$

$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or $$I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA} \quad \textbf{Ans.}$$

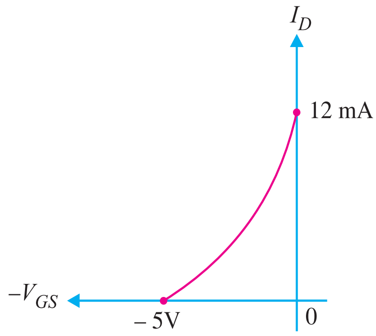


Fig. 19.14

Example 19.2. *A JFET has the following parameters: I_{DSS} = 32 mA ; $V_{GS\,(off)}$ = – 8V ; V_{GS} = – 4.5 V. Find the value of drain current.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$
$$= \textbf{6.12 mA}$$

Example 19.3. *A JFET has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 6 V, find the value of (i) V_{GS} and (ii) V_P.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

or $$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$

or $$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(i) ∴ $$V_{GS} = \mathbf{-1.76\ V}$$

(ii) and $$V_P = -V_{GS\,(off)} = \mathbf{6\ V}$$

Example 19.4. *For the JFET in Fig. 19.15, $V_{GS\,(off)}$ = – 4V and I_{DSS} = 12 mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS\,(off)}$ = – 4V, V_P = 4V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with V_{GS} = 0V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$
$$= 4\text{V} + (12 \text{ mA})(560\Omega) = 4\text{V} + 6.72\text{V} = \textbf{10.72V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

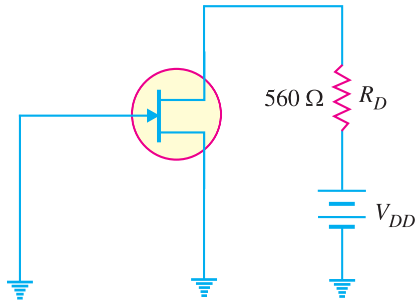


Fig. 19.15

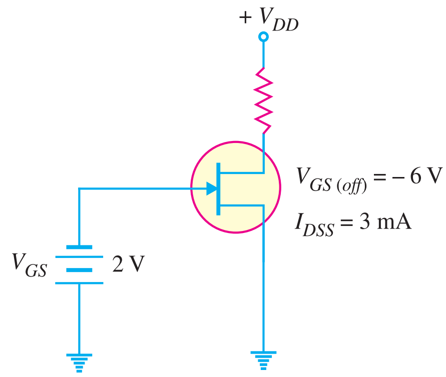


Fig. 19.16

Example 19.5. *Determine the value of drain current for the circuit shown in Fig. 19.16.*

Solution. It is clear from Fig. 19.16 that $V_{GS} = -2$V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3\text{ mA})\,(0.444) = \mathbf{1.33\ mA}$$

Example 19.6. *A particular p-channel JFET has a $V_{GS\,(off)} = +4$V. What is I_D when $V_{GS} = +6$V?*

Solution. The *p*-channel *JFET* requires a positive gate-to-source voltage to pass drain current I_D. The more the positive voltage, the less the drain current. When $V_{GS} = 4$V, $I_D = 0$ and *JFET* is cut off. Any further increase in V_{GS} keeps the *JFET* cut off. Therefore, at $V_{GS} = +6$V, $I_D =$ **0A.**

19.12 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(i) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(ii) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(iii) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(iv) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(v) A *JFET* has a smaller size, longer life and high efficiency.

19.13 Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are *(i)* a.c. drain resistance *(ii)* transconductance *(iii)* amplification factor.

***(i)* a.c. drain resistance (r_d).** Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then,

$$\text{a.c. drain resistance, } r_d = \frac{2\text{ V}}{0.02\text{ mA}} = 100\text{ k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 19.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) Transconductance (g_{fs}). The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage i.e.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} = 3 \times 10^{-3}\text{ A/V or mho or } S \text{ (siemens)}$$

$$= 3 \times 10^{-3} \times 10^{6}\ \mu\text{ mho} = 3000\ \mu\text{ mho (or } \mu\text{S)}$$

(*iii*) Amplification factor (μ). *It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

19.14 Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 19.7. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is 10^{-3} μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15\text{ V}\ ;\ I_G = 10^{-3}\ \mu\text{A} = 10^{-9}\text{ A}$

∴ Gate to source resistance $= \dfrac{V_{GS}}{I_G} = \dfrac{15\text{ V}}{10^{-9}\text{ A}} = 15 \times 10^9\ \Omega =$ **15,000 MΩ**

This example shows the major difference between a *JFET* and a bipolar transistor. Whereas the input impedance of a *JFET* is several hundred MΩ, the input impedance of a bipolar transistor is only hundreds or thousands of ohms. The large input impedance of a *JFET* permits high degree of isolation between the input and output.

Example 19.8. *When V_{GS} of a JFET changes from –3.1 V to –3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance ?*

Solution. $\Delta V_{GS} = 3.1 - 3 = 0.1\text{ V}$ ... magnitude

$\Delta I_D = 1.3 - 1 = 0.3\text{ mA}$

∴ Transconductance, $g_{fs} = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3\text{ mA}}{0.1\text{ V}} = 3\text{ mA/V} =$ **3000 μ mho**

Example 19.9. *The following readings were obtained experimentally from a JFET :*

V_{GS}	*0 V*	*0 V*	*– 0.2 V*
V_{DS}	*7 V*	*15 V*	*15 V*
I_D	*10 mA*	*10.25 mA*	*9.65 mA*

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor.

Solution. ***(i)*** With V_{GS} constant at 0V, the increase in V_{DS} from 7 V to 15 V increases the drain current from 10 mA to 10.25 mA *i.e.*

Change in drain-source voltage, $\Delta V_{DS} = 15 - 7 = 8\text{ V}$

Change in drain current, $\Delta I_D = 10.25 - 10 = 0.25\text{ mA}$

∴ a.c. drain resistance, $r_d = \dfrac{\Delta V_{DS}}{\Delta I_D} = \dfrac{8\text{ V}}{0.25\text{ mA}} =$ **32 kΩ**

(ii) With V_{DS} constant at 15 V, drain current changes from 10.25 mA to 9.65 mA as V_{GS} is changed from 0 V to – 0.2 V.

$\Delta V_{GS} = 0.2 - 0 = 0.2\text{ V}$

$\Delta I_D = 10.25 - 9.65 = 0.6\text{ mA}$

∴ Transconductance, $g_{fs} = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.6\text{ mA}}{0.2\text{ V}} = 3\text{ mA/V} =$ **3000 μ mho**

(iii) Amplification factor, $\mu = r_d \times g_{fs} = (32 \times 10^3) \times (3000 \times 10^{-6}) =$ **96**

19.15 Variation of Transconductance (g_m or g_{fs}) of JFET

We have seen that transconductance g_m of a *JFET* is the ratio of a change in drain current (ΔI_D) to a change in gate-source voltage (ΔV_{GS}) at constant V_{DS} *i.e.*

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

The transconductance g_m of a *JFET* is an important parameter because it is a major factor in determining the voltage gain of *JFET* amplifiers. However, the transfer characteristic curve for a *JFET* is nonlinear so that the value of g_m depends upon the location on the curve. Thus the value of g_m at point *A* in Fig. 19.17 will be different from that at point *B*. Luckily, there is following equation to determine the value of g_m at a specified value of V_{GS} :

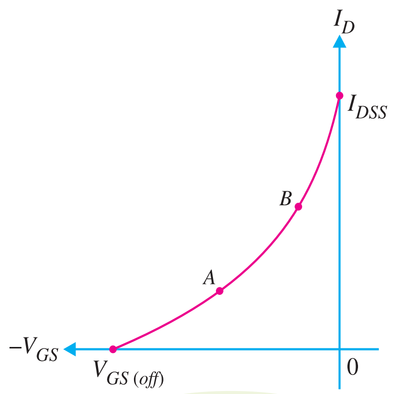


Fig. 19.17

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

where g_m = value of transconductance at any point on the transfer characteristic curve

g_{mo} = value of transconductance(maximum) at $V_{GS} = 0$

Normally, the data sheet provides the value of g_{mo}. When the value of g_{mo} is not available, you can approximately calculate g_{mo} using the following relation :

$$g_{mo} = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|}$$

Example 19.10. *A JFET has a value of g_{mo} = 4000 μS. Determine the value of g_m at V_{GS} = – 3V. Given that $V_{GS\,(off)}$ = – 8V.*

Solution.

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= 4000\ \mu S\left(1-\frac{-3V}{-8V}\right)$$

$$= 4000\ \mu S\ (0.625) = \mathbf{2500\ \mu S}$$

Example 19.11. *The data sheet of a JFET gives the following information : I_{DSS} = 3 mA, $V_{GS\,(off)}$ = – 6V and $g_{m\,(max)}$ = 5000 μS. Determine the transconductance for V_{GS} = – 4V and find drain current I_D at this point.*

Solution. At $V_{GS} = 0$, the value of g_m is maximum *i.e.* g_{mo}.

∴ g_{mo} = 5000 μS

Now

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= 5000\ \mu S\left(1-\frac{-4V}{-6V}\right)$$

$$= 5000\ \mu S\ (1/3) = \mathbf{1667\ \mu S}$$

Also

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\ mA\left(1-\frac{-4}{-6}\right)^2 = \mathbf{333\ \mu A}$$

19.16 JFET Biasing

For the proper operation of *n*-channel *JFET*, gate must be negative *w.r.t.* source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery. In this method, *JFET* is biased by a bias battery V_{GG}. This battery ensures that gate is always negative *w.r.t.* source during all parts of the signal.

2. Biasing circuit. The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are (*i*) self-bias (*ii*) potential divider method. We shall discuss each method in turn.

19.17 JFET Biasing by Bias Battery

Fig. 19.18 shows the biasing of a *n*-channel *JFET* by a bias battery $-V_{GG}$. This method is also called *gate bias.* The battery voltage $-V_{GG}$ ensures that gate – source junction remains reverse biased.

Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \quad V_{GS} = V_{GG}$$

We can find the value of drain current I_D from the following relation :

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

The value of V_{DS} is given by ;

$$V_{DS} = V_{DD} - I_D\,R_D$$

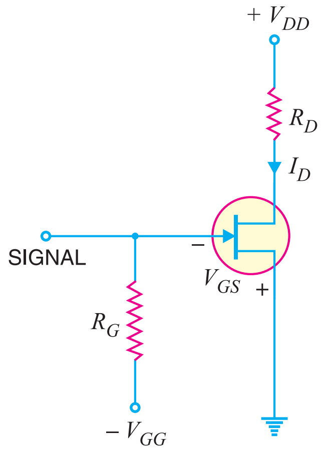


Fig. 19.18

Thus the d.c. values of I_D and V_{DS} stand determined. The operating point for the circuit is V_{DS}, I_D.

Example 19.12. *A JFET in Fig. 19.19 has values of $V_{GS\,(off)}$ = – 8V and I_{DSS} = 16 mA. Determine the values of V_{GS}, I_D and V_{DS} for the circuit.*

Solution. Since there is no gate current, there will be no voltage drop across R_G.

$$\therefore \quad V_{GS} = V_{GG} = \mathbf{-5V}$$

Now
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 16\text{ mA}\left(1-\frac{-5}{-8}\right)^2$$

$$= 16\text{ mA }(0.1406) = \mathbf{2.25\ mA}$$

Also
$$V_{DS} = V_{DD} - I_D\,R_D$$

$$= 10\text{ V} - 2.25\text{ mA} \times 2.2\text{ k}\Omega = \mathbf{5.05\ V}$$

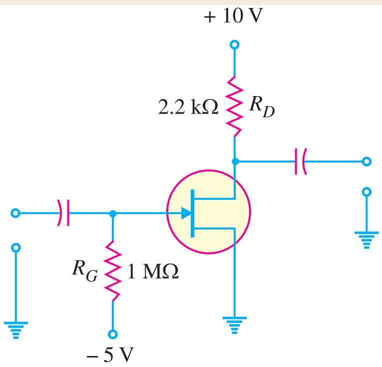


Fig. 19.19

Note that operating point for the circuit is 5.05V, 2.25 mA.

19.18 Self-Bias for JFET

Fig. 19.20 shows the self-bias method for *n*-channel *JFET*. The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage.

$$\text{Voltage across } R_S,\ V_S = I_D\,R_S$$

Since gate current is negligibly small, the gate terminal is at d.c. ground *i.e.*, $V_G = 0$.

$$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S$$

or
$$V_{GS} = -{}^{*}I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative *w.r.t.* source.

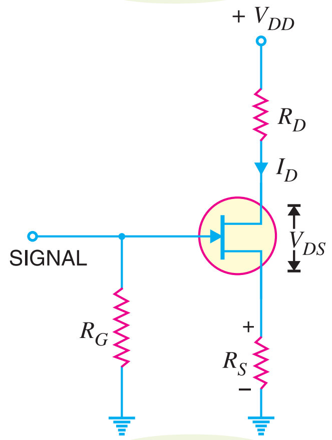


Fig. 19.20

* $V_{GS} = V_G - V_S$ = Negative. This means that V_G is negative w.r.t. V_S. Thus if V_G = 2V and V_S = 4V, then V_{GS} = 2 – 4 = – 2V *i.e.* gate is less positive than the source. Again if V_G = 0V and V_S = 2V, then V_{GS} = 0 – 2 = – 2V. Note that V_G is less positive than V_S.

Operating point. The operating point (*i.e.*, zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the *JFET* are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Also $$V_{DS} = V_{DD} - I_D\,(R_D + R_S)$$

Thus d.c. conditions of *JFET* amplifier are fully specified *i.e.* operating point for the circuit is V_{DS}, I_D.

Also, $$R_S = \frac{|V_{GS}|}{|I_D|}$$

Note that gate resistor *R_G does not affect bias because voltage across it is zero.

Midpoint Bias. It is often desirable to bias a *JFET* near the midpoint of its transfer characteristic curve where $I_D = I_{DSS}/2$. When signal is applied, the midpoint bias allows a maximum amount of drain current swing between I_{DSS} and 0. It can be proved that when $V_{GS} = V_{GS\,(off)}/\,3.4$, midpoint bias conditions are obtained for I_D.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = I_{DSS}\left(1 - \frac{V_{GS\,(off)}/3.4}{V_{GS\,(off)}}\right)^2 = 0.5\ I_{DSS}$$

To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

Example 19.13. *Find V_{DS} and V_{GS} in Fig. 19.21, given that I_D = 5 mA.*

Solution.

$$V_S = I_D\,R_S = (5\text{ mA})\,(470\ \Omega) = 2.35\text{ V}$$

and $$V_D = V_{DD} - I_D\,R_D$$
$$= 15\text{V} - (5\text{ mA}) \times (1\text{ k}\Omega) = 10\text{V}$$

$\therefore$ $$V_{DS} = V_D - V_S = 10\text{V} - 2.35\text{ V} = \mathbf{7.65V}$$

Since there is no gate current, there will be no voltage drop across R_G and $V_G = 0$.

Now $$V_{GS} = V_G - V_S = 0 - 2.35\text{V} = \mathbf{-\,2.35\ V}$$

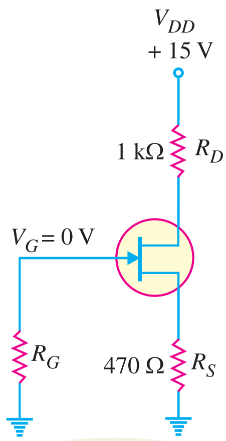


Fig. 19.21

Example 19.14. *The transfer characteristic of a JFET reveals that when V_{GS} = – 5V, I_D = 6.25 mA. Determine the value of R_S required.*

Solution.

$$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{6.25\text{ mA}} = \mathbf{800\ \Omega}$$

Example 19.15. *Determine the value of R_S required to self-bias a p-channel JFET with I_{DSS} = 25 mA, $V_{GS\,(off)}$ = 15 V and V_{GS} = 5V.*

Solution.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2 = 25\text{ mA}\left(1 - \frac{5\text{ V}}{15\text{ V}}\right)^2 = 25\text{mA}\ \ (1 - 0.333)^2 = 11.1\text{ mA}$$

$\therefore$ $$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{5\text{V}}{11.1\text{ mA}} = \mathbf{450\ \Omega}$$

* R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.

Example 19.16. *Select resistor values in Fig. 19.22 to set up an approximate midpoint bias. The JFET parameters are : I_{DSS} = 15 mA and $V_{GS\,(off)}$ = – 8V. The voltage V_D should be 6V (one-half of V_{DD}).*

Solution. For midpoint bias, we have,

$$I_D \simeq \frac{I_{DSS}}{2} = \frac{15\text{ mA}}{2} = 7.5\text{ mA}$$

and $$V_{GS} = \frac{V_{GS\,(off)}}{3.4} = \frac{-8}{3.4} = -2.35\text{ V}$$

$\therefore$ $$R_S = \frac{|V_{GS}|}{|I_D|} = \frac{2.35\text{V}}{7.5\text{ mA}} = \mathbf{313\Omega}$$

Now $$V_D = V_{DD} - I_D R_D$$

$\therefore$ $$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{12\text{V} - 6\text{V}}{7.5\text{ mA}} = \mathbf{800\Omega}$$

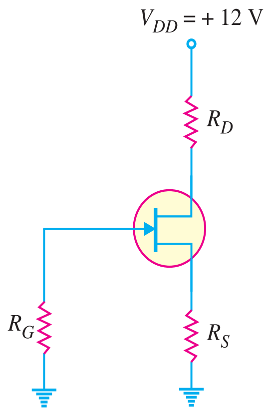


Fig. 19.22

Example 19.17. *In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5 mA and V_{DS} =10 V. The JFET parameters are I_{DSS} = 5 mA and $V_{GS\,(off)}$ = – 2 V. Find the values of R_S and R_D. Given that V_{DD} = 20 V.*

Solution. Fig. 19.23 shows the circuit arrangement.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or $$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

or $$1 + \frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55$$

or $$V_{GS} = -0.9\text{ V}$$

Now $$V_{GS} = V_G - V_S$$

or $$V_S = V_G - V_{GS} = 0 - (-0.9) = 0.9\text{ V}$$

$\therefore$ $$R_S = \frac{V_S}{I_D} = \frac{0.9\text{ V}}{1.5\text{ mA}} = \mathbf{0.6\ k\,\Omega}$$

Applying Kirchhoff's voltage law to the drain circuit, we have,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or $$20 = 1.5\text{ mA} \times R_D + 10 + 0.9$$

$\therefore$ $$R_D = \frac{(20 - 10 - 0.9)\text{ V}}{1.5\text{ mA}} = \mathbf{6\ k\,\Omega}$$

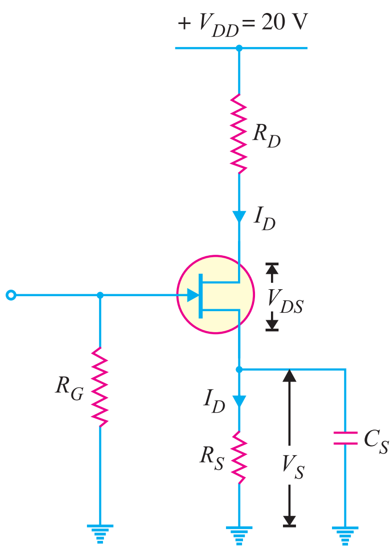


Fig. 19.23

Example 19.18. *In the JFET circuit shown in Fig. 19.24, find (i) V_{DS} and (ii) V_{GS} .*

Solution.

(i) $$V_{DS} = V_{DD} - I_D(R_D + R_S) = 30 - 2.5\text{ mA}\,(5 + 0.2) = 30 - 13 = \mathbf{17\ V}$$

(ii) $$V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = \mathbf{-0.5\ V}$$

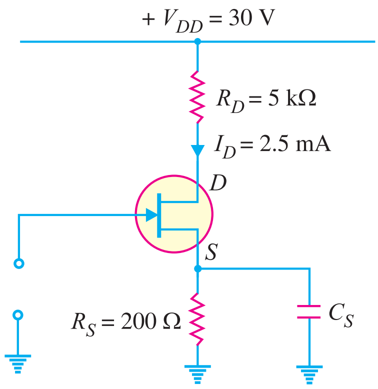


Fig. 19.24

Example 19.19. *Figure 19.25 shows two stages of JFET amplifier. The first stage has I_D = 2.15mA and the second stage has I_D = 9.15mA. Find the d.c. voltage of drain and source of each stage w.r.t. ground.*

Solution. Voltage drop in 8.2 kΩ = 2.15 mA × 8.2 kΩ = 17.63 V

D.C. potential of drain of first stage *w.r.t.* ground is

$$V_D = V_{DD} - 17.63 = 30 - 17.63 = \mathbf{12.37\ V}$$

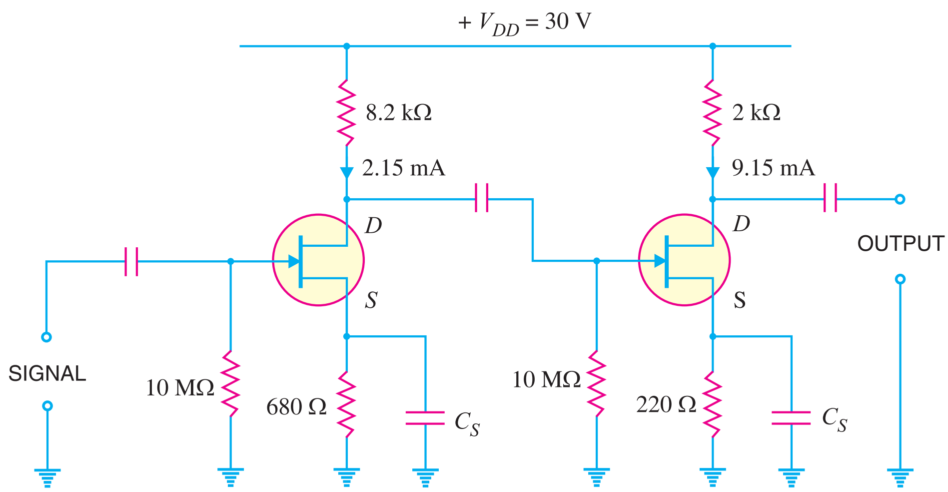


Fig. 19.25

D.C. potential of source of first stage to ground is

$$V_S = I_D R_S = 2.15\text{ mA} \times 0.68\text{ k}\Omega = \mathbf{1.46\ V}$$

Voltage drop in 2 kΩ = 9.15 mA × 2 kΩ = 18.3 V

D.C. potential of drain of second stage to ground is

$$V_D = V_{DD} - 18.3 = 30 - 18.3 = \mathbf{11.7\ V}$$

D.C. potential of source of second stage to ground is

$$V_S = I_D R_S = 9.15 \text{ mA} \times 0.22 \text{ k}\Omega = \mathbf{2.01 \text{ V}}$$

19.19 JFET with Voltage-Divider Bias

Fig. 19.26 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 (= V_G)across R_2 provides the necessary bias.

$$V_2 = V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $\quad V_2 = V_{GS} + I_D R_S$

or $\quad V_{GS} = V_2 - I_D R_S$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under :

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $\quad V_{DS} = V_{DD} - I_D (R_D + R_S)$

Although the circuit of voltage-divider bias is a bit complex, yet the advantage of this method of biasing is that it provides good stability of the operating point. The input impedance Z_i of this circuit is given by ;

$$Z_i = R_1 \parallel R_2$$

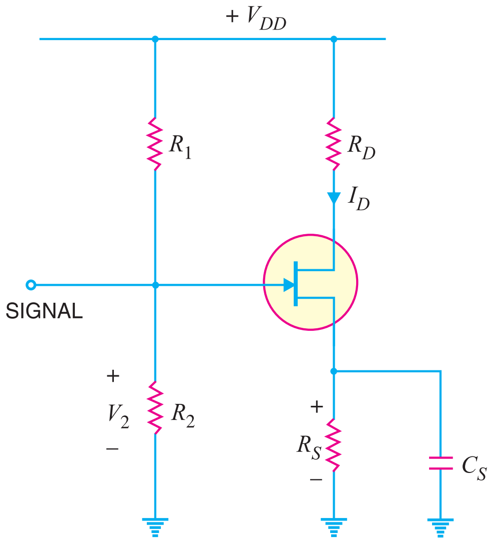


Fig. 19.26

Example 19.20. *Determine I_D and V_{GS} for the JFET with voltage-divider bias in Fig. 19.27, given that V_D = 7V.*

Solution.

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{V} - 7\text{V}}{3.3 \text{ k}\Omega}$$

$$= \frac{5\text{V}}{3.3 \text{ k}\Omega} = \mathbf{1.52 \text{ mA}}$$

$$V_S = I_D R_S = (1.52 \text{ mA}) (1.8 \text{ k}\Omega) = 2.74\text{V}$$

$$V_G = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{12\text{V}}{7.8 \text{ M}\Omega} \times 1 \text{ M}\Omega = 1.54\text{V}$$

$$\therefore \quad V_{GS} = V_G - V_S = 1.54 \text{ V} - 2.74 \text{ V} = \mathbf{-1.2V}$$

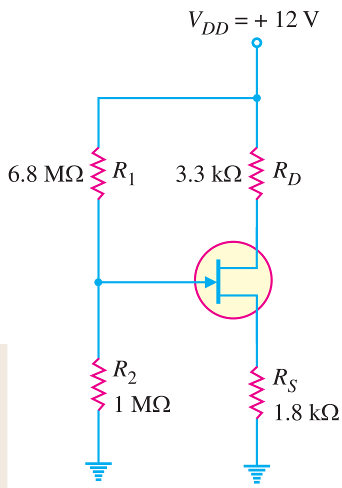


Fig. 19.27

Example 19.21. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at I_D = 2.5 mA and V_{DS} = 8V. If V_{DD} = 30 V, R_1 = 1 MΩ and R_2 = 500 kΩ, find the value of R_S. The parameters of JFET are I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 5 V.*

Solution. Fig. 19.28 shows the conditions of the problem.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

or $$2.5 = 10\left(1 + \frac{V_{GS}}{5}\right)^2$$

or $$1 + \frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

or $$V_{GS} = -\,2.5 \text{ V}$$

Now, $$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{30}{1000 + 500} \times 500$$

$$= 10 \text{ V}$$

Now $$V_2 = V_{GS} + I_D R_S$$

or $$10 \text{ V} = -\,2.5 \text{ V} + 2.5 \text{ mA} \times R_S$$

$$\therefore \quad R_S = \frac{10 \text{ V} + 2.5 \text{ V}}{2.5 \text{ mA}} = \frac{12.5 \text{ V}}{2.5 \text{ mA}}$$

$$= \mathbf{5\ k\Omega}$$

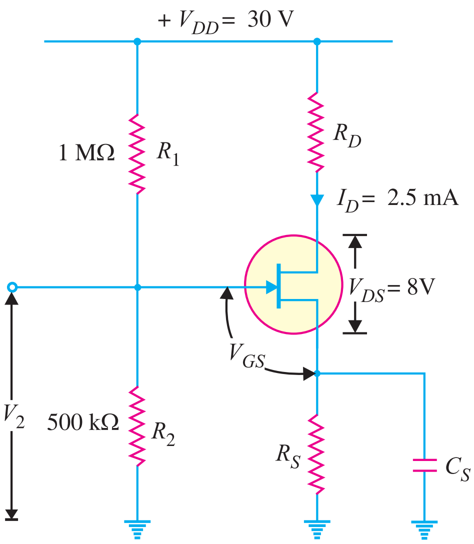


Fig. 19.28

19.20 JFET Connections

There are three leads in a *JFET viz*., source, gate and drain terminals. However, when *JFET* is to be connected in a circuit, we require four terminals ; two for the input and two for the output. This difficulty is overcome by making one terminal of the *JFET* common to both input and output terminals. Accordingly, a *JFET* can be connected in a circuit in the following three ways :

(i) Common source connection ***(ii)*** Common gate connection

(iii) Common drain connection

The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal *i.e.*, output signal is 180° out of phase with the input signal. Fig. 19.29 shows a common source *n*-channel *JFET* amplifier. Note that source terminal is common to both input and output.

Note. A common source *JFET* amplifier is the *JFET* equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

19.21 Practical JFET Amplifier

It is important to note that a *JFET* can accomplish faithful amplification only if proper associated circuitry is used. Fig. 19.29 shows the practical circuit of a *JFET*. The gate resistor R_G serves two purposes. It keeps the gate at approximately 0 V dc (∵ gate current is nearly zero) and its large value (usually several megaohms) prevents loading of the a.c. signal source. The bias voltage is created by the drop across R_S. The bypass capacitor C_S bypasses the a.c. signal and thus keeps the source of the *JFET* effectively at a.c. ground. The coupling capacitor C_{in} couples the signal to the input of *JFET* amplifier.

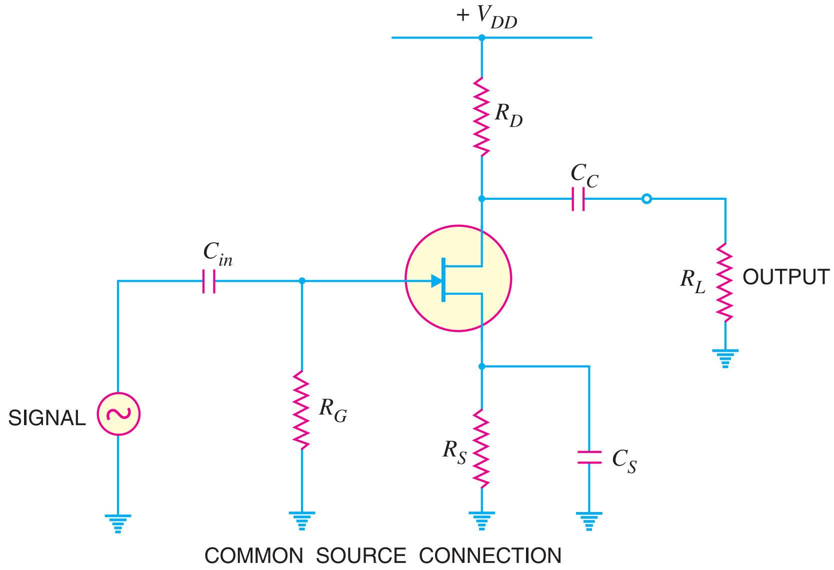


Fig. 19.29

19.22 D.C. and A.C. Equivalent Circuits of JFET

Like in a transistor amplifier, both d.c. and a.c. conditions prevail in a *JFET* amplifier. The d.c. sources set up d.c. currents and voltages whereas the a.c. source (*i.e.* signal) produces fluctuations in the *JFET* currents and voltages. Therefore, a simple way to analyse the action of a *JFET* amplifier is to split the circuit into two parts *viz. d.c. equivalent circuit* and *a.c. equivalent circuit.* The d.c. equivalent circuit will determine the operating point (d.c. bias levels) for the circuit while a.c. equivalent circuit determines the output voltage and hence voltage gain of the circuit.

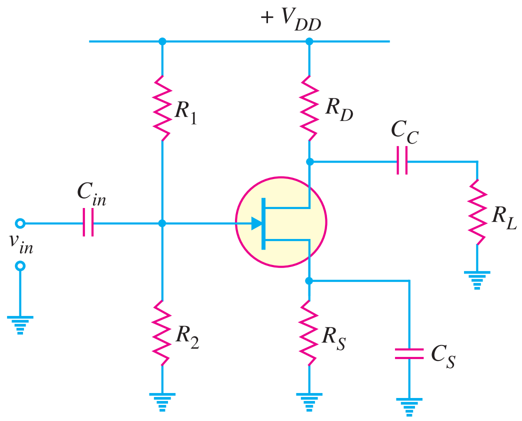


Fig. 19.30

We shall split the *JFET* amplifier shown in Fig. 19.30 into d.c. and a.c. equivalent circuits. Note that biasing is provided by voltage-divider circuit.

1. **D. C. equivalent circuit.** In the d.c. equivalent circuit of a *JFET* amplifier, only d.c. conditions are considered *i.e.* it is presumed that no signal is applied. As direct current cannot

flow through a capacitor, *all the capacitors look like open circuits in the d.c. equivalent circuit.* It follows, therefore, that in order to draw the d.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all a.c. sources to zero.

(*ii*) Open all the capacitors.

Applying these two steps to the *JFET* amplifier circuit shown in Fig. 19.30, we get the d.c. equivalent circuit shown in Fig. 19.31. We can easily calculate the d.c. currents and voltages from this circuit.

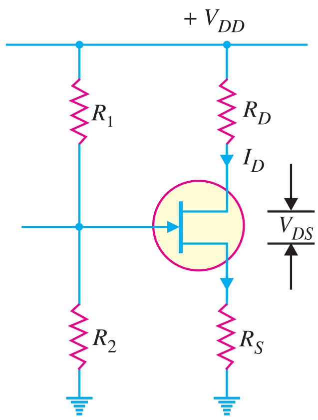


Fig. 19.31

2. A. C. equivalent circuit. In the a.c. equivalent circuit of a *JFET* amplifier, only a.c. conditions are to be considered. Obviously, the d.c. voltage is not important for such a circuit and may be considered zero. The capacitors are generally used to couple or bypass the a.c. signal. The designer intentionally selects capacitors that are large enough to appear as *short circuits* to the a.c. signal. It follows, therefore, that in order to draw the a.c. equivalent circuit, the following two steps are applied to the *JFET* amplifier circuit :

(*i*) Reduce all d.c. sources to zero (*i.e.* $V_{DD} = 0$).

(*ii*) Short all the capacitors.

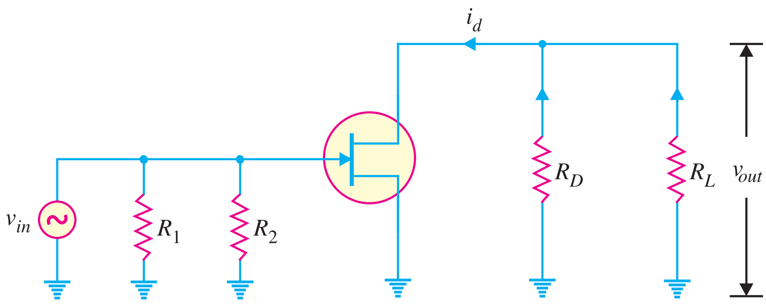


Fig. 19.32

Applying these two steps to the circuit shown in Fig. 19.30, we get the a.c. *equivalent circuit shown in Fig. 19.32. We can easily calculate the a.c. currents and voltages from this circuit.

19.23 D.C. Load Line Analysis

The operating point of a *JFET* amplifier can be determined graphically by drawing d.c. load line on the drain characteristics ($V_{DS} - I_D$ curves). This method is identical to that used for transistors.

The d.c. equivalent circuit of a *JFET* amplifier using voltage-divider bias is shown in Fig. 19.33 (*i*). It is clear that :

$$V_{DD} = V_{DS} + I_D (R_D + R_S)$$

or

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \quad \text{... } (i)$$

* Note that one end of R_1 and R_2 is connected to one point (See Fig. 19.32) and the other end of R_1 and R_2 is connected to ground. Therefore, $R_1 \parallel R_2$. Similar is the case with R_D and R_L so that $R_D \parallel R_L$.

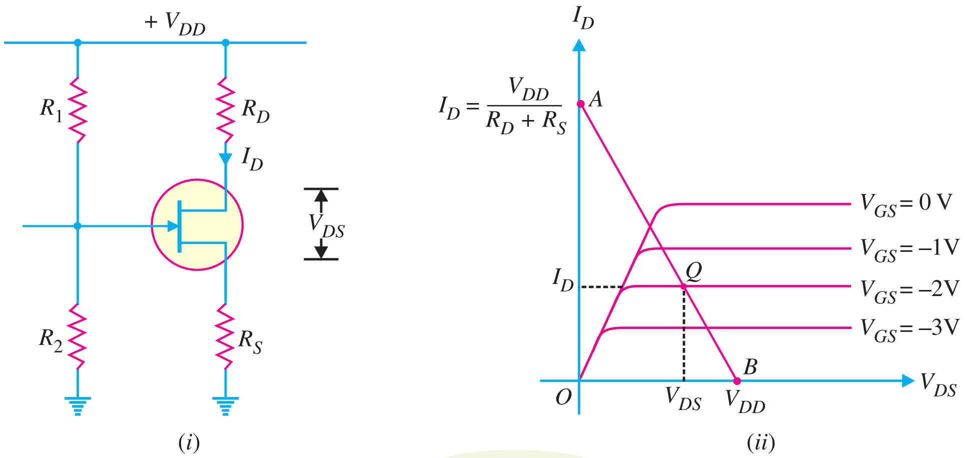


Fig. 19.33

As for a given circuit, V_{DD} and $(R_D + R_S)$ are constant, therefore, exp. (*i*) is a first degree equation and can be represented by a straight line on the drain characteristics. This is known as d.c. load line for *JFET* and determines the locus of I_D and V_{DS} (*i.e.* operating point) in the absence of the signal. The d.c. load line can be readily plotted by locating the *two end points* of the straight line.

(*i*) The value of V_{DS} will be maximum when $I_D = 0$. Therefore, by putting $I_D = 0$ in exp. (*i*) above, we get,

$$\text{Max. } V_{DS} = V_{DD}$$

This locates the first point *B* ($OB = V_{DD}$) of the d.c. load line on drain-source voltage axis.

(*ii*) The value of I_D will be maximum when $V_{DS} = 0$.

$$\therefore \quad \text{Max. } I_D = \frac{V_{DD}}{R_D + R_S}$$

This locates the second point *A* ($OA = V_{DD} / R_D + R_S$) of the d.c. load line on drain current axis.

By joining points *A* and *B*, d.c. load line *AB* is constructed [See Fig. 19.33 (*ii*)].

The operating point *Q* is located at the intersection of the d.c. load line and the drain curve which corresponds to V_{GS} provided by biasing. If we assume in Fig. 19.33 (*i*) that $V_{GS} = -2$V, then point *Q* is located at the intersection of the d.c. load line and the $V_{GS} = -2$V curve as shown in Fig. 19.33 (*ii*). The I_D and V_{DS} of *Q* point are marked on the graph.

Example 19.22. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.34 (i).*

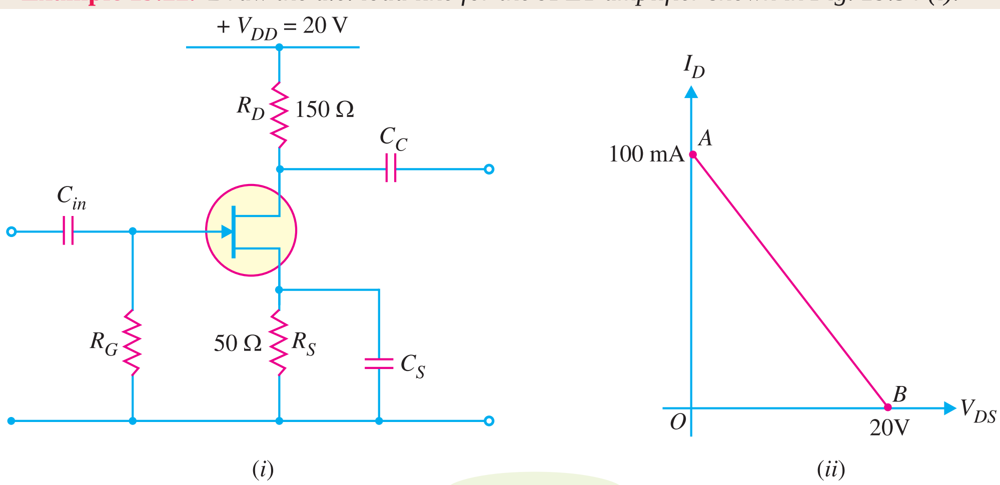


Fig. 19.34

Solution. To draw d.c. load line, we require two end points *viz.*, max V_{DS} and max. I_D points.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

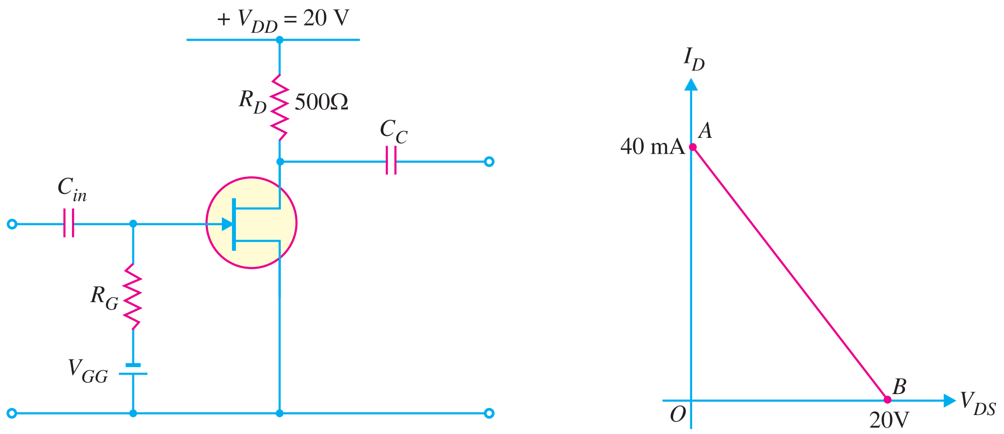
This locates point B (OB = 20V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D + R_S} = \frac{20\text{V}}{(150+50)\,\Omega}$$

$$= \frac{20\text{V}}{200\Omega} = 100 \text{ mA}$$

This locates point A (OA = 100 mA) of the d.c. load line. Joining A and B, d.c. load line AB is constructed as shown in Fig. 19.34 (*ii*).

Example 19.23. *Draw the d.c. load line for the JFET amplifier shown in Fig. 19.35 (i).*



(*i*) (*ii*)

Fig. 19.35

Solution.

$$\text{Max. } V_{DS} = V_{DD} = 20\text{V}$$

This locates the point B (OB = 20V) of the d.c. load line.

$$\text{Max. } I_D = \frac{V_{DD}}{R_D} = \frac{20\text{V}}{500\Omega} = 40 \text{ mA}$$

This locates the point A (OA = 40 mA) of the d.c. load line.

Fig. 19.35 (*ii*) shows the d.c. load line AB.

19.24 Voltage Gain of JFET Amplifier

The a.c. equivalent circuit of *JFET* amplifier was developed in Art. 19.22 and is redrawn as Fig. 19.36 (*i*) for facility of reference. Note that $R_1 \| R_2$ and can be replaced by a single resistance R_T. Similarly, $R_D \| R_L$ and can be replaced by a single resistance R_{AC} (= total a.c. drain resistance). The a.c. equivalent circuit shown in Fig. 19.36 (*i*) then reduces to the one shown in Fig. 19.36 (*ii*).

We now find the expression for voltage gain of this amplifier. Referring to Fig. 19.36 (*ii*), output voltage (v_{out}) is given by ;

$$v_{out} = i_d R_{AC} \qquad \text{... (i)}$$

Remember that we define g_m as :

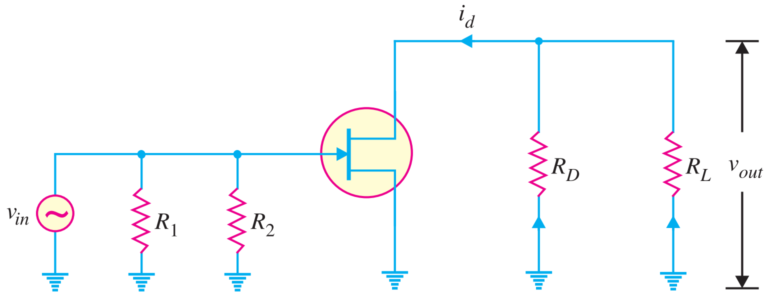


Fig. 19.36 (*i*)

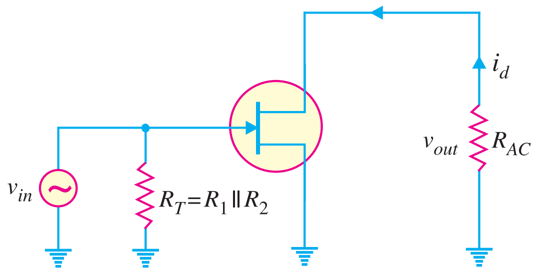


Fig. 19.36 (*ii*)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

or $$g_m = \frac{i_d}{v_{gs}}$$

or $$i_d = g_m v_{gs}$$

Putting the value of i_d (= $g_m v_{gs}$) in eq. (*i*), we have,

$$v_{out} = g_m v_{gs} R_{AC}$$

Now $v_{in} = v_{gs}$ so that a.c. output voltage is

$$v_{out} = g_m v_{in} R_{AC}$$

or $$v_{out}/v_{in} = g_m R_{AC}$$

But v_{out}/v_{in} is the voltage gain (A_v) of the amplifier.

$\therefore$ Voltage gain, $A_v = g_m R_{AC}$ ... for loaded amplifier

$= g_m R_D$ ... for unloaded amplifier

Example 19.24. *The JFET in the amplifier of Fig. 19.37 has a transconductance g_m = 1 mA/V. If the source resistance R_S is very small as compared to R_G, find the voltage gain of the amplifier.*

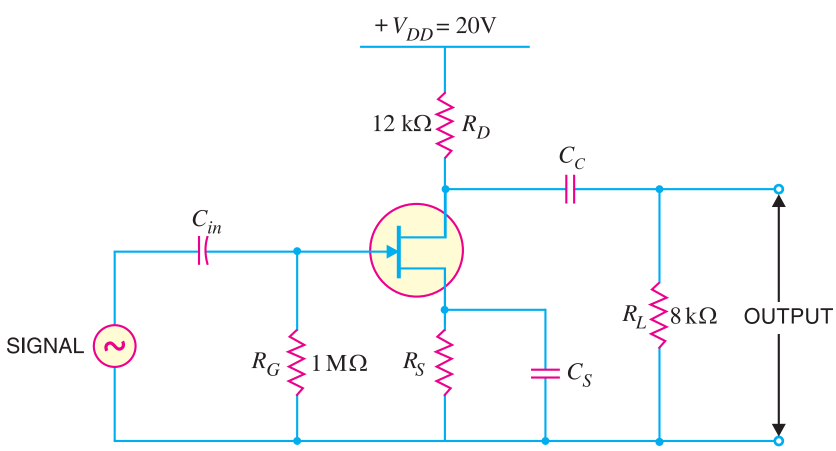


Fig. 19.37

Solution.

Transconductance of *JFET*, g_m = 1 mA/V

$$= 1000\ \mu\text{ mho} = 1000 \times 10^{-6}\text{ mho}$$

The total *ac* load (*i.e.* R_{AC}) in the drain circuit consists of the parallel combination of R_D and R_L *i.e.*

$$\text{Total a.c. load, } R_{AC} = R_D \parallel R_L$$

$$= 12\text{ k}\Omega \parallel 8\text{ k}\Omega = \frac{12 \times 8}{12 + 8} = 4.8\text{ k}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m \times R_{AC}$$

$$= (1000 \times 10^{-6}) \times (4.8 \times 10^{3}) = \mathbf{4.8}$$

Example 19.25. *The transconductance of a JFET used as a voltage amplifier is 3000 µmho and drain resistance is 10 kΩ. Calculate the voltage gain of the amplifier.*

Solution.

$$\text{Transconductance of JFET, } g_m = 3000\ \mu\text{mho} = 3000 \times 10^{-6}\text{ mho}$$

$$\text{Drain resistance, } R_D = 10\text{ k}\Omega = 10 \times 10^{3}\Omega$$

$$\therefore \quad \text{Voltage gain, } A_v = g_m R_D = (3000 \times 10^{-6})(10 \times 10^{3}) = \mathbf{30}$$

Example 19.26. *What is the r.m.s. output voltage of the unloaded amplifier in Fig. 19.38? The* I_{DSS} *= 8 mA,* $V_{GS\,(off)}$ *= – 10V and* I_D *= 1.9 mA.*

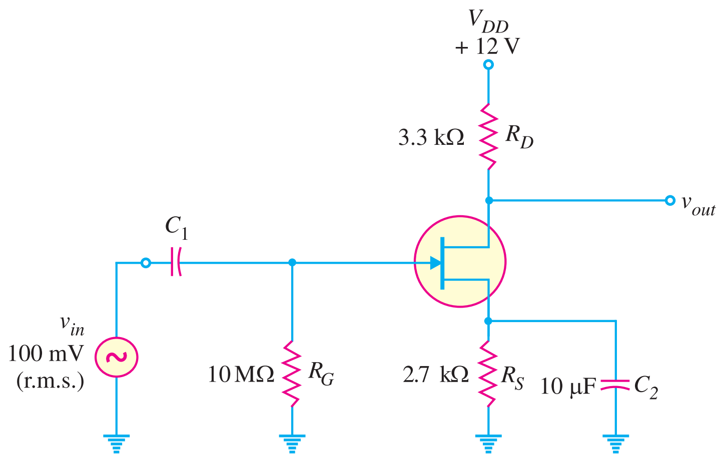


Fig. 19.38

Solution.

$$V_{GS} = -I_D R_S = -1.9\text{ mA} \times 2.7 \times 10^{3}\Omega = -5.13\text{V}$$

$$g_{mo} = \frac{2\, I_{DSS}}{|V_{GS\,(off)}|} = \frac{2 \times 8\text{ mA}}{10\text{ V}} = 1.6 \times 10^{-3}\text{S}$$

$$\therefore \quad g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right) = 1.6 \times 10^{-3}\left(1 - \frac{-5.13\text{V}}{-10\text{V}}\right) = 779 \times 10^{-6}\text{ S}$$

$$\text{Voltage gain, } A_v = g_m R_D = (779 \times 10^{-6})(3.3 \times 10^{3}) = 2.57$$

$$\therefore \quad \text{Output voltage, } v_{out} = A_v\, v_{in} = 2.57 \times 100\text{ mV} = \mathbf{257\text{ mV (r.m.s.)}}$$

Example 19.27. *If a 4.7 kΩ load resistor is a.c. coupled to the output of the amplifier in Fig. 19.38 above, what is the resulting r.m.s. output voltage?*

Solution. The value of g_m remains the same. However, the value of total a.c. drain resistance R_{AC} changes due to the connection of load R_L (= 4.7 kΩ).

$$\text{Total a.c. drain resistance, } R_{AC} = R_D \parallel R_L$$

$$= \frac{R_D R_L}{R_D + R_L} = \frac{(3.3 \text{ k}\Omega)(4.7 \text{ k}\Omega)}{3.3 \text{ k}\Omega + 4.7 \text{ k}\Omega} = 1.94 \text{ k}\Omega$$

$\therefore$ Voltage gain, $A_v = g_m R_{AC} = (779 \times 10^{-6})(1.94 \times 10^3) = 1.51$

Output voltage, $v_{out} = A_v v_{in} = 1.51 \times 100 \text{ mV} =$ **151 mV (r.m.s.)**

19.25 Voltage Gain of JFET Amplifier (*With Source Resistance R_S*)

Fig. 19.39 (*i*) shows the *JFET* amplifier with source resistor R_S unbypassed. This means that a.c. signal will not be bypassed by the capacitor C_S.

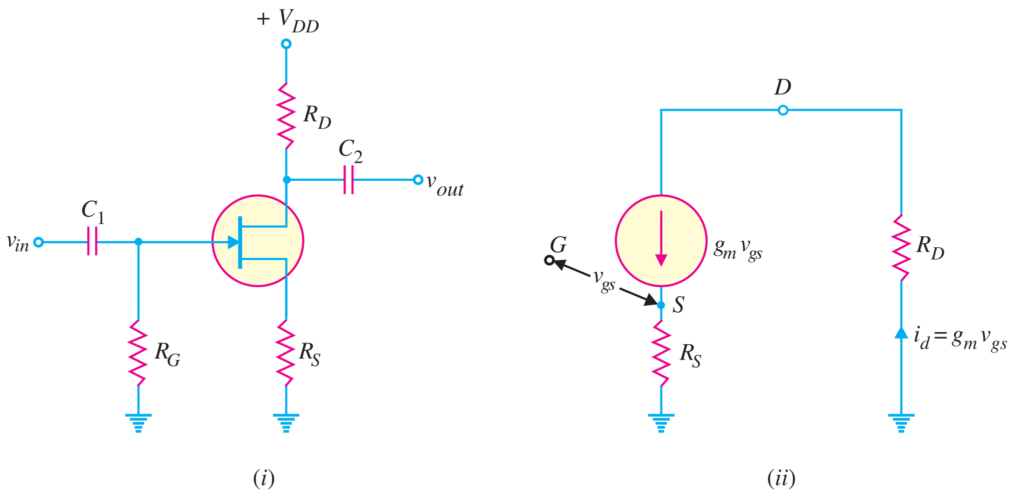


Fig. 19.39

Fig. 19.39 (*ii*) shows the simplified a.c. equivalent circuit of the *JFET* amplifier. Since $g_m = i_d/v_{gs}$, a current source $i_d = g_m v_{gs}$ appears between drain and source. Referring to Fig. 19.39 (*ii*),

$$v_{in} = v_{gs} + i_d R_S$$

$$v_{out} = i_d R_D$$

$\therefore$ Voltage gain, $$A_v = \frac{v_{out}}{v_{in}} = \frac{i_d R_D}{v_{gs} + i_d R_S}$$

$$= \frac{g_m v_{gs} R_D}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_D}{v_{gs}(1 + g_m R_S)} \qquad (\because i_d = g_m v_{gs})$$

$\therefore$ $$A_v = \frac{g_m R_D}{1 + g_m R_S} \quad \text{... for unloaded amplifier}$$

$$= \frac{g_m R_{AC}}{1 + g_m R_S} \quad \text{... for loaded amplifier}$$

Note that R_{AC} $(= R_D \,||\, R_L)$ is the total a.c. drain resistance.

Example 19.28. *In a JFET amplifier, the source resistance R_S is unbypassed. Find the voltage gain of the amplifier. Given g_m = 4 mS; R_D = 1.5 kΩ and R_S = 560Ω.*

Solution.

Voltage gain, $$A_v = \frac{g_m R_D}{1 + g_m R_S}$$

Here $g_m = 4\text{mS} = 4 \times 10^{-3}$ S ; $R_D = 1.5 \text{ k}\Omega = 1.5 \times 10^3 \Omega$; $R_S = 560\Omega$

$$\therefore \qquad A_v = \frac{(4\times10^{-3})(1.5\times10^{3})}{1+(4\times10^{-3})(560)} = \frac{6}{1+2.24} = \mathbf{1.85}$$

If R_S is bypassed by a capacitor, then,

$$A_v = g_m R_D = (4 \times 10^{-3})(1.5 \times 10^{3}) = 6$$

Thus with unbypassed R_S, the gain = 1.85 whereas with R_S bypassed by a capacitor, the gain is 6. Therefore, voltage gain is reduced when R_S is unbypassed.

Example 19.29. *For the JFET amplifier circuit shown in Fig. 19.40, calculate the voltage gain with (i) R_S bypassed by a capacitor (ii) R_S unbypassed.*

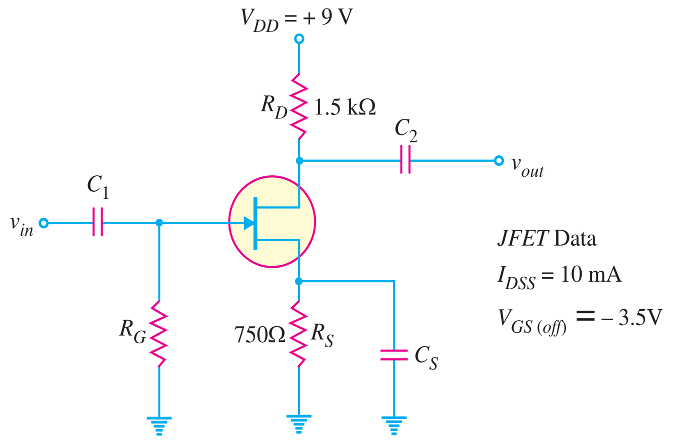


Fig. 19.40

Solution. From the d.c. bias analysis, we get, *I_D = 2.3 mA and V_{GS} = – 1.8V.

The value of g_m is given by;

$$g_m = \frac{2\,I_{DSS}}{|V_{GS\,(off)}|}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

$$= \frac{2\times10}{3.5}\left(1-\frac{-1.8}{-3.5}\right) = (5.7 \text{ mS})\,(0.486) = 2.77 \text{ mS}$$

(*i*) The voltage gain with R_S bypassed is

$$A_v = g_m R_D = (2.77 \text{ mS})\,(1.5 \text{ k}\Omega) = \mathbf{4.155}$$

(*ii*) The voltage gain with R_S unbypassed is

$$A_v = \frac{g_m R_D}{1+g_m R_S} = \frac{4.155}{1+(2.77 \text{ mS})\,(0.75 \text{ k}\Omega)} = \mathbf{1.35}$$

19.26 JFET Applications

The high input impedance and low output impedance and low noise level make *JFET* far superior to the bipolar transistor. Some of the circuit applications of *JFET* are :

* $$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2 \text{ and } V_{GS} = -\,I_D R_S$$

The unknown quantities V_{GS} and I_D can be found from these two equations.

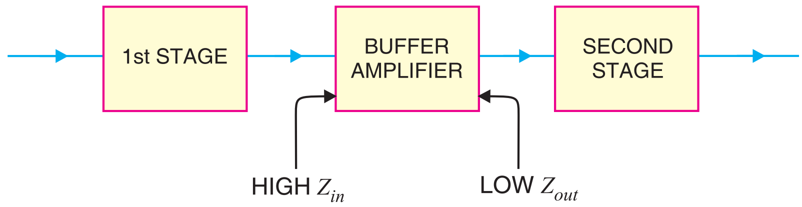


Fig. 19.41

(*i*) As a buffer amplifier. A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance, a *JFET* can act as an excellent buffer amplifier (See Fig. 19.41). The high input impedance of *JFET* means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the buffer input. The low output impedance of *JFET* can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.

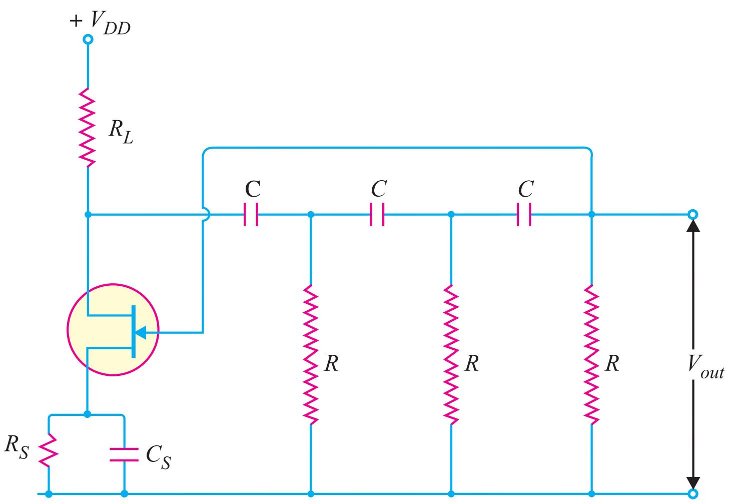


Fig. 19.42

(*ii*) Phase-shift oscillators. The oscillators discussed in chapter 14 will also work with *JFETs*. However, the high input impedance of *JFET* is especially valuable in phase-shift oscillators to minimise the loading effect. Fig. 19.42 shows the phase-shift oscillator using *n*-channel *JFET*.

(*iii*) As RF amplifier. In communication electronics, we have to use *JFET RF* amplifier in a receiver instead of *BJT* amplifier for the following reasons :

(*a*) The noise level of *JFET* is very low. The *JFET* will not generate significant amount of noise and is thus useful as an *RF* amplifier.

(*b*) The antenna of the receiver receives a very weak signal that has an extremely low amount of current. Since *JFET* is a voltage controlled device, it will well respond to low current signal provided by the antenna.

19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as ***depletion-mode* operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

*A field effect transistor (FET) that can be operated in the enhancement-mode is called a **MOSFET**.*

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.
2. Enhancement-type *MOSFET* or ***E-MOSFET*.** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons ($\because$ it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

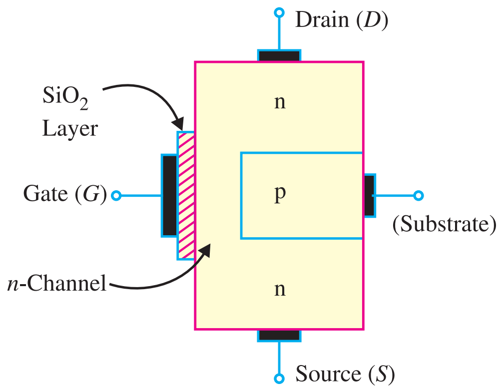
(ii) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

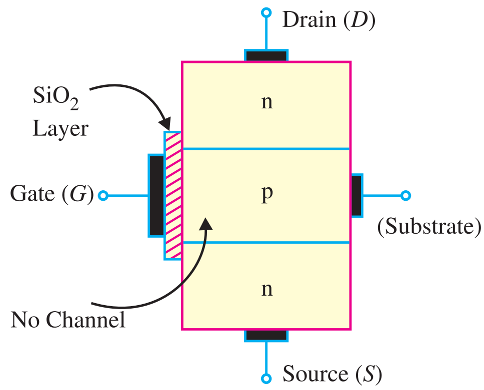
* With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.

** With gate reverse biased, the channel is depleted (*i.e.* emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.



n-Channel D-MOSFET

Fig. 19.43



n-Channel E-MOSFET

Fig. 19.44

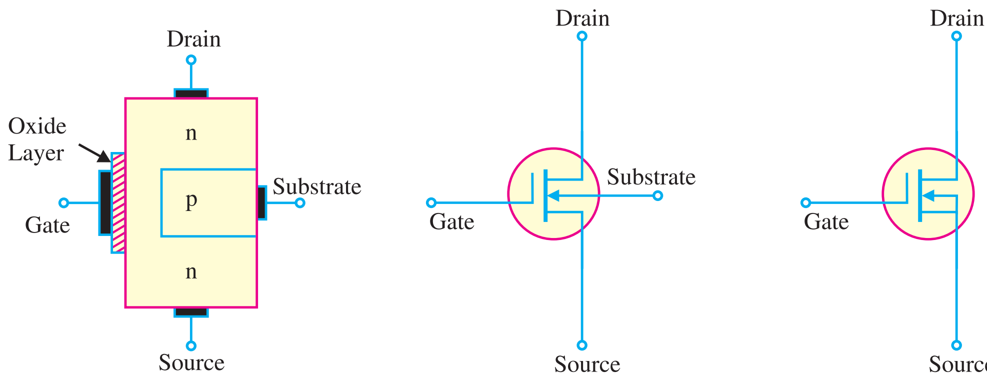
2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET.* Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET.* Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET).* However, this term is rarely used in place of the term *MOSFET*.

19.29 Symbols for D-MOSFET

There are two types of *D-MOSFETs viz (i) n*-channel *D-MOSFET* and *(ii) p*-channel *D-MOSFET*.

(*i*) n-channel D-MOSFET. Fig. 19.45 (*i*) shows the various parts of *n*-channel *D-MOSFET*. The *p*-type substrate constricts the channel between the source and drain so that only a small passage



n-Channel D-MOSFET
(*i*)

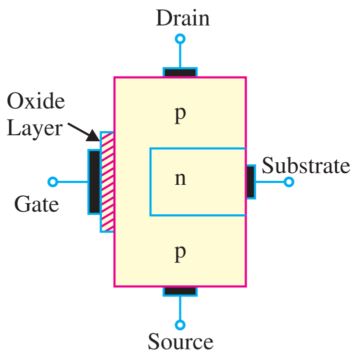
Symbol
(*ii*)

Symbol
(*iii*)

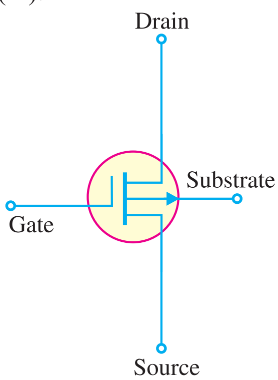
Fig. 19.45

remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel *D-MOSFET* is shown in Fig. 19.45 (*ii*). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel *D-MOSFET*. It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (*iii*). This gives rise to a three-terminal device.

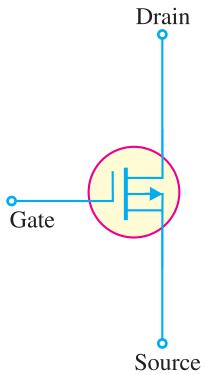
(*ii*) *p*-channel D-MOSFET. Fig. 19.46 (*i*) shows the various parts of *p*-channel *D-MOSFET*. The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel *D-MOSFET* is shown in Fig. 19.46 (*ii*). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (*iii*).



p-Channel D-MOSFET
(*i*)



Symbol
(*ii*)



Symbol
(*iii*)

Fig. 19.46

19.30 Circuit Operation of D-MOSFET

Fig. 19.47 (*i*) shows the circuit of *n*-channel *D-MOSFET*. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive-gate operation is known as *enhancement mode.*

(*i*) Depletion mode. Fig. 19.47 (*i*) shows depletion-mode operation of *n*-channel *D-MOSFET*. Since gate is negative, it means electrons are on the gate as shown is Fig. 19.47 (*ii*). These electrons *repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (*ii*). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of *D-MOSFET* is similar to *JFET*. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode.*

* If one plate of the capacitor is negatively charged, it induces positive charge on the other plate.

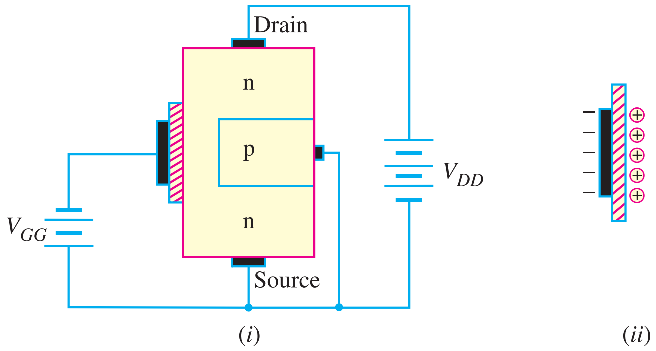


Fig. 19.47

(ii) Enhancement mode. Fig. 19.48 (*i*) shows enhancement-mode operation of *n*-channel *D-MOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (*ii*). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially *zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode.*

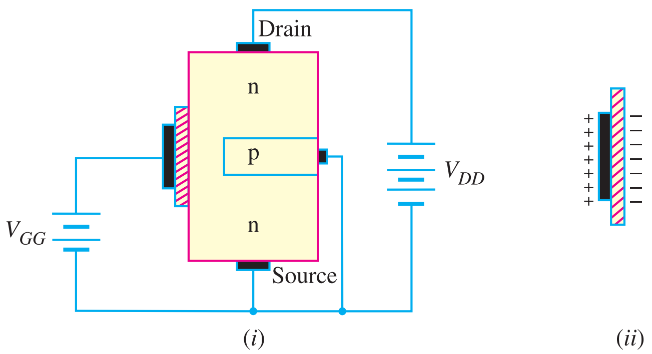


Fig. 19.48

The following points may be noted about *D-MOSFET* operation :

(i) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(ii) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(iii) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether

* Note that gate of *JFET* is always reverse biased for proper operation. However, in a *MOSFET*, because of the insulating layer, a negligible gate current flows whether we apply negative or positive voltage to gate.

positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.

(*iv*) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(*i*) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* $V_{GS} = 0$.

(*ii*) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS\,(off)}$ just as with *JFET*.

(*iii*) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

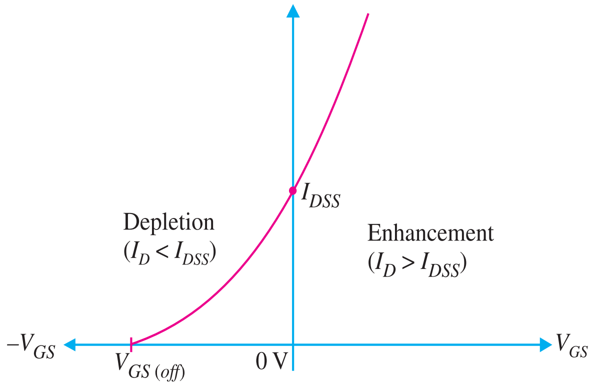


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation *viz.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Example 19.30. *For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS\,(off)}$ = – 8V.*

(*i*) *Is this an n-channel or a p-channel ?*

(*ii*) *Calculate I_D at V_{GS} = – 3V.*

(*iii*) *Calculate I_D at V_{GS} = + 3V.*

Solution.

(*i*) The device has a negative $V_{GS\,(off)}$. Therefore, it is ***n*-channel *D-MOSFET***.

(*ii*)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{-3}{-8}\right)^2 = \mathbf{3.91\ mA}$$

(iii)
$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$
$$= 10\text{ mA}\left(1-\frac{+3V}{-8V}\right)^2 = \mathbf{18.9\text{ mA}}$$

Example 19.31. *A D-MOSFET has parameters of $V_{GS\,(off)}$ = – 6V and I_{DSS} = 1 mA. How will you plot the transconductance curve for the device ?*

Solution. When V_{GS} = 0 V, $I_D = I_{DSS}$ = 1 mA and when $V_{GS} = V_{GS\,(off)}$, I_D = 0A. This locates two points *viz* I_{DSS} and $V_{GS\,(off)}$ on the transconductance curve. We can locate more points of the curve by *changing V_{GS} values.

When V_{GS} = – 3V ; $I_D = 1\text{ mA}\left(1-\dfrac{-3V}{-6V}\right)^2$ = 0.25 mA

When V_{GS} = – 1V ; $I_D = 1\text{ mA}\left(1-\dfrac{-1V}{-6V}\right)^2$ = 0.694 mA

When V_{GS} = + 1V ; $I_D = 1\text{ mA}\left(1-\dfrac{+1V}{-6V}\right)^2$ = 1.36 mA

When V_{GS} = + 3V ; $I_D = 1\text{ mA}\left(1-\dfrac{+3V}{-6V}\right)^2$ = 2.25 mA

Thus we have a number of $V_{GS} - I_D$ readings so that transconductance curve for the device can be readily plotted.

19.32 Transconductance and Input Impedance of D-MOSFET

These are important parameters of a *D-MOSFET* and a brief discussion on them is desirable.

***(i)* D-MOSFET Transconductance (g_m).** The value of g_m is found for a *D-MOSFET* in the same way that it is for the *JFET i.e.*

$$g_m = g_{mo}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)$$

***(ii)* D-MOSFET Input Impedance.** The gate impedance of a *D-MOSFET* is extremely high. For example, a typical *D-MOSFET* may have a maximum gate current of 10 pA when V_{GS} = 35V.

$$\therefore \quad \text{Input impedance} = \frac{35\text{ V}}{10\text{ pA}} = \frac{35\text{V}}{10\times10^{-12}\text{ A}} = 3.5\times10^{12}\,\Omega$$

With an input impedance in this range, *D-MOSFET* would present virtually no load to a source circuit.

19.33 D-MOSFET Biasing

The following methods may be used for *D-MOSFET* biasing :

(i) Gate bias *(ii)* Self-bias

(iii) Voltage-divider bias *(iv)* Zero bias

The first three methods are exactly the same as those used for *JFETs* and are not discussed here. However, the last method of zero-bias is widely used in *D-MOSFET* circuits.

Zero bias. Since a *D-MOSFET* can be operated with either positive or negative values of V_{GS}, we can set its Q-point at V_{GS} = 0V as shown in Fig. 19.50. Then an input a.c. signal to the gate can produce variations above and below the Q-point.

* We can only change V_{GS} because the values of I_{DSS} and $V_{GS\,(off)}$ are constant for a given *D-MOSFET*.

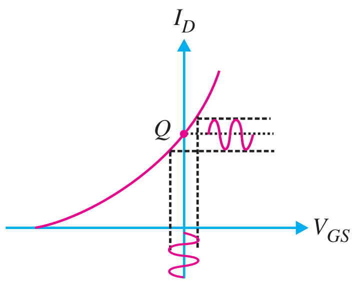


Fig. 19.50

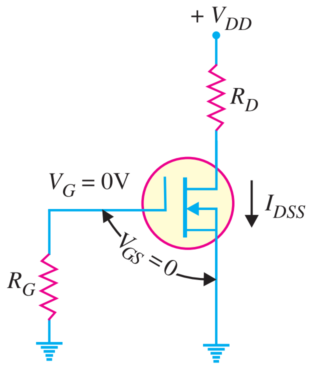


Fig. 19.51

We can use the simple circuit of Fig. 19.51 to provide zero bias. This circuit has V_{GS} = 0V and I_D = I_{DSS}. We can find V_{DS} as under :

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Note that for the *D-MOSFET* zero bias circuit, the source resistor (R_S) is not necessary. With no source resistor, the value of V_S is 0V. This gives us a value of V_{GS} = 0V. This biases the circuit at I_D = I_{DSS} and V_{GS} = 0V. For mid-point biasing, the value of R_D is so selected that V_{DS} = $V_{DD}/2$.

Example 19.32. *Determine the drain-to-source voltage (V_{DS}) in the circuit shown in Fig. 19.51 above if V_{DD} = +18V and R_D = 620Ω. The MOSFET data sheet gives $V_{GS\,(off)}$ = – 8V and I_{DSS} = 12 mA.*

Solution. Since $I_D = I_{DSS}$ = 12 mA, the V_{DS} is given by;

$$V_{DS} = V_{DD} - I_{DSS} R_D$$
$$= 18\text{V} - (12\text{ mA})(0.62\text{ k}\Omega) = \mathbf{10.6V}$$

19.34 Common-Source D-MOSFET Amplifier

Fig. 19.52 shows a common-source amplifier using *n*-channel *D-MOSFET.* Since the source terminal is common to the input and output terminals, the circuit is called *common-source amplifier. The circuit is zero biased with an a.c. source coupled to the gate through the coupling capacitor C_1. The gate is at approximately 0V d.c. and the source terminal is grounded, thus making V_{GS} = 0V.

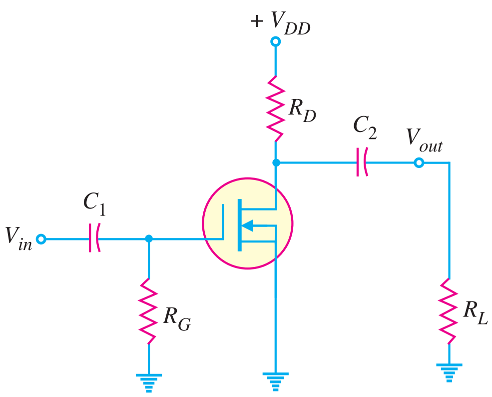


Fig. 19.52

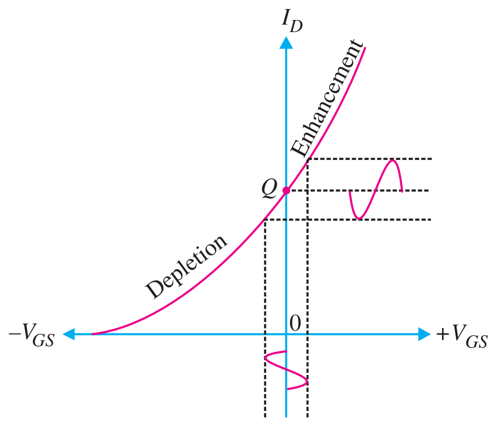


Fig. 19.53

* It is comparable to common-emitter transistor amplifier.

Operation. The input signal (V_{in}) is capacitively coupled to the gate terminal. In the absence of the signal, d.c. value of V_{GS} = 0V. When signal (V_{in}) is applied, V_{gs} swings above and below its zero value ($\because$ d.c. value of V_{GS} = 0V), producing a swing in drain current I_d.

(i) A small change in gate voltage produces a large change in drain current as in a *JFET*. This fact makes *MOSFET* capable of raising the strength of a weak signal; thus acting as an amplifier.

(ii) During the positive half-cycle of the signal, the positive voltage on the gate increases and produces the enhancement-mode. This increases the channel conductivity and hence the drain current.

(iii) During the negative half-cycle of the signal, the positive voltage on the gate decreases and produces depletion-mode. This decreases the conductivity and hence the drain current.

The result of above action is that a small change in gate voltage produces a large change in the drain current. This large variation in drain current produces a large a.c. output voltage across drain resistance R_D. In this way, *D-MOSFET* acts as an amplifier. Fig. 19.53 shows the amplifying action of *D-MOSFET* on transconductance curve.

Voltage gain. The a.c. analysis of *D-MOSFET* is similar to that of the *JFET*. Therefore, voltage gain expressions derived for *JFET* are also applicable to *D-MOSFET*.

Voltage gain, $A_v = g_m R_D$ ... for unloaded *D-MOSFET* amplifier

$= g_m R_{AC}$ ... for loaded *D-MOSFET* amplifier

Note the total a.c. drain resistance $R_{AC} = R_D \parallel R_L$.

Example 19.33. *The D-MOSFET used in the amplifier of Fig. 19.54 has an I_{DSS} = 12 mA and g_m = 3.2 mS. Determine (i) d.c. drain-to-source voltage V_{DS} and (ii) a.c. output voltage. Given v_{in} = 500 mV.*

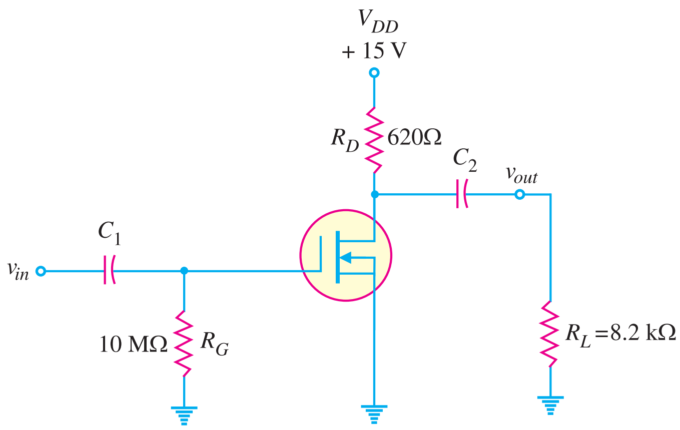


Fig. 19.54

Solution.

(i) Since the amplifier is zero biased, $I_D = I_{DSS}$ = 12 mA.

$$\therefore \quad V_{DS} = V_{DD} - I_{DSS} R_D$$

$$= 15\text{V} - (12 \text{ mA}) (0.62 \text{ k}\Omega) = \mathbf{7.56V}$$

(ii) Total a.c. drain resistance R_{AC} of the circuit is

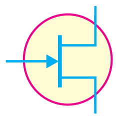
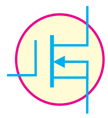
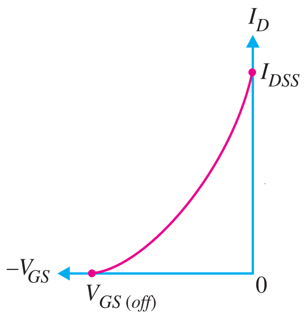
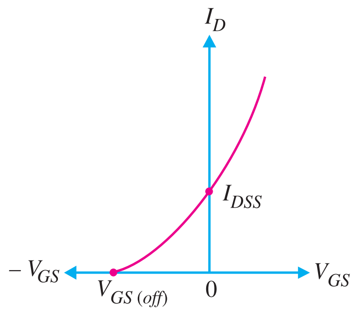
$$R_{AC} = R_D \parallel R_L = 620\Omega \parallel 8.2 \text{ k}\Omega = 576\Omega$$

$$\therefore \quad v_{out} = A_v \times v_{in} = (g_m R_{AC}) (v_{in})$$

$$= (3.2 \times 10^{-3} \text{ S} \times 576 \ \Omega) (500 \text{ mV}) = \mathbf{922 \text{ mV}}$$

19.35 D-MOSFETs Versus JFETs

Table below summarises many of the characteristics of *JFETs* and *D-MOSFETs*.

Devices:	*JFETs*	*D-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion only	Depletion and enhancement
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias	Gate bias Self bias Voltage-divider bias Zero bias
Advantages:	Extremely high input impedance.	Higher input impedance than a comparable *JFET*. Can operate in both modes (depletion and enhancement).
Disadvantages:	Bias instability. Can operate only in the depletion mode.	Bias instability. More sensitive to changes in temperature than the *JFET*.

19.36 E-MOSFET

Two things are worth noting about *E-MOSFET*. First, *E-MOSFET* operates *only* in the enhancement mode and has no depletion mode. Secondly, the *E-MOSFET* has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig. 19.55 (*i*)]. It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the *E-MOSFET* is called *Threshold voltage* [$V_{GS\,(th)}$]. The *n*-channel device requires positive V_{GS} ($\geqslant V_{GS\,(th)}$) and the *p*-channel device requires negative V_{GS} ($\geqslant V_{GS\,(th)}$).

Operation. Fig. 19.55 (*i*) shows the circuit of *n*-channel *E-MOSFET*. The circuit action is as under :

(*i*) When V_{GS} = 0V [See Fig. 19.55(*i*)], there is no channel connecting the source and drain. The *p* substrate has only a few thermally produced free electrons (minority carriers) so that drain current is essentially zero. For this reason, *E-MOSFET* is normally *OFF* when V_{GS} = 0 V. Note that this behaviour of *E-MOSFET* is quite different from *JFET* or *D-MOSFET*.

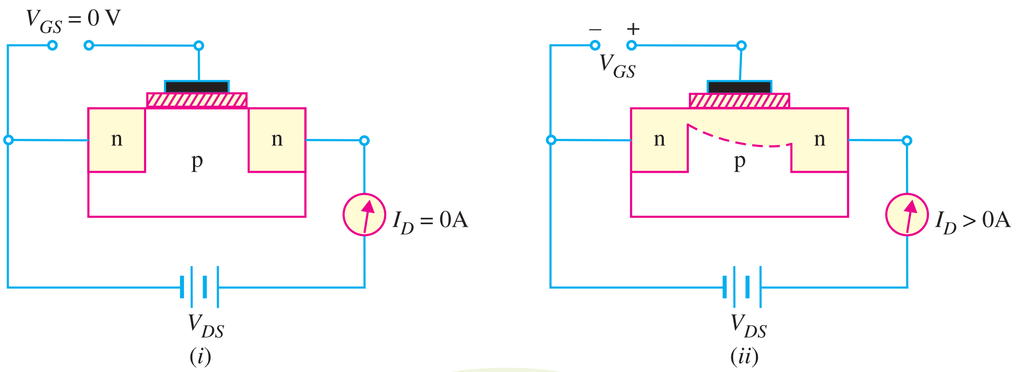


Fig. 19.55

(ii) When gate is made positive (*i.e.* V_{GS} is positive) as shown in Fig. 19.55 (*ii*), it attracts free electrons into th *p* region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is the same as creating a thin layer of *n*-type material (*i.e.* inducing a thin *n*-channel) adjacent to the SiO_2 layer. Thus the *E-MOSFET* is turned *ON* and drain current I_D starts flowing form the source to the drain.

The minimum value of V_{GS} that turns the E-MOSFET ON is called ***threshold voltage*** [$V_{GS\,(th)}$].

(iii) When V_{GS} is less than $V_{GS\,(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS\,(th)}$, the *E-MOSFET* is turned *ON* and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS\,(th)}$, if the value of V_{GS} is *increased*, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS\,(th)}$], the channel becomes narrower and I_D will decrease. This fact is revealed by the transconductance curve of *n*-channel *E-MOSFET* shown in Fig. 19.56. As you can see, $I_D = 0$ when $V_{GS} = 0$. Therefore, the value of I_{DSS} for the *E-MOSFET* is zero. Note also that there is no drain current until V_{GS} reaches $V_{GS\,(th)}$.

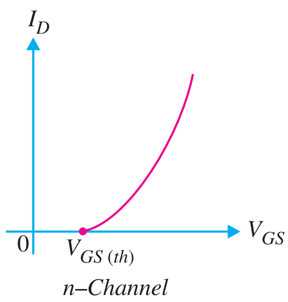


Fig. 19.56

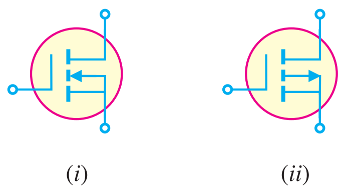


Fig. 19.57

Schematic Symbols. Fig. 19.57 (*i*) shows the schematic symbols for *n*-channel *E-MOSFET* whereas Fig. 19.57 (*ii*) shows the schematic symbol for *p*-channel *E-MOSFET.* When $V_{GS} = 0$, the *E-MOSFET* is *OFF* because there is no conducting channel between source and drain. The broken channel line in the symbols indicates the normally *OFF* condition.

Equation for Transconductance Curve. Fig. 19.58 shows the transconductance curve for *n*-channel *E-MOSFET*. Note that this curve is different from the transconductance curve for *n*-channel *JFET* or *n*-channel *D-MOSFET*. It is because it starts at $V_{GS\,(th)}$ rather than $V_{GS\,(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the *E-MOSFET* transconductance curve (for $V_{GS} > V_{GS\,(th)}$) is

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

The constant K depends on the particular *E-MOSFET* and its value is determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Any data sheet for an *E-MOSFET* will include the current $I_{D(on)}$ and the voltage $V_{GS\,(on)}$ for one point well above the threshold voltage as shown in Fig. 19.58.

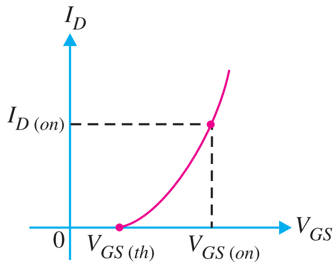


Fig. 19.58

Example 19.34. *The data sheet for an E-MOSFET gives $I_{D(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V. Determine the drain current for V_{GS} = 5V.*

Solution. Here $V_{GS\,(on)}$ = 10 V.

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2 \quad \text{... }(i)$$

Here
$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2} = \frac{500\text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17\text{ mA/V}^2$$

Putting the various values in eq. (*i*), we have,

$$I_D = 6.17\,(5\text{V} - 1\text{V})^2 = \mathbf{98.7\ mA}$$

Example 19.35. *The data sheet for an E-MOSFET gives $I_{D\,(on)}$ = 3 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 3V. Determine the resulting value of K for the device. How will you plot the transconductance curve for this MOSFET ?*

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

Here $I_{D\,(on)}$ = 3 mA ; $V_{GS\,(on)}$ = 10V ; $V_{GS\,(th)}$ = 3V

$\therefore$
$$K = \frac{3\text{ mA}}{(10\text{V} - 3\text{V})^2} = \frac{3\text{ mA}}{(7\text{V})^2} = \mathbf{0.061 \times 10^{-3}\ A/V^2}$$

Now
$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

In order to plot the transconductance curve for the device, we shall determine a few points for the curve by changing the value of V_{GS} and noting the corresponding values of I_D.

For V_{GS} = 5V ; $I_D = 0.061 \times 10^{-3}\,(5\text{V} - 3\text{V})^2 = 0.244$ mA

For V_{GS} = 8V ; $I_D = 0.061 \times 10^{-3}\,(8\text{V} - 3\text{V})^2 = 1.525$ mA

For V_{GS} = 10V ; $I_D = 0.061 \times 10^{-3}\,(10\text{V} - 3\text{V})^2 = 3$ mA

For V_{GS} = 12V ; $I_D = 0.061 \times 10^{-3}\,(12\text{V} - 3\text{V})^2 = 4.94$ mA

Thus we can plot the transconductance curve for the *E-MOSFET* from these V_{GS}/I_D points.

19.37 E-MOSFET Biasing Circuits

One of the problems with *E-MOSFET* is the fact that many of the biasing circuits used for *JFETs* and *D-MOSFETs* cannot be used with this device. For example, *E-MOSFETs* must have V_{GS} greater than the threshold value ($V_{GS\,(th)}$) so that zero bias cannot be used. However, there are two popular methods for *E-MOSFET* biasing *viz.*

(*i*) Drain-feedback bias

(*ii*) Voltage-divider bias

(*i*) **Drain-feedback bias.** This method of *E-MOSFET* bias is equivalent to collector-feedback bias in transistors. Fig. 19.59 (*i*) shows the drain-feedback bias circuit for *n*-channel *E-MOSFET*. A high resistance R_G is connected between the drain and the gate. Since the gate resistance is superhigh, no current will flow in the gate circuit (*i.e.* $I_G = 0$). Therefore, there will be no voltage drop across R_G. Since there is no voltage drop across R_G, the gate will be at the same potential as the drain. This fact is illustrated in the d.c. equivalent circuit of drain-feedback bias as in Fig. 19.59 (*ii*).

$$\therefore \quad V_D = V_G \quad \text{and} \quad V_{DS} = V_{GS}$$

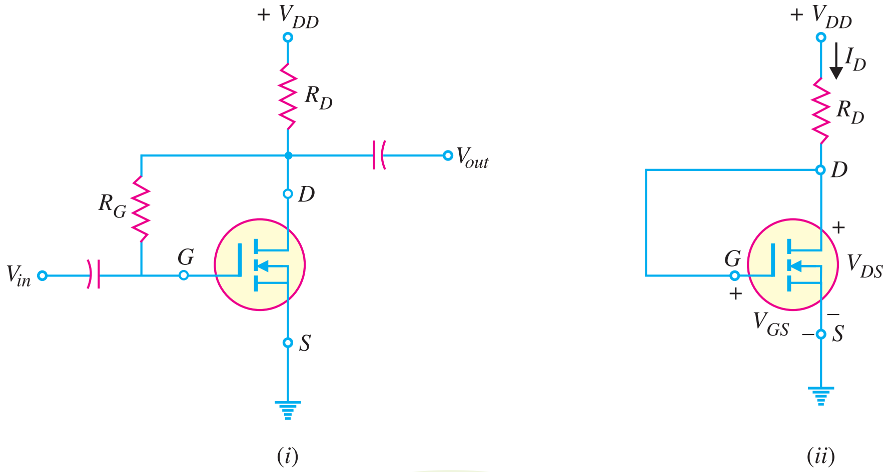


Fig. 19.59

The value of drain-source voltage V_{DS} for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D$$

$$\text{Since} \quad V_{DS} = V_{GS},\ V_{GS} = V_{DD} - I_D R_D$$

$$\text{Since in this circuit} \quad V_{DS} = V_{GS}\ ;\ I_D = I_{D\,(on)}.$$

Therefore, the *Q*-point of the circuit stands determined.

***(ii)* Voltage-divider Bias.** Fig. 19.60 shows voltage divider biasing arrangement for *n*-channel *E-MOSFET*. Since $I_G = 0$, the analysis of the method is as follows :

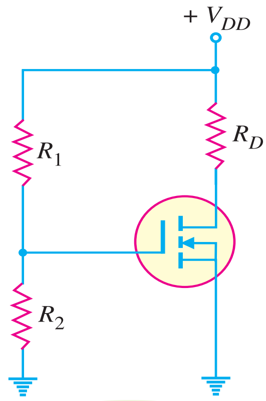


Fig. 19.60

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

and

$$V_{DS} = V_{DD} - I_D R_D$$

where

$$I_D = K\,(V_{GS} - V_{GS\,(th)})^2$$

Once I_D and V_{DS} are known, all the remaining quantities of the circuit such as V_D etc. can be determined.

Example 19.36. *Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Fig. 19.61. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V.*

Solution. Referring to the circuit shown in Fig. 19.61, we have,

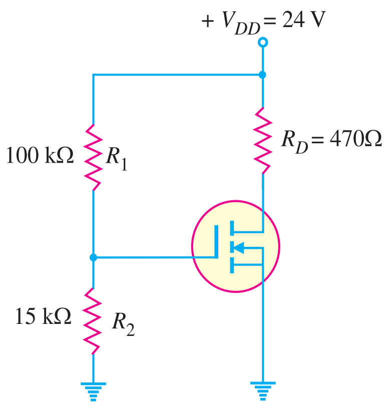


Fig. 19.61

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{24\text{V}}{(100 + 15)\ \text{k}\Omega} \times 15\ \text{k}\Omega = \mathbf{3.13V}$$

The value of *K* can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{500 \text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17 \text{ mA/V}^2 \quad [\because \; V_{GS\,(on)} = 10\text{V}]$$

$$\therefore \quad I_D = K\,(V_{GS} - V_{GS\,(th)})^2 = 6.17 \text{ mA/V}^2\,(3.13\text{V} - 1\text{ V})^2 = 28 \text{ mA}$$

$$\therefore \quad V_{DS} = V_{DD} - I_D\,R_D = 24\text{V} - (28 \text{ mA})\,(470\Omega) = \mathbf{10.8V}$$

Example 19.37. *Determine the values of I_D and V_{DS} for the circuit shown in Fig. 19.62. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 10 mA when $V_{GS} = V_{DS}$.*

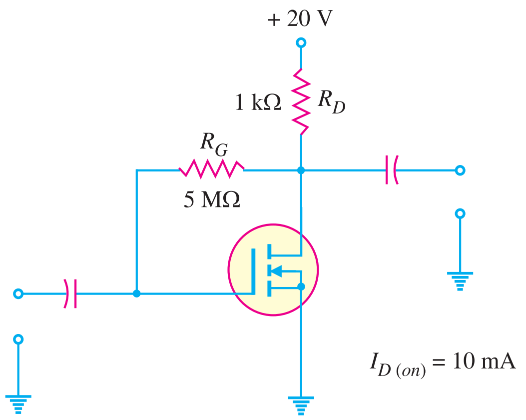


Fig. 19.62

Solution. Since in the drain-feedback circuit $V_{GS} = V_{DS}$,

$$\therefore \quad I_D = I_{D\,(on)} = \mathbf{10\ mA}$$

The value of V_{DS} (and thus V_{GS}) is given by ;

$$V_{DS} = V_{DD} - I_D\,R_D$$

$$= 20\text{V} - (10 \text{ mA})\,(1 \text{ k}\Omega) = 20\text{V} - 10\text{V} = \mathbf{10V}$$

Example 19.38. *Determine the value of I_D for the circuit shown in Fig. 19.63. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 10 mA at V_{GS} = 10 V and $V_{GS\,(th)}$ = 1.5 V.*

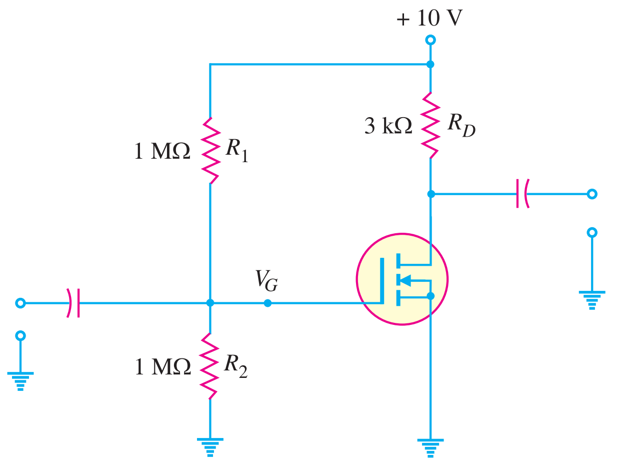


Fig. 19.63

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{10 \text{ mA}}{(10\text{ V} - 1.5\text{V})^2} = 1.38 \times 10^{-1} \text{ mA/V}^2 \quad [\because\ V_{GS\,(on)} = 10\text{V}]$$

From the circuit, the source voltage is seen to be 0V. Therefore, $V_{GS} = V_G - V_S = V_G - 0 = V_G$. The value of V_G (= V_{GS}) is given by ;

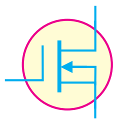
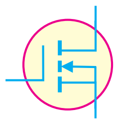
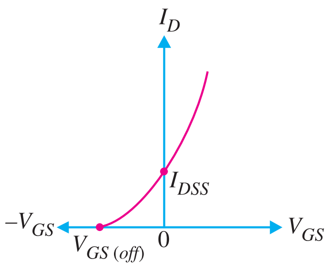
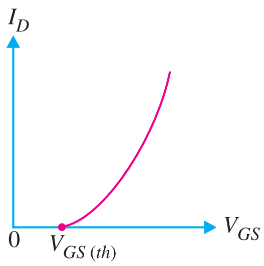
$$V_G \text{ (or } V_{GS}) = \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{10\text{V}}{(1+1)\text{ M}\Omega} \times 1\text{M}\Omega = 5\text{V}$$

$$\therefore \quad I_D = K(V_{GS} - V_{GS\,(th)})^2$$

$$= (1.38 \times 10^{-1} \text{ mA/V}^2)(5\text{V} - 1.5\text{V})^2 = \mathbf{1.69 \text{ mA}}$$

19.38 D-MOSFETs Versus E-MOSFETs

Table below summarises many of the characteristics of *D-MOSFETs* and *E-MOSFETs*

Devices:	*D-MOSFETs*	*E-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion and enhancement.	Enhancement only.
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias Zero bias	Gate bias Voltage-divider bias Drain-feedback bias

MULTIPLE-CHOICE QUESTIONS

1. A *JFET* has three terminals, namely ....
   (*i*) cathode, anode, grid
   (*ii*) emitter, base, collector
   (*iii*) source, gate, drain
   (*iv*) none of the above

2. A *JFET* is similar in operation to .... valve.
   (*i*) diode (*ii*) pentode
   (*iii*) triode (*iv*) tetrode

3. A *JFET* is also called .... transistor.
   (*i*) unipolar (*ii*) bipolar
   (*iii*) unijunction (*iv*) none of the above

4. A *JFET* is a .... driven device.

(*i*) current
(*ii*) voltage
(*iii*) both current and voltage
(*iv*) none of the above

5. The gate of a *JFET* is .... biased.
(*i*) reverse
(*ii*) forward
(*iii*) reverse as well as forward
(*iv*) none of the above

6. The input impedance of a *JFET* is .... that of an ordinary transistor.
(*i*) equal to (*ii*) less than
(*iii*) more than (*iv*) none of the above

7. In a *p*-channel *JFET*, the charge carriers are ....
(*i*) electrons
(*ii*) holes
(*iii*) both electrons and holes
(*iv*) none of the above

8. When drain voltage equals the pinch-off voltage, then drain current .... with the increase in drain voltage.
(*i*) decreases
(*ii*) increases
(*iii*) remains constant
(*iv*) none of the above

9. If the reverse bias on the gate of a *JFET* is increased, then width of the conducting channel ....
(*i*) is decreased
(*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

10. A *MOSFET* has .... terminals.
(*i*) two (*ii*) five
(*iii*) four (*iv*) three

11. A *MOSFET* can be operated with ....
(*i*) negative gate voltage only
(*ii*) positive gate voltage only
(*iii*) positive as well as negative gate voltage
(*iv*) none of the above

12. A *JFET* has .... power gain.
(*i*) small (*ii*) very high
(*iii*) very small (*iv*) none of the above

13. The input control parameter of a *JFET* is ....
(*i*) gate voltage (*ii*) source voltage
(*iii*) drain voltage (*iv*) gate current

14. A common base configuration of a *pnp* transistor is analogous to .... of a *JFET*.
(*i*) common source configuration
(*ii*) common drain configuration
(*iii*) common gate configuration
(*iv*) none of the above

15. A *JFET* has high input impedance because ....
(*i*) it is made of semiconductor material
(*ii*) input is reverse biased
(*iii*) of impurity atoms
(*iv*) none of the above

16. In a *JFET*, when drain voltage is equal to pinch-off voltage, the depletion layers ....
(*i*) almost touch each other
(*ii*) have large gap
(*iii*) have moderate gap
(*iv*) none of the above

17. In a *JFET*, I_{DSS} is known as ....
(*i*) drain to source current
(*ii*) drain to source current with gate shorted
(*iii*) drain to source current with gate open
(*iv*) none of the above

18. The two important advantages of a *JFET* are ....
(*i*) high input impedance and square-law property
(*ii*) inexpensive and high output impedance
(*iii*) low input impedance and high output impedance
(*iv*) none of the above

19. .... has the lowest noise-level.
(*i*) triode (*ii*) ordinary transistor
(*iii*) tetrode (*iv*) *JFET*

20. A *MOSFET* is sometimes called .... *JFET*.
(*i*) many gate (*ii*) open gate
(*iii*) insulated gate (*iv*) shorted gate

21. Which of the following devices has the highest input impedance ?
(*i*) *JFET*

(*ii*) *MOSFET*
(*iii*) crystal diode
(*iv*) ordinary transistor

22. A *MOSFET* uses the electric field of a .... to control the channel current.
(*i*) capacitor (*ii*) battery
(*iii*) generator (*iv*) none of the above

23. The pinch-off voltage in a *JFET* is analogous to .... voltage in a vacuum tube.
(*i*) anode
(*ii*) cathode
(*iii*) grid cut off
(*iv*) none of the above

24. The formula for a.c. drain resistance of a *JFET* is ....
(*i*) $\frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}
(*ii*) $\frac{\Delta V_{GS}}{\Delta I_D}$ at constant V_{DS}
(*iii*) $\frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}
(*iv*) $\frac{\Delta I_D}{\Delta V_{DS}}$ at constant V_{GS}

25. In class *A* operation, the input circuit of a *JFET* is .... biased.
(*i*) forward (*ii*) reverse
(*iii*) not (*iv*) none of the above

26. If the gate of a *JFET* is made less negative, the width of the conducting channel ....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

27. The pinch-off voltage of a *JFET* is about ....
(*i*) 5 V (*ii*) 0.6 V
(*iii*) 15 V (*iv*) 25 V

28. The input impedance of a *MOSFET* is of the order of ....
(*i*) Ω (*ii*) a few hundred Ω
(*iii*) k Ω (*iv*) several M Ω

29. The gate voltage in a *JFET* at which drain current becomes zero is called .... voltage.
(*i*) saturation (*ii*) pinch-off
(*iii*) active (*iv*) cut-off

30. The drain current I_D in a *JFET* is given by ....
(*i*) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
(*ii*) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$
(*iii*) $I_D = I_{DSS}\left(1 - \frac{V_P}{V_{GS}}\right)^2$
(*iv*) $I_D = I_{DSS}\left(1 + \frac{V_P}{V_{GS}}\right)^{1/2}$

31. In a *FET*, there are .... *pn* junctions at the sides.
(*i*) three (*ii*) four
(*iii*) five (*iv*) two

32. The transconductance of a *JFET* ranges from ....
(*i*) 100 to 500 mA/V
(*ii*) 500 to 1000 mA/V
(*iii*) 0.5 to 30 mA/V
(*iv*) above 1000 mA/V

33. The source terminal of a *JFET* corresponds to .... of a vacuum tube.
(*i*) plate (*ii*) cathode
(*iii*) grid (*iv*) none of the above

34. The output characteristics of a *JFET* closely resemble the output characteristics of a .... valve.
(*i*) pentode (*ii*) tetrode
(*iii*) triode (*iv*) diode

35. If the cross-sectional area of the channel in *n*-channel *JFET* increases, the drain current ....
(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

36. The channel of a *JFET* is between the ....
(*i*) gate and drain
(*ii*) drain and source
(*iii*) gate and source
(*iv*) input and output

37. For V_{GS}= 0 V, the drain current becomes con-

stant when V_{DS} exceeds ....
(*i*) cut off (*ii*) V_{DD}
(*iii*) V_P (*iv*) 0 V

38. A certain *JFET* data sheet gives $V_{GS(off)}$ = – 4 V. The pinch-off voltage V_p is ....
(*i*) + 4 V (*ii*) – 4 V
(*iii*) dependent on V_{GS}
(*iv*) data insufficient

39. The constant-current region of a *JFET* lies between ....
(*i*) cut off and saturation
(*ii*) cut off and pinch-off
(*iii*) 0 and I_{DSS}
(*iv*) pinch-off and breakdown

40. At cut-off, the *JFET* channel is ....
(*i*) at its widest point
(*ii*) completely closed by the depletion region
(*iii*) extremely narrow
(*iv*) reverse biased

41. A *MOSFET* differs from a *JFET* mainly because ....
(*i*) of power rating
(*ii*) the *MOSFET* has two gates
(*iii*) the *JFET* has a *pn* junction
(*iv*) none of above

42. A certain *D-MOSFET* is biased at V_{GS} = 0V. Its data sheet specifies I_{DSS} = 20 mA and $V_{GS\ (off)}$ = – 5V. The value of the drain current is ....
(*i*) 20 mA (*ii*) 0 mA
(*iii*) 40 mA (*iv*) 10 mA

43. An *n*-channel *D-MOSFET* with a positive V_{GS} is operating in ....
(*i*) the depletion-mode
(*ii*) the enhancement-mode
(*iii*) cut off (*iv*) saturation

44. A certain *p*-channel E-MOSFET has a $V_{GS\ (th)}$ = – 2V. If V_{GS} = 0V, the drain current is ....
(*i*) 0 mA (*ii*) $I_{D\ (on)}$
(*iii*) maximum (*iv*) I_{DSS}

45. In a common-source *JFET* amplifier, the output voltage is ....
(*i*) 180° out of phase with the input
(*ii*) in phase with the input
(*iii*) 90° out of phase with the input
(*iv*) taken at the source

46. In a certain common-source *D-MOSFET* amplifier, V_{ds} = 3.2 V r.m.s. and V_{gs} = 280 mV r.m.s. The voltage gain is ....
(*i*) 1 (*ii*) 11.4
(*iii*) 8.75 (*iv*) 3.2

47. In a certain *CS JFET* amplifier, R_D = 1 kΩ, R_S = 560Ω, V_{DD} = 10 V and g_m = 4500 µS. If the source resistor is completely bypassed, the voltage gain is ....
(*i*) 450 (*ii*) 45
(*iii*) 2.52 (*iv*) 4.5

48. A certain common-source *JFET* has a voltage gain of 10. If the source bypass capacitor is removed, ...
(*i*) the voltage gain will increase
(*ii*) the transconductance will increase
(*iii*) the voltage gain will decrease
(*iv*) the Q-point will shift

49. A *CS JFET* amplifier has a load resistance of 10 kΩ and R_D = 820Ω. If g_m = 5 mS and V_{in} = 500 mV, the output signal voltage is ...
(*i*) 2.05 V (*ii*) 25 V
(*iii*) 0.5 V (*iv*) 1.89 V

50. If load resistance in Q. 49 is removed, the output voltage will ....
(*i*) increase (*ii*) decrease
(*iii*) stay the same (*iv*) be zero

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*i*)	**14.** (*iii*)	**15.** (*ii*)
16. (*i*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*iii*)
21. (*ii*)	**22.** (*i*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*i*)	**28.** (*iv*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*iii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)
41. (*iii*)	**42.** (*i*)	**43.** (*ii*)	**44.** (*i*)	**45.** (*i*)
46. (*ii*)	**47.** (*iv*)	**48.** (*iii*)	**49.** (*iv*)	**50.** (*i*)

Chapter Review Topics

1. Explain the construction and working of a *JFET*.
2. What is the difference between a *JFET* and a bipolar transistor ?
3. How will you determine the drain characteristics of *JFET* ? What do they indicate?
4. Define the *JFET* parameters and establish the relationship between them.
5. Briefly describe some practical applications of *JFET*.
6. Explain the construction and working of *MOSFET*.
7. Write short notes on the following :
   (*i*) Advantages of *JFET* (*ii*) Difference between *MOSFET* and *JFET*

Problems

1. A *JFET* has a drain current of 5 mA. If I_{DSS} = 10 mA and $V_{GS(off)}$ is – 6 V, find the value of (*i*) V_{GS} and (*ii*) V_P. **[(*i*) – 1.5 V (*ii*) 6 V]**
2. A *JFET* has an I_{DSS} of 9 mA and a $V_{GS\,(off)}$ of – 3V. Find the value of drain current when V_{GS} = –1.5V. **[2.25mA]**
3. In the *JFET* circuit shown in Fig. 19.64 if I_D = 1.9 mA, find V_{GS} and V_{DS}. **[– 1.56V; 13.5V]**

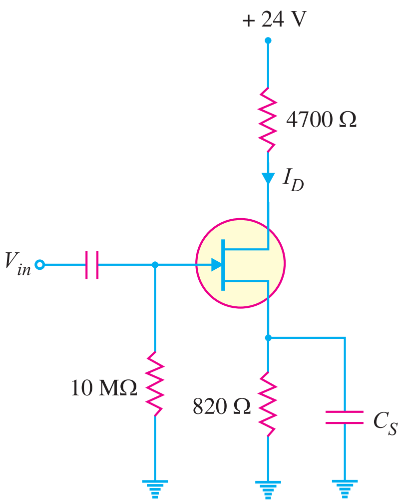


Fig. 19.64

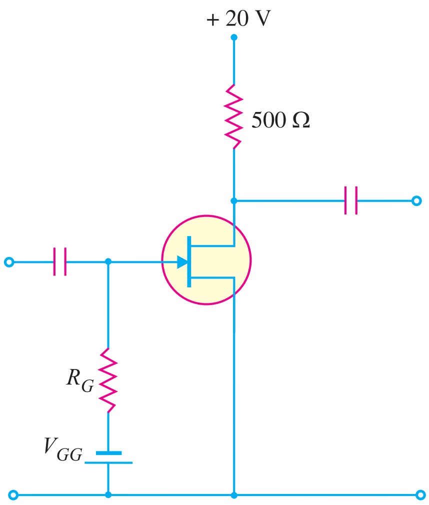


Fig. 19.65

4. For the *JFET* amplifier shown in Fig. 19.65, draw the d.c. load line.

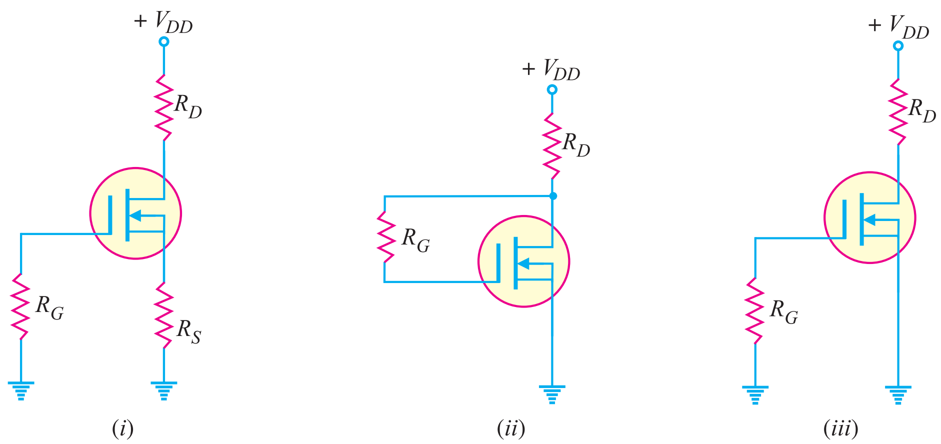


Fig. 19.66

5. For a *JFET*, I_{DSS} = 9 mA and V_{GS} = –3.5 V. Determine I_D when (*i*) V_{GS} = 0 V (*ii*) V_{GS} = – 2V. **[(*i*) 9mA (*ii*) 1.65 mA]**
6. Sketch the transfer curve for a *p*-channel *JFET* with I_{DSS} = 4 mA and V_P = 3 V.
7. In a *D-MOSFET*, determine I_{DSS}, given I_D = 3 mA, V_{GS} = – 2V and $V_{GS\,(off)}$ = – 10V. **[4.69 mA]**
8. Determine in which mode each *D-MOSFET* in Fig. 19.66 is biased. **[(*i*) Depletion (*ii*) Enhancement (*iii*) Zero bias]**
9. Determine V_{DS} for each circuit in Fig. 19.67. Given I_{DSS} = 8 mA. **[(*i*) 4V (*ii*) 5.4V (*iii*) – 4.52V]**

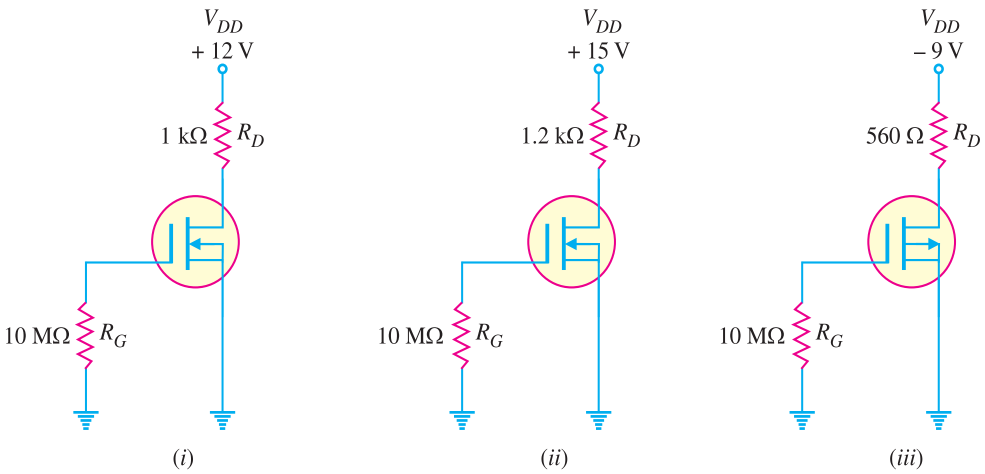


Fig. 19.67

10. If a 50 mV r.m.s. input signal is applied to the amplifier in Fig. 19.68, what is the peak-to-peak output voltage? Given that g_m = 5000 µS. **[920 mV]**

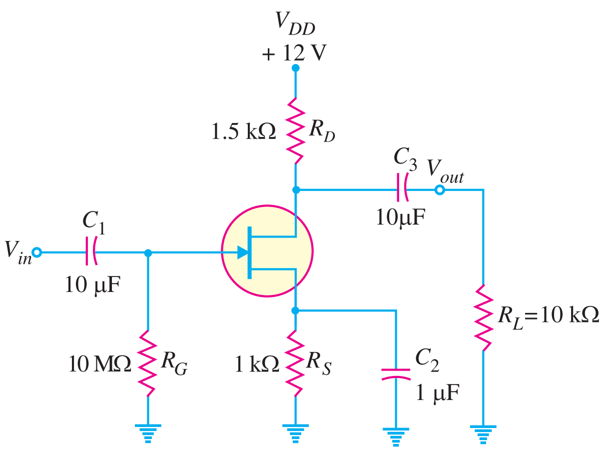


Fig. 19.68

Discussion Questions

1. Why is the input impedance of *JFET* more than that of the transistor ?
2. What is the importance of *JFET* ?
3. Why is *JFET* called unipolar transistor ?
4. What is the basic difference between *D-MOSFET* and *E-MOSFET* ?
5. What was the need to develop *MOSFET* ?

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