SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: MBA Tech (Computer) Year: II Semester: III

Academic Year: 2017-2018

Subject: Computer Organization & Architecture

Date: 25 November 2017

Marks: 70
Time: 2.00 pm - 5.00 pm
Durations: 3 Hrs
No. of Pages : 02

Final-Examination

Instructions: Candidates should read carefully the instruction printed on the question paper and on the cover of the Answer Book, which is provided for their use.

1) Question 1 is compulsory.
2) Out of remaining question, attempt any 4 questions.
3) **In all 5 question to be attempted.**
4) All question carry equal marks.
5) **Answer to each new question to be started on afresh page.**
6) **Figuresin brackets on the right hand side indicate full marks.**
7) **Assume suitable data if necessary.**

Q.1 a. Elaborate the functions of the following: [5]
- i. Program counter
- ii. Memory address register
- iii. Instruction register
- iv. Memory buffer register
- v. Accumulator

b. Explain with the help of instruction cycle state diagram, how an instruction is executed. [6]

c. What is computer architecture? How it is different from computer organization? [3]

Q.2 a. Explain program flow of control without and with interrupts.{consider WRITE interrupts} [8]

b. Consider the following block reference string: [6]
0, 2, 1, 6, 4, 0, 1, 0, 3, 1, 2, 1
How many page fault would occur for the following block replacement algorithm assuming 4 lines in a cache memory?
- i. FIFO
- ii. LRU

Q.3 a. Consider a main memory of 32 GB, cache memory of 32KB and block size is of 32B, represent the memory address(i.e tag, line,set, offset) along with tag diraectory size and number of comparator in the following scheme. [9]
{consider system is of byte addressable memory}
- i. Direct mapping
- ii. Set-Associative(consider-set size=4)
- iii. Fully associative

b. List & explain the different types cache memories. [5]

Q.4 a. Explain Booth's multiplication algorithm. Multiply $(14)_{10}$ with $(-5)_{10}$ by using Booth's Multiplication. Give Flow table of the multiplication. [7]

b. Explain floating point arithmetic with suitable example. [7]

Q.5 a. Explain the following mode of transfer: [7]

i. Programmed I/O
ii. Interrupt Driven I/O
iii. Direct Memory Access

b. What is Structural dependency in a pipelined processor? How can we resolve this. [5]

c. Calculate (22-26) in 5-bit using 2's complement. [2]

Q.6 a. Explain Micro programmed control unit with diagram. [8]

b. List & explain all the pipeline hazards in detail. [6]

Q.7 Write a short note on any **TWO**:- [7X2]

a. Static RAM and Dynamic RAM with diagram of single bit storage cell
b. Flynn's classification
c. Synchronous and Asynchronus bus timing