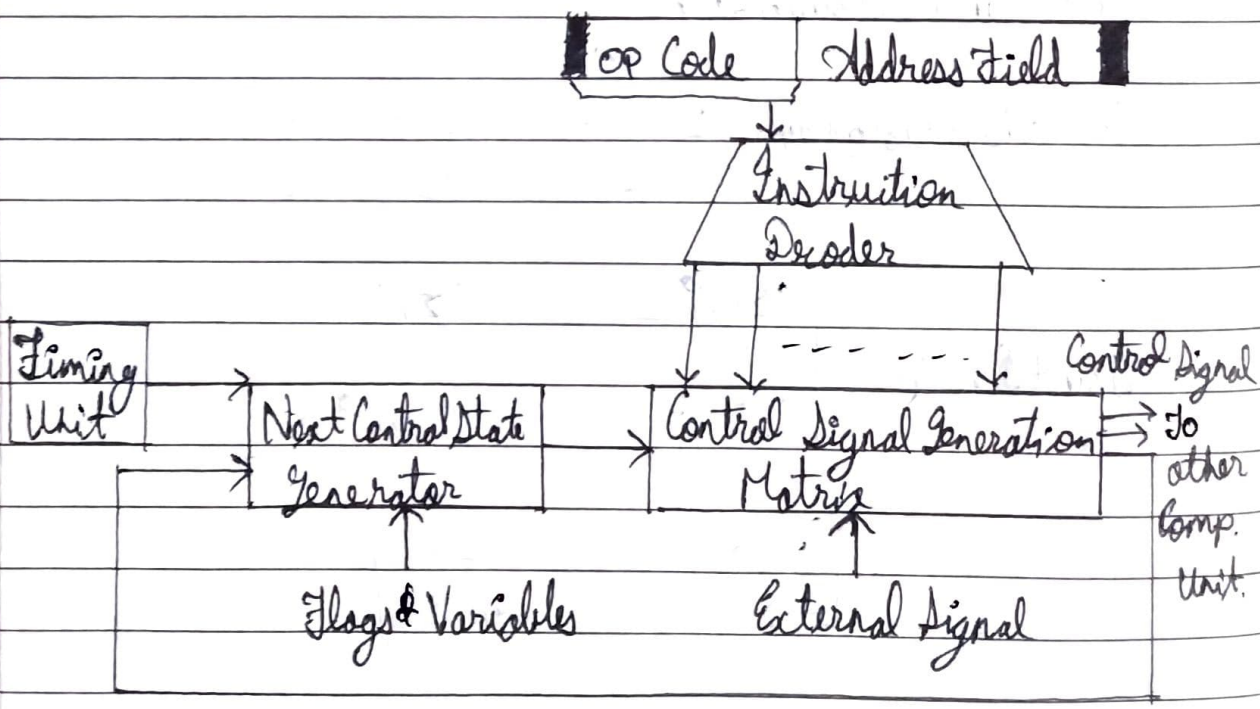
Varun Khadayate A016 26-10-20

COA

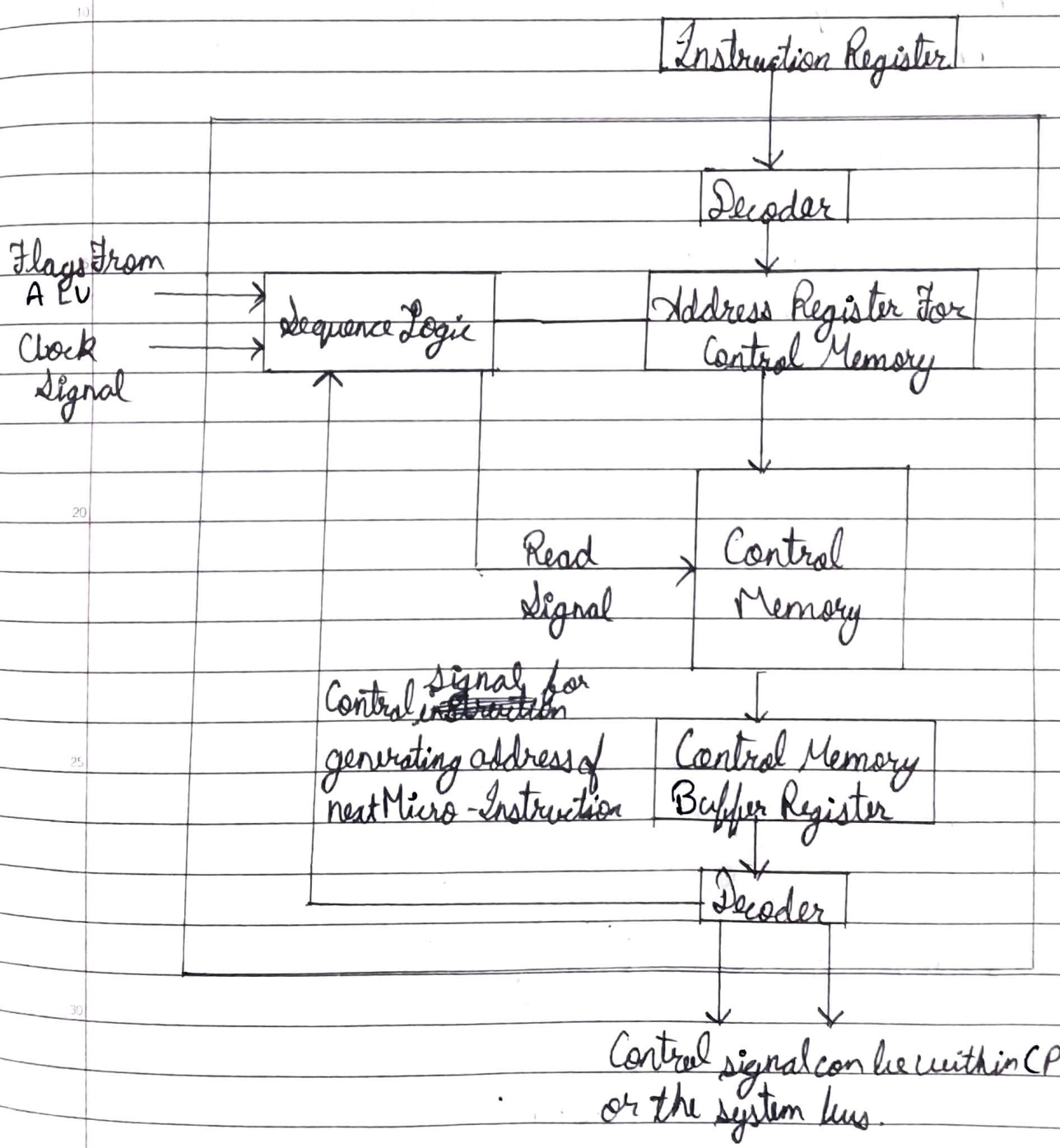
Assignment-II

Q1. The control hardware can be viewed as a state machine that can change from one state to another in every clock cycle, depending on the contents of the instruction register, the conditional codes are the external inputs. The outputs of the state machine are the control signal. The sequence of the operation carried out by this machine is determined ~~as~~ by the wiring of the logic elements and hence named as 'hardwired'

- Fixed logic circuits that correspond directly to the boolean expression are used to generate the control signal.
- Hardwired control is faster than micro-programmed.
- A controller that uses this approach can operate at high speed.
- RISC architecture is based on hardwired control unit.



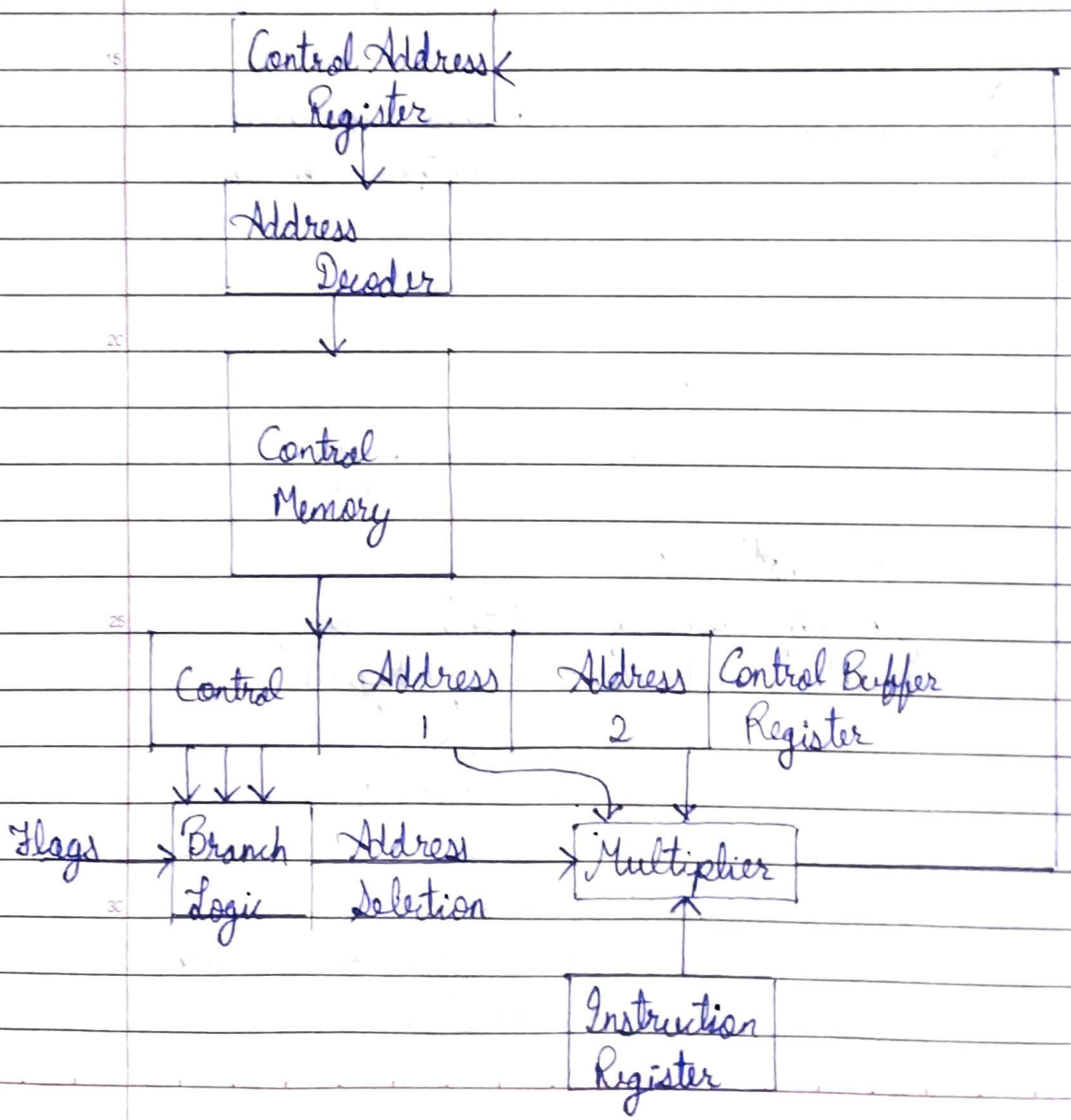
Q2. • The control signal associated with operations are stored in special memory units inaccessible by the programmer as control words.
• Control signals are generated by a program are similar to machine language programs.
• Micro-programmed control units is slower in speed because of the time it takes to fetch microinstruction from the control memory.



The micro-instruction are stored in the control memory. The address register for the control memory contains the address of the next instruction that is to be read. A micro-instruction execution primarily involves the generation of desired control signals or signals used to determine the next micro-instruction to be executed.

Q3. There are 3 types of micro-instruction sequencing techniques named as:

1. Two Address Fields

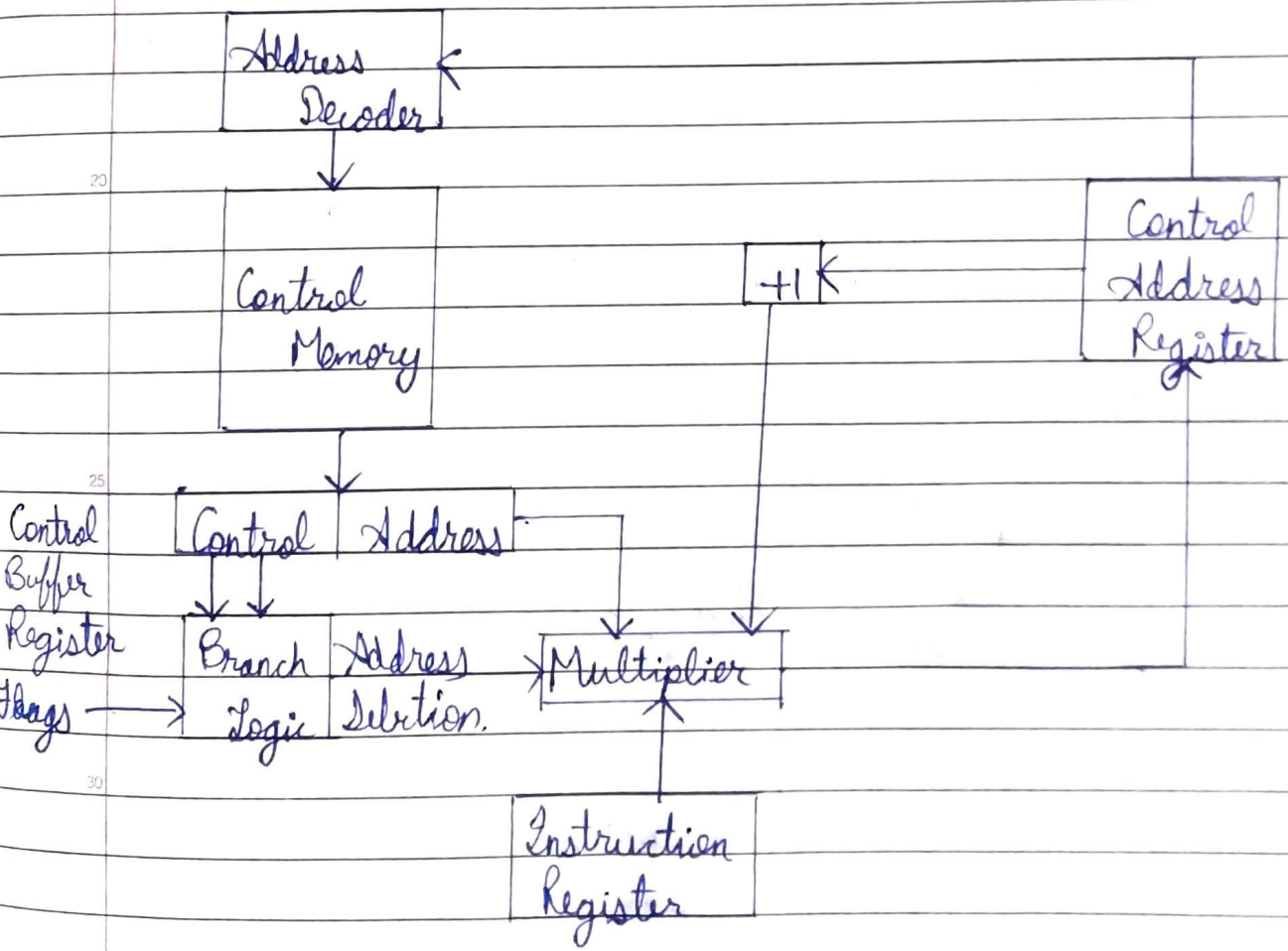


In the 2 address field sequencing & logic the multiplexer server as a defination destination for both address fields plus the instruction register. The multiplexer transmits either opcode or one of the address based on the address-selection input. This output from multiplexer is transferred to a control address register which subsequently decodes the next microinstructional address.

The address-selection signals are provided by a branch logic module whose input consist of control unit flags plus bits from the control portion of microinstruction.

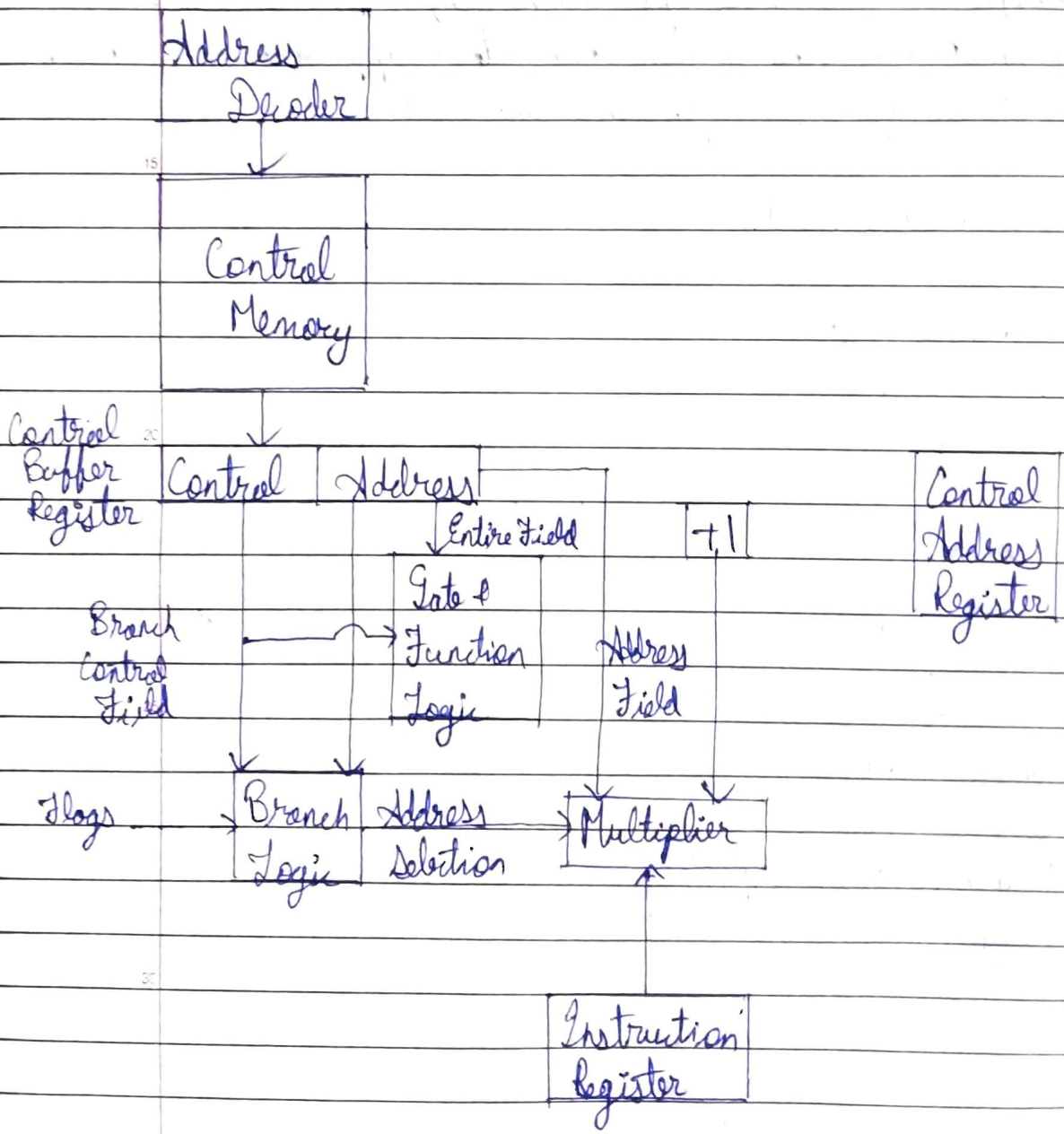
Although the 2 address approach is simple it requires more bits in the microinstruction than other approaches. With some additional logic, savings can be achieved.

2. Single Address Field.



With single field register address approach, the next address has an address field, an instruction register code and next sequential address.
The address selection signal determines the option to be selected. This approach reduces the number of address fields to one, however, the address field is not used efficiently.

3. Variable Format.



In Variable format there are 2 entirely different microinstruction formats. One-bit designates which format is being used and the remaining bits are used to activate control signals. Some of the bits are used for the branch logic module, and the remaining bits provide the address.
By this approach, one entire cycle is consumed with each branch microinstruction which is a disadvantage. Whereas, in other approaches a address generation occurs as part of the same cycle as control signal generation, minimizing control memory.