**SVKM's NMIMS**
**MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING/**
**SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING**

Programme: MBA Tech (Computer) Year: II Semester: III

**Academic Year: 2018-2019**

Subject: Computer Organization & Architecture

Date: 22 November 2018

Marks: 70
Time: 2.00 pm to 5.00 pm
Durations: 3 (hrs)
No. of Pages: 02

**Final Examination (2018-19)/ Re Exam (2017-18)**

**Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.**

1) Question No. 1 is compulsory.
2) Out of remaining questions, attempt any 4 questions.
3) **In all 5 questions to be attempted.**
4) All questions carry equal marks.
5) **Answer to each new question to be started on a fresh page.**
6) **Figures in brackets on the right hand side indicate full marks.**
7) **Assume suitable data if necessary.**

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|---|---|---|---|
| Q.1. | | Attempt All | |
| | A) | List and briefly define the main structural components of a computer | (3) |
| | B) | Compare RISC with CISC | (3) |
| | C) | Give an example and Explain Base Index Addressing | (3) |
| | D) | What do you mean by instruction cycle, machine cycle and T states? | (3) |
| | E) | What is a multiprocessor System? | (2) |
| Q.2. | A) | With a neat diagram explain the expanded structure of IAS Computer | (7) |
| | B) | Draw and Explain flow chart for Floating point Division | (7) |
| Q.3. | A) | A computer has 16MB main memory and 64 KB cache. The block size is 16 bytes.<br>1. How many cache lines does the computer have?<br>2. How many blocks does the main memory have?<br>3. Give the starting address of memory blocks which are directly mapped to cache lines.<br>4. Explain how a given address is retrieved from the memory system. | (7) |
| | B) | Explain the memory hierarchy pyramid, showing both primary and secondary memories in the diagram and also explain the relationship of cost, speed amid capacity. | (7) |

Q.4 A) What is Cache Hit and Cache Miss in cache memory organization? (7)
A two level memory (M1, M2) has the access times $t_{A1}=10^{-8}$ sec. and $t_{A2} = 10^{-3}$. What must the hit ratio H be in order for the access efficiency to be at least 65% of its maximum possible value?

B) Explain the working of control unit with the help of block diagram. (7)

Q.5 A) What is the difference between DRAM and SRAM in terms of application? (7)

B) Explain how Booth's algorithm is work for signed multiplication operation with flow chart. (7)
Multiply given signed 2's compliment numbers using bit-pair recoding
A= *110101* Multiplicand (-11)
B= *011011* Multiplier (+27)

Q.6 A) Write the comparison between Seven Levels of RAID. (7)

B) Explain the design aspect in implementation of the pipeline. (7)

Q.7

A) A processor executes 50,000 000 cycles in one second. A printer device is sent 8 bytes in programmed I/O mode. The printer can print 500 characters per second and does not have a print-buffer. (2)
(a) How much time will be taken to acknowledge the character status?
(b) How many processor cycles are used in transferring just 8 bytes?

B) Write the difference between Program Driven IO and Interrupt Driven IO, Discuss the advantage of Interrupt Driven IO over Program Driven IO. (5)

C) Explain Flynn's Classification with respect to computer architecture. (7)

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