SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: MBA Tech (Computer) Year: II Semester: III

Batch: 2016-17

Academic Year: 2017-2018

Subject: Computer Organization & Architecture

Date: 25 November 2017

Marks: 70
Time: 2.00 pm - 5.00 pm
Durations: 3 Hrs
No. of Pages: 02

Re-Examination

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.

1) Question No. 1 is compulsory.
2) Out of remaining questions, attempt any 4 questions.
3) In **all 5 questions** to be attempted.
4) All questions carry equal marks.
5) Answer to **each new** question to be started on a fresh page.
6) Figures in brackets on the right hand side indicate full marks.
7) Assume suitable data if necessary.

Q.1 a) Explain PCI bus. [2]

b) Explain MBR and MAR. [2]

c) What is memory access time and memory cycle time. [2]

d) Explain fixed and floating point numbers with an example. [2]

e) Explain immediate and direct addressing modes with an example. [2]

f) What are applications of microprogramming? [2]

g) What are device drivers? [2]

Q.2 (a) Cache can hold 64 KB of data. Data is transferred between main memory and cache in blocks of 4 bytes each. Main memory consists of 16 MB. Find the distribution of main memory address in all the three mapping techniques i.e. direct mapping, associative and set associative mapping. (Assume 1 word= 1 byte). Assume two ways set associative.

[9]

(b) Differentiate between SRAM and DRAM. [5]

Q.3 (a) Explain IEEE 754 single precision 32-bit format. [7]

(b) Explain memory hierarchy with the help of a diagram. [7]

Q.4 (a) Multiply the following two numbers using Booth's algorithm 4 x 6. Comment on the efficiency of Booth's algorithm. [7]

(b) Explain addressing modes with the help of example. [7]

Q.5 (a) Write a short note on different modes of DMA transfer. [7]

(b) Explain six stage instruction pipeline with the help of timing diagram. [7]

Q.6 (a) Explain different parallel processing architectures. [7]

(b) Explain hardwired control unit in detail. [7]

Q.7 (a) Explain daisy chain, polling and independent requesting with advantages and disadvantages. [7]

(b) Draw and explain instruction cycle state diagram with interrupts. [7]