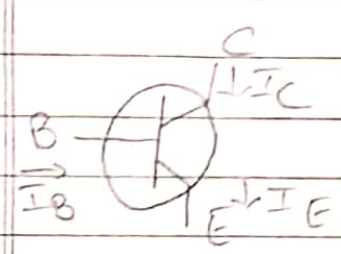
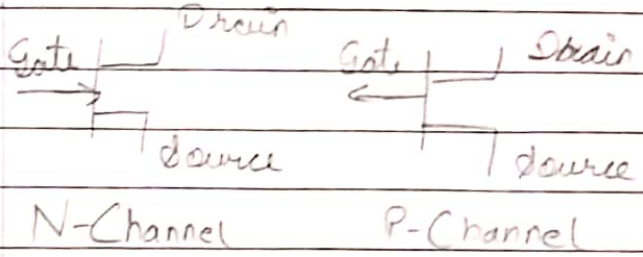
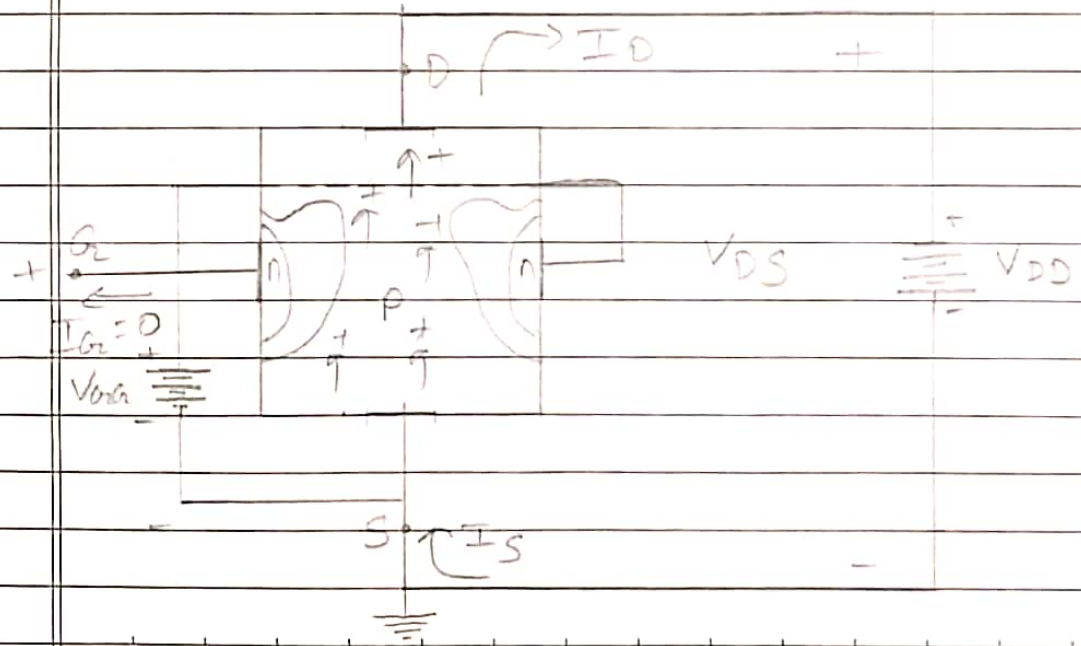
Q1.

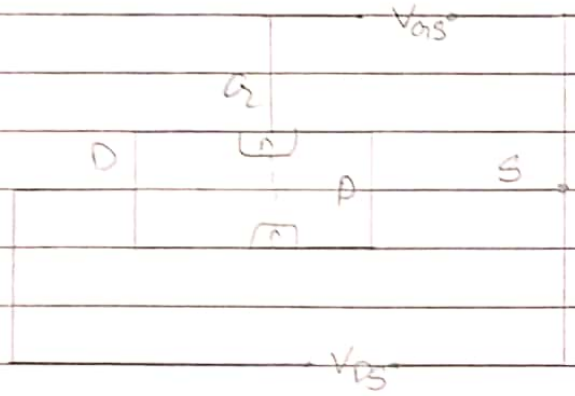
BJT	FET
	
- Consist of 3 terminals namely:- - Base - Collector - ~~Emitter~~ Emitter	Consist of 3 terminals namely:- - Gate - Drain - Source
- It is reffered to as transistor with bipolar junction	It is reffered to as transistor with unipolar junction.
- Operation is dependent on both charge carriers	Operation is performed due to majority of carriers it may be either due to electrons or holes.
- Known for current control	- Known for voltage control
- Offset voltage is required	- No offset voltage required
- Consumption of power is more	- Consumption of power is less
- Transistor gain is more	Transistor gain is less.

- Output value of impedance becomes high its gain value is high.	- Lesser the gain lesser will be its output value impedance.
- Used as an amplifier or switch which can be used as in mobile phones, industrial control, TV.	Used as amplifier in oscilloscope, electronic voltmeter.

Q2# The p-channel JFET the major portion is p-type in which the embedded are the 2 small n-type regions. Thus, it has n type gate and p type as source and drain causing the channel to be p-type where holes will be the majority charge carriers.



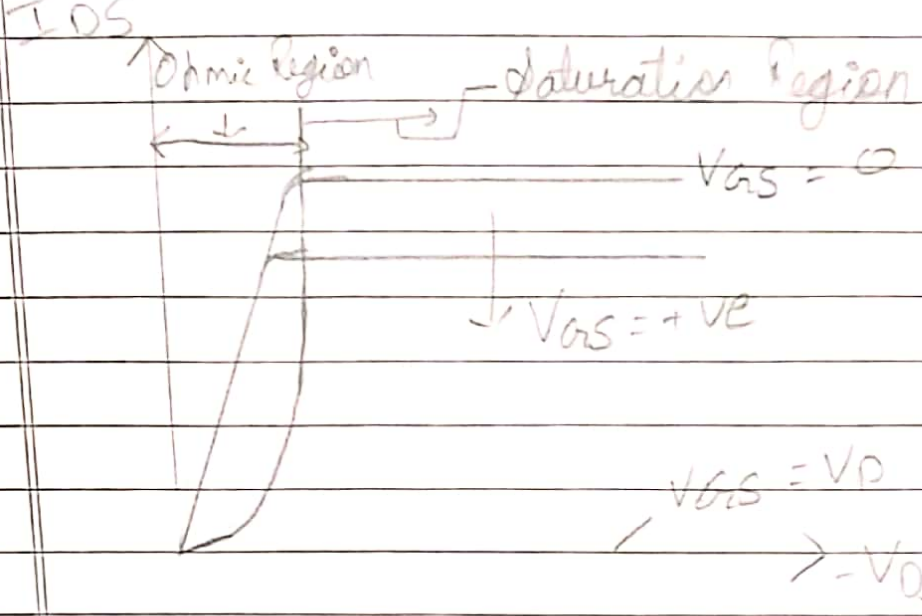
Working



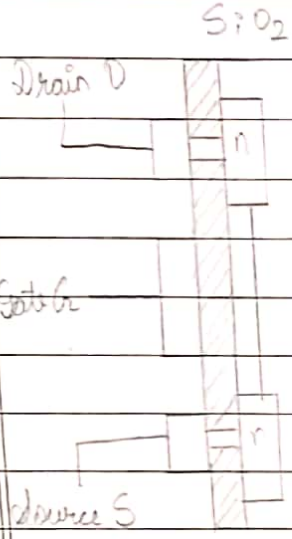
C-I: If $V_{DS} = 0$ and $V_{GS} = 0$, the device will be idle with no current [$I_{DS} = 0$]

C-II: Now, consider V_{DS} as -ve and $V_{GS} = 0$. At this state, the current flows from the source to the drain as the holes from p-substrate move towards the drain while being repelled from the source. The value of this current is restricted only by the channel resistance and is seen to increase with decrease in V_{DS} (Ohmic Region)

C-III: Now, let V_{GS} = +ve and V_{DS} = -ve. Here the effect exhibited is similar to that in C-II with the fact that saturation ~~region~~ occurs faster since V_{GS} becomes more and more +ve.



b.



In n-channel MOSFET the substrate is made up of p-type material and through metallic contacts the drain and source terminal are connected to the n type material. This oxide layer isolates the gate terminal ~~isolates~~ the and p-type substrate. But here, there is no channel between drain and source terminal. So, whenever we apply the control voltage between the gate and source terminal, then the channel is formed between the drain and source terminal. Here, the application of the control voltage enhances the no. of charge carrier in this region and due to that the channel is getting created that's why its called as enhancement type of mosfet.

Working

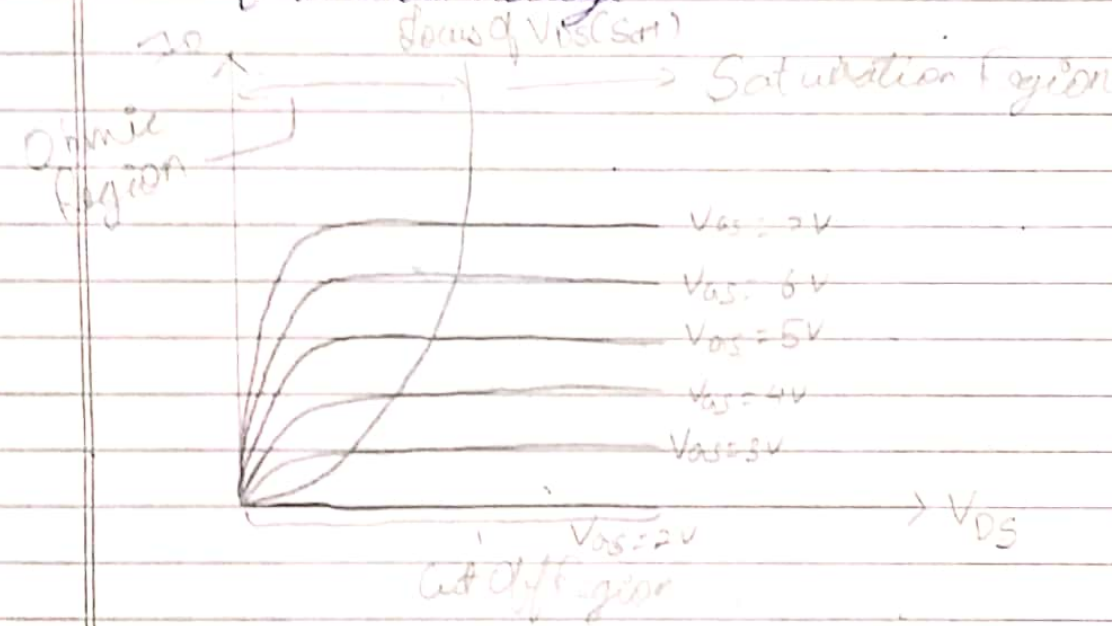
- When V_{GS} is kept 0 and the voltage is applied between the drain and source terminal due to absence of channel, there will be no flow of current through this MOSFET

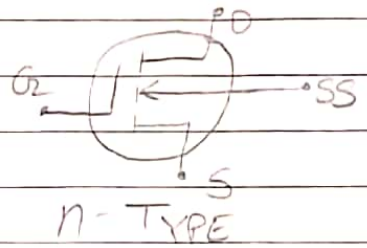
- When we apply +ve value of V_{GS} and for a moment assume that $V_{DS} = 0$. Now, holes are majority carriers in p-type substrate and whenever we apply the +ve voltage at this gate terminal, then the holes which are near this oxide layer will be pushed away from this gate terminal and at the same time, the electrons which are the minority carriers in this p-type substrate will also get attracted to this gate terminal. But, at lower ~~value~~ voltage of V_{GS}, these electrons will get recombined with the majority charge carriers. Now, as we keep on increasing V_{GS}, then the holes will be pushed more and more deeper into the substrate and the electrons will be able to overcome this recombination with holes and they will be sent to the gate terminal. But, due to this insulating layer, they will not be able to cross this oxide layer. And, they will start accumulating near this oxide layer. So eventually, the inversion layer of free electrons will be created near this oxide layer and this inversion region will act as a channel between ~~drain~~ drain and source terminal. And now, suppose if we apply voltage between drain and source terminal, then the current can flow through this channel. So, the value at which the gate to source is created is called THRESHOLD VOLTAGE and below this there will not be any flow of current.

When we apply V_{DS}, then electrons get attracted towards the positive terminal and in this way, current is established in the circuit and the conventional current will flow from drain to source terminal. Since the voltage at Drain terminal is high the width of depletion region will increase and due to that, the effective channel width towards drain terminal will reduce. So, the difference between drain and gate is given by $V_{GS} - V_{DS}$ and since the source terminal is grounded we can say that $V_G - V_{DS}$ so, as the value of V_{DS} will increase, then the difference between these 2 voltage will reduce. And as we keep on increasing V_{DS} then at one particular voltage the pinch off will take place and the voltage at which this pinch off condn. occurs is known as SATURATION VOLTAGE

$V_{DS[SAT]} = V_{GS} - V_t$

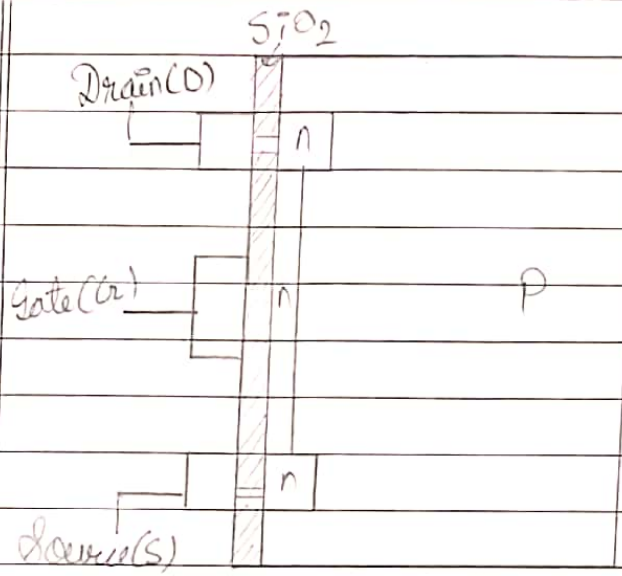
V_t = Threshold Voltage





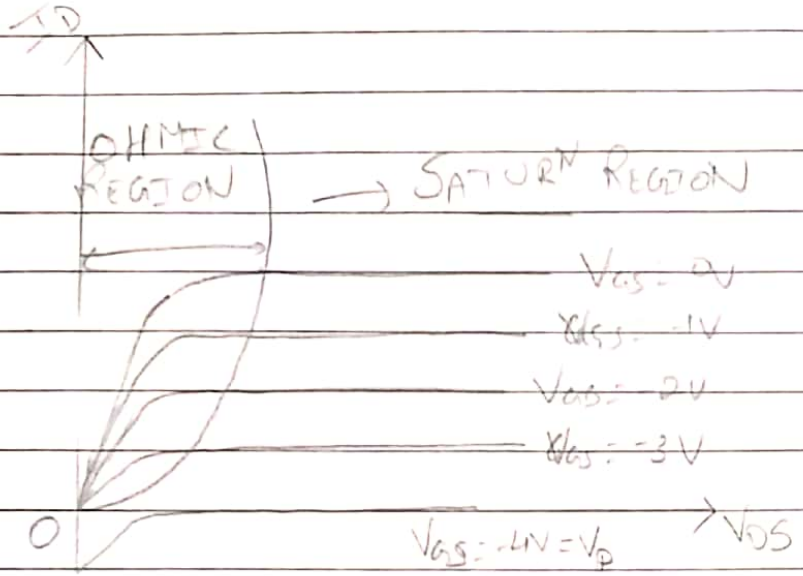
n - TYPE

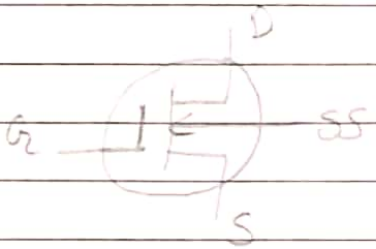
Co



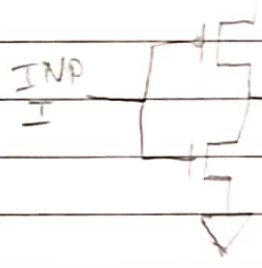
Working

Let us assume that gate and source terminal is connected together and connected to ground terminal and let's assume that $V_{GS} = 0$ and +ve voltage is applied between drain and source. So as we apply +ve voltage then the e^- in n channel will get attracted towards this +ve terminal. So in this way the current will get established in n-channel. So the conventional current will flow from drain to source terminal





Q4. CMOS is a technology used to develop IC. Its found in several devices like microprocessors, batteries, digital camera image sensor. CMOS transistor are known for their efficient use electrical power. They require no electric current except when they are changing from one state to another. The inverter circuit consist of PMOS 2 NMOS FET. The input A serves as Gate voltage for both transistors.



I	O
0	1
1	0

It usually serves as AND Gate.