SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: MBA. Tech (COMPUTER) Year: II Semester: III

Academic Year: 2015-2016

Subject: Computer Organization & Architecture

Date: 03/12/2015

Marks : 60
Time : 2.00 pm to 5.00 pm
Durations : 3 (hrs)

Final-Examination

Instruction: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.

NB:
1) Question No. **1** is compulsory.
2) Out of remaining questions, attempt any **FOUR questions.**
3) In all **FIVE** questions to be attempted.
4) Answer to each new question to be started on a fresh page.
5) Figures in brackets on the right hand side indicate full marks.
6) Assume Suitable data if necessary

Q.1 a. Compare Computer Organization and Architecture [4]

b. Define Following [8]

i. Bus Arbitration
ii. Pipelining
iii. Define SIMD and MIMD
iv. SRAM

Q.2 a. What are the main four components of any general purpose computer? Describe briefly. [6]

b. What do you mean by initialization of DMA controller? How DMA controller works? Explain with suitable block diagram [6]

Q.3 a. What do you mean by direct mapping method to determine the cache location to store memory block? [6]

b.Consider a cache (M1) and memory (M2) hierarchy with the following characteristics: [6]
M1 : 16 K words, 50 ns access time
M2 : 1 M words, 400 ns access time Assume 8 words cache blocks and a set size of 256 words with set associative mapping.

(i) Show the mapping between M2 and M1.
(ii)Calculate the Effective Memory Access time with a cache hit ratio of h = .95.

Q.4 a. Discuss Memory hierarchy in detail [6]

b. Explain the internal organization of bit cells in a memory chip which can store 16 words of 8 bit each. [6]

Q.5 a. Using booth's multiplication algorithm to multiply the following, showing all the steps. -8 x 2 [6]

b. Differentiate between single precision and double precision IEEE standard floating point representations with an example [6]

Q.6 a. Explain the 'instruction cycle' for the processing of a single instruction in a computer [6]

b. Explain following techniques to perform Input/ Output operations. [6]

(i) Programmed I/O mode

(ii) Interrupt initiated I/O mode

Q.7 a. Explain Instruction set format with example [6]

b Give the hardware organization of associative memory. Why associative memory is faster than other memories. Deduce the logic equation used to find the match in the associative memory. Explain how four-bit argument register is realized [6]