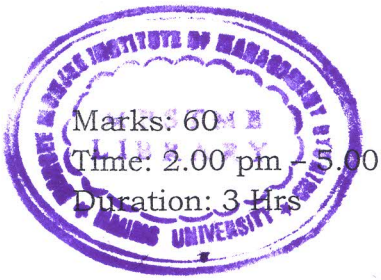
SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: MBA TECH (COMPUTER) Year: II Semester: III

Academic Year: 2015-16



Batch: 2015-16
Subject: Computer Organization & Architecture

Marks: 60
Time: 2.00 pm – 5.00 pm
Duration: 3 Hrs

Date: 13 June 2016

Re-Examination

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the answer book, which is provided for their use.

NB:

1. Question No. 1 compulsory.
2. Out of the remaining questions, attempt any 4 questions.
3. In all 5 questions to be attempted.
4. Answer to each question to be started on a fresh paper.

Q.1 (a) Explain functional view of a computer system. [06]

(b) Discuss Memory Hierarchy. [06]

Q.2 (a) Draw & Explain the Block Diagram of DMA Controller. Why read and write Lines of DMA controller are bidirectional? [06]

(b) Describe Parallel processor based on Instruction and data stream with the help Of suitable diagram. [06]

Q.3 (a) Explain RISC & CISC characteristics & comparison. [06]

(b) Multiply $(-7)_{10}$ with $(3)_{10}$ by using Booth's Multiplication. Give the Flow table of the multiplication. [06]

Q.4 (a) What are the different addressing modes supported by 8086 microprocessor? Explain each with examples. [06]

(b) Draw the timing diagram for a four segment pipeline showing the time it takes to process eight instructions. [06]

Q.5 (a) Explain Cache Memory Organization. Which mapping technique used in cache memory. [06]

(b) Compare & Differentiate Programmed I/O and Interrupt Driven I/O. [06]

Q.6 (a) Explain in detail the Element of Bus Design. [06]

(b) Explain the different between Hardwired Control and Micro programmed Control unit. Is it possible to have a hardwired control associated with a Control memory? [06]

Q.7 Write short note on (any two) [12]
(i) Instruction Set Architecture
(ii) Bus Arbitration
(iii) SRAM v/s DRAM
(iv) PCI Bus Architecture
