SVKM's NMIMS
MUKESH PATEL SCHOOL OF TECHNOLOGY MANAGEMENT & ENGINEERING

Programme: B.Tech (Computer) Year: II Semester: III

Academic Year: 2019-20

Subject: Computer Organization and Architecture

Date: 07 November 2019

Marks: 100
Time: 2.00 pm - 5.00 pm
Durations: 3 (hrs)
No. of Pages: 2

Final Examination (2019-20)

Instructions: Candidates should read carefully the instructions printed on the question paper and on the cover of the Answer Book, which is provided for their use.

1) Question No. _1___ is compulsory.
2) Out of remaining questions, attempt any __4___ questions.
3) **In all ___5_ questions to be attempted.**
4) All questions carry equal marks.
5) **Answer to each new question to be started on a fresh page.**
6) **Figures in brackets on the right hand side indicate full marks.**
7) **Assume suitable data if necessary.**

Sr. No		Questions	Marks
Q.1			
	a.	Explain the polling bus arbitration technique in detail with diagram.	6
	b.	Why is there a need for memory replacement algorithms? Three page frames (0, 1, 2) are present in the memory. The processor requires pages from virtual memory in the following sequence: 2,3,2,1,5,2,4,5,3,2,5,2 Find the HIT ratio using the implementation of FIFO and LRU	6
	c.	Compare Interrupt driven I/O vs Programmed I/O	4
	d.	What are addressing modes? Explain the following addressing modes with an example for each i) Immediate addressing mode ii) Direct addressing mode iii) Implied addressing mode iv) Register Relative addressing mode	4
Q.2			
	a.	Draw and explain the instruction cycle state diagram with interrupts.	10

b.	Explain Two way set associative mapping in detail with diagram. A computer architecture consists of 4 GB Memory, 16 MB Cache memory and Block size as 32 bytes. Find the physical address format (Tag size, Line size and Word size) for the computer for two way set associative memory.	10

Q.3

a.	Draw and explain the flowchart for Booth's multiplication. Using it, compute the answer for (10) * (- 5).	10
b.	Explain the typical Micro-programmed Control Unit in detail with diagram. Give its advantages, disadvantages and two applications.	10

Q.4

a.	Attempt the following questions:	10
i)	Compare RISC vs CISC computers	
ii)	What is the IEEE floating point standard for conversion? Convert the number $(148.25)_{10}$ into IEEE single and double precision format.	
b.	Explain Flynn's Classification in detail.	10

Q.5

a.	Explain the synchronous bus timing diagram in detail.	10
b.	Explain the 6-stage pipelining in detail with diagram. Also explain any two hazards of pipelining.	10

Q.6

a.	Explain the characteristics of memory.	10
b.	Explain DMA transfer mechanism for input-output units in detail with diagram.	10

Q.7

a.	What are micro-operations? Show the micro operations used for the following:	6
	i) ADD BL , 36 H	
	ii) MOV AL , [3000H]	
b.	Explain the daisy chaining method for bus arbitration with diagram	6
c.	Compare SRAM vs DRAM	4
d.	Explain the Von Neumann Architecture with diagram.	4
