ECE3270 Digital System Design
Lab 2: State Machines

Lab Overview: The purpose of this lab is to implement a state machine that keeps track of the current signal status. The state machine will then need to have the libraries signals added to work with OpenCL. The requirements of this lab consist of completing the VHDL design, submitting **ALL** modified source files to the box folder, and completing the report using the LaTeX template previously provided. You **MUST** include discussion of the state machine generated by Quartus (screenshot this for your report!!) and how this compares to your planned design.

Part I

You are to design a **Moore** state machine as described by exercise 14.25 in the book.

Include testbench(es) in your lab report and wrap this as a component on the board. It is suggested that you map the clock to KEY, as these pins have debouncing built in. The remaining inputs are best mapped to switches, and your outputs should be shown on LEDR.

Quartus will generate a state machine diagram if you follow the design method shown on slide 53 of Lecture 5a.

Submissions

You **MUST** upload all edited files to the Box Folder at Assignment 2 (include ALL edited files). You **MUST** also upload your report to Turnitin on the Canvas assignment.

Rubric	
Report - Proper format - All sections included - Valid images where applicable (if you wrote a testbench, include an image in the report of the waveform) - Proper grammar, punctuation, and spelling - **Refer to the lab manual for more information about the sections and guidelines when writing**	**50%** - 10% - 25% - 10% - 5%
Demo - Live Demonstration o Includes working code and answering questions from the TA - Proper modular design o Thoughtful I/O and Signal names included - Comments o Thoughtful comments, not English translations of code	**40%** - 30% - 5% - 5%
Proper Box Folder Code Submission	**10%**