# TIC1001—Introduction to Computing and Programming National University of Singapore

### Lecture 8: Memory & Cache

#### Question 1: DRAM vs SRAM

Select all areas where DRAM is better than SRAM in the following.

#### Speed, i.e. DRAM is faster than SRAM

Density, i.e. DRAM takes smaller space compared to SRAM

Simplicity, i.e. DRAM needs lesser components to build compared to SRAM

Power consumptions, i.e. DRAM needs less power to maintain compared to SRAM.

#### Question 2: Memory Hierarchy

With your new understanding, identify the different memory technologies that may be involved when your program tries to access a variable, e.g. "i = 123;"?

Register

Cache

Physical Memory (RAM)

External Storage (USB drive, network drive etc.)

Memory item get loaded into register.

Instruction "i = 123" and the data "i" both get loaded into cache.

Instruction and Data were in the RAM.

#### Question 3: Locality Principle – 1

If we have the following C code fragment:

What kind of locality does the instructions in the for-loop exhibits?

**Temporal Locality** 

Spatial Locality

None of the above.

The same instruction get executed multiple times (due to looping).

When an instruction get executed, the instruction nearby is needed soon (due to sequential execution).

## Question 4: Locality Principles - 2

If we have the following C code fragment:

What kind of locality does the elements of array[] exhibits?

None of the above.

As the element is accessed randomly, no locality is exhibited.

## Question 5: Cache Block Size

Cache block size is larger than word size because.....

**Temporal Locality** 

Spatial Locality

# Question 6: Fully Associative Cache

Given a FA cache with 4 blocks (i.e. cache index = 0, 1, 2, 3), how many cache misses are there for the following **block number** access?

#### 19, 7, 6, 2, 6, 2, 3, 19

You can assume that we replace the oldest block (block that was in the cache for the longest time) whenever needed.

| 19 |
|----|
| 7  |
| 6  |
| 2  |
| 6  |
| 2  |
| 3  |
| 19 |

| 19 |    |   |   |
|----|----|---|---|
| 19 | 7  |   |   |
| 19 | 7  | 6 |   |
| 19 | 7  | 6 | 2 |
| 19 | 7  | 6 | 2 |
| 19 | 7  | 6 | 2 |
| 3  | 7  | 6 | 2 |
| 3  | 19 | 6 | 2 |
|    |    |   |   |

| Miss |
|------|
| Miss |
| Miss |
| Miss |
| Hit  |
| Hit  |
| Miss |
| Miss |

# **Question 7: Direct Mapped Cache**

Given a DM cache with 4 blocks (i.e. cache index = 0, 1, 2, 3), how many cache misses are there for the following **block number** access?

19, 7, 6, 2, 6, 2, 3, 19

You can assume that we replace the **oldest** block (block that was in the cache for the longest time) whenever needed.

| 19 |
|----|
| 7  |
| 6  |
| 2  |
| 6  |
| 2  |
| 3  |
| 19 |

| 0 | 1 | 2 | 3  |
|---|---|---|----|
|   |   |   | 19 |
|   |   |   | 7  |
|   |   | 6 | 7  |
|   |   | 2 | 7  |
|   |   | 6 | 7  |
| 2 |   | 6 | 7  |
| 2 | 3 | 6 | 7  |
| 2 | 3 | 6 | 19 |

| 19 % 4 = 3 | Miss |
|------------|------|
| 7 % 4 = 3  | Miss |
| 6 % 4 = 2  | Miss |
| 2 % 4 = 2  | Miss |
| 6 % 4 = 2  | Miss |
| 2 % 2 = 0  | Miss |
| 3 % 2 = 1  | Miss |
| 19 % 4 = 3 | Miss |