Tutorial 07

1. If we call function f() in a loop:

**for** **(**int i **=** 0**;** i **<** 100**;** i**++)** **{**

f**();**

**}**

**What is the largest number of stack frame for function f() on the stack at any point in**

**time?**

1 Stack, stack frame for f()

1. **Sketch the stack frames for the following code when the execution reaches the point**

**indicated. Pay attention to the relationship between the various variables i . Also, find out what is the value of i in main() at the end of execution.**

Main() I = 0

Main() I = 0

f() I = 11

g() I = 22

f() I = 22

Main() I = 0

h() I = 33

Main() I = 0

g() I = 33

f() I = 33

#include <iostream>

**using** **namespace** std**;**

10. Input 0x969696 to h()

11. Update i pointer to 33

6. input 0x696969 to g()

7. Update i pointer to 22

9. Pass ref of i pointer to h()

12. i is now 33

3. input 0 to f()

4. i is now 11 in f()

5. Pass ref of i into g()

8. i is now 22

13. i is now 33

1. Initialization

2. Pass f(0)

Void h(0x696969)

i = 33

Void g(\*&i) = g(11)

i = ~~22~~

i = 33

h(22)

Void f(0)

i = ~~11~~

g(&i) = g(0x696969)

i = ~~22~~

i = 33

i = 0

f(i)

void h**(**int**&** i**)**

**{**

i **=** 33**;** // point α

**}**

void g**(**int**\*** i**)**

**{**

**\***i **=** 22**;**

h**(** **\***i **);**

**}**

void f**(**int i**)**

**{**

i **=** 11**;**

g**(** **&**i **);**

**}**

int main**()**

**{**

int i **=** 0**;**

f**(** i **);**

**}**

i in main() is still 0 after execution. Function f() neither return an i value nor update i via pointers.

3. Suppose we access the memory block in the following sequence:

Blocks: 6, 1, 1, 7, 6, 2, 3, 0, 2, 4, 5, 3, 5, 4, 0, 7

Given a cache that can hold 4 memory blocks, i.e. the cache indices are 0, 1, 2 and 3,

attempt the following:

**(a) If the cache is fully associative and we replace the “oldest” block when needed, calculate the number of cache hits.**

Replace older block LRA

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | Older | | Newer | |  |
| 6 |  | 6 |  |  |  | Miss | |
| 1 |  | 6 | 1 |  |  | Miss | |
| 1 |  | 6 | 1 |  |  | Hit | |
| 7 |  | 6 | 1 | 7 |  | Miss | |
| 6 |  | 6 | 1 | 7 |  | Hit | |
| 2 |  | 6 | 1 | 7 | 2 | Miss | |
| 3 |  | 3 | 1 | 7 | 2 | Miss | |
| 0 |  | 3 | 0 | 7 | 2 | Miss | |
| 2 |  | 3 | 0 | 7 | 2 | Hit | |
| 4 |  | 3 | 0 | 4 | 2 | Miss | |
| 5 |  | 3 | 0 | 4 | 5 | Miss | |
| 3 |  | 3 | 0 | 4 | 5 | Hit | |
| 5 |  | 3 | 0 | 4 | 5 | Hit | |
| 4 |  | 3 | 0 | 4 | 5 | Hit | |
| 0 |  | 3 | 0 | 4 | 5 | Hit | |
| 7 |  | 7 | 0 | 4 | 5 | Miss | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | Older | | Newer | |  |
| 6 |  | 6 |  |  |  | Miss | |
| 1 |  | 6 | 1 |  |  | Miss | |
| 1 |  | 6 | 1 |  |  | Hit | |
| 7 |  | 6 | 1 | 7 |  | Miss | |
| 6 |  | 1 | 7 | 6 |  | Hit | |
| 2 |  | 1 | 7 | 6 | 2 | Miss | |
| 3 |  | 7 | 6 | 2 | 3 | Miss | |
| 0 |  | 6 | 2 | 3 | 0 | Miss | |
| 2 |  | 6 | 3 | 0 | 2 | Hit | |
| 4 |  | 3 | 0 | 2 | 4 | Miss | |
| 5 |  | 0 | 2 | 4 | 5 | Miss | |
| 3 |  | 2 | 4 | 5 | 3 | Miss | |
| 5 |  | 2 | 4 | 3 | 5 | Hit | |
| 4 |  | 2 | 3 | 5 | 4 | Hit | |
| 0 |  | 3 | 5 | 4 | 0 | Miss | |
| 7 |  | 5 | 4 | 0 | 7 | Miss | |

**(b) If the main memory has an access speed of 50 ns, and the cache takes only 5 ns, what**

**is the average access time for the above accesses?**

7 hits, 9 misses. So,

**(c) Repeat (a) and (b) by using a direct mapped cache.**

1. In DM cache

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | 0 | 1 | 2 | 3 |  |  |  | |
|  |  | *0/4* | *1/5* | *2/6* | *3/7* |  |  |  | |
| 6 |  |  |  | 6 |  |  | 6 % 4 = 2 | Miss |
| 1 |  |  | 1 | 6 |  |  | 1 % 4 = 1 | Miss |
| 1 |  |  | 1 | 6 |  |  | 1 % 4 = 1 | Hit |
| 7 |  |  | 1 | 6 | 7 |  | 7 % 4 = 3 | Miss |
| 6 |  |  | 1 | 6 | 7 |  | 6 % 4 = 2 | Hit |
| 2 |  |  | 1 | 2 | 7 |  | 2 % 4 = 2 | Miss |
| 3 |  |  | 1 | 2 | 3 |  | 3 % 4 = 3 | Miss |
| 0 |  | 0 | 1 | 2 | 3 |  | 0 % 4 = 4 | Miss |
| 2 |  | 0 | 1 | 2 | 3 |  | 2 % 4 = 2 | Hit |
| 4 |  | 4 | 1 | 2 | 3 |  | 4 % 4 = 0 | Miss |
| 5 |  | 4 | 5 | 2 | 3 |  | 5 % 4 = 1 | Miss |
| 3 |  | 4 | 5 | 2 | 3 |  | 3 % 4 = 3 | Hit |
| 5 |  | 4 | 5 | 2 | 3 |  | 5 % 4 = 1 | Hit |
| 4 |  | 4 | 5 | 2 | 3 |  | 4 % 4 = 0 | Hit |
| 0 |  | 0 | 5 | 2 | 3 |  | 0 % 4 = 4 | Miss |
| 7 |  | 0 | 5 | 2 | 7 |  | 7 % 4 = 3 | Miss |

6 hits, 10 misses. So,

4. **(a) Given a main memory access speed of 100 ns, and a cache of 10 ns access speed, what**

**is the cache hit rate to give an average access time of 20 ns?**

**(b) Expand the same idea for 2 level caches:**

i. Main memory has access speed of 100ns.

ii. Memory block is loaded into a L2 (level 2) cache of access speed 20 ns.

iii. Memory block from L2 cache is loaded into L1 cache of access speed 10 ns. Suppose

L1 cache hit rate is 80% and L2 cache hit rate is 90%, what is the average access

time of this setup?