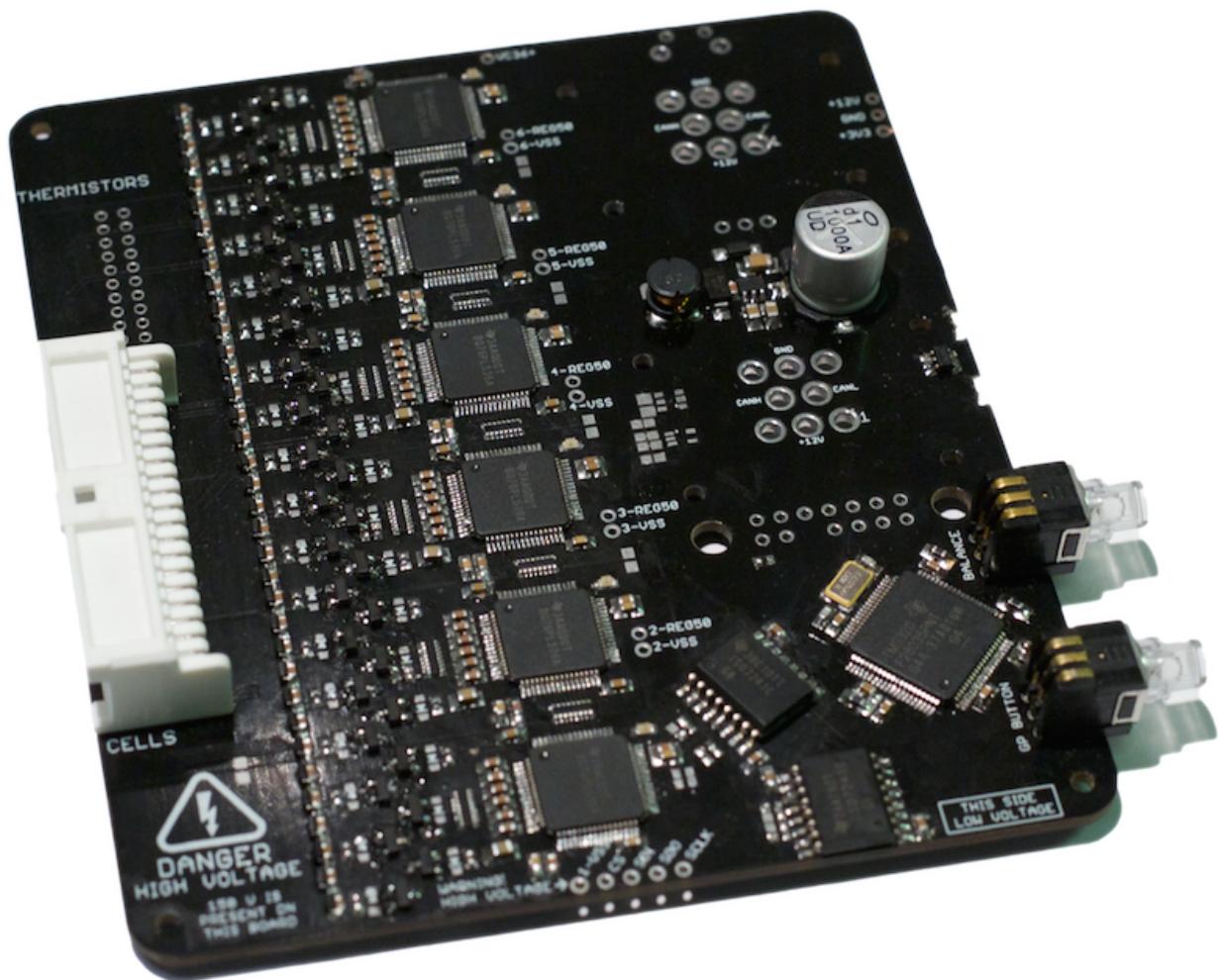


# Battery Interface Module

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## Introduction

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The Battery Interface Module is a 36-cell-capable lithium-ion battery monitoring circuit, designed to be installed on RW-2x, the second electric road racing motorcycle designed by Buckeye Current.



Figure 1: RW-2x, the electric road-racing motorcycle developed in 2013-2014 by Buckeye Current.

Buckeye Current is a student project team at the Ohio State University Center for Automotive Research, organized to design, build, and race electric motorcycles on road courses. The team's first motorcycle, RW-1, holds the collegiate electric motorcycle speed record at 144 mph. The second vehicle, RW-2, took third place in the prestigious Isle of Man TT Zero in 2013, and its successor, RW-2x, is due to compete at the 2014 TT Zero in June 2014.

Beginning with RW-2, the team has developed custom battery management hardware and software for their large lithium battery packs. The nominal pack voltage of RW-2 and RW-2x is 462 V, and the pack on RW-2x is 110 series cells, presenting formidable challenges for battery management system (BMS) hardware design.

As a team member and a technical lead, I have been developing the BMS system architecture and hardware since 2012. My entry for the 2014 TI Innovation Challenge is the most recent version of the battery management system hardware, developed during the 2013-2014 school year.

## Design history

The Battery Interface Module is the second generation of a battery monitor circuit based on the Texas Instruments BQ76PL536A Li-Ion battery monitor IC.

The first generation, the *Battery Management Module* (BMM), was capable of measuring 12 series cell voltages and four thermistor inputs, and included connectors that allowed access to the stack interface of the BQ76PL536A. Figure 2 shows a prototype Battery Management Module.

On the team's 2013 vehicle, RW-2, nine BMMs were installed in a daisy-chain configuration, spanning the 108-cell battery pack installed in the vehicle. Electrical isolation was provided by a separate PCB, the *BMM Iso*, and stack communications were managed by a control IC external to the system, using the Serial Peripheral Interface (SPI) protocol.

The BMM proved useful for battery measurement and balancing while the vehicle was otherwise inactive, but there were fundamental issues with the design:

- The BMM proved susceptible to electrical noise from the power inverter and the switch-mode power supply used to charge the battery pack. Stack communications were only reliable when no current was flowing in the high-voltage circuit.
- The large number of BQ76PL536A devices connected together in the communications stack caused large round-trip communications delays and required the use of an especially low SPI clock rate.
- The SPI protocol was poorly suited for the host interface. As installed on the vehicle, the cable length from the control processor to the BMM was long enough to present signal-integrity issues on the lines (ringing and overshoot), and the single-ended clock signal was prone to spurious clock edges when the power inverter was in operation.

For the 2013-2014 race season, I undertook a project to redesign the BMM from the ground up. The result is the *Battery Interface Module*, or BIM.

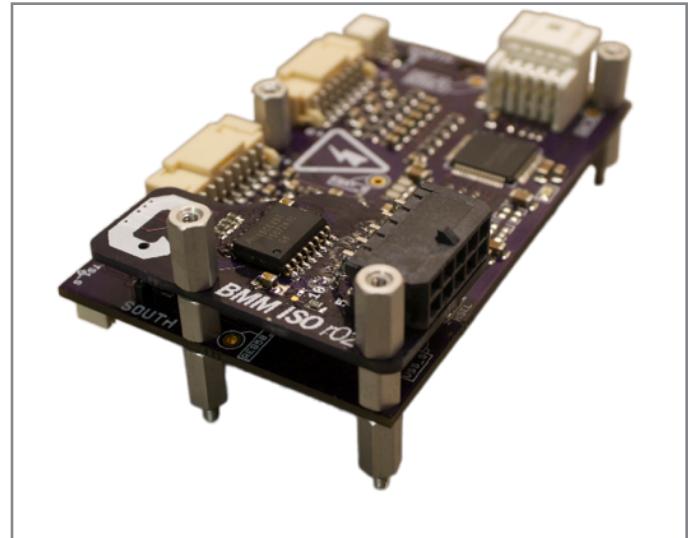


Figure 2: Battery Management Module (first generation).

The *BMM Iso* PCB, which provided an isolated communications interface, is mounted at the bottom of the BMM.

## Design

With the successes and failures of the Battery Management Module in mind, some key features of the Battery Interface Module were laid out:

- The stack height (number of daisy-chained battery monitor ICs) would be limited to 6 devices, in order to cap the maximum round-trip delay and resolve issues with stack communications. While multiple BIMs would still be installed on the vehicle, they would not be directly connected to each other.
- The control processor and isolated communications interface would be integrated into a single PCB to save space and improve signal integrity on the communications interface between the host processor and the battery cell monitor stack.
- The external communications interface to the module would use the Controller Area Network (CAN) protocol, which uses differential signaling at the physical layer and is much more robust to electrical interference than other single-ended communication schemes.
- The circuit board would be designed with accessibility and usability in mind, to address issues with mechanical integration and servicing experienced with the last generation.

Figure 3 shows the high-level block diagram of the BIM.

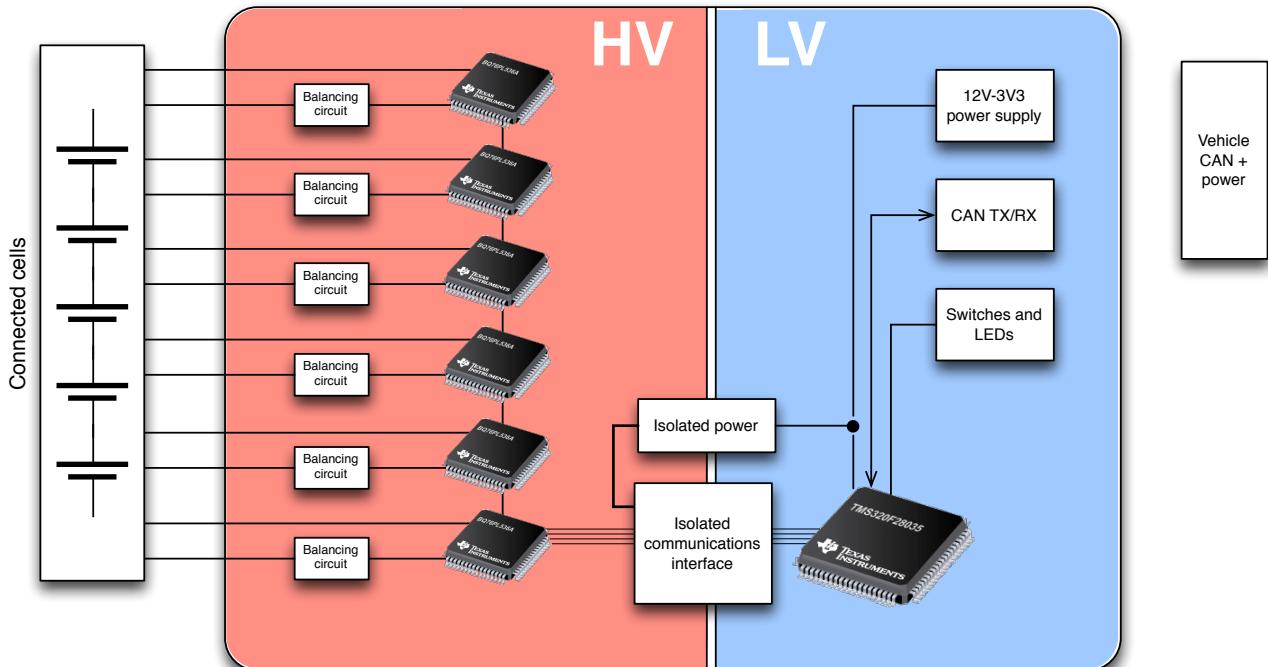


Figure 3: Battery Interface Module block diagram. The high-voltage and low-voltage circuits are connected by the isolated power and isolations communications interfaces, in the center of the figure.

The Battery Interface Module is a 9.8cm x 11.2 cm rectangular circuit board, 3.4 cm in height with connectors installed.

## Printed circuit board (PCB) layout

Based on experience with previous battery monitor designs and the requirements of the vehicle, I identified three design priorities for the Battery Interface Module:

1. Safety.
2. Noise robustness.
3. Accessibility, ease of servicing, and ease of testing.

These three priorities drove a number of design decisions:

### Electrical isolation

The team's safety policy requires that the high-voltage circuit (traction batteries, motor, and motor controller) is electrically isolated from the low-voltage circuit (CAN buses, low-voltage switching, accessories). Since the Battery Interface Module connects to both circuits, careful attention was paid to the interface between them.

#### High–to low–voltage interface

All communication between the BQ76PL536A stack and the host processor occurs between the base IC in the '536A stack and the host. The communications interface (Fig. 4) consists of four Serial Peripheral Interface protocol lines and four other asynchronous communication lines:

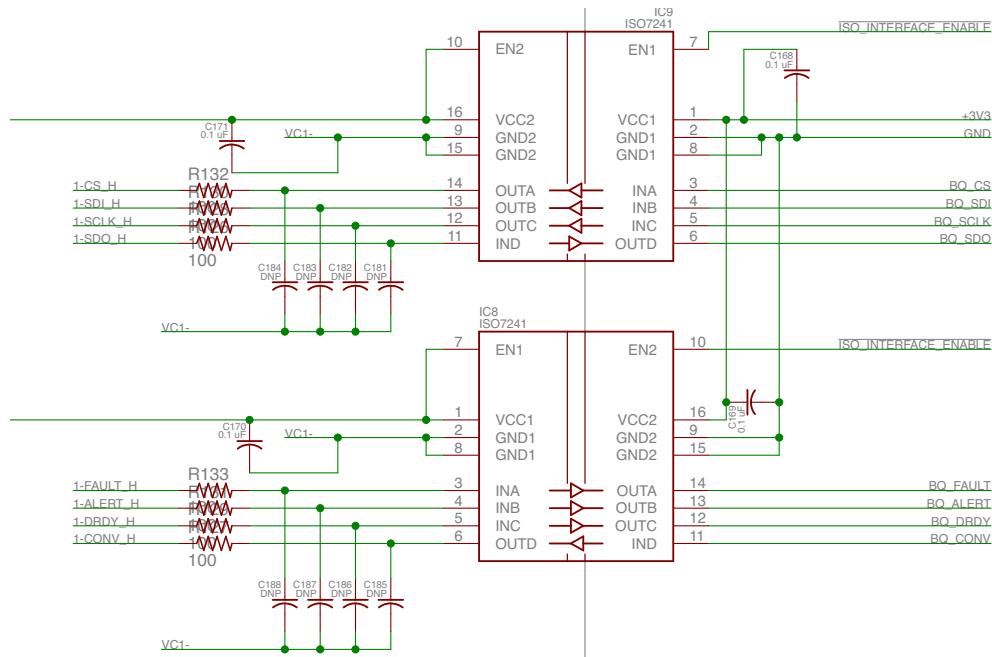


Figure 4: Isolated communications interface. The signals on the right side of the schematic are connected to the C2000 host processor; the signals on the left are connected to the host device in the BQ76PL536A stack.

The guidelines in section 2.10 of IEC standard 60950-1 were used to establish minimum creepage and clearance distances for the PCB layout. The minimum

acceptable creepage and clearance distances, as well as the creepage and clearance distances of the ISO7241C isolators used in the design, are listed in Table 1:<sup>1</sup>

**Table 1: Creepage and clearance distances on BIM**

	Minimum acceptable	ISO7241C
<b>Creepage distance</b>	4.6 mm	8.1 mm
<b>Clearance distance</b>	3.2 mm	8.34 mm

The PCB layout was arranged so that the pins on opposite sides of the isolators were the nearest conductors to either side of the isolation gap. Along the rest of the isolation boundary, 2 mm clearance was left between high- and low-voltage ground planes, well above the 0.1mm clearance required by IEC 60950-1 for coated conductors.

### Isolation between adjacent high-voltage ground planes

Within the high-voltage side of the circuit, there are six separate ground planes, one per IC. Figure 5 shows the layout of the ground planes on the PCB as viewed from the top of the board.

These ground planes are never exposed to open air except at the terminals of the devices they connect to. 0.75 mm clearance was left between adjacent ground planes on the high-voltage side of the PCB.

### Noise robustness (EMC)

The noise environment aboard the motorcycle is demanding. Space constraints mean that the module will necessarily be located very near the high-voltage circuit and power inverter, where large switching transients are present. Previous designs have suffered from communications failures and measurement inaccuracies when the power inverter is switching.

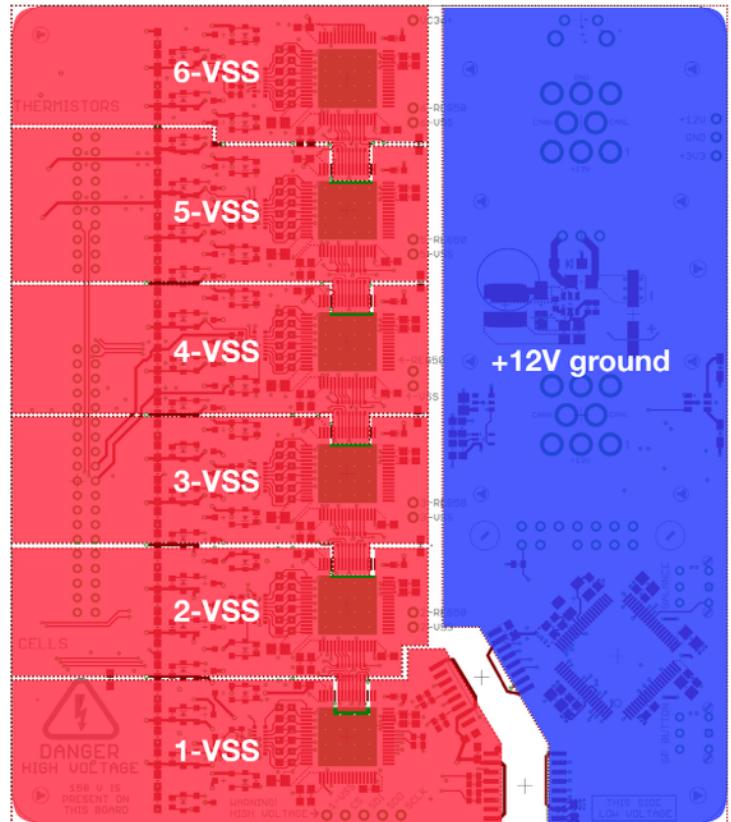


Figure 5: Ground planes on Battery Interface Module. The ground planes in red are connected to battery potentials, and the ground plane in blue is connected to the vehicle's low-voltage ground. All planes are isolated (floating) with respect to each other and the vehicle's chassis.

<sup>1</sup> Minimum acceptable clearance distances from IEC 60950-1, Tables 2K and 2N. Distances for ISO7241C ref. ISO7241C datasheet (SLLS868O), p. 16.

In attempting to reduce the effect of electromagnetic noise on device operation, two goals were set:

- Reduce the effect of noise on the measured cell voltages and temperatures..
- Reduce the effect of noise on stack communications.

To reduce the effect of noise on measurements:

- Solid ground and power planes were included in the PCB layout.
- When signal traces (e.g., the traces carrying current to and from a thermistor) were run for distances greater than 5 mm, they were run side by side to minimize the loop area of the traces.
- The cell voltage filter circuit was located directly adjacent to the measurement pins on the '536A ICs, with no vias between the filter circuit and the measurement pin.

In order to reduce the effect of noise on stack communications:

- The distance between adjacent ICs was kept to a minimum (5mm pin to pin).
- Ground planes were run beneath the stack communication traces as recommended in TI Application Report SLUA562, *Improving Communications With The BQ76PL536*, terminating beneath the lower IC.

## Accessibility

The BIM was designed with servicing in mind. To that end, a number of features were included in the PCB layout:

- Since the board would be mounted “top-down” in its enclosure, all test points, debug headers, and indicators were included on the reverse side of the PCB.
- Test points for common signals were included on the PCB so that they could be probed more easily during debugging. On the high-voltage side, test points signals which should not be shorted together were placed on opposite sides of a component so that short circuiting them inadvertently was more difficult.
- Unpopulated pads for RC filters and series resistances were included on critical communications lines, in case the PCB design did not provide adequate protection against electromagnetic noise.
- Pads were provided to allow the PCB to be populated with fewer than 6 'PL536A devices, in order to allow for pack configurations that are not evenly divisible by 36 cells.

## Balancing circuit

One of the most important functions of the Battery Interface Module is its ability to discharge individual cells in order to equalize the charge in each connected cell. The components and values selected for the balancing circuit were based on the battery modules used by Buckeye Current and the team's operational requirements, but the design choices made should make the BIM useful for any application using cells of a similar capacity.

### Time-to-balance and resistor selection

The battery modules used by the team are 40 Ah lithium nickel manganese cobalt oxide cells, arranged in a 110 series cell (110s1p) string.

Two different balancing scenarios were considered:

1. *Gross balancing*: correcting a difference in charge of greater than 1 Ah (3600 coulomb) between any two cells (typically because the cells have been discharged at different rates or in different packs)
2. *Maintenance balancing*: correcting a difference in charge of less than 1 Ah between any two cells (typically due to variations in internal resistance or self-discharge between cells in a series string)

In designing the BIM, it was assumed that the entire pack would be gross balanced before it was assembled; the balancing circuit on the boards is specified to perform maintenance balancing only.

At the cells' nominal voltage of 3.3 V, the balancing circuit discharges each cell at 70 mA. At this balancing current, using the balancing resistors selected for the design, the worst-case capacity imbalance of 1 Ah would require 14 hours to discharge. The team is always allotted at least 24 hours between practice laps to service the vehicle, so the balancing circuit's capacity is adequate.

## Thermal considerations

While balancing, the balancing power from the cells being balanced is dissipated as heat in the balancing resistors on the underside of the Battery Interface Module PCB.

All 36 balancing resistors might be powered on simultaneously if the connected cells are being balanced down to an external setpoint voltage. In this case, with each cell at its nominal voltage of 3.6 V, the balancing power dissipated on the PCB is 9.92 W.

The module is mounted in a sealed, unventilated plastic enclosure with surface area about 0.25 m<sup>2</sup>. Given the input power, the estimated temperature rise above ambient within the enclosure was roughly estimated at 15-20 °C.<sup>2</sup>

Although the predicted temperature rise falls within the acceptable limits of the components on the PCB, many of the enclosures are mounted directly to the battery pack, the skin temperature of which can reach temperatures of 50° C or greater

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<sup>2</sup> ref. "Heat Dissipation in Electrical Enclosures", [http://www.hoffmanonline.com/stream\\_document.aspx?rRID=233309&pRID=162533](http://www.hoffmanonline.com/stream_document.aspx?rRID=233309&pRID=162533)

during competition. In order to protect the devices from overheating, each board includes two thermistors located near the balancing resistor array. Figure 6 shows the locations of the balancing resistors on the underside of the PCB.

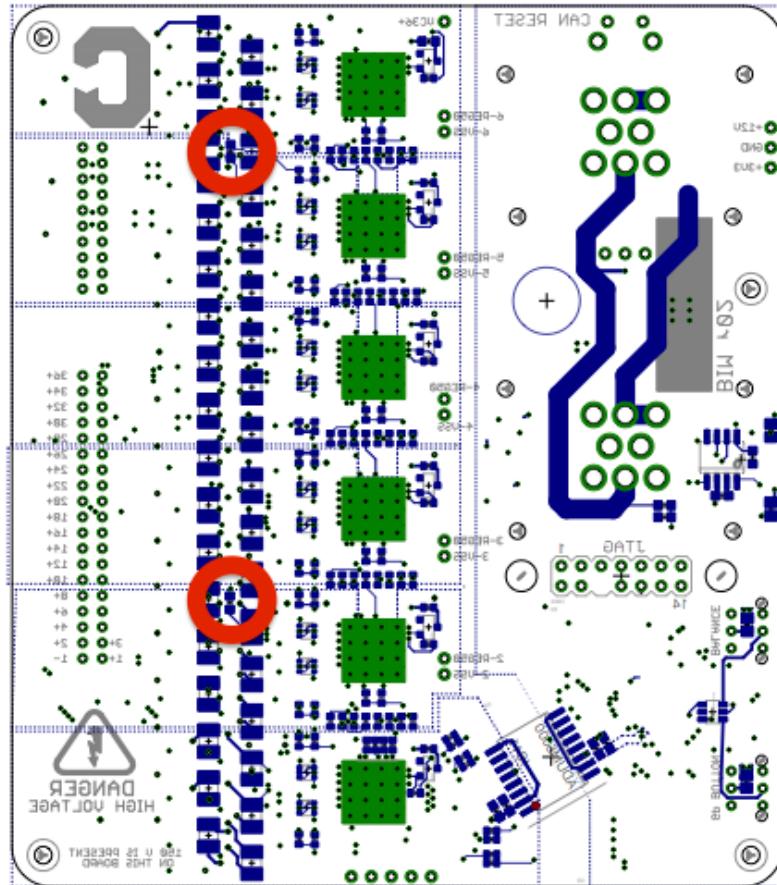


Figure 6: Balancing resistor thermistors (circled in red).

These thermistors are connected to the temperature measurement channels on devices 2 and 5. During balancing, the host processor is able to monitor the PCB temperature and temporarily halt balancing if it exceeds a threshold value.

## BQ76PL536A communications

### Timing

During competition, battery voltages are monitored for data logging and later performance analysis only: no control decisions are made in real time.

During balancing, the maximum balance current of ~95 mA means that even an update rate of 1 Hz would result in a maximum discharge of 0.00007% of the cell's 40 Ah capacity between measurements. This time granularity is sufficient to make control decisions (balancing start/stop).

The host processor must read 19 bytes in order to measure each of the 6 cell voltages and two thermistor measurements on each '536A device.<sup>3</sup> In order to read in all cell voltages from all devices at 1 Hz, and including the overhead in inter-packet delay time and CS line lead and lag delays, the minimum SPI clock rate is 912 Hz. This clock rate is easily achievable with the C2000's onboard SPI module; in the final design, a clock rate of about 62 kHz was selected for practical reasons related to the C2000's LSPCLK divider.

### Communications robustness

Electromagnetic interference is a serious concern on the vehicle. In previous designs, '536A stacks of more than 10 devices were unreliable due to interference and round-trip delays in the stack communications interface.

The stack communication circuit includes resistors at the origin of each current-mode signal to increase the holding current of the current-mode communications stack to about 10  $\mu$ A, in accordance with the recommendations in *Improving Communications With The BQ76PL536*.<sup>4</sup> This increase in holding current improves the signal-to-noise ratio of the current-mode communications.

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<sup>3</sup> Two bytes per cell voltage, two bytes per thermistor, one byte address, one byte read length, one byte CRC.

<sup>4</sup> Texas Instruments Application Report SLUA562

## Power supply

The Battery Interface Module is designed to be connected to the vehicle's CAN bus through a standardized 8-pin CAN interface, which provides +12V power from an auxiliary battery. The input voltage is unregulated and can vary between 9 V and 15 V during normal operation.

The primary load on the low-voltage side of the PCB is the C2000 processor, which draws about 100 mA during normal operation and a maximum of 153 mA. Other loads on the low-voltage power supply are listed in Table 2:

**Table 2: Low-voltage current budget**

<b>Load</b>	<b>Current consumption</b>	
	Typical	Maximum
<b>Host processor: TMS320F28035</b>	100 mA	153 mA
<b>Indicator LEDs (4)</b>	60 mA	80 mA
<b>CAN transceiver: SN65HVD230</b>	10 mA	17 mA
<b>Isolated interface: primary side (ISO7241C)</b>	12 mA	18 mA
<b>Isolated interface: secondary side</b>	40 mA	60 mA
<b>Other loads</b>	10 mA	20 mA
<b>Total</b>	<b>232 mA</b>	<b>348 mA</b>

Another Texas Instruments IC, the LMR14206, was selected as the switch-mode power supply controller and switch. The LMR14206 is a step-down converter IC with a fixed switching frequency of 1.25 MHz and an integrated switch. Its wide input voltage range makes it particularly suitable for the BIM, whose input power is an unregulated supply from an auxiliary battery.

Texas Instruments' WEBENCH online design tool was used to select component values for the step-down power supply circuit, based on a typical input voltage of 14 V and a desired output voltage of 3.3 V. Based on the expected typical load current of 150 mA (without indicator LEDs), the power supply efficiency is about 82%.<sup>5</sup>

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<sup>5</sup> LMR14206 datasheet, TI literature number SNVS733D, page 1

## Power loss detection and safe shutdown functionality

While the thermistor circuits are powered up, they draw supply current that can be as high as about 2.5 mA. During normal vehicle operation, this load is not significant, but if the devices are powered up and connected to cells for an extended period of time, the drain on the cells could cause some to be discharged beyond their minimum open-circuit voltage. Furthermore, this supply current contributes to pack imbalance (the current is drawn only from every sixth cell in the pack).

If the C2000 controller IC on the Battery Interface Module loses power while reading cell voltages, the BQ76PL536A stack could be left in a high-power state. To prevent this, a power loss detection circuit is included in the design, and an onboard capacitor provides sufficient energy to power the C2000 processor while the ‘536A stack is put into a low-power state.

### Detection

The power supply circuit in the Battery Interface Module includes a voltage divider connecting the +12V input to one of the comparator inputs on the processor, shown in Figure 7:

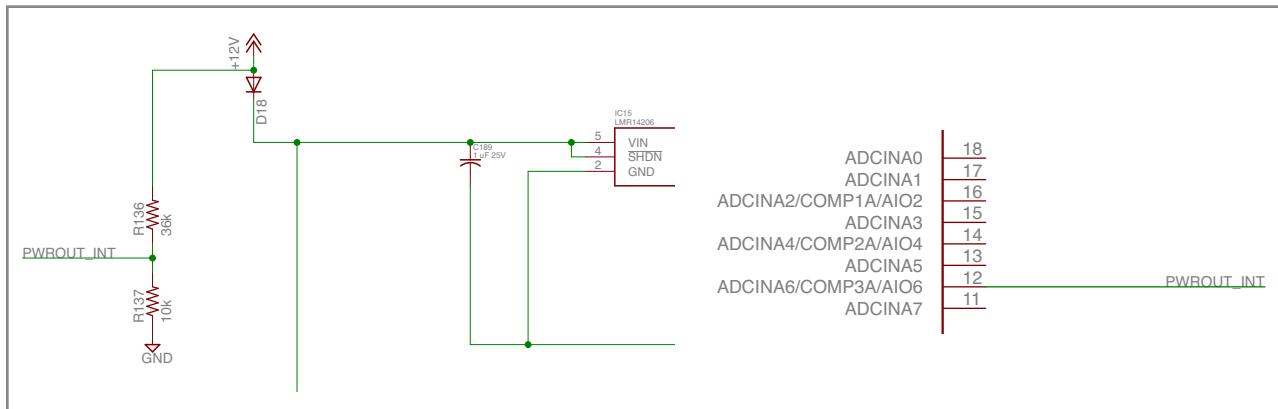


Figure 7: Power loss detection circuit. The voltage divider R136-R137 scales the input +12V power so that +12V undervolt can trigger the comparator COMP3A.

The comparator COMP3A triggers an interrupt that puts the BQ76PL536A stack into a low-power state when the +12V input falls below a configurable threshold.

The Schottky diode D18 on the input doubles as reverse-polarity input protection for the +12V input.

### Timing

The sequence of writes required to put the stack into a low-power state is three bytes long:

7F 31 04 D0    7F 20 04 92    7F 20 00 8E

The minimum time required to shut down the stack is dominated by the SPI communications time. With an SPI clock of 125 kHz, the SPI communications time

is 15.9  $\mu$ s. To accommodate for other delays in execution, the minimum execution time specified for the power loss capacitor is 20  $\mu$ s.

With the 3.3V bus at its minimum voltage of 3.2 V, and assuming a bus load of 200 mA, the minimum capacitor size is 17.4  $\mu$ F. A readily available 1000  $\mu$ F capacitor easily satisfies the minimum execution time requirement and provides headroom for additional tasks should they be necessary in the future.

## Manufacturing

The printed circuit fabrication was done by a third-party fabrication house. The circuit layout was done with 6 mil ( $\approx$ 0.15 mm) clearance between adjacent signals (“6/6 trace/space”), and a minimum via drill of 10 mil ( $=$ 0.254 mm), in order to ensure the PCB could be manufactured at moderate cost at a wide variety of PCB fabrication houses.

Due to budget constraints, all component population and final assembly was done by hand, using manual soldering, hot-air rework, and a custom reflow process.

## Solder reflow

The BQ76PL536A has a thermal pad on the underside of the package that must be soldered to the board. In order to inexpensively reflow this solder joint, a procedure was developed using a laboratory hot plate, summarized below:

1. All components on the top side of the PCB are populated by hand, except the BQ76PL536As. Solder paste is applied to the central pad of the BQ76PL536A footprints on the PCB.
2. The ‘536A devices are placed on the PCB, and the remaining pins are soldered manually, using the method of drag soldering.<sup>6</sup>
3. The PCB is cleaned of flux and residues using a solvent, and fresh soldering flux is applied.
4. The PCB is placed on a hot plate set to 250-300° C and left until all visible solder joints have reflowed. (Figure 8). It is removed immediately from the hot plate and left to cool in air.



Figure 8: Hot plate reflow. The PCB (black) is in the center of the hot plate.

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<sup>6</sup> The drag soldering process is described, for example, here: <http://www.howardelectronics.com/jbc/dрагsoldering.html>

## Prototyping and validation

Several prototypes were built and tested before the final modules were installed on the vehicle. The prototyping process revealed several issues with the design requiring modifications to the circuit and the manufacturing procedure.

### Manufacturing

While the hot-plate reflow method reduced the costs of manufacturing, it required about 2 hours total manual inspection time per PCB manufactured. The reliability of the process was poor, with nearly 50% of assembled boards requiring some manual rework.

The most common issues observed was poor quality of solder joints on the BQ76PL536A device pins. Often, the solder would wet to the pad without joining to the device pin. Cleaning the device thoroughly with acetone, refluxing, and reflowing the pins would often resolve the issue; this resulted in the addition of step 3. in the solder reflow process above.

Taking into account device losses due to manufacturing errors and the additional manufacturing time required, the cost of the hot-plate reflow method was nearly equal to the cost of having the boards assembled at a prototype fabrication facility. Professional assembly would ease debugging, increase device reliability, and increase speed of fabrication. It is recommended for future production.

### Hot-plug issues

The first BIM prototypes were tested successfully when BQ76PL536A ICs were powered individually, but when testing with a full battery pack, an issue was observed where one or more ICs would be destroyed when the cell connector was plugged in to the board. Figure 9 shows a destroyed device. The device destruction was not consistent: some ICs which had survived several plug-unplug cycles would be destroyed on a later connection.

The damage to the IC was often in the same area near pins 3 and 4, which was found to be near the wire bond pads for the BAT1 and BAT2 pins.

I suspect the device destruction issue was caused by the large inrush current through the BAT1 and BAT2 pins when the device support capacitors are charged.

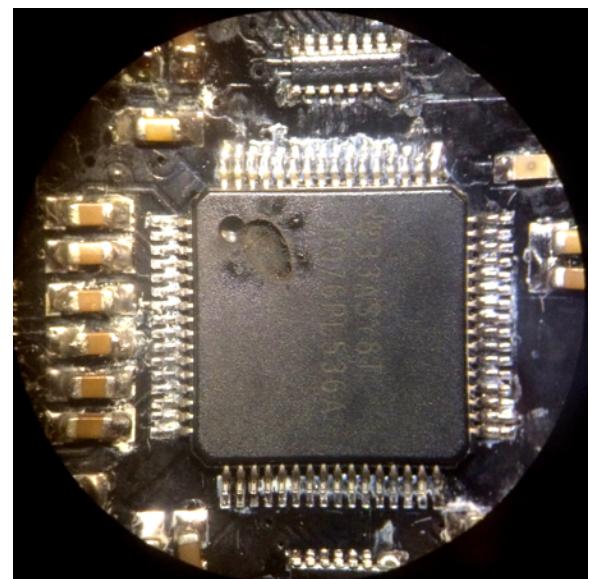


Figure 9: BQ76PL536A destroyed on connection to cells

Figure 10 shows the capacitances that are charged by the inrush current on device connection. All capacitances listed are low-ESR ceramic capacitors.

In order to reduce the inrush current during hot-plug, a  $5\Omega$  series resistor was added in series with the device power path, between the BAT pins and the connected cell. This modification resolved the issue, and it will be included in the next revision of the circuit board.

## Zener diode placement

Early revisions of the BIM schematic included 5.1V Zener diodes connected between cell voltages to protect against overvoltage inputs and provide a path for hot-plug currents to flow (Figure 11).

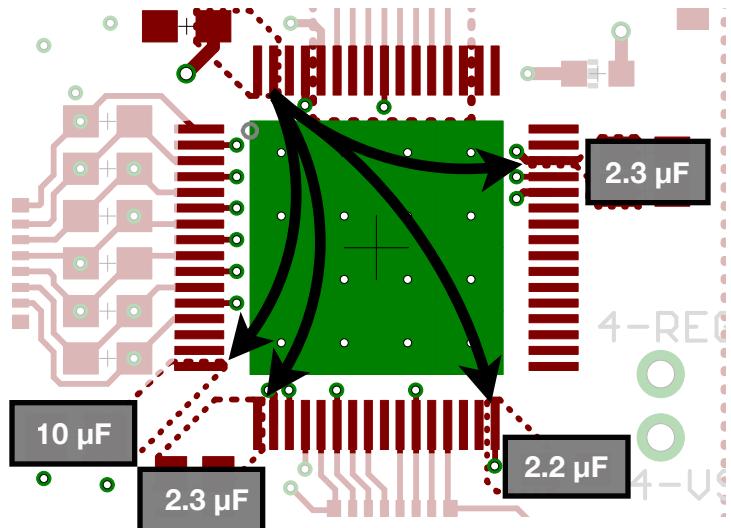


Figure 10: Capacitances charged by inrush current. The BAT pins are visible in the upper-left corner of the device. The black arrows represent the direction of current flow when the device is connected to power (although they do not represent the physical current path).

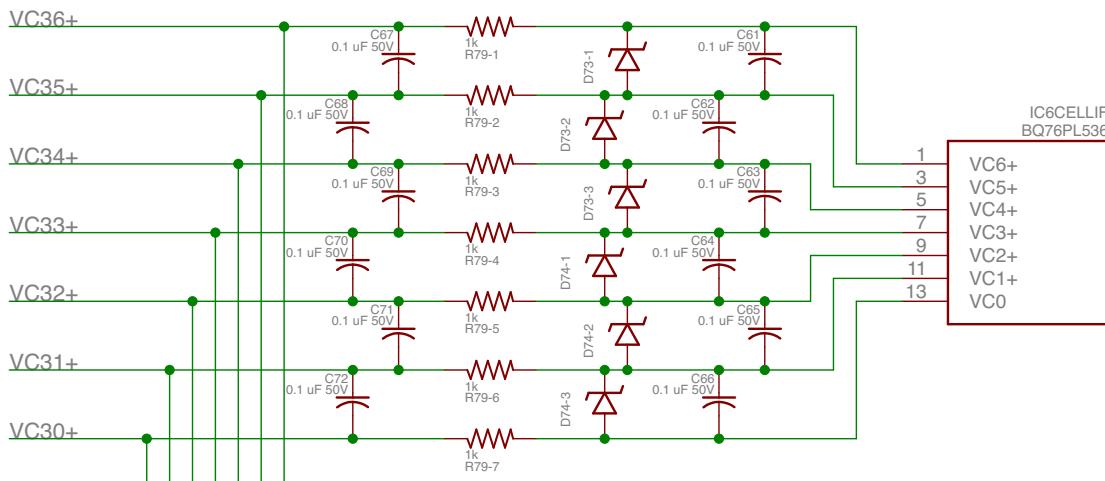


Figure 11: Zener diodes between cell voltages (here, D73 and D74 1-3)

The diodes were connected after the 1k series resistor in order to limit fault currents in the event that a cell was connected backwards. However, the component selected, a packaged diode array, had a turn-on characteristic that resulted in a small current flowing at higher cell voltages ( $>4.0$  V). The voltage drop across the 1k series resistor affected measurement accuracy where it is most critical.

The Zener diodes in question were not populated in later prototypes, and discrete 5.1V diodes were connected on the opposite side of the 1k series resistor, in parallel with the first cell filter capacitors (C67–C72 in Figure 11). In addition to improving

measurement accuracy, TI application engineers suggested that the hot-plug reliability might be improved by this configuration.

Cell overvoltage protection and cell reversal protection is maintained in this configuration, although only in the transient case. Protection against continuous reverse connection of battery cells will be provided by keyed battery connectors on the cell side of the wiring harness.

## Thermal performance

A thermal camera was used to observe the heat distribution on the PCB in a typical balancing situation, with about 20% of the resistors enabled. Figure 12 shows the temperatures of the balancing resistors after about 1 minute of balancing.

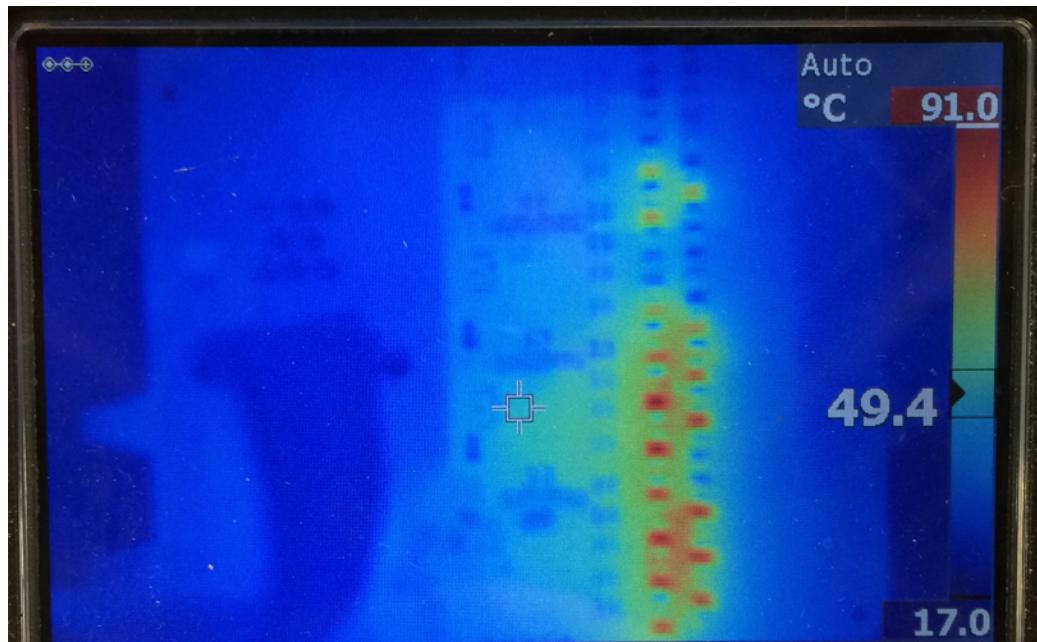


Figure 12: Temperature of balancing resistors during cell balancing

While this test does not prove the device will not overheat in its enclosure, it allows the team to make preliminary estimates of the duty cycle capability of the balancing resistors. Based on the results of this test and the analysis performed during design, I expect the Battery Interface Module to correct up to 1 Ah of cell imbalance within the targeted balance time of 24 hours.

## Communication issues

Communications with the host device in the BQ76PL536A stack were sometimes unreliable, and this behavior was unpredictable.

### No reply from device (0xFF)

Several prototype devices failed to reply to any reads or writes from the host processor. In some cases, these devices would clock out only **0xFF**. For example:

```
SDI: 00 00 01 00 00
SDO: FF FF FF FF FF
```

This issue occurred intermittently, and finding a definitive cause was difficult. In some cases, the stack would begin clocking back **0xFF** only after a certain device was addressed. In those cases, the root cause was usually a poor electrical connection to the device just above the one that had just been addressed. For example, during one troubleshooting session, the stack began clocking out **0xFF** after device 2 was addressed. The problem was found to be a poor solder joint on the series resistor in the communications lines between devices 2 and 3. This issue can cause communications with the entire stack to fail if there is an issue with a single connection on a single IC.

To mitigate this issue, a thorough visual inspection and electrical test of the components in the communications circuit was performed on each PCB before it was installed on the vehicle.

### No reply from device (0x00)

In other cases, the stack would reply only **0x00** to all reads and writes, in the same way as the **0xFF** issue described above.

This issue was also intermittent, and less common than the **0xFF** issue. Sometimes, cleaning the boards thoroughly with acetone would resolve the issue. I suspect that contamination from the fluxes used during the hand soldering process causes spurious currents somewhere in the stack communications circuit.

The issue was mitigated by cleaning each board before it was installed in the vehicle. The enclosures are sealed and designed to exclude contamination.

## Results

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As of May 2014, seven working Battery Interface Modules have been built and tested (five modules are installed on the vehicle, plus two spares). Buckeye Current has developed software to interface the BIM with the vehicle's CAN bus, including network functionality that allows the five BIMs installed on the vehicle to communicate with one another to balance the full battery pack.

The modules underwent on-vehicle testing in March 2014 and performed well, with one communications dropout during four days of high-speed track testing.

In June 2014, the Battery Interface Module will ride on RW-2x in the 2014 Isle of Man TT Zero, on one of the most demanding road race circuits in the world, the Snaefell Mountain Course. During the practice laps, the circuit will allow the team to identify and troubleshoot issues with powertrain thermal and electrical performance, and data gathered from the BIM during this year's competition will be critical to the design of RW-3 in 2014-2015.

## Acknowledgements

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Thanks to Prof. Marcello Canova, for his support of the team and me both. And, as always, thanks to Prof. Betty Lise Anderson, for always-prompt, always-insightful editorial guidance and support.

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