APPLICATION NOTE

Product Name	**S76G** **LoRa and GNSS Wireless Communication Module**
Version	**C**
Doc No	**902-10701**
Date	**Apr 2nd 2019**

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Document History

Date	Revised Contents	Revised By	Version
2017/12/19	Initial release	Kenny	A
2018/03/20	Update reference circuit	Kenny	B
2019/04/02	RF external components and interference for GNSS receiver	Jack	C

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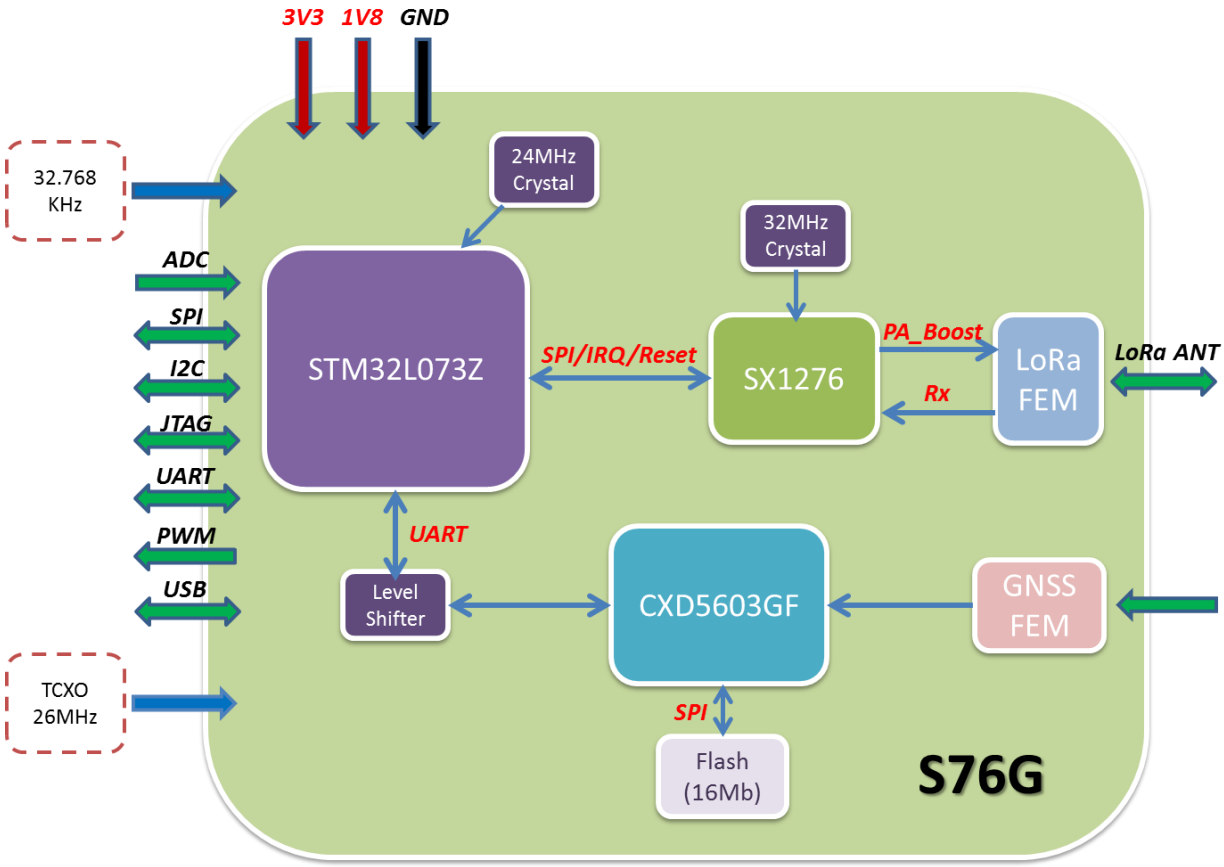
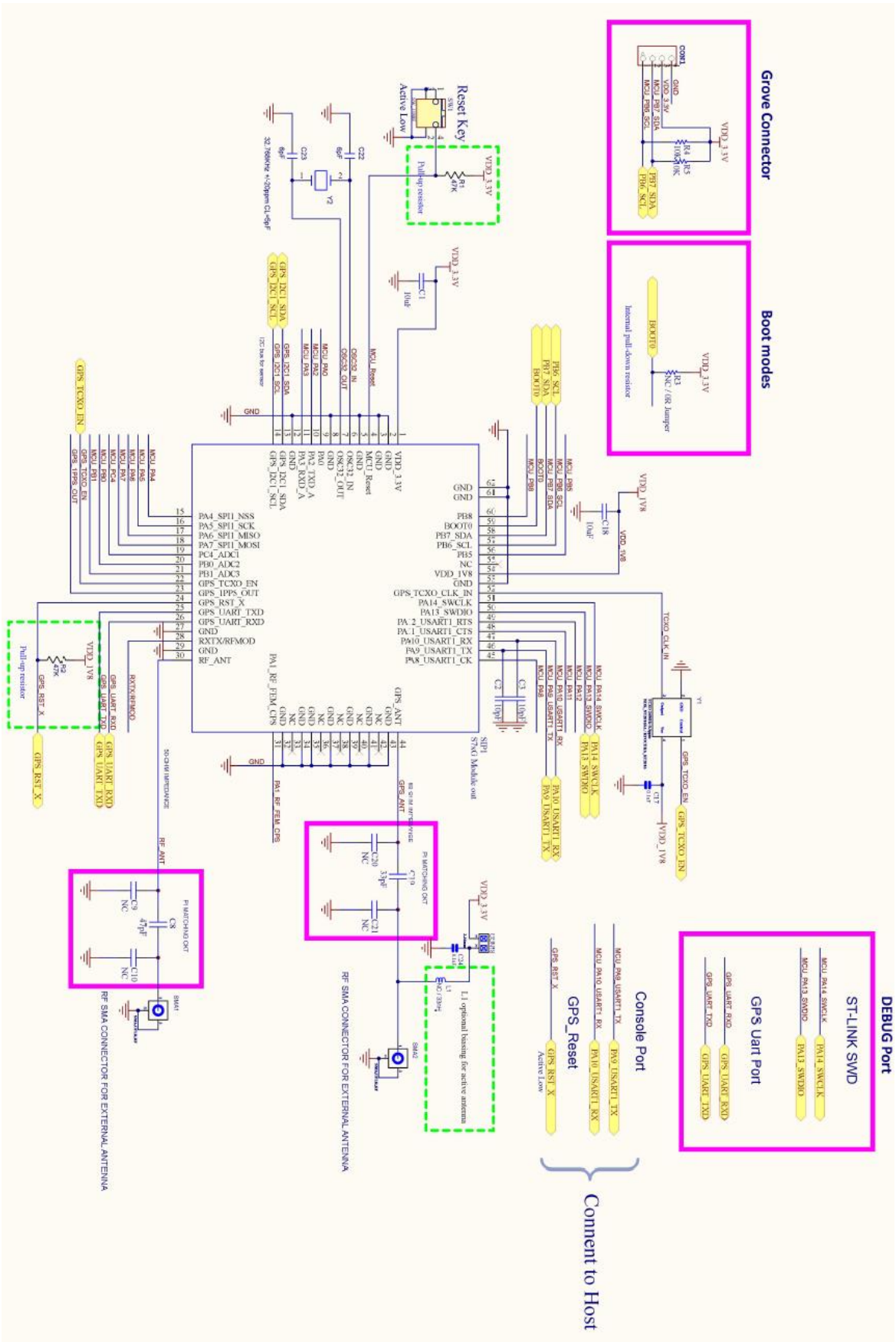
1. Block Diagram



Supporting global 868 MHz or 915 MHz ISM-Bands.

2. Application Circuit



3. Layout Guide

3-1. Power Trace Management

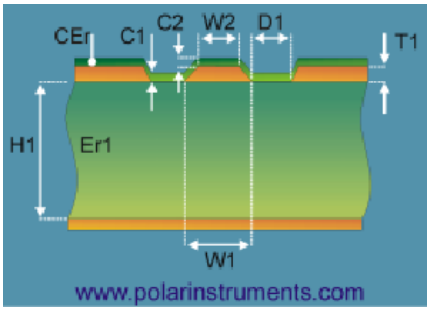
- Power traces should be directly connected with regulator outputs. And add 10uF bypass capacitors close to module on each power trace.
- Never let power trace cross the other one or high speed signal trace.

3-2. Ground Management

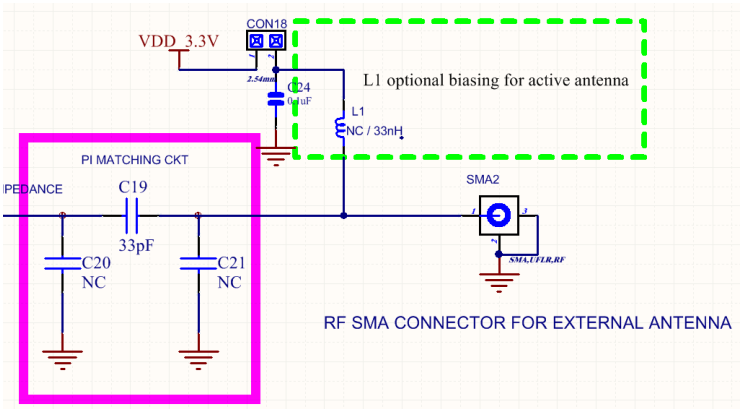
- Please ensure: (1).GND polygon regions used for module are as complete as possible and (2).well established GND via holes, in order to keep good heat dissipation and RF performance.
- The ref. ground planes of RF trace need to add via holes and we recommend the distance between each adding ones less than 1/8λ.

3-3. RF Trace Management

- CPWG model is recommended for RF trace calculation, which has better EMC and RF capability. And please discuss with PCB manufacturer to evaluate and keep RF trace in 50ohm.

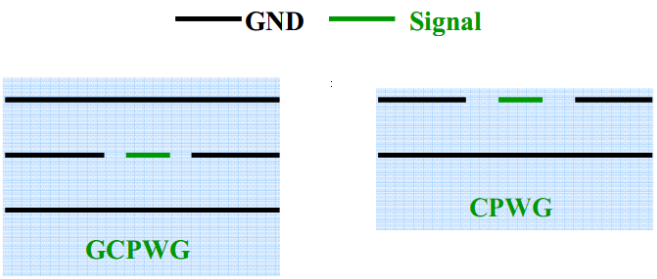


- Suggest customer deploy Pi-matching circuits close to Lora / GNSS antennas.
- L1(33nH_LQW18AN33NJ10)/C24/CON18 are optional biasing circuitry for GNSS active antenna.



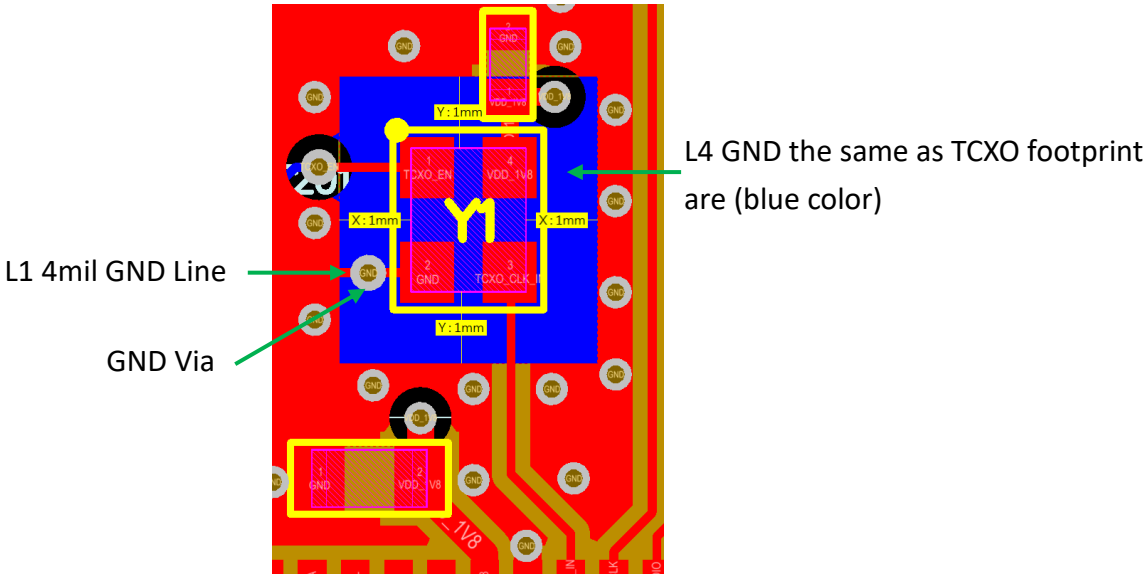
3-4. 26MHz TCXO Management

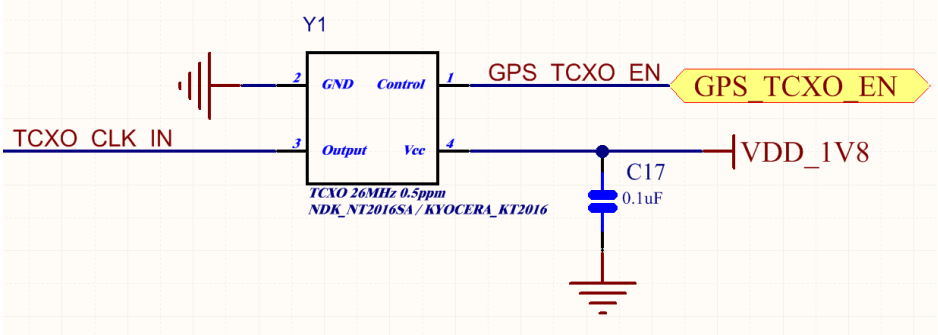
- Keep TCXO as close as possible to S76G or will cause signal swing and EMC problems.
- Keep signal trace of 26MHz in CPWG/GCPWG model to prevent Rx de-sense issue.



- Instructions for TCXO layout:
  - L1~L3 Forbidden (keep-out) area is green rectangle shown as below figure.
  - R or C can put cross the GND gap
  - Reserve Bottom GND below TCXO and its area is the same as TCXO footprint
  - Power branch trace width toward TCXO is 6mil
  - GND pin connection trace width is 4mil

  Example:





- Recommended Parts List

  Nihon Dempa Kogyo Co., Ltd. / NT2016SA (26MHz +/- 0.5ppm)

  KYOCERA Crystal Device Corporation / KT2016 (26MHz +/- 0.5ppm)

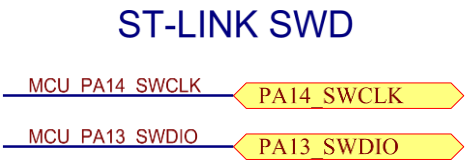
3-5. Shielding Land

- Please reserve solder mask opening area for EMC shielding, which must enclose S76G relative circuitry, like TCXO/32K/de-cap,..etc.

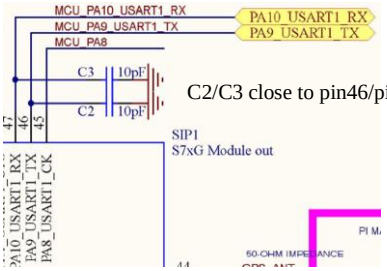
3-6. Other peripheral schematic

- ST-LINK SWD Port

  User needs to connect this two SWDIO & SWCLK pins with ST-LINK/V2 unit.



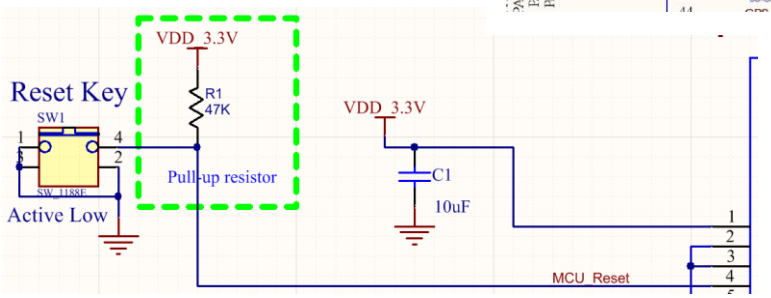
- UART1 Console Port



C2/C3 close to pin46/pin47

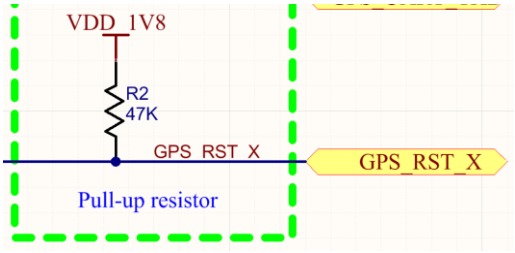
- MCU Reset

  System Reset, Active Low.

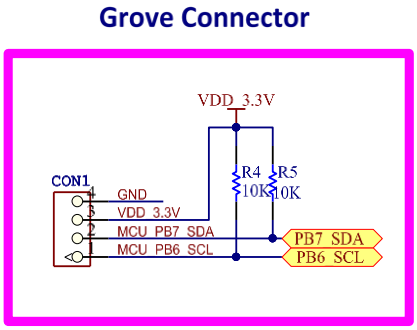


- GPS_RST_X (in 1.8V voltage domain)

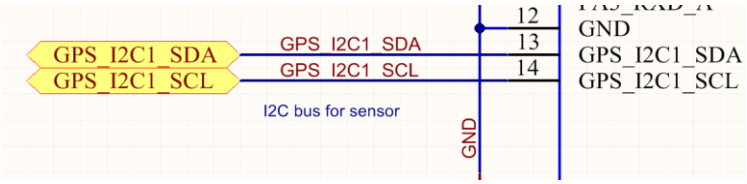
  GPS Reset, Active Low



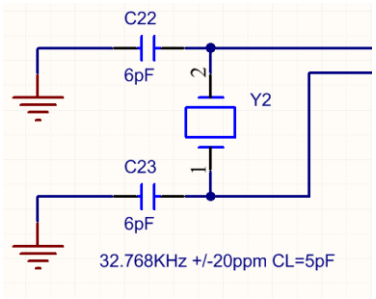
- I2C



- GPS I2C bus for sensor (in 1.8V voltage domain)
  Equipped with Sensor Fusion functionality, realizing seamless and high-precision position measurement for both indoor and outdoor location

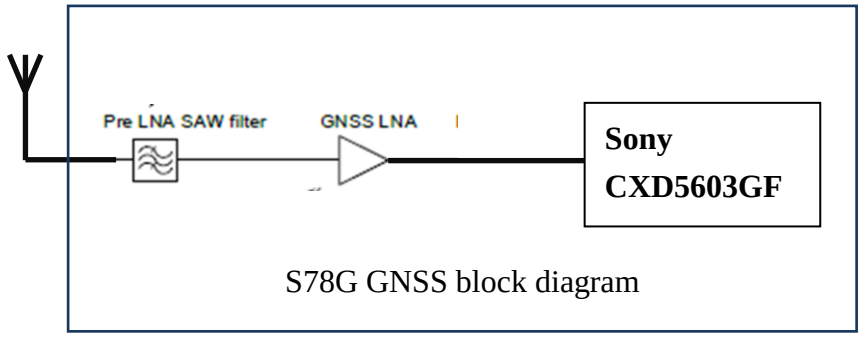


- RTC Low-speed external clock

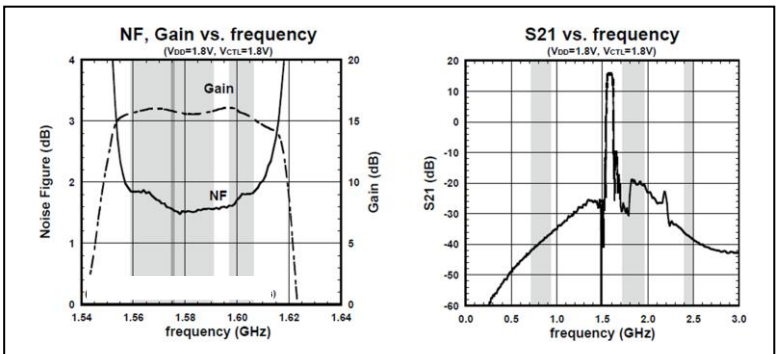


3.7 RF external components and interference for GNSS receiver

To avoid sensitivity degradation by out band interference and reduce cost. The S78G integrate a front-end module (FEM) designed for GNSS including GPS, GLONASS, BeiDou, and Galileo applications. This FEM offers low noise figure, high linearity, and high out-band rejection characteristics brought by included high performance pre-SAW filter and low noise amplifier (LNA).

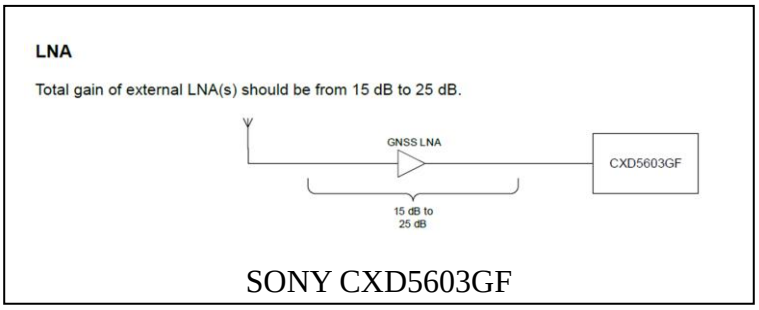


S78G GNSS block diagram



Pre LNA +SAW filter

According to SONY CXD5603GF application note, the total gain of external LNA(s) should be from 15dB to 25dB

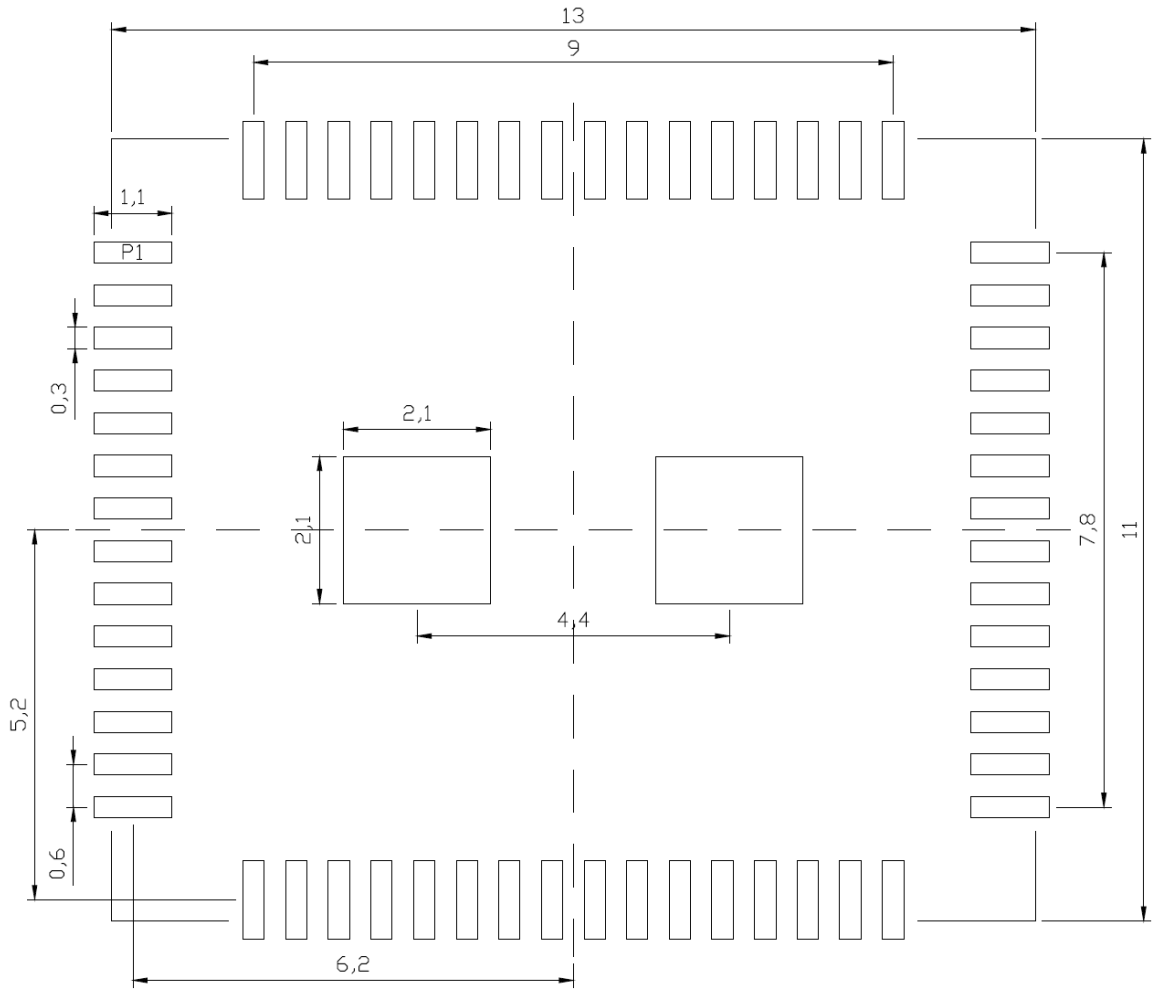


SONY CXD5603GF

If there is an additional LNA before S78G GNSS receiver input, please take care of the LNA gain to avoid the high gain making multi-path and out-band interference.

3-8. Recommended Footprint

Unit: mm



TOP View

4. Other information

- Do not put any signal trace or power trace on system PCB top layer under S76G series module.
- Discuss with AcSiP engineer after schematic and layout finished.