Departamento Tecnología Electrónica

UC3M

LAB MANUAL

COMPUTER TECHNOLOGY

(SESSIONS 3 & 4)

DEGREE ON COMPUTER SCIENCIE & ENGINEERING

1st Year, 2nd Term

Academic Year 2020-2021

uc3m | Universidad Carlos III de Madrid

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

GENERAL RULES OF USE OF THE ELECTRONICS LABORATORY

Each laboratory session has a duration of 2 hours unless otherwise stated.

Due to the big number of students using the laboratory during each course, it is convenient to follow the following general rules.

It is strictly forbidden:

- **Smoking in the building.**
- **Introducing any kind of food or drink in the laboratory**. Drinks are especially forbidden not only to keep the laboratory clean but also for safety reasons. Spilling liquids over the equipment may cause irreversible damage and even fire.
- **Doing any activity other** than the specific laboratory work.
- **The entry to the private zones** allowed only to the laboratory staff.
- **Deliberately damaging the equipment** of the laboratory.
- **Taking outside**, even temporarily, **any equipment or materials from the laboratory**. This is serious misconduct and will be immediately informed to the Polytechnic School Management Office to take the necessary measures.

While working in the laboratory, the following behavior rules are also suggested:

- Avoid speaking loud or southing. You just need to listen to your lab group partner and the teacher.
- Avoid bothering the other students who are working at the laboratory.
- The teachers are at the laboratory to help you; do not hesitate to ask them for support. However, **it is strongly recommended that you try first to solve the problems by yourself instead of calling the teacher as soon as you encounter any difficulty**; this is an important part of the learning process.
- Your time at the laboratory should be used for assembly and test and to take the necessary measurements.

Besides the equipment available at each laboratory place, additional materials may be required for some lab work.

- STUDENTS MUST BRING THEIR OWN PLIER AND TRIMMER.

The additional materials are lent to each lab group only for the time of each laboratory session; all materials must be returned to the laboratory staff when the session ends. The staff keeps a strict record of the materials lent to each group for each session. If any materials are missing, the staff will easily identify the responsible and will take the necessary actions. Do not lend your materials or equipment to anyone from another group; you are the only responsible for the materials lent to you.

The goal of the laboratory work in the field of Electronic Technology is to acquire the necessary practical skills of an engineer. Following these rules and suggestions will make your work at the laboratory much more productive towards that goal.

ALL THE STUDENTS INVOLVED IN ANY ATTEMPT TO PASS THE LABORATORY WORK BY ANY FRAUDULENT MEANS (COPYING, CHEATING...) WILL AUTOMATICALLY FAIL THE SUBJECT. **THIS RULE IS APPLIED EQUALLY TO THOSE WHO TRY TO PASS BY ANY MEANS OTHER THAN THEIR OWN EFFORT, AND TO THOSE WHO HELP OTHERS TO DO SO.**

SAFETY RULES

In the Voltage, Current and small magnitude measurements it is not required to pay any special attention or to take any special precaution. In the cases in which high voltages should be measured, the incorrect use of the equipment can cause serious injuries. Therefore, it is a good precaution to perform those measurements with only one hand, touching your back with the other.

During the lab sessions, any injury or damage to equipment should be noticed to the person in charge of the lab. A not repaired breakdown can create bigger problems.

Following these safety rules, some recommendations should be made to avoid any damage to the lab equipment's user or others:

1. Do not use the multimeter if the probe points are broken.
2. Switches or similar components should be in the right position to perform the measurement. The instrument should be prepared to perform the desired type of measurement: current, voltage, etc, …
3. The scale selector should be at the highest position when an unknown voltage or current is measured.
4. When electric measurements are performed, you should NEVER be touching the ground potential. You should always work isolated, standing on a rubber mat, with rubber shoes, etc, and you should NEVER touch any water pipe or any metallic part with your body when performing a measurement.
5. Do not exceed the maximum specified voltages in any measurement. You could damage the equipment and yourself.
6. Do not exceed the maximum voltage between neutral (GND, black connector) and EARTH (green connector).
7. Be extremely cautious if you are measuring voltages that exceed 60V DC or 30V AC RMS.
8. If you have to manipulate a circuit (soldering, cutting, mounting, etc…) be sure that the general circuit supply is disconnected.

It is recommended to read the "Servicio de Prevención de Riesgos Laborales" webpage for more information:

http://www.uc3m.es/uc3m/serv/GR/SPRL/prevrlsegurid.htm

PERSON IN CHARGE OF THE ELECTRONICS TECHNOLOGY DEPARTMENT LABORATORIES

INTRODUCTION TO THE LAB SESSIONS OF DIGITAL ELECTRONICS

One of the main characteristics of digital electronics is its high integration level when fabricating integrated circuits. A digital integrated circuit may contain millions of logic gates. The great complexity of the latest digital systems makes needful the use of CAD tools and hardware description languages (HDL) for circuit designing. That's why we will be using those tools in this class, specifically VHDL programming through Altera's Quartus-II tool. More specifically, we will be using ***Quartus-II 9.1***. Quartus-II is a professional work environment which allows us, among other functions, to do synthesis and simulation of digital circuits from VHDL code and their implementation on Altera's FPGAs. **Please, use only this version of Quartus-II for this laboratory**.
For a detailed explanation of Quartus-II and instructions on how to complete every design step (programming, simulation, etc.) you may consult *Altera's Quartus-II basic Manual*.

The laboratory work has been divided into 4 sessions. In all sessions, students will design digital circuits using the Quartus-II tool. The performance of the whole system will be verified through simulation in all online sessions. Sessions 1 & 2 will be an introduction to the digital design of combinational circuits using the Quartus II tool. In sessions 3 and 4, sequential circuits will be designed and simulated. In each session, the deliveries or questionnaires to be carried out for the assessment of the sessions will be expressly indicated. Deliveries will be made through a delivery task in the aula global that belongs to the problems group (not magistral group). ALL STUDENTS BELONGING TO THE SAME WORKING GROUP (3 STUDENTS) MUST MAKE THE DELIVERY, INDICATING IN THE FILES PROVIDED: WORKING GROUP AND THE FIRST LAST NAMES OF THE STUDENTS IN THE WORKING GROUP. The following format will be followed: GROUPX_N_Surname1_Surname2_Surname3 (where X is the group number). Deliveries will only have one file. Thus, the students must compress the files in a * .zip.

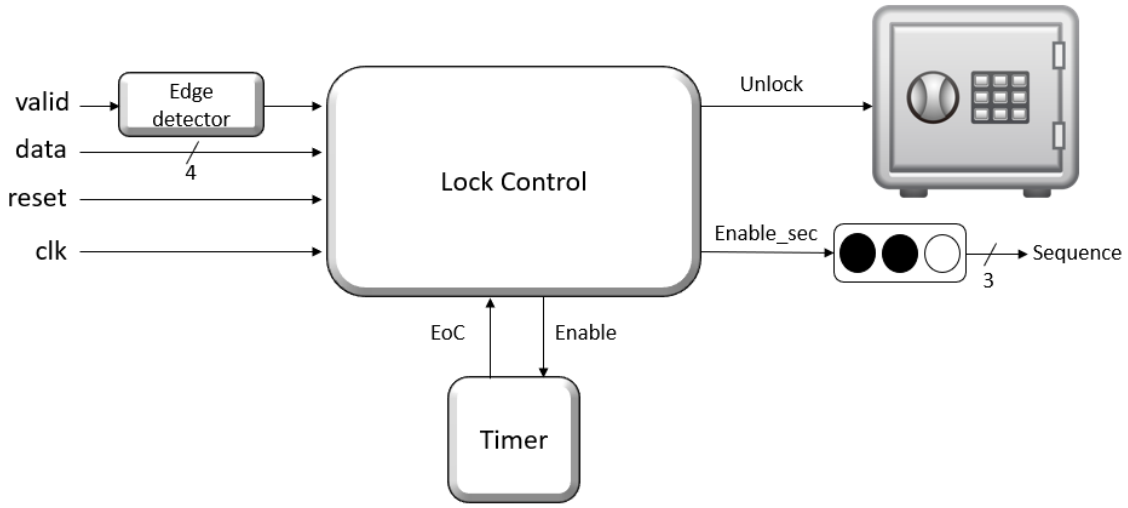
For each circuit to be designed, you must obtain a solution using the concepts as seen in theory classroom sessions. Then you will check if the solution is correct (achieves all the specifications) by simulating the circuit. For this, you will have to draw all the clock diagrams for each input signal, do the simulation and check that the output values are like the expected ones.

The lab sessions of Computer Technology have been designed as a complement to facilitate the theory classes' conceptual learning. Remember that lab sessions are **mandatory**. The working groups are composed of **3 students**. If there would be any problem that could prevent to carry out the laboratory sessions. Please contact with the teachers of the subject.

Introduction to Lab 2

The aim of this session is the design and simulation of a circuit that controls the lock of a security box. The control is based on the detection of a predefined sequence of 3 keyboard presses. The user needs to press an additional button after each key for the control circuit to acknowledge the key press. The system will show the current state of the sequence detection to the user during the process (number of digits that have been already introduced).

The design will be done using Altera Quartus-II 9.1 software. The target device for the design is an EPM7064SLC44-10 Altera device.



Note: For the sake of clarity, clock and reset signals have not been included in all modules that require them.

Inputs of the circuit:

- Data: 4-bit input that corresponds to the encoding of the key that has been pressed. The keyboard has ten numeric keys (0-9) that are encoded using natural **BCD code**, and a "close" key which is encoded with the "1111" encoding. The rest of the combinations are not used.
- Valid: signal from a push button that indicates that the current value in "Data" can be considered a key press. This signal comes from an edge detector, so "Valid" is active high for exactly one clock period when the button is pushed.
- Clk: clock signal. Active by rising edge.
- Reset: asynchronous initialization signal. This signal is active-high.

Outputs of the circuit:

- Unlock: signal that controls the lock of the security box. If Unlock=1 the security box will be unlocked. If Unlock=0 the security box will be locked.

- Sequence: 3-bit signal that shows the current state of the sequence. “000” indicates that the system is waiting for the first digit. “100” indicates that the system is waiting for the 2nd digit. “110” indicates that the system is waiting for the 3rd digit, and finally, “111” indicates if the sequence was finished and the sequence was correct (and therefore the security box was unlocked and the system is waiting for the user to lock it again).

Additional considerations:

- The security box must be unlocked with a sequence that includes the LSB of the NIA of each of the members of the lab group.
- The sequence will contain only digits in the range 0-9. Therefore, the close encoding “1111” cannot be used as a digit for the combination.
- Once the security box is open, it can only accept the “close” keypress. If that happens then the security box will be locked again and will be ready for the introduction of a new sequence.
- The user should not identify if the introduced digits are correct or not during the process. The user will only know if the full sequence was correct or not once the third digit of the sequence is introduced, when the security box will be unlocked or not depending on the correctness of the sequence.
- If the sequence entered is wrong, the password cannot be re-entered inmediatly and the user should wait for 10 clock cycles.
- The sequence output will be generated through a shift register.

Session 2. Preliminary Study

Before starting, open a virtual classroom and log in with your username and password.

(https://aulavirtual.uc3m.es/login/). Enter the W7 machine and open Quartus II. Alternatively, you can run the application on your computer if you have Quartus II installed.

This practice session is online, students must connect to the BlackBoard Collaborate (BBC) session in the small group section in Aula Global (65* and 95). In the BBC sessions the teachers will create groups so that the students can work during the session together. In groups, audio and screen can be shared to facilitate group work. Students can ask teachers for help using the BBC chat. The teachers will visit the groups during the session to check the development of the work by the students and to answer questions.

A. Simulating a Synchronous Sequential circuit

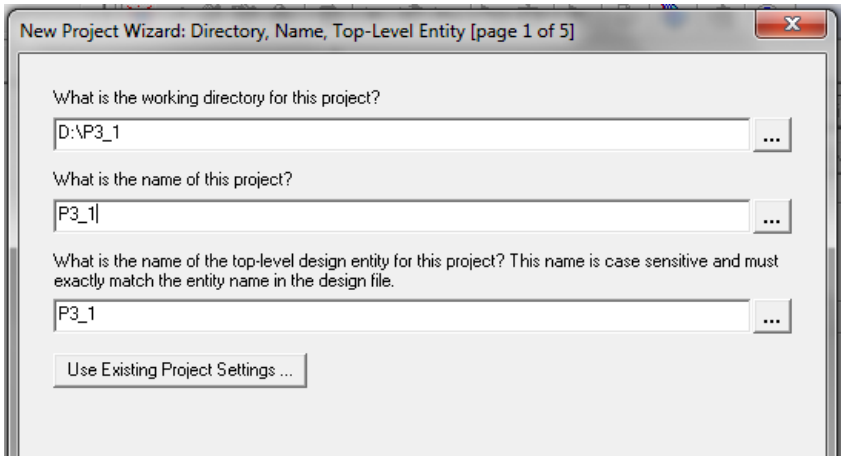
In this practical session, the students will apply the knowledge acquired in the theory sessions to analyze and simulate Synchronous Sequential circuits. In this part, the file P3_1.vhd available in Aula Global will be added to the Project created in Quartus II with the same name. Finally, the simulation will be carried out with a waveform file specified in the statement.
Perform the following steps:

1- Create a new Project in Quartus II:

a. Go to New Project Wizard and create a new project.

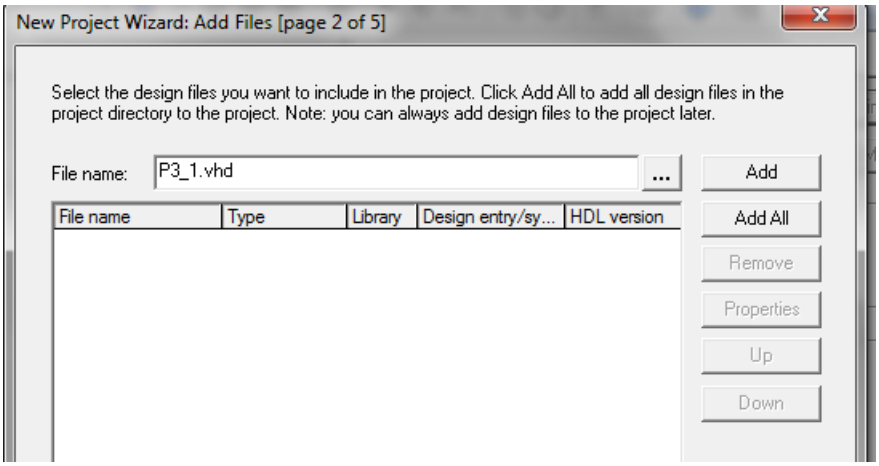
b. Project name and path:

In this window, you will decide where to save the project and its name. Please, use as name P3_1 and place it in a folder with the same name.

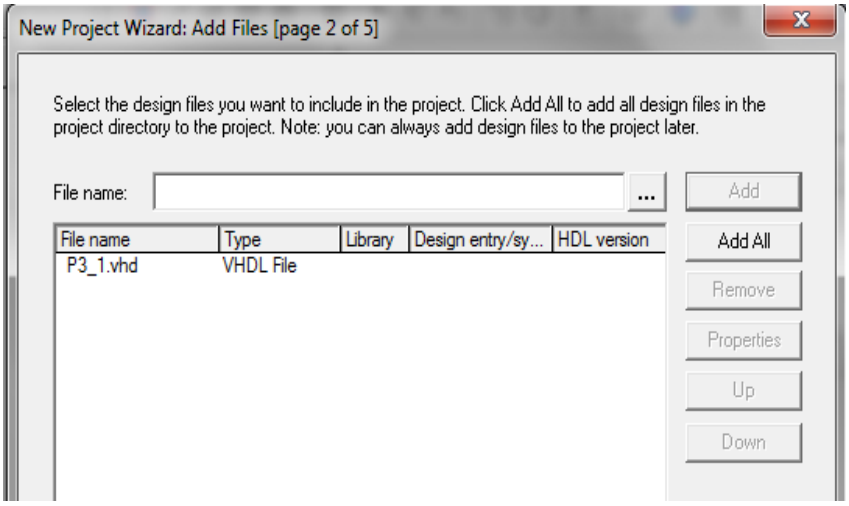


Click on Next.

c. **Add Files**. Click the button with the three points next to “File name” and add the vhdl file **P3_1.vhd**, that you have previously downloaded from AulaGlobal.



Next, click on Add.



Click Next

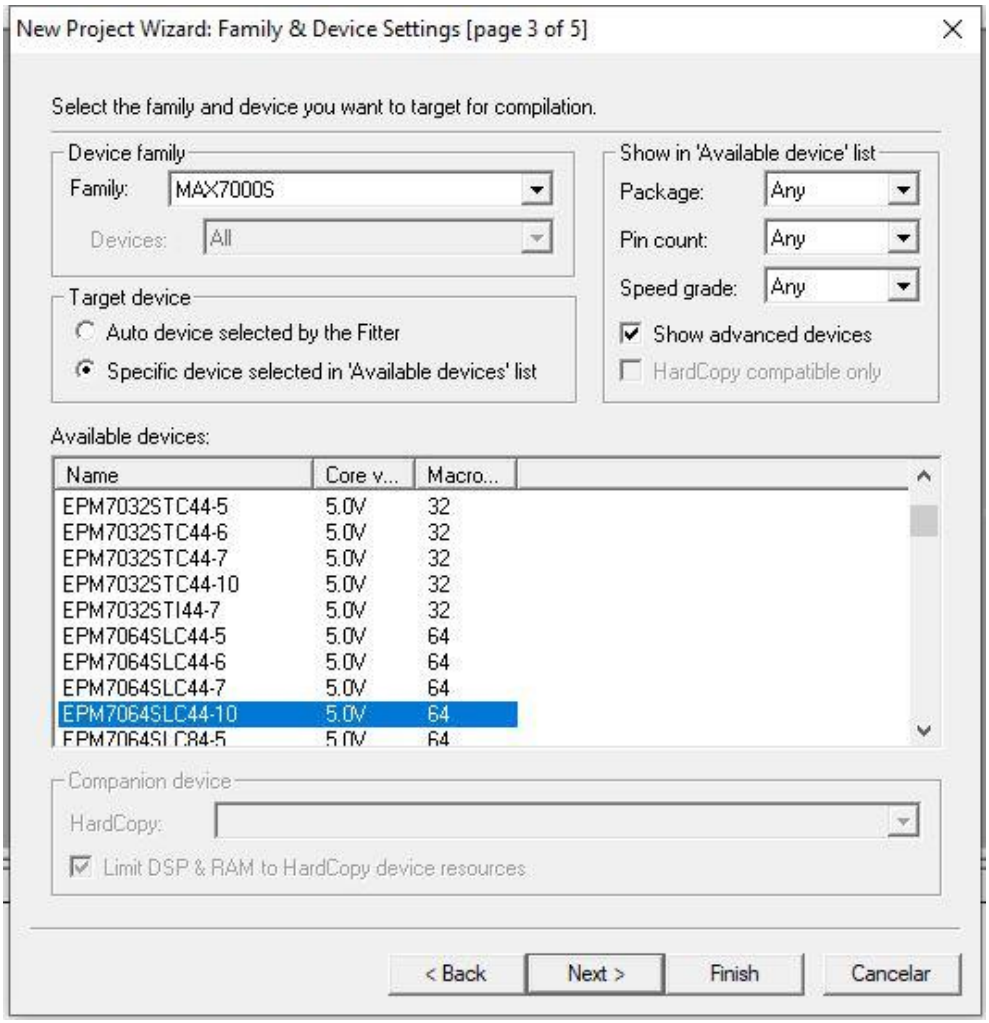
d. Device selection (FPGA).

   As the next figure shows, select the device:

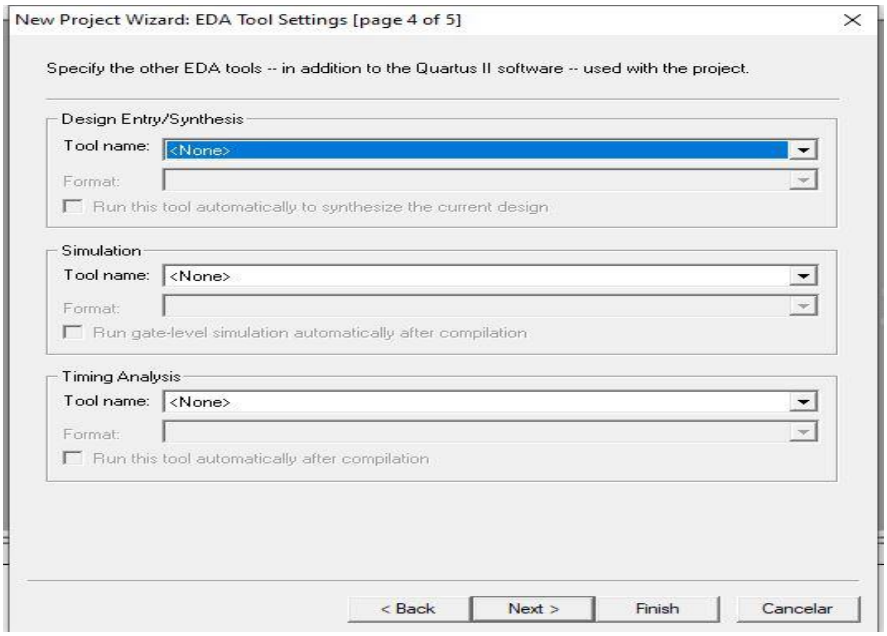
   1- Search the device family: **MAX 7000S**

   2- Search the device in “Available devices”: **EPM7064SLC44-10**

   Click on Next.



e. Click Next in the following window:



f. Again, click Next in the following window.

g. Click Finish to end the process of generating the project.

2- Open the file P3_1.vhd and compile the project

Check that you have no compilation errors.

When the compilation is finished, press the Report button, and check the compilation report.

QUESTION 1

Open the RTL View in Quartus II and determine the number of flip-flops in the synthesized design. Which type are these bistables? Is it a synchronous or asynchronous circuit? Justify the answer. Copy and paste the RTL view into your document.

Check that the number of flip-flops is the same as in the compilation report (Section Fitter->Resource section->Resource usage summary->Registers).

3- Functional simulation

a) Open a new waveform file and save it with the name P3_1.wvf.

b) Insert all inputs and outputs (Insert->Insert Node or Bus->Node Finder: Filter =pins(all), press List and add all pins in the Selected nodes window, then press OK)

c) Configure the Waveform file as follows:

1- Total Simulation Time 20 ms

2- Grid size 1 ms. Adjust the window to display the entire simulation ("Fit in window")

3- Periodic Frequency **CLK** signal = 1 KHz. Press "INV" in the left menu to match the grid size with the rising edge of this signal.

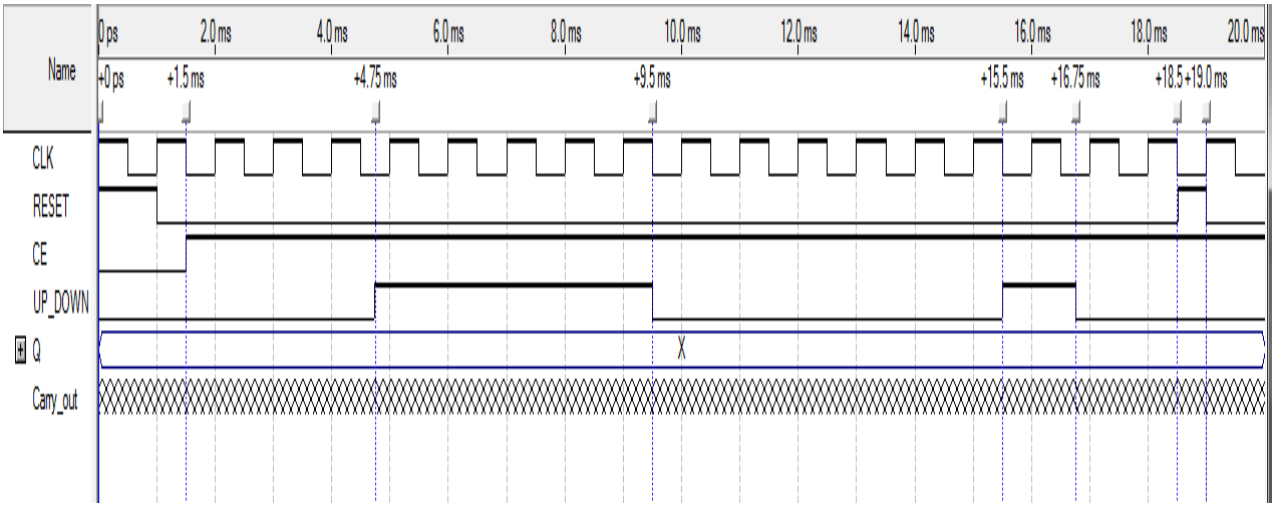
4- **RESET** signal equal to "1" between 0 and 1 ms and between 18.5 y 19 ms. Rest "0".

5- **CE** signal equal to "0" between 0 and 1.5 ms. Rest equal to "1".

6- **UP_DOWN** signal equal to "1" between 4.75 ms and 9.5 ms and between 15.5 and 16.75 ms. Rest "0".

Unselect the option “Snap to Grid” in the corresponding icon of the vertical menu, in order to fit the signals as per the requirements.

You should obtain the following chronogram:



d) Complete the simulation

QUESTION 2

a. Copy and paste the result of the simulation on this document

Considering the simulation:

b. What operation does the circuit perform?

c. Analyzing the VHDL code and the result of the simulation, explain the Function and nature (**synchronous or asynchronous**) of the following inputs and outputs:

- **RESET**
- **CE**
- **UP_DOWN**
- **Q**
- **Carry_out**

B. Modify the circuit according the following requirements

Create a new project: P3_2. Add the previous files P3_1 .vhd and P3_1.vwf to the project, renaming both as P3_2 with its corresponding extension.

Modify the previous VHDL code so that the circuit complies with the following:

- Include the LOAD and D inputs in your design (LOAD must be synchronous).
- Skip the state "13_{10}" (i.e. count 11,12,14,15... in ascending mode and 15,14,12,11.. in descending mode).

Modify the Waveform file as follows:

LOAD Signal must be "1" between 2.0 and 3.5 ms and between 13.5 y 14.75 ms. Rest of the time must be in "0".

The number to be loaded must be decimal number "15".

Run the simulation

Explain what happens in the two cases for LOAD signal is "1" and write it down on the answer report.

QUESTION 3

Include both the resulting VHDL code and the simulation result in the document, clearly showing that both requirements are met.

QUESTION 4

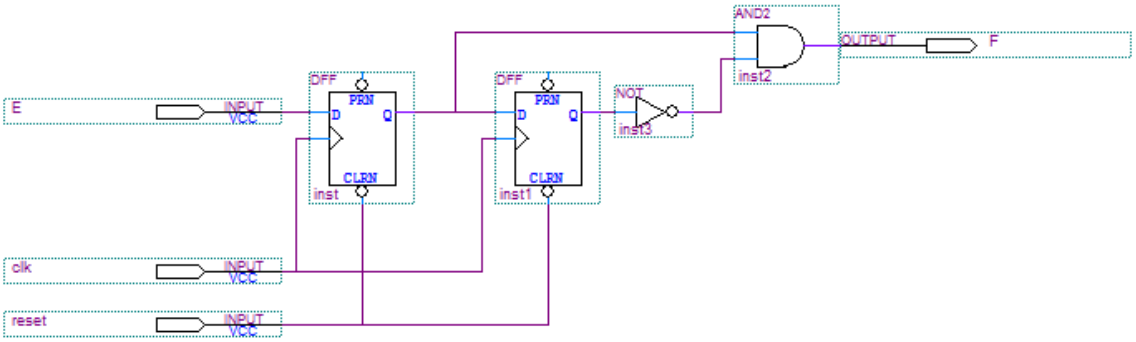
Considering the functionality described for the security box, draw the state transition graph of the state machine that controls this functionality.

Labwork sessions 3

This lab session is online, **students must connect to the BlackBoard Collaborate session** created at the problems group. In the BB sessions the teachers will create groups so that the students can work during the session together. In groups, **audio and screen can be shared to facilitate group work**. Students can ask teachers for help using the BlackBoard Collaborate chat. The teachers will visit the groups during the session to check the development of the work by the students and to answer questions. **Session 4 will be dedicated only to the evaluation of the lab, so the students will have to bring a functional version of their solution to be evaluated.**

Student's work:

1. Create the circuit entity by properly describing the inputs and outputs.
2. Describe in VHDL a process for the edge detector containing the following hardware.



3. Describe in VHDL a timer/counter for counting 10 clock cycles.
4. Write the VHDL code that implements the finite state machine designed in the previous study.
5. Describe in VHDL a shift register for the generation of the output *sequence*.

6. Simulate the circuit in Quartus II. This simulation must include at least the following situations (students can consider more cases, but at least these ones must be shown):
   a. A case where the user enters the correct sequence
   b. A case where the user locks the box after been unlocked
   c. A case where the user enters the correct first digit but the second and third are wrong
   d. A case where the user enters the correct first and second digits but the last one is wrong
   e. A case where the user enters a non-valid digit (10-15).
   f. A case where the user enters digits while the box is unlocked

   The simulation must show the values of the outputs unlock and sequence, and additionally an output with the value of the FSM state.

The report to be delivered for this session, to be uploaded in a pdf document using the task enabled in Aula Global, must contain:

- VHDL code implementing the system entity and architecture with the functionality of the described elements. Use a single entity and single architecture for the entire system.

- Explanation of the code of each of the blocks and justification of the signals used.

- Captures of simulations demonstrating the proper operation of the system, showing at least proposed situations in question 2.

Additionally, students must submit a copy of the Quartus project that includes: * file. vhd and * file. vwf. In addition, they must include in the delivery a text file (Word or pdf) with capture of the complete simulation explaining the results of their simulation. You can display simulation results in parts.

Everything will be included in a single compressed file.

1- Each student in the group must submit the work, done as a team, individually in the Aula Global enabled task.
2- All members of the practice group must be identified in the delivery, in the file name itself, as in the text documents that are delivered. The practice group number must also be included in the delivery. For the names of the files follow the following format: **GrupoX_apellido1_apellido2_apellido3**. Being X the number of the practice group and surname1, last name2 and last name3 the first surnames of the three students' members of the group.